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INTERNATIONAL STANDARD

colour inside

Semiconductor devices – Stress migration test standard – Part 1: Copper stress migration test standard

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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CONTENTS

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SEMICONDUCTOR DEVICES – STRESS MIGRATION TEST STANDARD –

Part 1: Copper stress migration test standard

FOREWORD

International Standard IEC 62880-1 has been prepared by IEC technical committee 47: Semiconductor devices.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
47/2407/FDIS	47/2416/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62880 series, published under the general title *Semiconductor devices – Stress migration test standard*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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SEMICONDUCTOR DEVICES – STRESS MIGRATION TEST STANDARD –

Part 1: Copper stress migration test standard

1 Scope

This part of IEC 62880 describes a constant temperature (isothermal) aging method for testing copper (Cu) metallization test structures on microelectronics wafers for susceptibility to stress-induced voiding (SIV). This method is to be conducted primarily at the wafer level of production during technology development, and the results are to be used for lifetime prediction and failure analysis. Under some conditions, the method can be applied to package-level testing. This method is not intended to check production lots for shipment, because of the long test time.

Dual damascene Cu metallization systems usually have liners, such as tantalum (Ta) or tantalum nitride (TaN) on the bottom and sides of trenches etched into dielectric layers. Hence, for structures in which a single via contacts a wide line below it, a void under the via can cause an open circuit at almost the same time as any percentage resistance shift that would satisfy a failure criterion.

2 Normative references

There are no normative references in this document.

NOTE Related documents are listed in the Bibliography.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
stress migration
SM
crucial failure phenomenon of the semiconductor device interconnects

3.2
stress induced voiding
SIV
voiding generated in the semiconductor device interconnects which is caused by thermal stress

Note 1 to entry: In copper interconnect, voiding occurs under VIA or inside VIA, and causes resistance increase or open failure.

Note 2 to entry: See Annex B for mechanism.

3.3
wide pattern
chain pattern, which VIA connects wide pattern

Note 1 to entry: There are some combinations of connection.

SEE: Figure 1

3.4
nose pattern
chain pattern, narrow pattern connected to a VIA and attached to a wider pattern

Note 1 to entry: THe SIV risk of this VIA is determined by the width of the plate and the distance of the VIA away from the plate (described in 4.1).

SEE: Figure 1

3.5
nose length
length of a narrow pattern portion of the nose pattern

SEE: Figure 1

3.6
nose width
width of a narrow pattern portion of the nose pattern

SEE: Figure 1

3.7
DRC
Design Rule Compliant
pattern rule that the designer shall follow, e.g. permitted pattern width, VIA location ,etc.

3.8
VIM
VIA-in-the-middle
wide pattern type of VIA chain

Note 1 to entry: See Figure 1 and Annex A.

3.9
co-axial stacked VIA
SM test structure where VIA is stacked in the vertical direction and coaxially

Note 1 to entry: See Figure 2 and 4.1.

3.10
off-center stacked VIA
SM test structure where VIA is aligned in the vertical direction and the center of VIA is shifted

Note 1 to entry: See Figure 2 and 4.1; a zig-zag type and a spiral type are proposed.

3.11
mesh type VIA
SM test structure chain pattern, VIA is connected to narrow pattern and narrow pattern is connected to the mesh type wide pattern

Note 1 to entry: See Figure 2 and 4.1.

4 Test method

4.1 Test structures

To test the susceptibility to stress voiding of the technology under evaluation, structures that emphasize each extreme risk of the technology shall be designed, evaluated, and used in the test procedure.

Typical SM test structures are in the formats of VIA chains and single VIAs. Special considerations shall be carried out to assure that the appropriate test structures are used. The following are the structures that shall be used in the evaluation of stress migration reliability:

– Design rule compliant (DRC) linewidth test structures:
  - Around 100-VIA chains, both conventional (VIA-at-end) and the VIA-in-the-middle (VIM) VIA chains. Bi-polar or plate-above VIA and plate-below VIA types. Modest VIA numbers of around 100 to a few hundred are recommended to ensure resistance sensitivity for SIV risk detections.
  - VIA chains with larger VIA numbers such as around 1 000 to around 1E5, are used at the individual company's discretion in case of needs for VIA scaling.
  - Single Kelvin VIA structures, VIM type.

– For test structures, specific dimensions (nose length/width) shall correspond to each user's processes and designs. Potential options may range from 10x min to 100x min width or its equivalence (e.g., slotted plates) VIM VIA chains, for measuring SM margin and estimated SM lifetime within limited testing time.

Figure 1 shows the sketches of test structure formats of:

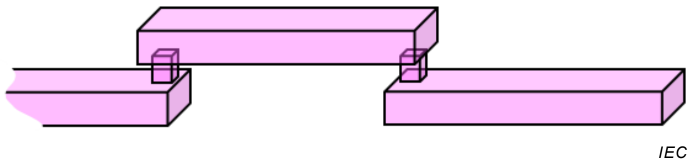
a) conventional VIA chains (around 10 µm interconnect length);

b) VIA-in-the-middle (VIM) VIA chains (around 10 µm interconnect length);

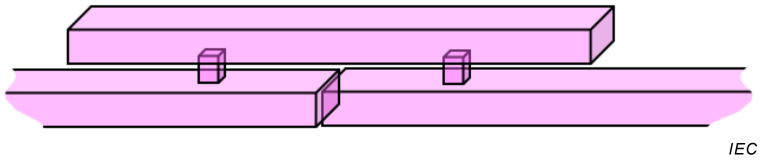
c) single Kelvin VIA (L-shaped);

d) SM nose VIA chain structure of plate-below and plate-above VIA chains.

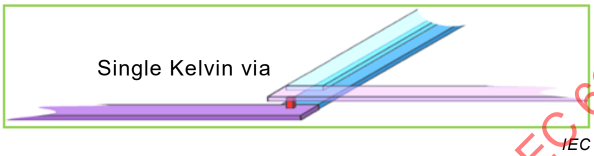
The plate widths of VIA chains, single Kelvin VIA and SM nose VIA chains can be DRC and wide plate widths.



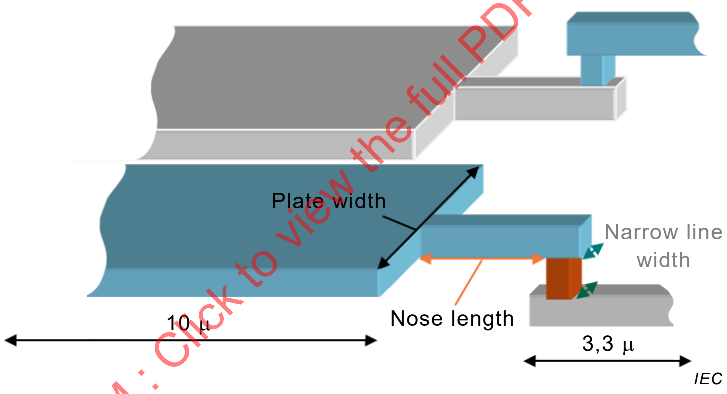
a) conventional VIA chain



b) VIA-in-the-middle (VIM) VIA chain



c) Single Kelvin VIA (L-shaped)



d) SM nose VIA chains

Key

a) usual wide pattern, VIA is located at edge or near the edge of wide pattern;

b) wide pattern but VIA is located near the center of wide pattern;

c) conventional Kelvin VIA;

d) VIA is located at the narrow pattern and narrow pattern is connected to the wide pattern.

Figure 1 – SM test structure sketches

For SM nose VIA cases where a narrow extension connecting to a VIA is attached to a wider plate, the SIV risk of this VIA is determined by the width of the plate and the distance of the VIA away from the plate [6] [1]. The application of nose VIA structures for SIV reliability assessment shall correspond to their allowable design rules and technologies. If nose VIA designs are permissible, then nose VIA test structures are part of the product-level SIV evaluation for SM quantification. Technologies that do not allow nose VIA designs would naturally conduct SIV evaluations without nose VIA test structures. SM in nose VIA cases are product specifics and it is each individual company's discretion to handle the specifics based on the principle of SM mechanism introduced in this standard. Additional optional SM test structures for the qualification include:

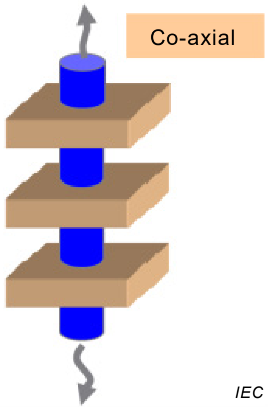
a) stacked co-axial VIA chains;

b) off-center stacked VIA chains;

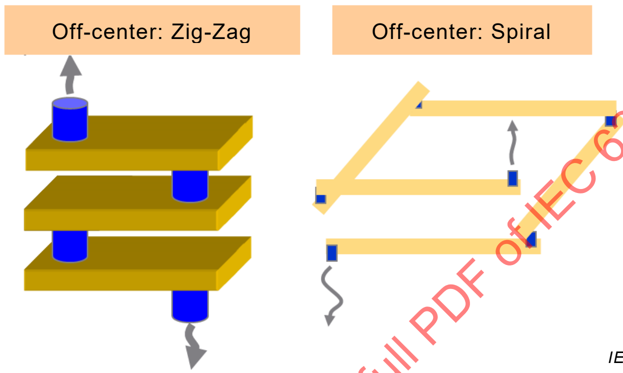
c) mesh type VIA chains (minimum line widths) with mesh-above and mesh-below the VIA.

The illustrative sketches of those structures are shown in Figure 2. Those SM test structures are designed to explore the SIV risk under certain extreme and specific product geometry cases and they are optional choices of each individual company for its SM qualification tests.

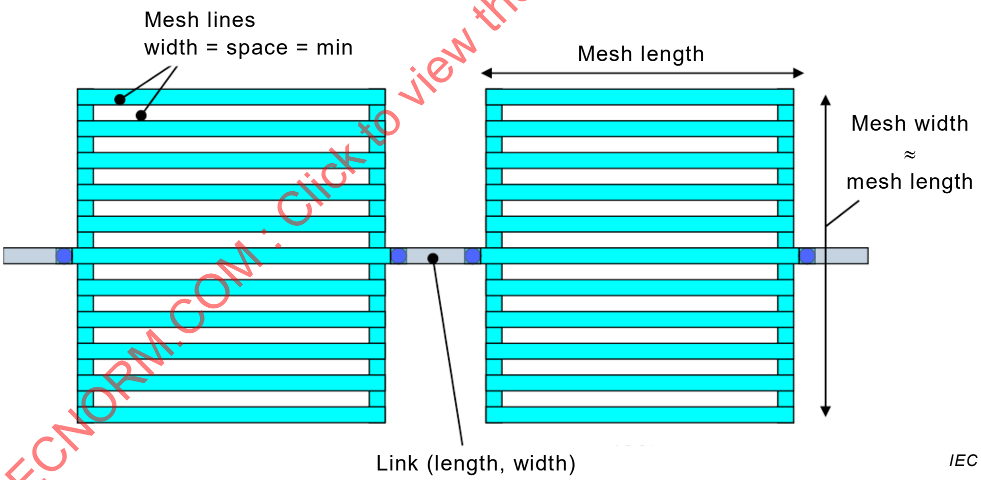
1 Numbers in square brackets refer to the Bibliography.



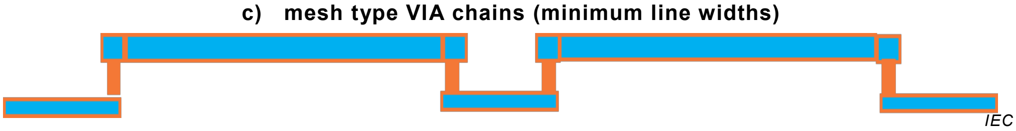
a) **co-axial stacked VIA chain**



b) **two formats of off-center stacked VIA chain**



c) **mesh type VIA chains (minimum line widths)**



d) **mesh type VIA chains (minimum line widths)**

Key

a) VIA, chains stacked vertically and coaxially;

b) stack VIA ,center of VIA are shifted each other;

c) top view of mesh type VIA chains (minimum line widths);

d) cross section of Figure 2 c).

Figure 2 – SM test structure sketches – Illustrative sketches of proposed optional SM test structures

4.2 Test equipment

A calibrated thermal chamber shall be required to subject the wafers or packaged test structures to the specified temperature for the specified time. Additionally, measurement instruments shall have sufficient resolution for slight resistance change.

4.3 Test temperatures

Based on the temperature dependence described in Clause A.2, wafer level SM stress temperatures are the following:

a) Selected constant temperatures between 150 °C – 275 °C.

b) For each SM tests, minimum three temperatures shall be required, covering temperature range from low to high, e.g., 150 °C, 175 °C & 225 °C.

4.4 Test conditions, sample size and measurements

Wafer level tests are recommended for constant Cu stress migration reliability tests due to the following advantages: 1) capable of testing chips throughout the wafer without possible influence introduced by packaging tests. 2) capable of testing large number of SM test structures from the same wafer which is not possible for packaging tests.

Sample size of the wafer level SM tests:

a) Minimum 3 wafers (i.e., 1 wafer/lot from 3 lots) for each stress temperature, e.g. 150 °C, 175 °C & 225 °C.

b) Minimum 30-40 dies per wafer, per metal level, to be tested.

Additional test temperatures (at least four temperatures is recommended) and wafers may be added for quantitative SM modelling verification and lifetime extrapolations if desired by each individual company.

Test measurement readout: Resistance value changes of each test structures are monitored on a required schedule. The minimum is readout at 0 h and 1 000 h. It is optional to perform additional readout within the 1 000 h for better tracking the SM behaviour. For example, 0 h, 250 h, 500 h, 750 h, 1 000 h.

4.5 Failure criteria

The following criteria are failure criteria for general practice in SM reliability evaluations. Individual company can revise the resistance increase numbers in their special cases if needed.

a) Resistance increase (ΔR) for VIA chains > 10 %;

b) Resistance increase (ΔR) for single VIA > 100 %.

4.6 Passing criteria

Criterion a) below is the traditional method of “zero fails during a fixed time period”, which will explore the SIV risk of DRC test structures as well as extrinsic defects during the 1 000 h tests. This is a must-have passing criterion.

For the purpose of estimating the SM margin and the extrapolation of product SM lifetime, we introduce criterion b) for the company to follow. The details of the execution of this second criterion are based on the company’s choice on an accelerated method of SM lifetime model (see Clause A.7).

a) Zero DRC test structure fails for all testing temperatures within 1000 h.

b) Zero SM fails for selected wide line VIA chains within a fixed period, e.g., 250 h, 500 h or shorter, depending on the choices of wide line widths of the test structures. For example, if there is zero 2 µm VIA chain fail within 500 h at 175 ºC for 32 nm and 28 nm, the product SM lifetime will reach the ten-year goal. The detailed choices of selected line width value and no fail hour period can be determined by each company, based on the SM model described in Clause A.7.

5 Data to be reported

After completion of the test, the information listed in items a) to h) shall be reported:

a) Bake temperatures (see 4.3).

b) Measurement intervals. List the cumulative time between the beginning of the test and each resistance readout (see 4.4).

c) Failure criterion. List the criteria used to define failure (e.g. percentage resistance shift, open circuit, etc.) (see 4.5).

d) Sample tested. Describe the sample tested, including the number of wafers, the number of chips per wafer, the macro names and number of structures on each chip (see 4.3 and 4.1).

e) Stress structure. Describe the features of each test structure used, and illustrate with drawings if practical (see 4.1),

f) Initial resistance: plot distribution plots of initial resistance of each test structure (see 4.3).

g) Stress data. Plot the distributions of fractional resistance change versus stress time for each structure and indicate the failure criteria on the plot (see 4.4 and 4.5).

h) Estimated SM margin and lifetime at use conditions: based on the failure conditions of wide line SM test structures, which are non-DRC. It is possible to estimate the SM reliability lifetime by applying the SM lifetime model as presented in Clause A.7. As an example, if there are no fails from 2 µm width VIA chains within 500 h at 175 ºC for 32 nm and 28 nm technology wafers, the SM lifetime will reach the ten-year lifetime goal.

Annex A
(informative)

Explanation for stress migration, stress induced voiding – Temperature, geometry dependence

A.1 Stress-induced voids

Stress migration (SM) or stress-induced-voiding (SIV) is one of the key aspects of Cu interconnect technology reliability qualification. The SIV damages are caused by the stress gradient as driving force through the means of diffusion. For Cu interconnects, it is known qualitatively that the intrinsic SIV risk is higher for a wide line relatively to a narrow line structure with a fixed single VIA size [4-7, 10-14]. As industrial standards, SM reliability data have been treated qualitatively to define pass or fail criteria. The agreed guard-band of "zero fails during a fixed time period" as SM qualification passing criteria has been generally accepted by the industry [8]. This approach was inherited from Al SIV testing method for Cu SIV guard-band but with certain degrees of uncertainty. With the further technology scaling, the Cu SIV reliability margin becomes narrower. Therefore, the old traditional standard could lead to even larger error bars for reliability projections. In order to overcome this known trend of increasing SIV risk, a quantitative SIV lifetime estimation method is needed.

In recent years, the SIV mechanism has been investigated to reduce SIV risk and established SM qualification methodology [4-7, 10]. Due to the improvement of integration process, progress has been made in SM reliability performance in meeting the design lifetime goals. In general, observation of SM failures is not expected for design rule compliant (DRC) linewidth structures even at the worst temperatures during SM reliability testing period (i.e. 500 h to 1 000 h).

It is possible to measure SM failures from reasonable wide linewidth test structures within reasonable testing period of time. In [5, 6], a geometry linewidth dependent factor was introduced to support an SM model for lifetime extrapolation. The quantified linewidth dependent SM data from 45 nm, 32 nm and 28 nm show a common power-law factor M. This further supports the SM model with a geometry linewidth factor for acceleration [5, 6]. In this document, in addition to the traditional method, we will apply the SM lifetime model and the equation to develop an SM reliability qualification methodology for meeting the product design lifetime.

A.2 Stress temperature

Cu SM data show a strong temperature dependence of SM lifetime. Based on the Creep voiding rate model by McPherson and Dunn [4-6, 19, 20], we have the following median time-to-fail (MTF) relationship:

$$MTF = \mathrm{A}(T_0 - T)^{-N} \exp(E_\mathrm{A} / k_B T) \qquad \text{(A.1)}$$

where T_0 is the stress-free temperature at which the thermomechanical stress transits from tensile to compressive, N is the thermal stress component, E_A is the diffusion activation energy, k_B is the Boltzmann constant and A is the normalisation constant.

As an example, Figure A.1 shows the MTF distribution of the 5 μm linewidth VIA chains from 32 nm wafers as a function of temperature in the range of 125 °C to 275 °C. No SM failures were measured from the 325 °C test.

Equation (A.1) was used to fit the five-temperature failure distributions from the PL-SM data of the 5 µm VIA chains as shown in [5, 6]. During the fitting process, parameters of T_0, N and E_A are allowed to vary to minimize the standard fitting error function. As a result, the T_0 value is 277 °C, N is 1,25 and E_A is 0,72 eV in this case. The results of fitting parameters were applied to Equation (A.1) and the calculated MTF values are shown as a model fit in Figure A.3. The model fit calculations and the MTF SM data distributions are consistent with each other. It is necessary to point out that the E_A value can vary depending on the quality of Cu/cap interface and Cu grain boundary diffusion. A relative weak Cu/cap interface assisted by gain boundary diffusion will lower the E_A. The E_A values can be in the range of around 1,0 eV to 0,5 eV.

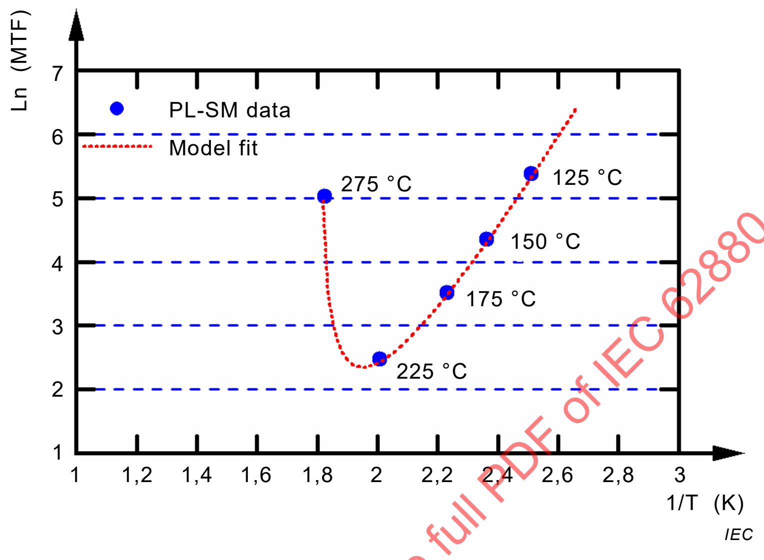


Figure A.1 – Temperature dependent behaviour of SM MTF values of 5 µm VIA chains in the range of 125 °C – 275 °C

The results shown in Figure A.1 demonstrate the following important SM behavior:

a) Above T_0, no SM fails will occur due to the compressive thermo-mechanical stress. The fact we have measured no SM fails from the 325 °C tests confirms this;

b) MTF increases as temperature decreases below T_0. MTF reaches its minimum at a "sweet spot" near 200 °C to 225 °C. The location of the "sweet spot" may vary depending on wafer process details;

c) Below T_0 but above the "sweet spot", the MTF distribution reverses its direction;

d) Close to the operating temperature range, i.e., around 125 °C to 100 °C, the SM data are mostly Arrhenius-like and dominated by the diffusion term. The temperature dependence below the "sweet spot" (i.e., around 175 °C to 100 °C) can be approximately treated by Arrhenius model.

A.3 Geometry linewidth dependence of SIV risk

The linewidth dependence of SIV risk is an important feature for setting design rules and reliability qualification tests. As shown in Figure A.2, SM MTF values are linewidth dependent. In general, the SIV risk increases as linewidth increases for a single VIA. The MTF values follow a power-law as a function of linewidth as shown in Figure A.2. The MTF power-law relation can be expressed as:

$$MTF = \mathrm{C}W^{-2,94} \qquad \text{(A.2)}$$

where W is the linewidth or plate size and C is a normalisation constant. 2,94 is the power-law component value from the fit.

Figure A.2 shows the MTF power-law relation of linewidth measured from wafers of technologies of 45 nm, 32 nm and 28 nm. It is noticeable that SM data from all three technologies follow the power-law by linewidth and the power components of the three sets of data are nearly the same, around 2,94. The power component value of around 3 indicates the possible relation to a particular voiding nucleation mechanism [17,18]. We believe that the MTF power-law relation of linewidth reflects the intrinsic nature of SM linewidth scaling. It can be expressed in general terms as:

$$MTF = \mathrm{C}W^{-M} \tag{A.3}$$

where M is the geometry stress component. The M values can be fitted and checked from SM testing results. Its value may be altered in accordance to the wafer process and presence of intrinsic failures. For this illustration, the M values extracted from three technologies are consistently close to 3. It is recommended that characterization is performed to understand the intrinsic SM property and establish validity and correlation to this prescribed model in order to determine applicability, especially in the smaller regions adjacent or outside line width of Figure A.2.

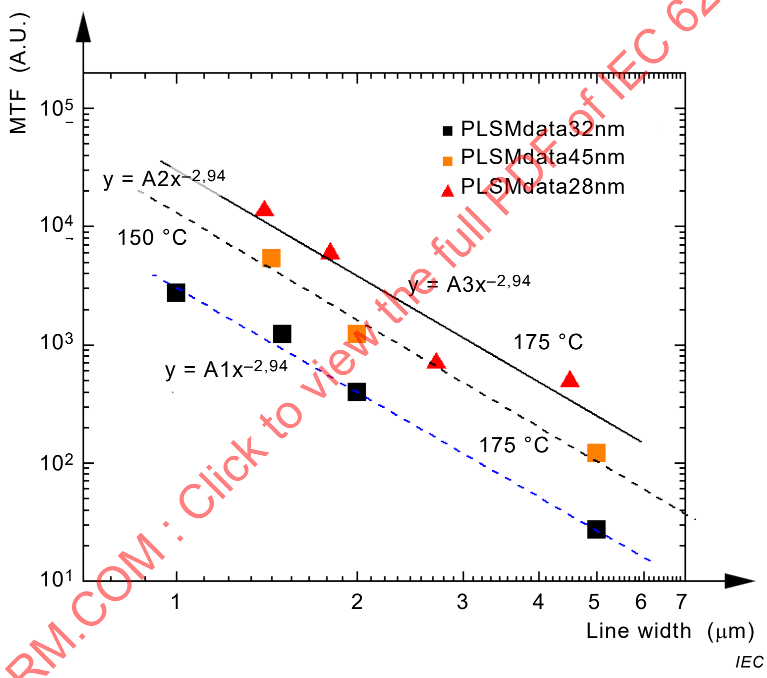


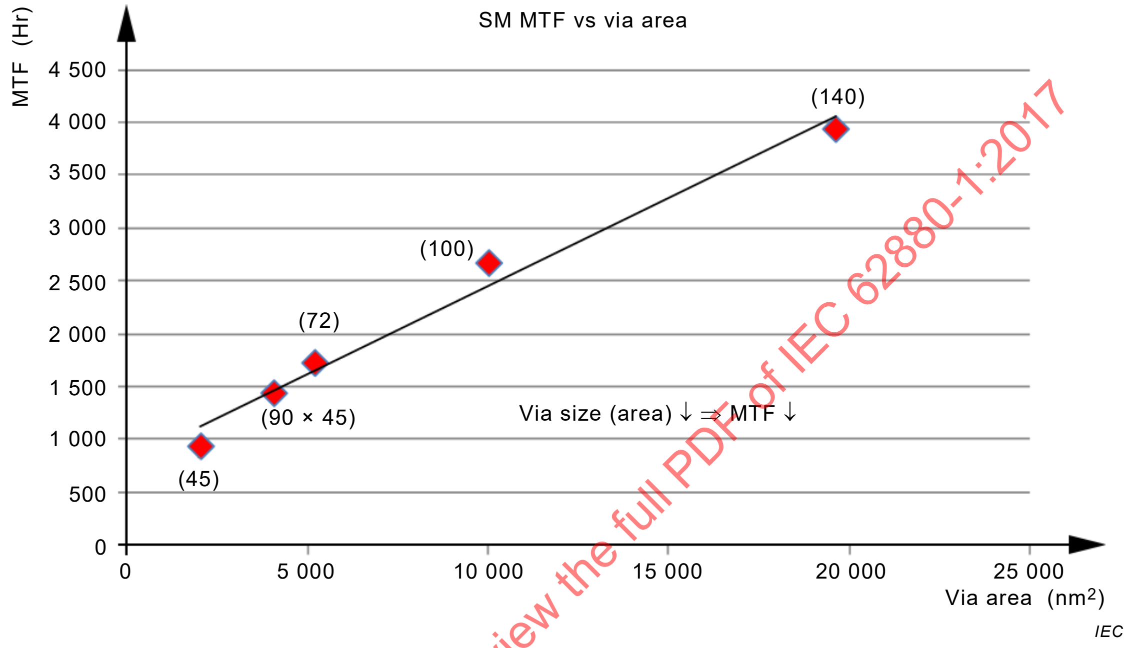
Figure A.2 – Power-law relation of MTF vs linewidth

From Figure A.2, it is noticeable since the DRC linewidth is << 1 µm, the MTF values of DRC VIA chains are in years and are unmeasurable during realistic testing timeframe. On the other hand, the MTF values of wide line VIA chains, e.g., 5 µm VIA chains, are in the order of 100 h. The new linewidth dependent relation (Formula (A.3)) provides the possibility to accelerate the SM tests by using the wide line or wide plate test structures and estimate the DRC SM lifetime quantitatively for the reliability evaluations.

It has been reported that some of the nose VIA cases, in which a nose VIA connected to a wide plate through a minimum width narrow line in highly scaled technology, showed voiding in trenches, VIAs as well as under the nose VIAs [15,16]. In those cases, the linewidth dependence of SIV and traditional SM multiple VIA rules were not effective to protect the circuits from SIV damages. However, the voiding mode can be controlled by optimizing the integration process, e.g. trench barriers, etc. Those voiding modes were probably caused by the extrinsic defects related with non-optimized process especially during the early stage of a highly scaled new technology.

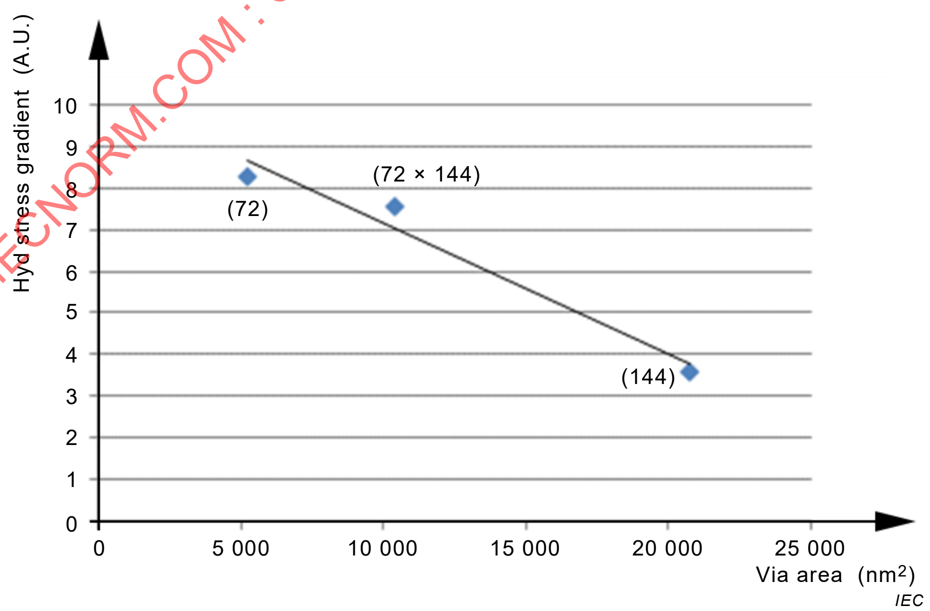
A.4 VIA size dependence of SIV risk

Figure A.3 shows the SM MTF values from a group of 100 VIA chains with different VIA sizes ranging from 45 nm to 140 nm, including a VIA bar, measured by PL-SM at 175 ºC, respectively. The SM data show that the MTF values are a linear function of VIA cross section area. As the VIA size decreases, the MTF decreases, i.e., the SIV risk decreases. This is consistent with the calculation of maximum stress gradient versus VIA cross session area under a 3D linear elastic model assumption as shown in Figure A.4. As Figure A.4 shows, a smaller VIA is related with higher stress gradient and thus resulting in higher SIV risk.



The VIA diameters are labelled in brackets in the units of nanometers.

Figure A.3 – Median time-to-fail SM data as a function of VIA sizes



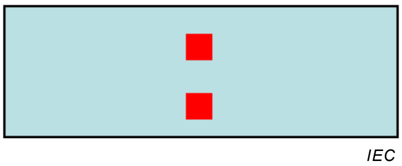
The VIA diameters are labelled in brackets in the units of nanometers.

Figure A.4 – Hydrostatic stress gradient at near room temperatures vs VIA size (area)

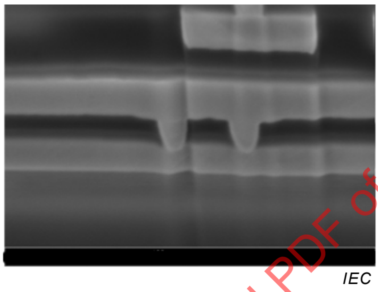
A.5 SIV under multiple VIAs

The cause of SIV damages can be avoided by using multiple VIA configurations, in which the additional VIAs are sacrificed, reducing the stress gradient by non-fatal voiding. The electrical connectivity is maintained by keeping at least one VIA being undamaged in multiple VIA configuration.

Figure A.5 shows an example of a two-VIA case (a). The FA images of unstressed VIAs are shown in (b) and SM stressed VIAs in (c). We can see the structure is still electrically functioning after the SIV damage of one VIA occurred. The MTF value can be greatly increased under multiple VIA configurations. As shown in Figure A.5 (d), MTF values from a 5,0 µm VIA chain were measured under 1 - 4 VIA configurations, respectively. It is shown that the around 10x MTF value increase was observed from 1 VIA to 4 VIA cases. The SM multiple VIA rule method is commonly used today in integrated circuits (ICs) designs to prevent or reduce the SIV risk to the product.



a)



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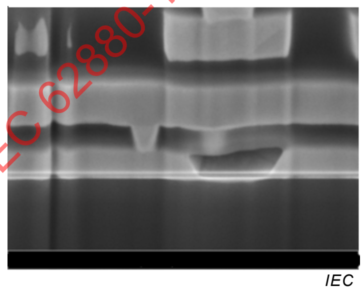

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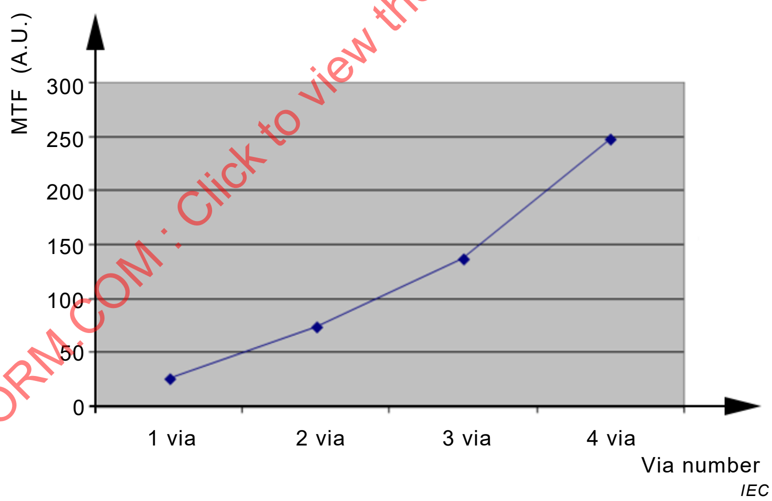
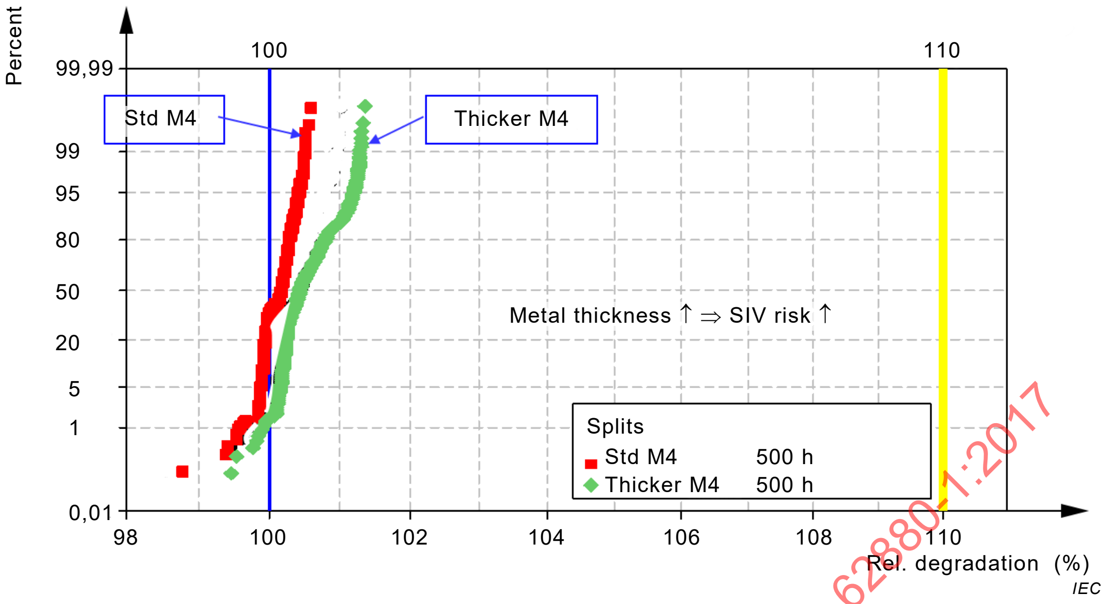


d)

Figure A.5 – FA images of two VIA case and MTF vs multiple VIA of SM

A.6 Metal thickness dependence of SIV risk

Figure A.6 shows the resistance changes versus VIA chains with different metal thicknesses under SM testing at 175 °C. The SM data show the thicker the metal the larger the resistance changes. This means that an increase in metal thickness will lead to SIV risk increase.



The "Std M4" (in red) and the "thicker M4" (in green) were measured after 500 h testing at 175 °C.

Figure A.6 – Metal thickness versus resistance increase under SM tests

A.7 SM lifetime model

Based on the studies of SIV dependence on both temperature and linewidth, we can combine Equations (A.1) and (A.3) into Equation (A.4) as a SM lifetime model:

$$MTF = AW^{-M}(T_0 - T)^{-N}\exp(E_A / k_B T) \qquad \text{(A.4)}$$

where W is the linewidth or plate size, M is the geometry stress component, T_0 is the stress-free temperature, N is the thermal stress component, E_A is the diffusion activation energy, k_B is the Boltzmann constant and A is the normalisation constant.

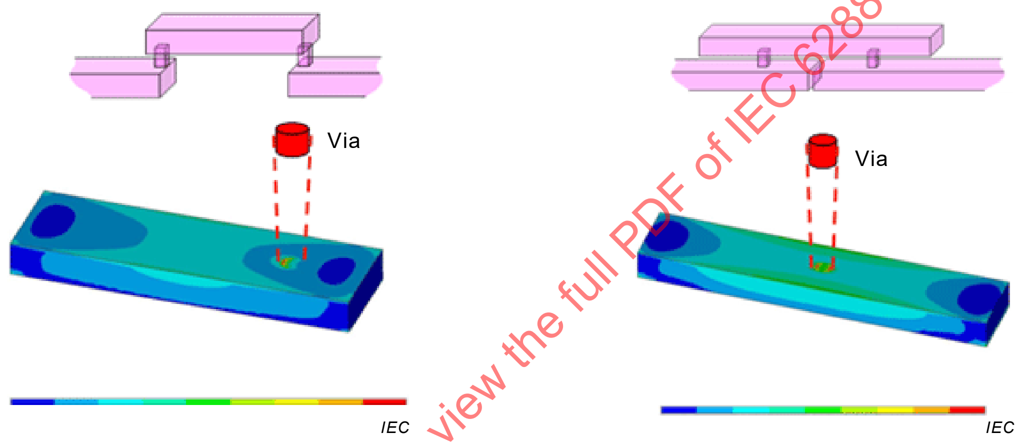
Equation (A.4) is in essence an empirical equation based on SM experimental data and the Creep model assumptions. The SIV driving forces are 1) stress temperature T and 2) linewidth W. The diffusion term serves as a path for SIV. The establishment of Equation (A.4) provides opportunities of making quantitative SIV risk analysis and SM lifetime estimation. Figure A.1 shows that the ratio of temperature dependent MTF values from 125 °C to 225 °C is around 18x for the 5 µm VIM VIA chains. Figure A.2 shows that the linewidth dependent MTF ratio from DRC (i.e., 0,18 µm) to 5 µm is around 16 400x. It is clear that the linewidth geometry provides much better acceleration for SM testing. It is then possible to apply this equation to design SM reliability qualification methodology to quantitatively meet the design lifetime goals. We can perform the SM tests on DRC and selected wide line test structures and estimate the lifetime of unmeasurable DRC test structures in an accelerated manner.

It shall be pointed out that the essence of SIV driving force is the stress gradient. The stress gradient can be generated by absolute stress under stress temperature and geometric configuration including linewidths as shown in Equation (A.4). In addition, SIV mechanism is also critically related with diffusion mechanism and nucleation site density including T_0 defects. Those factors are closely related with Cu interconnect process and are not expressed by separate terms in Equation (A.4) but their influences are included in components N, M, E_A and A.

The extrinsic defects induced SIV described in Clause A.3 is not covered by this model and Equation (A.4). Addressing extrinsic related SIV issues shall be explored and appropriately mitigated during process development and accounted for during qualification periods to understand their overall impact.

A.8 Sensitivity for test structure

Due to the nature of stress gradient distribution in VIA/Cu line configurations [4,7], the sensitivity of exploring the SIV risk can be different for SM test structures with different designs. Figure A.7 shows two types of VIA chains for SM testing in (a) and (b). In (a), a conventional VIA chain is designed with the VIAs located near the end of the metal lines. In (b), a VIA-in-the-middle (VIM) VIA chain is designed with the VIAs located in the middle of the metal lines. Due to the VIA location difference, the stress gradient distributions are quite different, i.e., single side towards the middle of line for (a) and both sides towards both ends of line for (b). The double side stress gradient distributions for VIM VIA chains in (b) determines that the sensitivity of SIV risk is higher for VIM than conventional VIA chains.

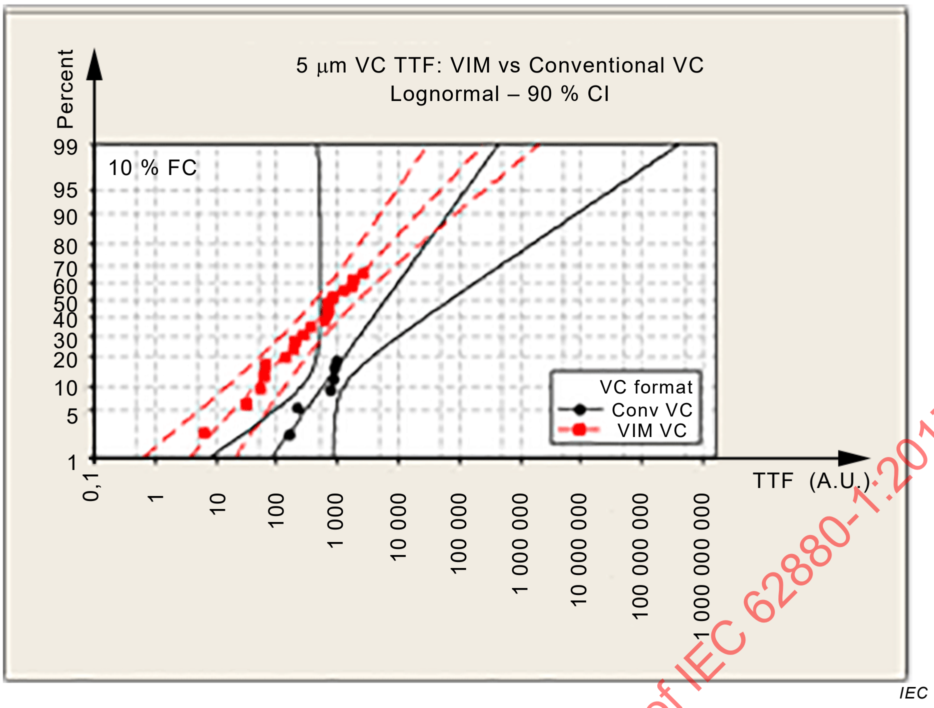


a) Conventional via chain **b) VIM via chain**

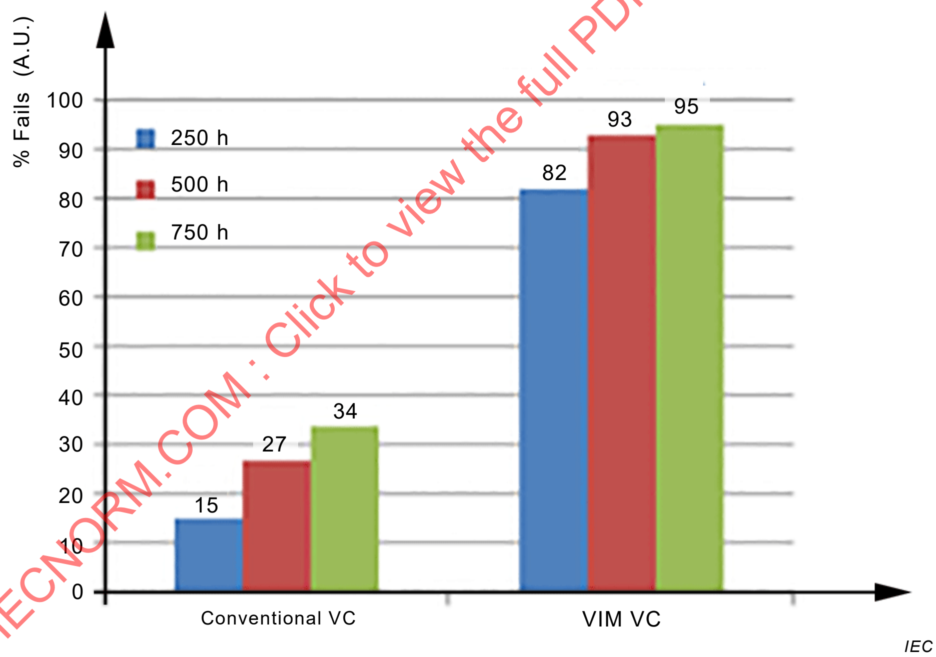
All colours indicate values of "stress gradient" with red colour on high side and blue colour on the low side of the values. Stress gradient is the difference of tensile stress between from the Cu plate and from the Cu via.

Figure A.7 – Stress profile of conventional and VIM VIA chains

Figure A.7 shows the comparison of results between conventional and VIM VIA chains from both PL-SM and wafer-level (WL) SM tests. PL-SM results show higher time-to-fail (TTF) values for conventional VIA chains in (a) while WL-SM results in (b) show higher failure percentage for VIM VIA chains at each readout of 250 h, 500 h and 750 h, respectively. Both tests were performed at 175 °C on 5,0 µm width VIA chains from 28 nm wafers. Both results indicate that the VIM VIA chains are more sensitive to SIV risk under the same linewidth and testing temperature. This is consistent with the stress gradient distribution shown in Figure A.8 and stress analysis studies in [4,7]. It is necessary to point out that in general, most of the VIA/metal line configurations in ICs products are VIM cases. Therefore, the types of VIM VIA chains or single VIA structures are recommended for SM qualification tests.



a)



b)

Figure A.8 – SM data of conventional and VIM VIA chains