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Universal serial bus interfaces for data and power – Part 1-3: Common components – USB Type-C® cable and connector specification

Interfaces de bus universel en série pour les données et l'alimentation électrique – Partie 1-3: Composants communs – Spécification des câbles et des connecteurs USB Type-C®



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Part 1-3: Common components – USB Type-C® cable and connector specification

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Draft	Report on voting
100/4139/CDV	100/4177/RVC

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Universal Serial Bus Type-C Cable and Connector Specification

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Contents

FOREWORD 2
Specification Editor 21
Specification Work Group Contributors 21
Pre-Release Draft Industry Reviewing Companies That Provided Feedback 29
Revision History 29
1 Introduction 30
1.1 Purpose 30
1.2 Scope 30
1.3 Related Documents 30
1.4 Conventions 31
1.4.1 Precedence 31
1.4.2 Keywords 31
1.4.3 Numbering 32
1.5 Terms and Abbreviations 32
2 Overview 37
2.1 Introduction 37
2.2 USB Type-C Receptacles, Plugs and Cables 38
2.3 Configuration Process 39
2.3.1 Source-to-Sink Attach/Detach Detection 39
2.3.2 Plug Orientation/Cable Twist Detection 40
2.3.3 Initial Power (Source-to-Sink) Detection and Establishing the Data (Host-to-Device) Relationship 40
2.3.4 USB Type-C VBUS Current Detection and Usage 41
2.3.5 *USB PD* Communications 41
2.3.6 Functional Extensions 42
2.4 VBUS 42
2.5 VCONN 42
2.6 Hubs 43
3 Mechanical 44
3.1 Overview 44
3.1.1 Compliant Connectors 44
3.1.2 Compliant Cable Assemblies 44
3.1.3 Compliant USB Type-C to Legacy Cable Assemblies 45
3.1.4 Compliant USB Type-C to Legacy Adapter Assemblies 46
3.2 USB Type-C Connector Mating Interfaces 46
3.2.1 Interface Definition 46

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3.2.2 Reference Designs 67
3.2.3 Pin Assignments and Descriptions 74
3.3 Cable Construction and Wire Assignments 75
3.3.1 Cable Construction (*Informative*) 75
3.3.2 Wire Assignments 77
3.3.3 Wire Gauges and Cable Diameters (*Informative*) 78
3.4 Standard USB Type-C Cable Assemblies 80
3.4.1 USB Full-Featured Type-C Cable Assembly 80
3.4.2 *USB 2.0* Type-C Cable Assembly 82
3.4.3 USB Type-C Captive Cable Assembly 82
3.4.4 USB Type-C Thumb Drive Assembly 83
3.5 Legacy Cable Assemblies 83
3.5.1 USB Type-C to *USB 3.1* Standard-A Cable Assembly 84
3.5.2 USB Type-C to *USB 2.0* Standard-A Cable Assembly 85
3.5.3 USB Type-C to *USB 3.1* Standard-B Cable Assembly 86
3.5.4 USB Type-C to *USB 2.0* Standard-B Cable Assembly 87
3.5.5 USB Type-C to *USB 2.0* Mini-B Cable Assembly 88
3.5.6 USB Type-C to *USB 3.1* Micro-B Cable Assembly 89
3.5.7 USB Type-C to *USB 2.0* Micro-B Cable Assembly 90
3.6 Legacy Adapter Assemblies 90
3.6.1 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly 90
3.6.2 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly 92
3.7 Electrical Characteristics 92
3.7.1 Raw Cable (*Informative*) 93
3.7.2 USB Type-C to USB Type-C Passive Cable Assemblies 94
3.7.3 Mated Connector (*Informative – USB 3.2* Gen2 and *USB4* Gen2) 116
3.7.4 Receptacle Connector SI Requirements and Testing (*Normative – USB4* Gen3/Gen4) 120
3.7.5 USB Type-C to USB Legacy Cable Assemblies (*Normative*) 122
3.7.6 USB Type-C to USB Legacy Adapter Assemblies (*Normative*) 126
3.7.7 Shielding Effectiveness Requirements (*Normative*) 129
3.7.8 DC Electrical Requirements (*Normative*) 131
3.8 Mechanical and Environmental Requirements (*Normative*) 133
3.8.1 Mechanical Requirements 134
3.8.2 Environmental Requirements 139
3.9 Docking Applications (*Informative*) 140
3.10 Implementation Notes and Design Guides 141
3.10.1 EMC Management (*Informative*) 141

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3.10.2 Stacked and Side-by-Side Connector Physical Spacing (*Informative*) 144
3.10.3 Cable Mating Considerations (*Informative*) 144
3.11 Extended Power Range (EPR) Cables 145
3.11.1 Electrical Requirements 145
3.11.2 EPR Cable Identification Requirements 145
4 Functional 146
4.1 Signal Summary 146
4.2 Signal Pin Descriptions 146
4.2.1 *USB 3.2*/*USB4* Pins 146
4.2.2 *USB 2.0* Pins 147
4.2.3 Auxiliary Signal Pins 147
4.2.4 Power and Ground Pins 147
4.2.5 Configuration Pins 147
4.3 Sideband Use (SBU) 147
4.4 Power and Ground 147
4.4.1 IR Drop 147
4.4.2 VBUS 148
4.4.3 VCONN 150
4.5 Configuration Channel (CC) 154
4.5.1 Architectural Overview 154
4.5.2 CC Functional and Behavioral Requirements 166
4.5.3 USB Port Interoperability Behavior 202
4.6 Power 219
4.6.1 Power Requirements during USB Suspend 220
4.6.2 VBUS Power Provided Over a USB Type-C Cable 221
4.7 USB Hubs 226
4.8 Power Sourcing and Charging 227
4.8.1 DFP as a Power Source 227
4.8.2 Non-USB Charging Methods 229
4.8.3 Sinking Host 230
4.8.4 Sourcing Device 230
4.8.5 Charging a System with a Dead Battery 230
4.8.6 USB Type-C Multi-Port Chargers 230
4.9 Electronically Marked Cables 234
4.9.1 Parameter Values 235
4.9.2 Active Cables 235
4.10 VCONN-Powered Accessories (VPAs) and VCONN-Powered USB Devices (VPDs) 236

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4.10.1 VCONN-Powered Accessories (VPAs) 236
4.10.2 VCONN-Powered Devices (VPDs) 236
4.11 Parameter Values 238
4.11.1 Termination Parameters 238
4.11.2 Timing Parameters 240
4.11.3 Voltage Parameters 243
5 *USB4* Discovery and Entry 245
5.1 Overview of the Discovery and Entry Process 245
5.2 *USB4* Functional Requirements 246
5.2.1 *USB4* Host Functional Requirements 246
5.2.2 USB Device Functional Requirements 246
5.2.3 *USB4* Alternate Mode Support 246
5.3 *USB4* Power Requirements 247
5.3.1 Source Power Requirements 247
5.3.2 Sink Power Requirements 247
5.3.3 Device Power Management Requirements 247
5.4 *USB4* Discovery and Entry Flow Requirements 248
5.4.1 USB Type-C Initial Connection 248
5.4.2 USB Power Delivery Contract 248
5.4.3 *USB4* Discovery and Entry Flow 248
5.4.4 *USB4* Post-Entry Operation 253
5.5 *USB4* Hub Connection Requirements 254
5.5.1 *USB4* Hub Port Initial Connection Requirements 254
5.5.2 *USB4* Hub UFP and Host Capabilities Discovery 254
5.5.3 Hub DFP Connection Requirements 255
5.5.4 Hub Ports Connection Behavior Flow Examples 255
5.5.5 Connecting to Downstream *USB4* Hubs 261
5.5.6 Fallback Functional Requirements for *USB4* Hubs 261
5.6 *USB4* Device Connection Requirements 261
5.6.1 Fallback Mapping of *USB4* Peripheral Functions of USB Device Class Types 261
5.7 Parameter Values 263
5.7.1 Timing Parameters 263
6 Active Cables 264
6.1 General Specifications for All Active Cables 264
6.1.1 Discovering Active Cable Characteristics 264
6.1.2 Electrical Requirements 266
6.1.3 Mechanical Requirements 298

IECNORM.COM : Click to view the full PDF of IEC 62680-1-3:2024

6.2 Additional Specifications for Copper and Hybrid-Optical Active Cables 299
6.2.1 Active Cable Block Diagram 300
6.2.2 *USB4* Asymmetric Mode Support 300
6.2.3 Active Cable *USB PD* Requirements 300
6.2.4 Active Cable Behaviors in Response to *USB PD* Events 300
6.2.5 Active Cable Power Requirements 301
6.3 Additional Specifications for Optically Isolated Active Cables 301
6.3.1 OIAC Block Diagrams 302
6.3.2 OIAC Limitations and General Requirements 304
6.3.3 OIAC Cable Power Requirements 305
6.3.4 OIAC *USB PD* Requirements 305
6.3.5 OIAC Connection Flow and State Diagrams 315
6.3.6 Additional Electrical Requirements for OIAC 333
6.3.7 Additional Mechanical Requirements for OIAC 336
A Liquid Corrosion Mitigation Mode 337
A.1 Overview 337
A.2 Detail 337
A.3 Liquid Detection Methods 339
A.3.1 Liquid Measurement Method 339
A.3.2 Pulsed Measurement Method 339
A.3.3 Impedance Measurement Method 340
A.4 Liquid Detection Pins in the Connector 343
B Debug Accessory Mode 346
B.1 Overview 346
B.2 Functional 346
B.2.1 Signal Summary 346
B.2.2 Port Interoperability 347
B.2.3 Debug Accessory Mode Entry 347
B.2.4 Connection State Diagrams 347
B.2.5 DTS Port Interoperability Behaviors 356
B.2.6 Orientation Detection 365
B.3 Security/Privacy Requirements 365
C USB Type-C Digital Audio 366
C.1 Overview 366
C.2 USB Type-C Digital Audio Specifications 366
D Thermal Design Considerations for Active Cables 367
D.1 Introduction 367

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D.2 Model 367
D.2.1 Assumptions 367
D.2.2 Model Architecture 368
D.2.3 Heat Sources 368
D.2.4 Heat Flow 369
D.3 *USB 3.2* Single-Lane Active Cable 370
D.3.1 *USB 3.2* Single-Lane Active Cable Design Considerations 370
D.4 Dual-Lane Active Cables 373
D.4.1 *USB 3.2* Dual-Lane Active Cable Design Considerations 373
D.4.2 *USB 3.2* Dual-Lane Active Cable in a Multiple Port Configuration 375
D.5 *USB 3.2* Host and Device Design Considerations 376
D.5.1 Heat Spreading or Heat Sinking from Host or Device 376
D.5.2 Motherboard Temperature Control 377
D.5.3 Wider Port Spacing for Multi-Port Applications 377
D.5.4 Power Policies 377
E Alternate Modes 378
E.1 Alternate Mode Architecture 378
E.2 Alternate Mode Requirements 378
E.2.1 Alternate Mode Pin Reassignment 379
E.2.2 Alternate Mode Electrical Requirements 379
E.3 Parameter Values 382
E.4 Example Alternate Mode – USB DisplayPort™ Dock 383
E.4.1 USB DisplayPort™ Dock Example 383
E.4.2 Functional Overview 383
E.4.3 Operational Summary 384
E.5 Example Alternate Mode Entry Flow with Cable Warnings 385
E.5.1 Operational Summary 386
F Thunderbolt™ 3 Compatibility Discovery and Entry 387
F.1 *TBT3* Compatibility Mode Functional Requirements 387
F.1.1 *TBT3*-Compatible Power Requirements 387
F.1.2 *TBT3*-Compatible Host Requirements 387
F.1.3 *TBT3*-Compatible Device Upstream Requirements 387
F.1.4 *TBT3*-Compatible Device Downstream Requirements 387
F.1.5 *TBT3*-Compatible Self-Powered Device Without Predefined Upstream Port Rules 388
F.1.6 *TBT3*-Compatible Devices with a Captive Cable 388
F.2 *TBT3* Discovery and Entry Flow 388
F.2.1 *TBT3* Passive Cable Discover Identity Responses 389

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F.2.2 *TBT3* Active Cable Discover Identity Responses 392
F.2.3 *TBT3* Device Discover Identity Responses 395
F.2.4 *TBT3* Discover SVID Responses 396
F.2.5 *TBT3* Device Discover Mode Responses 397
F.2.6 *TBT3* Cable Discover Mode Responses 398
F.2.7 *TBT3* Cable Enter Mode Command 399
F.2.8 *TBT3* Device Enter Mode Command 400
F.2.9 *TBT3* Cable Functional Difference Summary 402
G Extracting Pulse Response from Sampled Data and Calculating Non-Linearity Noise 403
H *USB PD* High-Voltage Design Considerations 405
H.1 Potential for Arcing Damage During Cable Withdrawal 405
H.2 Arcing During USB Type-C Cable Withdrawal 405
H.3 Mitigating Arcing Damage During Cable Withdrawal Due to Sink Discharge 407
H.3.1 Limiting Sink Discharge Rate 408
H.3.2 Load Removal 409
H.3.3 Limiting Source Current Capability 412
I *USB PD* Encoding Guidelines for USB Type-C Product Types 413
I.1 USB Type-C Product Type Definitions and *USB PD* Encodings 413
I.2 *USB PD* Encoding Guidelines Tables 414
I.3 Detailed Examples 421
I.3.1 *USB 3.2* Host – no DC – Power Consumer : DRP (Source or Sink) / Not DRD (DFP) 421
I.3.2 *USB 3.2* Peripheral – Power Provider : DRP (Source or Sink) / Not DRD (UFP) 421
I.3.3 *USB4* Host – Power Consumer : DRP (Source or Sink) / Not DRD (DFP) 422
I.3.4 *USB4* Host – *USB4* DC – Partial or no USB Equivalent : DRP (Source or Sink) / DRD 422
I.3.5 *USB4* Peripheral : UFP (Sink) 423
I.3.6 *USB4* Dock (Upstream) – Power Provider : DRP (Source or Sink) / Not DRD (UFP) 424
I.3.7 *USB4* Hub (Downstream) – DFP (Source) 424
J Design Assumptions for the *USB4* Gen4 LRD Cable Specification 426

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Figures

Figure 2-1 USB Type-C Receptacle Interface (Front View) 37
Figure 2-2 USB Full-Featured Type-C Plug Interface (Front View) 38
Figure 3-1 USB Type-C Receptacle Interface Dimensions 49
Figure 3-2 Reference Design USB Type-C Plug External EMC Spring Contact Zones 52
Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions 53
Figure 3-4 Reference Footprint for a USB Type-C Vertical Mount Receptacle (*Informative*) 56
Figure 3-5 Reference Footprint for a USB Type-C Dual-Row SMT Right-Angle Receptacle (*Informative*) 57
Figure 3-6 Reference Footprint for a USB Type-C Hybrid Right-Angle Receptacle (*Informative*) 58
Figure 3-7 Reference Footprint for a USB Type-C Mid-Mount Dual-Row SMT Receptacle (*Informative*) 59
Figure 3-8 Reference Footprint for a USB Type-C Mid-Mount Hybrid Receptacle (*Informative*) 60

Figure 3-9 Reference Footprint for a *USB 2.0* Type-C Through Hole Right Angle Receptacle (*Informative*) 61
Figure 3-10 Reference Footprint for a *USB 2.0* Type-C Single Row Right Angle Receptacle (*Informative*) 62
Figure 3-11 *USB 2.0* Type-C Plug Interface Dimensions 63
Figure 3-12 USB Type-C Plug EMC Shielding Spring Tip Requirements 66
Figure 3-13 Reference Design of Receptacle Mid-Plate 67
Figure 3-14 Reference Design of Retention Latch 68
Figure 3-15 Illustration of the Latch Soldered to the Paddle Card Ground 68
Figure 3-16 Reference Design of the USB Full-Featured Type-C Plug Internal EMC Spring 69
Figure 3-17 Reference Design of the *USB 2.0* Type-C Plug Internal EMC Spring 70
Figure 3-18 Reference Design of Internal EMC Pad 71
Figure 3-19 Reference Design of a USB Type-C Receptacle with External EMC Springs 72
Figure 3-20 Reference Design of a USB Full-Featured Type-C Plug Paddle Card 73
Figure 3-21 Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example with VCONN 76
Figure 3-22 Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example without VCONN 76
Figure 3-23 USB Full-Featured Type-C Standard Cable Assembly 80
Figure 3-24 USB Type-C to *USB 3.1* Standard-A Cable Assembly 84
Figure 3-25 USB Type-C to *USB 2.0* Standard-A Cable Assembly 85
Figure 3-26 USB Type-C to *USB 3.1* Standard-B Cable Assembly 86
Figure 3-27 USB Type-C to *USB 2.0* Standard-B Cable Assembly 87
Figure 3-28 USB Type-C to *USB 2.0* Mini-B Cable Assembly 88
Figure 3-29 USB Type-C to *USB 3.1* Micro-B Cable Assembly 89
Figure 3-30 USB Type-C to *USB 2.0* Micro-B Cable Assembly 90
Figure 3-31 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly 91
Figure 3-32 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly 92
Figure 3-33 Illustration of Test Points for a Mated Cable Assembly 94
Figure 3-34 Recommended Differential Insertion Loss Requirement (*USB 3.2* Gen2 and *USB4* Gen2) 95
Figure 3-35 Recommended Differential Return Loss Requirement 95
Figure 3-36 Recommended Differential Crosstalk Requirement 96
Figure 3-37 Recommended Differential Near-End and Far-End Crosstalk Requirement between USB D+/D– Pair and TX/RX Pair 97
Figure 3-38 Recommended Differential Insertion Loss Requirement (*USB4* Gen3/Gen4) 97
Figure 3-39 Illustration of Insertion Loss Fit at Nyquist Frequency 98
Figure 3-40 Input Pulse Spectrum 99
Figure 3-41 IMR Limit as Function of ILfitatNq 100
Figure 3-42 IRL Limit as Function of ILfitatNq 102
Figure 3-43 Differential-to-Common Mode Conversion Requirement 102
Figure 3-44 IMR Limit as Function of ILfit at 10 GHz (*USB4* Gen3/Gen4) 106
Figure 3-45 Definition of Port, Victim, and Aggressor 107
Figure 3-46 IXT_DP and IXT_USB Limit as Function of ILfit at 10 GHz (*USB4* Gen3/Gen4) 107
Figure 3-47 IRL Limit as Function of ILfit at 10 GHz (*USB4* Gen3/Gen4) 108
Figure 3-48 Differential-to-Common Mode Conversion Requirement (*USB4* Gen3/Gen4) 108
Figure 3-49 Cable Assembly in System 109
Figure 3-50 Requirement for Differential Coupling between CC and D+/D– 112
Figure 3-51 Requirement for Single-Ended Coupling between CC and D– in *USB 2.0* Type-C Cables 112
Figure 3-52 Requirement for Single-Ended Coupling between CC and D– in USB Full-Featured Type-C Cables 113
Figure 3-53 Requirement for Differential Coupling between VBUS and D+/D– 113
Figure 3-54 Requirement for Single-Ended Coupling between SBU_A and SBU_B 114
Figure 3-55 Requirement for Single-Ended Coupling between SBU_A/SBU_B and CC 115

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Figure 3-56 Requirement for Coupling between SBU_A and differential D+/D−, and SBU_B and differential D+/D− 115
Figure 3-57 Illustration of USB Type-C Mated Connector 116
Figure 3-58 Recommended Impedance Limits of a USB Type-C Mated Connector 117
Figure 3-59 Recommended Ground Void Dimensions for USB Type-C Receptacle 117
Figure 3-60 Recommended Differential Near-End and Far-End Crosstalk Limits between D+/D− Pair and TX/RX Pairs 119
Figure 3-61 Recommended Limits for Differential-to-Common-Mode Conversion 120
Figure 3-62 IMR Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly 125
Figure 3-63 IRL Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly 125
Figure 3-64 Cable Assembly Shielding Effectiveness Testing 129
Figure 3-65 Shielding Effectiveness Pass/Fail Criteria 130
Figure 3-66 LLCR Measurement Diagram 131
Figure 3-67 Temperature Measurement Point 132
Figure 3-68 Example Current Rating Test Fixture Trace Configuration 133
Figure 3-69 Example of 4-Axis Continuity Test Fixture 135
Figure 3-70 Example Wrenching Strength Test Fixture for Plugs without Overmold 137
Figure 3-71 Reference Wrenching Strength Continuity Test Fixture 138
Figure 3-72 Example of Wrenching Strength Test Mechanical Failure Point 138
Figure 3-73 Wrenching Strength Test with Cable in Fixture 139
Figure 3-74 USB Type-C Cable Receptacle Flange Example 141
Figure 3-75 EMC Guidelines for Side Latch and Mid-Plate 142
Figure 3-76 EMC Finger Connections to Plug Shell 142
Figure 3-77 EMC Pad Connections to Receptacle Shell 143
Figure 3-78 Examples of Connector Apertures 143
Figure 3-79 Recommended Minimum Spacing between Connectors 144
Figure 3-80 Recommended Minimum Plug Overmold Clearance 144
Figure 3-81 Cable Plug Overmold and an Angled Surface 145
Figure 4-1 Cable IR Drop 148
Figure 4-2 Cable IR Drop for powered cables 148
Figure 4-3 Logical Model for Single-Lane Data Bus Routing across USB Type-C-based Ports 155
Figure 4-4 Logical Model for USB Type-C-based Ports for a Single-Lane Direct Connect Device 155
Figure 4-5 Pull-Up/Pull-Down CC Model 157
Figure 4-6 Current Source/Pull-Down CC Model 157
Figure 4-7 Source Functional Model for CC1 and CC2 160
Figure 4-8 Source Functional Model Supporting *USB PD* PR_Swap 161
Figure 4-9 Sink Functional Model for CC1 and CC2 161
Figure 4-10 Sink Functional Model Supporting *USB PD* PR_Swap and VCONN_Swap 162
Figure 4-11 DRP Functional Model for CC1 and CC2 163
Figure 4-12 Connection State Diagram: Source 168
Figure 4-13 Connection State Diagram: Sink 169
Figure 4-14 Connection State Diagram: Sink with Accessory Support 170
Figure 4-15 Connection State Diagram: DRP 171
Figure 4-16 Connection State Diagram: DRP with Accessory and Try.SRC Support 172
Figure 4-17 Connection State Diagram: DRP with Accessory and Try.SNK Support 173
Figure 4-18 Connection State Diagram: Charge-Through VPD 174
Figure 4-19 Sink Power Sub-States 196
Figure 4-20 Passive Cable eMarker State Diagram 198
Figure 4-21 Active Cable eMarker State Diagram 198
Figure 4-22 Cable Ra Management State Diagram 199
Figure 4-23 Source to Sink Functional Model 202

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Figure 4-24 Source to DRP Functional Model 203
Figure 4-25 DRP to Sink Functional Model 204
Figure 4-26 DRP to DRP Functional Model – CASE 1 205
Figure 4-27 DRP to DRP Functional Model – CASES 2 & 3 206
Figure 4-28 Source to Source Functional Model 208
Figure 4-29 Sink to Sink Functional Model 208
Figure 4-30 DRP to VPD Model 209
Figure 4-31 Example DRP to Charge-Through VPD Model 210
Figure 4-32 Source to Legacy Device Port Functional Model 217
Figure 4-33 Legacy Host Port to Sink Functional Model 217
Figure 4-34 DRP to Legacy Device Port Functional Model 218
Figure 4-35 Legacy Host Port to DRP Functional Model 219
Figure 4-36 Sink Monitoring for Current in Pull-Up/Pull-Down CC Model 222
Figure 4-37 Sink Monitoring for Current in Current Source/Pull-Down CC Model 223
Figure 4-38 *USB PD* over CC Pins 224
Figure 4-39 *USB PD* BMC Signaling over CC 224
Figure 4-40 USB Type-C Cable's Output as a Function of Load for Non-PD-based USB Type-C Charging 228
Figure 4-41 0 – 3 A *USB PD*-based Charger USB Type-C Cable's Output as a Function of Load 229
Figure 4-42 3 – 5 A *USB PD*-based Charger USB Type-C Cable's Output as a Function of Load 229
Figure 4-43 Electronically Marked Cable with VCONN connected through the cable 235
Figure 4-44 Electronically Marked Cable with SOP' at both ends 235
Figure 4-45 Example Charge-Through VCONN-Power USB Device Use Case 238
Figure 4-46 DRP Timing 240
Figure 5-1 *USB4* Discovery and Entry Flow Model 249
Figure 5-2 *USB4* Hub with *USB4* Host and Device Connection Flow Alignment 256
Figure 5-3 *USB4* Hub with *USB 3.2* Host and *USB4* Device Connection Flow Alignment 257
Figure 5-4 *USB4* Hub with *USB4* Host and *USB 3.2* Device Connection Flow Alignment 258
Figure 5-5 *USB4* Hub with *USB 3.2* Host and Device Connection Flow Alignment 259
Figure 5-6 *USB4* Hub with *USB4* Host and DP Alt Mode Device Connection Flow Alignment 260
Figure 5-7 *USB4* Hub with *USB 3.2* Host and DP Alt Mode Device Connection Flow Alignment 261
Figure 6-1 Active Cable Topologies 267
Figure 6-2 SuperSpeed USB Electrical Test Points 270
Figure 6-3 SuperSpeed USB Compliance Test Setup 270
Figure 6-4 Compliance Points Definition 273
Figure 6-5 RX Differential Return-Loss Mask 274
Figure 6-6 Re-timer-based Active Cable Compliance Test Setup 275
Figure 6-7 Example of Transmitter Frequency Variation During Clock Switching 277
Figure 6-8 Active Cable Functional Test Setup 278
Figure 6-9 Linear Re-driver-based Active Cable Compliance Setup 279
Figure 6-10 Gain Parameters Specified for the Linear Re-driver Active Cable 282
Figure 6-11 OUTPUT_NOISE Limit Versus *ILfitatNq* 283
Figure 6-12 Gain Parameters for *USB4* Gen4 LRD Active Cables 286
Figure 6-13 *USB4* LRD Active Cable Snooping of TxFFE Negotiation 291
Figure 6-14 *USB4* State Machine per Channel (*Informative*) 292
Figure 6-15 *USB4* Gen4 CL1/CL2 Exit Flow with LRD Active Cable 294
Figure 6-16 *USB4* Symmetric to Asymmetric Transition 295
Figure 6-17 *USB4* Asymmetric to Symmetric Transition 297
Figure 6-18 OIAC *USB PD* Message Forwarding 310
Figure 6-19 OIAC Successful Data Role Swap 313
Figure 6-20 OIAC Rejected Data Role Swap 313
Figure 6-21 OIAC Wait Data Role Swap 314

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Figure 6-22 OIAC Initiator Reject Data Role Swap 314
Figure 6-23 OIAC Initiator Wait Data Role Swap 315
Figure 6-24 OIAC Discovery – Phase 1 317
Figure 6-25 OIAC Reboot – Phase 2 318
Figure 6-26 OIAC Plug-A Configured as DFP – Phase 3 319
Figure 6-27 OIAC Plug-A Configured as UFP – Phase 3 320
Figure 6-28 OIAC Plug-A No Connection Possible Billboard – Phase 3 321
Figure 6-29 OIAC Plug-A State Diagram Part 1 (Phase 1 and 2) 322
Figure 6-30 OIAC Plug-A State Diagram Part 2 (Phase 3) 323
Figure 6-31 OIAC Plug-B State Diagram 329
Figure 6-32 Illustration of Usages for OIAC that Require an Adapter or Hub 335
Figure A-1 Electrolytic Liquid Corrosion Example 337
Figure A-2 Corrosion Mitigation in Pull-Up/Pull-Down CC Model 338
Figure A-3 Corrosion Mitigation in Current Source/Pull-Down CC Model 338
Figure A-4 Corrosion Mitigation in Current Source/Pull-Down CC Model with Alternate Mitigation 338
Figure A-5 Liquid Detection by Leakage Measurement 339
Figure A-6 Liquid Detection by Pulsed Measurement 340
Figure A-7 Example Measurement of a Dry Port 341
Figure A-8 Example Measurement of a Port with Reverse Osmosis Water 341
Figure A-9 Example Measurement of a Port with Tap Water 342
Figure A-10 Example Measurement of a Port with Artificial Sweat 342
Figure A-11 Example Measurement of a Port with Ocean Water 343
Figure A-12 Example Liquid Detect Pin(s)/Pad(s) Location Area 344
Figure A-13 Example Liquid Detect Pad Along All Connector Pins 344
Figure A-14 Example Liquid Detect Pins Adjacent to V_{BUS}/SBU/CC 345
Figure A-15 Example Liquid Detect Connector Surface Mount View 345
Figure B-1 USB Type-C Debug Accessory Layered Behavior 346
Figure B-2 DTS Plug Interface 346
Figure B-3 Connection State Diagram: DTS Source 348
Figure B-4 Connection State Diagram: DTS Sink 349
Figure B-5 Connection State Diagram: DTS DRP 350
Figure B-6 TS Sink Power Sub-States 354
Figure D-1 Active Cable Model (Single Port, Top Mount Receptacle) 368
Figure D-2 Model Architecture 368
Figure D-3 Heat Sources and Heat Flow Paths 369
Figure D-4 Vertically Stacked Horizontal Connectors 3x1 Configuration (VERT) 370
Figure D-5 Horizontally Stacked Vertical Connectors 1x3 Configuration (HZ90) 371
Figure D-6 Horizontally Stacked Horizontal Connectors 1x3 Configuration (HORZ) 371
Figure D-7 *USB 3.2* Single-Lane 3A Active Cable in a 3-Port Configuration 372
Figure D-8 *USB 3.2* Single-Lane 5A Active Cable in a 3-Port Configuration 372
Figure D-9 Impact of Overmold Power P_O and Thermal Boundary Temperature T_{MB} at 3 A V_{BUS} in a Single Port Configuration 374
Figure D-10 Impact of Overmold Power P_O and Thermal Boundary Temperature T_{MB} at 5 A V_{BUS} in a Single Port Configuration 374
Figure D-11 *USB 3.2* Active Cable Dongle Design (One End Shown) 375
Figure D-12 *USB 3.2* Dual-Lane 3A Active Cable in a 3-Port Configuration 375
Figure D-13 *USB 3.2* Dual-Lane 5A Active Cable in a 3-Port Configuration 376
Figure D-14 Example: Additional Heat Spreader on Receptacle in Host or Device 377
Figure D-15 Example: Heat Sinking on Chassis of Host or Device 377
Figure E-1 Pins Available for Reconfiguration over the Full-Featured Cable 379
Figure E-2 Pins Available for Reconfiguration for Direct Connect Applications 379

IECNORM.COM : Click to view the full PDF of IEC 62680-1-3:2024

Figure E-3 Alternate Mode Implementation using a USB Type-C to USB Type-C Cable 381
Figure E-4 Alternate Mode Implementation using a USB Type-C to Alternate Mode Cable or Device 381
Figure E-5 USB DisplayPort Dock Example 383
Figure E-6 *USB4* DFP Mode Entry Flow Example 385
Figure F-1 *TBT3* Discovery Flow 389
Figure H-1 Arcing Damage to USB Type-C VBUS Contacts 405
Figure H-2 Arcing Due to Discharge 406
Figure H-3 Arcing Prevention During Sink Discharge by Limiting Slew Rate 408
Figure H-4 Arcing Prevention During Sink Discharge by Load Removal 410

Tables

Table 2-1 Summary of power supply options 42
Table 3-1 USB Type-C Standard Cable Assemblies 45
Table 3-2 USB Type-C Legacy Cable Assemblies 46
Table 3-3 USB Type-C Legacy Adapter Assemblies 46
Table 3-4 USB Type-C Receptacle Interface Pin Assignments 74
Table 3-5 USB Type-C Receptacle Interface Pin Assignments for *USB 2.0*-only Support 75
Table 3-6 USB Type-C Standard Cable Wire Assignments 77
Table 3-7 USB Type-C Cable Wire Assignments for Legacy Cables/Adapters 78
Table 3-8 Reference Wire Gauges for standard USB Type-C Cable Assemblies 79
Table 3-9 Reference Wire Gauges for standard USB Type-C to Legacy Cable Assemblies 79
Table 3-10 USB Full-Featured Type-C Standard Cable Assembly Wiring 81
Table 3-11 *USB 2.0* Type-C Standard Cable Assembly Wiring 82
Table 3-12 USB Type-C to *USB 3.1* Standard-A Cable Assembly Wiring 84
Table 3-13 USB Type-C to *USB 2.0* Standard-A Cable Assembly Wiring 85
Table 3-14 USB Type-C to *USB 3.1* Standard-B Cable Assembly Wiring 86
Table 3-15 USB Type-C to *USB 2.0* Standard-B Cable Assembly Wiring 87
Table 3-16 USB Type-C to *USB 2.0* Mini-B Cable Assembly Wiring 88
Table 3-17 USB Type-C to *USB 3.1* Micro-B Cable Assembly Wiring 89
Table 3-18 USB Type-C to *USB 2.0* Micro-B Cable Assembly Wiring 90
Table 3-19 USB Type-C to *USB 3.1* Standard-A Adapter Assembly Wiring 91
Table 3-20 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly Wiring 92
Table 3-21 Differential Insertion Loss Examples for USB TX/RX with Twisted Pair Construction 93
Table 3-22 Differential Insertion Loss Examples for USB TX/RX with Coaxial Construction 94
Table 3-23 Key Parameters in COM Configuration File 110
Table 3-24 Electrical Requirements for CC and SBU Wires 111
Table 3-25 Coupling Matrix for Low Speed Signals 111
Table 3-26 Maximum Mutual Inductance (M) between VBUS and Low Speed Signal Lines 114
Table 3-27 USB D+/D– Signal Integrity Requirements for USB Type-C to USB Type-C Passive Cable Assemblies 116
Table 3-28 USB Type-C Mated Connector Recommended Signal Integrity Characteristics (*Informative*) 118
Table 3-29 USB Type-C Receptacle Connector Signal Integrity Characteristics for *USB4* Gen3 (*Normative*) 121
Table 3-30 USB D+/D– Signal Integrity Requirements for USB Type-C to Legacy USB Cable Assemblies (*Normative*) 122
Table 3-31 Design Targets for USB Type-C to *USB 3.1* Gen2 Legacy Cable Assemblies (*Informative*) 123
Table 3-32 USB Type-C to *USB 3.1* Gen2 Legacy Cable Assembly Signal Integrity Requirements (*Normative*) 124
Table 3-33 USB D+/D– Signal Integrity Requirements for USB Type-C to Legacy USB Adapter Assemblies (*Normative*) 126
Table 3-34 Design Targets for USB Type-C to *USB 3.1* Standard-A Adapter Assemblies (*Informative*) 127

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Table 3-35 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly Signal Integrity Requirements (*Normative*) 128
Table 3-36 Current Rating Test PCB 132
Table 3-37 Maximum DC Resistance Requirement (*Normative*) 133
Table 3-38 Force and Moment Requirements 136
Table 3-39 Environmental Test Conditions 139
Table 3-40 Reference Materials 140
Table 4-1 USB Type-C List of Signals 146
Table 4-2 VBUS Source Characteristics 149
Table 4-3 VBUS Sink Characteristics 149
Table 4-4 USB Type-C Source Port's VCONN Requirements Summary 150
Table 4-5 VCONN Source Characteristics 150
Table 4-6 Cable VCONN Sink Characteristics 151
Table 4-7 VCONN-Powered Accessory (VPA) Sink Characteristics 152
Table 4-8 VCONN-Powered Device (VPD) Sink Characteristics 153
Table 4-9 USB Type-C Port Interoperability 156
Table 4-10 Source Perspective 158
Table 4-11 Source (Host) and Sink (Device) Behaviors by State 158
Table 4-12 Recommended Implementation of Try.SRC and Try.SNK for Dual-Role Ports with Preferred Roles 165
Table 4-13 *USB PD* Swapping Port Behavior Summary 165
Table 4-14 Use of Power and Data Role Swaps for Dual-Role Ports with Preferred Roles 166
Table 4-15 Power Role Behavioral Model Summary 166
Table 4-16 Source Port CC Pin State 175
Table 4-17 Sink Port CC Pin State 175
Table 4-18 Mandatory and Optional States 200
Table 4-19 Precedence of Power Source Usage 220
Table 4-20 USB Type-C Current Advertisement and PDP Equivalent 222
Table 4-21 Sink Maximum Current Limit When Attached to CTVPD 225
Table 4-22 Example Charge-Through VPD Sink Maximum Currents based on VBUS Impedance and GND Impedance 226
Table 4-23 Examples of 4-port Shared Capacity Chargers and Power Sharing Policies 232
Table 4-24 SOP' and SOP" Timing 235
Table 4-25 Charge-Through VPD CC Impedance (RccCON) Requirements 237
Table 4-26 CTVPD Charge-Through Port VBUS Bypass Requirements 237
Table 4-27 Source CC Termination (Rp) Requirements 238
Table 4-28 Sink CC Termination (Rd) Requirements 239
Table 4-29 Powered Cable Termination Requirements 239
Table 4-30 CC Termination Requirements for Disabled state, ErrorRecovery state, and Unpowered Source 239
Table 4-31 SBU Termination Requirements 239
Table 4-32 VBUS and VCONN Timing Parameters 240
Table 4-33 DRP Timing Parameters 241
Table 4-34 CC Timing Parameters 242
Table 4-35 CC Voltages on Source Side – Default USB 243
Table 4-36 CC Voltages on Source Side – 1.5 A @ 5 V 243
Table 4-37 CC Voltages on Source Side – 3.0 A @ 5 V 243
Table 4-38 Voltages on Sink CC Pins – Default USB Type-C Current Only 243
Table 4-39 Voltages on Sink CC Pins – Multiple Source Current Advertisements 244
Table 4-40 CC Pin Clamping Voltage 244
Table 5-1 Certified Cables Where *USB4*-compatible Operation is Expected 251
Table 5-2 Fallback Mapping *USB4* Functions to USB Device Class Types 262

IECNORM.COM : Click to view the full PDF of IEC 62680-1-3:2024

Table 5-3 USB Billboard Device Class Availability Following *USB4* Device Entry Failure 263
Table 6-1 *USB4* Cable Identity Summary 265
Table 6-2 Active Cable Features 266
Table 6-3 Active Cable SBU Requirements 267
Table 6-4 Active Cable Power-on Requirements 268
Table 6-5 Maximum *USB 3.2* U0 Delay 269
Table 6-6 *USB 3.2* U-State Requirements 269
Table 6-7 Active Cable *USB 3.2* Stressed Source Swing, TP1 271
Table 6-8 Active Cable *USB 3.2* Stressed Source Jitter, TP1 271
Table 6-9 Active Cable *USB 3.2* Input Swing at TP2 (*Informative*) 272
Table 6-10 Active Cable *USB 3.2* Output Swing at TP3 (*Informative*) 272
Table 6-11 Compliance Points Definition 273
Table 6-12 *USB4* CL-State Requirements for Active Cables 274
Table 6-13 Re-timer-based *USB4* Active Cable Output Specifications Applied for All Speeds (at TP3') 276
Table 6-14 Stressed Receiver Conditions for *USB4* Gen2 and Gen3 Cable Compliance Testing (at TP2) 278
Table 6-15 Linear Re-driver-based Active Cable Output Parameters 280
Table 6-16 Input Signal at TP2 for Compliance Testing 281
Table 6-17 *USB4* Gen4 LRD-based Active Cable ILfitMask Limits 285
Table 6-18 *USB4* Gen4 LRD-based Active Cable Wiring Diagram for Compliance 287
Table 6-19 *USB4* Gen4 Active Cable SBx Transaction Snooping 288
Table 6-20 *USB4* LRD Active Cable Logical Timing Parameters 289
Table 6-21 *USB4* LRD Tuning Register Snooping 298
Table 6-22 Cable Temperature Requirements 299
Table 6-23 OIAC *USB PD* Message Handling 306
Table 6-24 Recommended OIAC Sink_Capabilities PDO (SOP) on Initial Connection 307
Table 6-25 Recommended OIAC Sink_Capabilities PDO (SOP) on Active Connection 307
Table 6-26 Recommended OIAC Active Sink RDO (SOP) 308
Table 6-27 OIAC *USB PD* Message Timing 311
Table 6-28 Port and Plug Capabilities 316
Table 6-29 *USB 3.2* U-State Requirements 335
Table 6-30 *USB4* CL-State Requirements for OIAC 336
Table A-1 Example Measurement Test Conditions 340
Table B-1 DTS to TS Port Interoperability 347
Table B-2 Rp/Rp Charging Current Values for a DTS Source 354
Table B-3 Mandatory and Optional States 356
Table D-1 Heat Sources and Heat Dissipation Example (1.5 W cable and 5 A) 369
Table D-2 *USB 3.2* Active Cable Design Single Port Case Study at 35 °C Ambient and 60 °C Thermal Boundary (Single Lane) 370
Table D-3 *USB 3.2* Active Cable Design Single Port Case Study at 35 °C Ambient and 60 °C Thermal Boundary (Dual Lane) 373
Table E-1 USB Safe State Electrical Requirements 382
Table E-2 USB Billboard Device Class Availability Following Alternate Mode Entry Failure 382
Table E-3 Alternate Mode Signal Noise Ingression Requirements 382
Table F-1 *TBT3* Passive Cable Discovery Identity VDO Responses 390
Table F-2 *TBT3* Passive Cable VDO for *USB PD* Revision 2.0, Version 1.3 391
Table F-3 *TBT3* Passive Cable VDO for *USB PD* Revision 3.0, Version 1.2 391
Table F-4 *TBT3* Active Cable Discovery Identity VDO Responses 392
Table F-5 *TBT3* Active Cable VDO for *USB PD* Revision 2.0, Version 1.3 393
Table F-6 *TBT3* Active Cable VDO 1 for *USB PD* Revision 3.0, Version 1.2 393
Table F-7 *TBT3* Active Cable VDO 2 for *USB PD* Revision 3.0, Version 1.2 394
Table F-8 *TBT3* Device Discovery Identity VDO Responses 395

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Table F-9 *TBT3* Discover SVID VDO Responses....396
Table F-10 *TBT3* Device Discover Mode VDO Responses....397
Table F-11 *TBT3* Cable Discover Mode VDO Responses....398
Table F-12 *TBT3* Cable Enter Mode Command....399
Table F-13 *TBT3* Device Enter Mode Command....400
Table F-14 *TBT3* Cable Functional Difference Summary....402
Table G-1 Linear Fit Pulse Extraction Parameters....404
Table I-1 USB Type-C Product Example Clarifying Notes....415
Table I-2 *USB PD* Encoding Guidelines for Example Products....418

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Pre-Release Draft Industry Reviewing Companies That Provided Feedback

Aces	JST Mfg. Co., Ltd.	Pericom
Fairchild Semiconductor	Korea Electric Terminal	Semtech Corporation
Fujitsu Ltd.	Marvell Semiconductor	Silicon Image
Industrial Technology Research Institute (ITRI)	Motorola Mobility LLC	SMK Corporation
Joinsoon Electronics Mfg. Co. Ltd.	PalCONN/PalNova (Palpilot International Corp.)	Toshiba Corporation

Revision History

Release	Date	Description
1.0	August 11, 2014	Initial Release
1.1	April 3, 2015	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
1.2	March 25, 2016	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
1.3	July 14, 2017	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
1.4	March 29, 2019	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
2.0	August 2019	New release primarily for enabling ***USB4*** over USB Type-C connectors and cables. Also includes incorporation of all approved ECNs as of the revision date plus editorial clean-up.
2.1	May 2021	New release primarily for enabling Extended Power Range (EPR) and defining EPR cables aligning with ***USB Power Delivery*** Specification R3.1 V1.0. Also includes incorporation of all approved ECNs as the revision date plus editorial clean-up.
2.2	October 2022	New release primarily for enabling ***USB4*** Version 2.0 (80 Gbps) over USB Type-C connectors and cables. Also includes incorporation of all approved ECNs as of the revision date plus editorial clean-up.
2.3	October 2023	New release primarily for *deprecating* the ***Audio Adapter Accessory Mode*** and *replacing it with* the ***Liquid Corrosion Mitigation Mode***, and for updating the ***Multi-port Charger Shared Capacity*** definition and behaviors. Also includes incorporation of all approved ECNs as of the revision date. Note: this release was created using a newly developed document template that includes some style adjustments and editorial clean-up.

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1 Introduction

With the continued success of the USB interface, there exists a need to adapt USB technology to serve newer computing platforms and devices as they trend toward smaller, thinner, and lighter form-factors. Many of these newer platforms and devices are reaching a point where existing USB receptacles and plugs are inhibiting innovation, especially given the relatively large size and internal volume constraints of the Standard-A and Standard-B versions of USB connectors. Additionally, as platform usage models have evolved, usability and robustness requirements have advanced, and the existing set of USB connectors were not originally designed for some of these newer requirements. This specification establishes a new USB connector ecosystem that addresses the evolving needs of platforms and devices while retaining all the functional benefits of USB that form the basis for this most popular of computing device interconnects.

1.1 Purpose

This specification defines the USB Type-C® receptacles, plug and cables.

The USB Type-C Cable and Connector Specification is guided by the following principles:

- Enable new and exciting host and device form-factors where size, industrial design and style are important parameters
- Work seamlessly with existing USB host and device silicon solutions
- Enhance ease of use for connecting USB devices with a focus on minimizing user confusion for plug and cable orientation

The USB Type-C Cable and Connector Specification defines a receptacle, plug, cable, and detection mechanisms that are compatible with existing USB interface electrical and functional specifications. This specification covers the following aspects that are needed to produce and use this new USB cable/connector solution in newer platforms and devices, and that interoperate with existing platforms and devices:

- USB Type-C receptacles, including electro-mechanical definition and performance requirements
- USB Type-C plugs and cable assemblies, including electro-mechanical definition and performance requirements
- USB Type-C to legacy cable assemblies and adapters
- USB Type-C-based device detection and interface configuration, including support for legacy connections
- ***USB Power Delivery*** optimized for the USB Type-C connector

The USB Type-C Cable and Connector Specification defines a standardized mechanism that supports ***Alternate Modes***, such as repurposing the connector for docking-specific applications.

1.2 Scope

This specification is intended as a supplement to the existing ***USB 2.0***, ***USB 3.2***, ***USB4***® and ***USB Power Delivery*** specifications. It addresses only the elements required to implement and support the USB Type-C receptacles, plugs and cables.

Normative information is provided to allow interoperability of components designed to this specification. ***Informative*** information, when provided, may illustrate possible design implementations.

1.3 Related Documents

USB 2.0 ***Universal Serial Bus Revision 2.0 Specification***
This includes the entire document release package.

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USB 3.2 ***Universal Serial Bus Revision 3.2 Specification***
This includes the entire document release package.
USB 3.1 Legacy Cable and Connector Specification, Revision 1.0

USB4 ***USB4 Specification, Version 2.0, October 2022***
(including posted errata and ECNs)

TBT3 *Chapter 13 of* ***USB4 Specification, Version 2.0, October 2022***

USB PD ***USB Power Delivery Specification, Revision 2.0, Version 1.3, January 12, 2017***
USB Power Delivery Specification, Revision 3.2, Version 1.0, October 2023
(including posted errata and ECNs)

USB BB ***USB Billboard Device Class Specification, Revision 1.2.2, January 29, 2021***

USB BC ***Battery Charging Specification, Revision 1.2, March 15, 2012***
(including posted errata and ECNs)

DP AM ***DisplayPort™ Alt Mode on USB Type-C Standard, Version 2.1, October 2022***

All USB-specific documents are available for download at http://www.usb.org/documents.
The ***DisplayPort Alt Mode*** specification is available from VESA (http://www.vesa.org).

1.4 Conventions

1.4.1 Precedence

If there is a conflict between text, figures, and tables, the precedence ***shall*** be tables, figures, and then text.

1.4.2 Keywords

The following keywords differentiate between the levels of requirements and options.

1.4.2.1 Informative

Informative is a keyword that describes information with this specification that intends to discuss and clarify requirements and features as opposed to mandating them.

1.4.2.2 May

May is a keyword that indicates a choice with no implied preference.

1.4.2.3 May Not

May not is a keyword that is the inverse of ***May***. Indicates a choice to not implement a given feature with no implied preference.

1.4.2.4 N/A

N/A is a keyword that indicates that a field or value is not applicable and has no defined value and ***shall not*** be checked or used by the recipient.

1.4.2.5 Normative

Normative is a keyword that describes features that are mandated by this specification.

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1.4.2.6 Optional and Optionally

Optional and ***Optionally*** are equivalent keywords that describe features not mandated by this specification. However, if an ***optional*** feature is implemented, the feature ***shall*** be implemented as defined by this specification (***optional normative***).

1.4.2.7 Reserved

Reserved is a keyword indicating reserved bits, bytes, words, fields, and code values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this specification and, unless otherwise stated, ***shall not*** be utilized, or adapted by vendor implementation. A reserved bit, byte, word, or field ***shall*** be set to zero by the sender and ***shall*** be ignored by the receiver. ***Reserved*** field values ***shall not*** be sent by the sender and, if received, ***shall*** be ignored by the receiver.

1.4.2.8 Shall

Shall is a keyword indicating a mandatory (***normative***) requirement. Designers are mandated to implement all such requirements to ensure interoperability with other compliant Devices.

1.4.2.9 Shall Not

Shall not is a keyword that is the inverse of ***Shall*** indicating non-compliant operation.

1.4.2.10 Should

Should is a keyword indicating flexibility of choice with a preferred alternative. Equivalent to the phrase “it is recommended that ...”.

1.4.2.11 Should Not

Should not is a keyword that is the inverse of ***Should***. Equivalent to the phrase “it is recommended that implementations do not ...”.

1.4.3 Numbering

Numbers that are immediately followed by a lowercase “b” (e.g., 01b) are binary values. Numbers that are immediately followed by an uppercase “B” are byte values. Numbers that are immediately followed by a lowercase “h” (e.g., 3Ah) are hexadecimal values. Numbers not immediately followed by either a “b”, “B”, or “h” are decimal values.

1.5 Terms and Abbreviations

Term	Description
Accessory Mode	A reconfiguration of the connector based on the presence of ***Rd***/***Rd*** on CC1/CC2, respectively.
Active cable	Active cables are USB Full-Featured Type-C Cables that incorporate repeaters in the ***USB 3.2*** data path. All active cables, regardless of length, are expected to comply with this specification, the ***USB 3.2*** Appendix E, and the ***USB 3.2*** active cable CTS. Active cables ***may*** incorporate repeaters in both ends of the cable, one end, or anywhere in the cable. See Chapter 6.
Alternate Mode	Operation defined by a vendor or standards organization that is associated with a SVID assigned by the ***USB-IF***. Entry and exit into and from an ***Alternate Mode*** is controlled by the ***USB PD*** Structured VDM Enter Mode and Exit Mode commands. See Appendix E.
Alternate Mode Adapter (AMA)	A ***USB PD*** Device which supports ***Alternate Modes*** and acts as a UFP.

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Term	Description
Audio Adapter Accessory Mode	The Accessory Mode defined by the presence of ***Ra***/***Ra*** on CC1/CC2, respectively. This mode is ***deprecated*** and replaced by ***Liquid Corrosion Mitigation Mode***.
BMC	Biphase Mark Coding used for ***USB PD*** communication over the CC wire.
Cable Port Partner	The USB Type-C DRP, Source, or Sink connected to the cable plug.
Captive cable	A cable that is terminated on one end with a USB Type-C plug and has a vendor-specific connect means (hardwired or custom detachable) on the opposite end.
CC	Configuration Channel (CC) used in the discovery, configuration, and management of connections across a USB Type-C cable. See Section 4.5.
Charge-Through VPD (***CTVPD***)	A VCONN-Powered USB Device that has the mechanism to pass power and CC communication from one port to the other without any reregulation. See Section 4.10.2.
Configuration Lane	The ***USB 3.2*** Configuration Lane is used to establish and manage dual-lane SuperSpeed USB operation. The Configuration Lane is specifically the SuperSpeed USB TX1/RX1 differential signal set in the cable/plug.
Debug Accessory Mode (DAM)	The Accessory Mode defined by the presence of ***Rd***/***Rd*** or ***Rp***/***Rp*** on CC1/CC2, respectively. See Appendix B.
Debug and Test System (DTS)	The combined hardware and software system that provides a system developer debug visibility and control when connected to a ***Target System*** in ***Debug Accessory Mode***.
Default VBUS	VBUS voltage as defined by the ***USB 2.0*** and ***USB 3.2*** specifications. Note: where used, 5V VBUS connotes the same meaning.
DFP	Downstream Facing Port, specifically associated with the flow of data in a USB connection. Typically, the ports on a host or the ports on a hub to which devices are connected. In its initial state, the DFP sources VBUS and VCONN, and supports data. A charge-only DFP port only sources VBUS.
Direct connect device	A device with either a captive cable or just a USB Type-C plug (e.g., thumb drive).
DRD (Dual-Role-Data)	The acronym used in this specification to refer to a USB port that can operate as either a DFP (Host) or UFP (Device). The role that the port initially takes is determined by the port's power role at attach. A Source port takes on the data role of a DFP and a Sink port takes on the data role of a UFP. The port's data role ***may*** be changed dynamically using ***USB PD*** Data Role Swap.
DRP (Dual-Role-Power)	The acronym used in this specification to refer to a USB port that can operate as either a Source or a Sink. The role that the port offers ***may*** be fixed to either a Source or Sink or ***may*** alternate between the two port states. Initially when operating as a Source, the port will also take on the data role of a DFP and when operating as a Sink, the port will also take on the data role of a UFP. The port's power role ***may*** be changed dynamically using ***USB PD*** Power Role Swap.
DR_Swap	***USB PD*** Data Role Swap.
Dual-lane (x2)	Dual-lane operation is defined as simultaneously signaling on both sets of USB transmit and receive differential pairs (TX1/RX1 and TX2/RX2 in the cable/plug).
Electronically Marked Cable	A USB Type-C cable that uses ***USB PD*** to provide the cable's characteristics. See Section 4.9.

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Term	Description
eMarker	The element in an Electronically Marked Cable that returns information about the cable in response to a ***USB PD Discover Identity*** command.
Hybrid Optical Active Cable	A cable that uses an intermediate optical transmission line for the high-speed signaling path (TX/RX) while retaining a metallic conductor-based solution for the rest of the defined interfaces, e.g., CC, ***USB 2.0***, SBUs, etc.
Initiator	The port initiating a Vendor Defined Message. It is independent of the port's PD role (e.g., Provider, Consumer, Provider/Consumer, or Consumer/Provider). In most cases, the Initiator will be a host.
Internal Temperature	In reference to an active cable, the temperature measured inside a plug. It is not the skin temperature. There is a relationship between the plug's internal temperature and the skin temperature, but that relationship is design dependent.
Liquid Corrosion Mitigation Mode	The mode defined by the presence of ***Ra***/***Ra*** on CC1/CC2, respectively. See Appendix A.
Local Plug	The cable plug being referred to.
Optically Isolated Active Cable (OIAC)	A cable that uses an intermediate optical transmission line for all signaling. This cable has no metallic conductors and is electrically isolated between the two plugs. This cable has a USB Type-C Plug on each end with one Cable Plug supporting SOP' and the other supporting SOP".
Passive cable	A cable that does not incorporate any electronics to condition the data path signals. A passive cable ***may*** or ***may not*** be electronically marked.
Port Partner	Refers to the port (device or host) a port is attached to.
Power Bank	A device with a battery whose primary function is to charge or otherwise extend the runtime of other USB Type-C devices.
Power Delivery Mode	A mode where the port partners are in a ***USB PD*** power contract (either Explicit or Implicit).
Power Sinking Devices (PSD)	Sink which draws power but has no other USB or ***Alternate Mode*** communication function, e.g., a USB-powered light.
Powered cable	A cable with electronics in the plug that requires VCONN indicated by the presence of ***Ra*** between the VCONN pin and ground.
PR_Swap	***USB PD*** Power Role Swap.
Re-driver	Re-driver refers to an analog component that operates on the signal without re-timing it. This ***may*** include equalization, amplification, and transmitter. The re-driver does not include a clock-data recovery (CDR) circuit. Re-drivers are beyond the scope of this document.
Remaining Shared Capacity	The remaining power available for a Shared Capacity group of ports after power has been allocated to one or more of its ports.
Remote Plug	A remote cable plug in the context of OIAC plugs is the plug at the other end of the Optically Isolated Active Cable.
Repeater	Repeater refers to any active component that acts on a signal in order to increase the physical lengths and/or interconnect loss over which the signal can be transmitted successfully. The category of repeaters includes both re-timers and re-drivers.

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Term	Description
Responder	The port responding to the Initiator of a Vendor Defined Message (VDM). It is independent of the port's ***USB PD*** role (e.g., Provider, Consumer, Provider/Consumer, or Consumer/Provider). In most cases, the Responder will be a device.
Re-timer	Re-timer refers to a component that contains a clock-data recovery (CDR) circuit that "retimes" the signal. The re-timer latches the signal into a synchronous memory element before re-transmitting it. It is used to extend the physical length of the system without accumulating high frequency jitter by creating separate clock domains on either side of the re-timer. Re-timers are defined in ***USB 3.2*** Appendix E and ***USB4***.
SBU	Sideband Use.
Shared Port Power Available	The power available, up to the port's PDP, to an unattached port in a Shared Capacity group of ports. This power represents what is available to each port in the group when a Sink is attached after considering power that is already allocated to ports with connected Sinks. This power will be a minimum of 7.5 W, initially offered as USB Type-C Current @ 1.5 A.
Short Active Cable (SAC)	A cable with a USB Type-C Plug on each end, at least one of which is a Cable Plug supporting SOP'. Cable length up to 5 meters.
SID	A Standard ID (SID) is a unique 16-bit value assigned by the ***USB-IF*** to identify an industry standard.
Single-lane (x1)	***USB 3.2*** single-lane operation is defined as signaling on only one set of SuperSpeed USB transmit and receive differential pairs (TX1/RX1 in the cable/plug).
Sink	Port asserting ***Rd*** on CC and when attached is consuming power from VBUS; most commonly a Device.
Skin Temperature	In reference to an active cable, the temperature of a plug's over-mold.
Source	Port asserting ***Rp*** on CC and when attached is providing power over VBUS; most commonly a Host or Hub DFP.
SVID	General reference to either a SID or a VID. Used by ***USB PD*** Structured VDMs when requesting SIDs and VIDs from a device.
Target System (TS)	The system being debugged in ***Debug Accessory Mode***.
Total Shared Capacity	The total power available for a Shared Capacity group of ports. This is the overall power available when none of the ports in the group are connected to Sinks.
Type-A	A general reference to all versions of USB "A" plugs and receptacles.
Type-B	A general reference to all versions of USB "B" plugs and receptacles.
Type-C Plug	A USB plug conforming to the mechanical and electrical requirements in this specification.
Type-C Port	The USB port associated to a USB Type-C receptacle. This includes the USB signaling, CC logic, multiplexers, and other associated logic.
Type-C Receptacle	A USB receptacle conforming to the mechanical and electrical requirements of this specification.
UFP	Upstream Facing Port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks VBUS and supports data.

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Term	Description
USB 2.0 Type-C Cable	A USB Type-C to Type-C cable that only supports ***USB 2.0*** data operation. This cable does not include ***USB 3.2*** or SBU wires.
USB 2.0 Type-C Plug	A USB Type-C plug specifically designed to implement the ***USB 2.0*** Type-C cable.
USB Full-Featured Type-C Cable	A USB Type-C to Type-C cable that supports ***USB 2.0***, ***USB 3.2*** and ***USB4*** data operation. This cable includes SBU wires and is an Electronically Marked Cable.
USB Full-Featured Type-C Plug	A USB Type-C plug specifically designed to implement the USB Full-Featured Type-C cable.
USB4 Hub	A ***USB4*** hub product is used for USB port expansion, includes only USB upstream and downstream ports, and does not include any additional capability that exposes other connector types or functions except as defined in Section 5.2.3 (***Alternate Modes*** Support).
USB4-based Dock	A ***USB4***-based dock product combines a ***USB4*** hub (including at least one exposed USB Type-C downstream port) with additional capabilities that either exposes other connector types and/or includes other user-visible functions, e.g., storage, networking, etc. Examples of functions that are not considered user-visible include firmware update and device authentication.
USB Safe State	The USB Safe State as defined by the ***USB PD*** specification.
VCONN-Powered Accessory (***VPA***)	An accessory that is powered from VCONN to operate in an ***Alternate Mode***. ***VPA***s cannot implement the charge-through mechanism described for ***VPD***s, and instead must intermediate by negotiating ***USB Power Delivery*** with both the connected host and source in order to enable similar functionality. See Section 4.10.1.
VCONN-Powered USB Device (***VPD***)	A USB direct-connect or captive-cable device that can be powered solely from either VCONN or VBUS. ***VPD***s ***may optionally*** support the ***VPD*** charge-through capability. See Section 4.10.2.
VCONN_Swap	***USB PD*** VCONN Swap.
VDM	Vendor Defined Message as defined by the ***USB PD*** specification.
VID	A Vendor ID (VID) is a unique 16-bit value assigned by the ***USB-IF*** to identify a vendor.
vSafe0V	VBUS “0 volts” as defined by the ***USB PD*** specification.
vSafe5V	VBUS “5 volts” as defined by the ***USB PD*** specification.
x1	See Single-lane.
x2	See Dual-lane.

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2 Overview

2.1 Introduction

The USB Type-C® receptacle, plug and cable provide a smaller, thinner, and more robust alternative to legacy USB interconnect (Standard and Micro USB cables and connectors). This solution targets use in very thin platforms, ranging from ultra-thin notebook PCs down to smart phones where existing Standard-A and Micro-AB receptacles are deemed too large, difficult to use, or inadequately robust.

Some key specific enhancements include:

- The USB Type-C receptacle may be used in very thin platforms as its total system height for the mounted receptacle is under 3 mm
- The USB Type-C plug enhances ease of use by being plug-able in either upside-up or upside-down directions
- The USB Type-C cable enhances ease of use by being plug-able in either direction between host and devices

While the USB Type-C interconnect no longer physically differentiates plugs on a cable by being an A-type or B-type, the USB interface still maintains such a host-to-device logical relationship. Determination of this host-to-device relationship is accomplished through a Configuration Channel (CC) that is connected through the cable. In addition, the Configuration Channel is used to set up and manage power and Alternate/Accessory Modes.

Using the Configuration Channel, the USB Type-C interconnect defines a simplified 5 volt VBUS-based power delivery and charging solution that supplements what is already defined in the ***USB 3.2*** Specification. More advanced power delivery and battery charging features over the USB Type-C interconnect are based on the ***USB Power Delivery*** specification. As a product implementation improvement, the USB Type-C interconnect shifts the ***USB PD*** communication protocol from being communicated over VBUS to being delivered across the USB Type-C Configuration Channel.

The USB Type-C receptacle, plug and cable designs are intended to support future USB functional extensions. As such, consideration was given to frequency scaling performance, pin-out arrangement and the configuration mechanisms when developing this solution. The definition of future USB functional extensions is not in the scope of this specification but rather will be provided in future releases of the base USB Specification, i.e., beyond the existing ***USB4*** Specification.

Figure 2-1 illustrates the comprehensive functional signal plan for the USB Full-Featured Type-C receptacle, not all signals shown are required in all platforms or devices. As shown, the receptacle signal list functionally delivers both ***USB 2.0*** (D+ and D−) and either ***USB 3.2*** or ***USB4*** (TX and RX pairs) data buses, USB power (VBUS) and ground (GND), Configuration Channel signals (CC1 and CC2), and two Sideband Use (SBU) signal pins. Multiple sets of USB data bus signal locations in this layout facilitate being able to functionally map the USB signals independent of plug orientation in the receptacle. For reference, the signal pins are labeled. For the ***USB 2.0*** Type-C receptacle, neither the ***USB 3.2*** nor ***USB4*** signals are implemented.

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Figure 2-1 USB Type-C Receptacle Interface (Front View)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	VBUS	CC1	D+	D−	SBU1	VBUS	RX2−	RX2+	GND
GND	RX1+	RX1−	VBUS	SBU2	D−	D+	CC2	VBUS	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Figure 2-2 illustrates the comprehensive functional signal plan for the USB Type-C plug. Only one CC pin is connected through the cable to establish signal orientation and the other CC pin is repurposed as VCONN for

powering electronics in the USB Type-C plug. Also, only one set of ***USB 2.0*** D+/D− wires are implemented in a USB Type-C cable. For USB Type-C cables that only intend to support ***USB 2.0*** functionality, the TX/RX and SBU signals are not implemented. For the USB Type-C Power-Only plug (intended only for USB Type-C Sink applications), only nine contacts are implemented to support CC, VBUS, and GND.

Figure 2-2 USB Full-Featured Type-C Plug Interface (Front View)

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

2.2 USB Type-C Receptacles, Plugs and Cables

Cables and connectors, including USB Type-C to USB legacy cables and adapters, are explicitly defined within this specification. These are the only connectors and cables that are authorized by the licensing terms of this specification. All licensed cables and connectors are required to comply with the compliance and certification requirements that are developed and maintained by the ***USB-IF***.

The following USB Type-C receptacles and plugs are defined.

- USB Full-Featured Type-C receptacle for ***USB 2.0***, ***USB 3.2***, ***USB4*** and full-featured platforms and devices.
- ***USB 2.0*** Type-C receptacle for ***USB 2.0*** platforms and devices.
- USB Full-Featured Type-C plug.
- ***USB 2.0*** Type-C plug.
- USB Type-C Power-Only plug.

The following USB Type-C cables are defined.

- USB Full-Featured Type-C cable with a USB Full-Featured Type-C plug at both ends for ***USB 3.2***, ***USB4*** and full-featured applications.
- ***USB 2.0*** Type-C cable with a ***USB 2.0*** Type-C plug at both ends for ***USB 2.0*** applications.
- Captive cable with either a USB Full-Featured Type-C plug or ***USB 2.0*** Type-C plug at one end.
- Active cables as defined in Chapter 6.

All of the defined USB Type-C receptacles, plugs and cables (except OIAC) support USB charging applications, including support for the ***optional*** USB Type-C-specific implementation of the ***USB Power Delivery*** specification (See Section 4.6.2.4).

All USB Full-Featured Type-C cables are electronically marked. ***USB 2.0*** Type-C cables ***may*** be electronically marked. See Section 4.9 for the requirements of Electronically Marked Cables.

The following USB Type-C to USB legacy cables and adapters are defined.

- ***USB 3.2*** Type-C to Legacy Host cable with a USB Full-Featured Type-C plug at one end and a ***USB 3.1*** Standard-A plug at the other end – this cable supports use of a USB Type-C-based device with a legacy USB host.
- ***USB 2.0*** Type-C to Legacy Host cable with a ***USB 2.0*** Type-C plug at one end and a ***USB 2.0*** Standard-A plug at the other end – this cable supports use of a USB Type-C-based device with a legacy ***USB 2.0*** host (primarily for mobile charging and sync applications).

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- ***USB 3.2*** Type-C to Legacy Device cable with a USB Full-Featured Type-C plug at one end and a ***USB 3.1*** Standard-B plug at the other end – this cable supports use of legacy ***USB 3.1*** hubs and devices with a USB Type-C-based host.
- ***USB 2.0*** Type-C to Legacy Device cable with a ***USB 2.0*** Type-C plug at one end and a ***USB 2.0*** Standard-B plug at the other end – this cable supports use of legacy ***USB 2.0*** hubs and devices with a USB Type-C-based host.
- ***USB 2.0*** Type-C to Legacy Mini Device cable with a ***USB 2.0*** Type-C plug at one end and a ***USB 2.0*** Mini-B plug at the other end – this cable supports use of legacy devices with a ***USB 2.0*** Type-C-based host.
- ***USB 3.2*** Type-C to Legacy Micro Device cable with a USB Full-Featured Type-C plug at one end and a ***USB 3.1*** Micro-B plug at the other end – this cable supports use of legacy ***USB 3.1*** hubs and devices with a USB Type-C-based host.
- ***USB 2.0*** Type-C to Legacy Micro Device cable with a ***USB 2.0*** Type-C plug at one end and a ***USB 2.0*** Micro-B plug at the other end – this cable supports use of legacy ***USB 2.0*** hubs and devices with a USB Type-C-based host.
- ***USB 3.2*** Type-C to Legacy Standard-A adapter with a USB Full-Featured Type-C plug at one end and a ***USB 3.1*** Standard-A receptacle at the other end – this adapter supports use of a legacy USB "thumb drive" style device or a legacy USB ThinCard device with a ***USB 3.2*** Type-C-based host.
- ***USB 2.0*** Type-C to Legacy Micro-B adapter with a ***USB 2.0*** Type-C plug at one end and a ***USB 2.0*** Micro-B receptacle at the other end – this adapter supports charging a USB Type-C-based mobile device using a legacy USB Micro-B-based chargers, either captive cable-based or used in conjunction with a legacy ***USB 2.0*** Standard-A to Micro-B cable.

USB Type-C receptacle to USB legacy adapters are explicitly not defined or allowed. Such adapters would allow many invalid, and potentially unsafe, cable connections to be constructed by users.

2.3 Configuration Process

The USB Type-C receptacle, plug and cable solution incorporates a configuration process to detect a downstream facing port to upstream facing port (Source-to-Sink) connection for VBUS management and host-to-device connected relationship determination.

The USB Type-C port configuration process is used for the following:

- Source-to-Sink attach/detach detection,
- plug orientation/cable twist detection,
- initial power (Source-to-Sink) detection and establishing the data (Host-to-Device) relationship,
- detect if cable requires VCONN,
- USB Type-C VBUS current detection and usage,
- ***USB PD*** communication, and
- discovery and configuration of functional extensions.

Two pins on the USB Type-C receptacle, CC1 and CC2, are used for this purpose. Within a standard USB Type-C cable, only a single CC pin position within each plug of the cable is connected through the cable.

2.3.1 Source-to-Sink Attach/Detach Detection

Initially, Source-to-Sink attach is detected by a host or hub port (Source) when one of the CC pins at its USB Type-C receptacle senses a specified resistance to GND. Subsequently, Source-to-Sink detach is detected when the CC pin that was terminated at its USB Type-C receptacle is no longer terminated to GND.

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Power is not applied to the USB Type-C host or hub receptacle (VBUS or VCONN) until the Source detects the presence of an attached device (Sink) port. When a Source-to-Sink attach is detected, the Source is expected to enable power to the receptacle and proceed to normal USB operation with the attached device. When a Source-to-Sink detach is detected, the port sourcing VBUS removes power.

2.3.2 Plug Orientation/Cable Twist Detection

The USB Type-C plug can be inserted into a receptacle in either one of two orientations, therefore the CC pins enable a method for detecting plug orientation in order to determine the lane ordering of the USB TX/RX data signal pairs functionally connected through the cable and identify the Configuration Lane for dual-lane operation when supported. This allows for signal routing, if needed, within a host or device to be established for a successful connection.

2.3.3 Initial Power (Source-to-Sink) Detection and Establishing the Data (Host-to-Device) Relationship

Unlike existing USB Type-A and USB Type-B receptacles and plugs, the mechanical characteristics of the USB Type-C receptacle and plug do not inherently establish the relationship of USB host and device ports. The CC pins on the receptacle also serve to establish an initial power (Source-to-Sink) and data (Host-to-Device) relationships prior to the normal USB enumeration process.

For the purpose of defining how the CC pins are used to establish the initial power relationship, the following port power behavior modes are defined.

1. Source-only – for this mode, the port exclusively behaves as a Source.
2. Sink-only – for this mode, the port exclusively behaves as a Sink.
3. Dual-Role-Power (DRP) – for this mode, the port can behave either as a Source or Sink.

Additionally, when a port supports USB data operation, a port's data behavior modes are defined.

1. DFP-only – for this mode, the port exclusively behaves as a DFP.
2. UFP-only – for this mode, the port exclusively behaves as a UFP.
3. Dual-Role-Data (DRD) – for this mode, the port can behave either as a DFP or UFP.

The DFP-only and UFP-only ports behaviorally map to traditional USB host ports and USB device ports, respectively but ***may not*** necessarily do USB data communication. When a host-only port is attached to a device-only port, the behavior from the user's perspective follows the traditional USB host-to-device port model. However, the USB Type-C connector solution does not physically prevent host-to-host or device-to-device connections. In this case, the resulting host-to-host or device-to-device connection results in a safe but non-functional situation.

Once initially established, the Source supplies VBUS and behaves as a DFP, and the Sink consumes VBUS and behaves as a UFP. ***USB PD***, when supported by both ports, ***may*** then be used to independently swap both the power and data roles of the ports.

A port that supports dual-role operation by being able to shift to the appropriate connected mode when attached to either a Source-only or Sink-only port is a DRP. In the special case of a DRP being attached to another DRP, an initialization protocol across the CC pins is used to establish the initial host-to-device relationship. Given no role-swapping intervention, the determination of which is DFP or UFP is random from the user's perspective.

Two independent sets of mechanisms are defined to allow a USB Type-C DRP to functionally swap power and data roles. When ***USB PD*** is supported, power and data role swapping is performed as a subsequent step following the initial connection process. For non-PD implementations, power/data role swapping can ***optionally*** be dealt with as part of the initial connection process. To improve the user's experience when connecting devices that are of categorically different types, products ***may*** be implemented to strongly prefer

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being a DFP or a UFP, such that the DFP/UFP determination becomes predictable when connecting two DRPs of differing categories. See Section 4.5.1.4 for more on available swapping mechanisms.

As an alternative to role swapping, a USB Type-C DRP ***may*** provide useful functionality by when operating as a host, exposing a CDC/network (preferably TCP/IP) stack or when operating as a device, exposing a CDC/network interface.

USB hubs have two types of ports, a UFP that is connected to a DFP (host or another hub) that initially functions as a Sink, and one or more DFPs for connecting other devices that initially function as Sources.

2.3.4 USB Type-C VBUS Current Detection and Usage

With the USB Type-C connector solution, a Source (host or downstream hub port) ***may*** implement higher source current over VBUS to enable faster charging of mobile devices or higher-power devices. All USB host and hub ports advertise via the CC pins the level of current that is presently available. The USB device port is required to manage its load to stay within the current level offered by the host or hub, including dynamically scaling back the load if the host or hub port changes its advertisement to a lower level as indicated over the CC pins.

Three current level advertisements at 5V VBUS are defined by ***USB Type-C Current***:

- ***USB Type-C Current*** at Default is the as-configured for high-power operation current value as defined by a USB Specification (500 mA for ***USB 2.0*** ports; 900 mA or 1,500 mA for ***USB 3.2*** ports operating in single-lane or dual-lane, respectively),
- ***USB Type-C Current*** at 1.5 A, and
- ***USB Type-C Current*** at 3.0 A.

There is a clear functional distinction between advertising ***USB Type-C Current*** at Default versus the ***USB Type-C Current*** at either 1.5 A or 3.0 A.

- ***USB Type-C Current*** at Default is intended for host operation in providing bus power to a connected device where the host manages the device's current consumption for the low-power, high-power and suspend states as defined in the USB base specifications.
- ***USB Type-C Current*** at either 1.5 A or 3.0 A is primarily intended for charging applications. The Sink can vary its current draw up to the advertised limit. Offering ***USB Type-C Current*** at either 1.5 A or 3.0 A is allowed for a host providing bus power to a device. The host needs to assume that the device will continuously draw up to the offered limit.

The higher ***USB Type-C Current*** levels that can be advertised allows hosts and devices that do not implement ***USB PD*** to take advantage of higher charging current.

2.3.5 *USB PD* Communications

USB Power Delivery is a feature on products (hosts, hubs, and devices). ***USB PD*** communications is used to:

- establish power contracts that allow voltage and current beyond existing USB data bus specifications,
- change the port sourcing VBUS,
- change the port sourcing VCONN,
- swap DFP and UFP roles, and
- communicate with cables.

The ***USB PD*** Bi-phase Mark Coded (BMC) communications are carried on the CC wire of the USB Type-C cable.

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2.3.6 Functional Extensions

Functional extensions, including ***USB4*** and ***Alternate Modes*** (see Appendix E) are enabled via a communications channel across CC using methods defined by the ***USB Power Delivery*** specification.

2.4 VBUS

VBUS provides a path to deliver power between a host and a device, and between a USB power charger and a host/device. A simplified high-current supply capability is defined for hosts and chargers that ***optionally*** support current levels beyond the ***USB 2.0***, ***USB 3.2***, and ***USB4*** specifications. The ***USB Power Delivery*** specification is supported.

Table 2-1 summarizes the power supply options available from the perspective of a device with the USB Type-C connector. Not all options will be available to the device from all host or hub ports – only the first two listed options are mandated by the base USB specifications and form the basis of ***USB Type-C Current*** at the Default USB Power level.

Table 2-1 Summary of power supply options

Mode of Operation	Voltage	Current	Notes
USB 2.0	5 V	See ***USB 2.0***	
USB 3.2	5 V	See ***USB 3.2***	
USB4	5 V	1.5 A	See Section 5.3.
USB BC 1.2	5 V	1.5 A[1]	Legacy charging
USB Type-C Current @ 1.5 A	5 V	1.5 A	Supports higher power devices
USB Type-C Current @ 3.0 A	5 V	3 A	Supports higher power devices
USB PD	Configurable up to 48 V	Configurable up to 5 A	Directional control and power level management

Note 1: Whereas ***USB BC 1.2*** specification permits a power provider to be designed to support a level of power between 0.5 A and 1.5 A, the USB Type-C specification requires that a Source port that supports ***USB BC 1.2*** be at a minimum capable of supplying 1.5 A and advertise ***USB Type-C Current*** @ 1.5 A in addition to supporting the ***USB BC 1.2*** power provider termination.

The USB Type-C receptacle is specified for current capability of 5 A whereas standard USB Type-C cable assemblies are rated for 3 A. The higher rating of the receptacle enables systems to deliver more power over directly attached docking solutions or using appropriately designed chargers with captive cables when implementing ***USB PD***. Also, USB Type-C cable assemblies designed for ***USB PD*** and appropriately identified via electronic marking are allowed to support up to 5 A.

USB Type-C cable assemblies designed for ***USB PD*** Extended Power Range (EPR) operation are required to have an electronic marking indicating EPR compatibility. These cables are required to be electronically marked for 5 A and 50 V and include the EPR Mode Capable bit set.

2.5 VCONN

Once the connection between host and device is established, the CC pin (CC1 or CC2) in the receptacle that is not connected via the CC wire through the standard cable is repurposed to source VCONN to power circuits in the plug needed to implement Electronically Marked Cables (see Section 4.9), ***VCONN-Powered Accessories*** and ***VCONN-Powered USB Devices***. Initially, the source supplies VCONN and the source of VCONN ***may*** be swapped using ***USB PD VCONN_Swap***.

Once VCONN is available, all electronically marked cables use it as the only power source. If VCONN is applied after VBUS, then until VCONN is available, the cable ***may*** remain unpowered or ***may*** draw power from VBUS.

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VCONN functionally differs from VBUS in that it is isolated from the other end of the cable. VCONN is independent of VBUS and, unlike VBUS which can use ***USB PD*** to support higher voltages, VCONN voltage stays within the range of 3.0 to 5.5 V.

2.6 Hubs

USB hubs implemented with USB Type-C receptacles are required to clearly identify the upstream facing port. This requirement is needed because a user can no longer know which port on a hub is the upstream facing port and which ports are the downstream facing ports by the type of receptacles that are exposed, i.e., USB Type-B is the upstream facing port and USB Type-A is a downstream facing port.

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3 Mechanical

3.1 Overview

This chapter defines the USB Type-C connectors and wired cable assemblies. Cables which include active elements in the data path are defined in Chapter 6 (Active Cables).

3.1.1 Compliant Connectors

The USB Type-C specification defines the following standard connectors:

- USB Full-Featured Type-C receptacle,
- ***USB 2.0*** Type-C receptacle,
- USB Full-Featured Type-C plug,
- ***USB 2.0*** Type-C plug, and
- USB Type-C Power-Only plug.

3.1.2 Compliant Cable Assemblies

Table 3-1 summarizes the USB Type-C standard cable assemblies along with the primary differentiating characteristics. All USB Full-Featured Type-C cables ***shall*** support simultaneous, independent signal transmission on both ***USB 3.2*** and ***USB4*** (TX and RX pairs) data buses. The cable lengths listed in the table are ***informative*** and represent the practical length based on cable performance requirements. For ***USB Power Delivery***, each cable assembly is identified as being either only usable for ***USB PD*** Standard Power Range (SPR) operation or usable for both ***USB PD*** SPR and ***USB PD*** Extended Power Range (EPR) operation. Existing ***USB PD*** SPR 5 A cables have been deprecated and replaced by ***USB PD*** EPR cables. All cables that are either full-featured and/or are rated at more than 3 A current are Electronically Marked Cables.

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Table 3-1 USB Type-C Standard Cable Assemblies

Cable Ref	Plug 1	Plug 2	USB Version	Cable Length[2]	Current Rating	USB Power Delivery	USB Type-C Electronically Marked
CC2-3	C	C	***USB 2.0***	≤ 4 m	3 A	Supported (SPR Only)	***Optional***
CC2-5[1]					5 A		***Required***
CC2-5E					5 A	Supported (SPR & EPR)	***Required***
CC3G1-3	C	C	***USB 3.2*** Gen1 and ***USB4*** Gen2	≤ 2 m	3 A	Supported (SPR Only)	***Required***
CC3G1-5[1]					5 A		
CC3G1-5E					5 A	Supported (SPR & EPR)	
CC3G2-3	C	C	***USB 3.2*** Gen2 and ***USB4*** Gen2	≤ 1 m	3 A	Supported (SPR Only)	***Required***
CC3G2-5[1]					5 A		
CC3G2-5E					5 A	Supported (SPR & EPR)	***Required***
CC4G3-3	C	C	***USB4*** Gen3 and ***USB4*** Gen4[3]	≤ 0.8 m	3 A	Supported (SPR Only)	***Required***
CC4G3-5[1]					5 A		
CC4G3-5E					5 A	Supported (SPR & EPR)	***Required***

Notes:
1. These cables are deprecated in favor of having all 5 A cables be EPR-capable versions.
2. The cable lengths listed in the table are ***informative*** and represent the practical lengths based on cable performance requirements.
3. ***USB4*** Gen4 passive cables are electrically equivalent to ***USB4*** Gen3 passive cables. For ***USB4*** Gen4 active cables, refer to Chapter 6 for the ***USB4*** Gen3 and Gen4 electrical requirements.

USB Type-C products are also allowed to have a captive cable. See Section 3.4.3.

3.1.3 Compliant USB Type-C to Legacy Cable Assemblies

Table 3-2 summarizes the USB Type-C legacy cable assemblies along with the primary differentiating characteristics. The cable lengths listed in the table are ***informative*** and represent the practical length based on cable performance requirements. All USB Type-C to legacy cable assemblies are only defined specific to ***USB 2.0*** and ***USB 3.2*** as there are no USB Type-C to legacy cables that are uniquely applicable to ***USB4***.

For USB Type-C legacy cable assemblies that incorporate ***Rp*** termination, the value of this termination is required to be specified to the Default setting of ***USB Type-C Current*** even though the cable assemblies are rated for 3 A. The ***Rp*** termination in these cables is intended to represent the maximum current of a compliant legacy USB host port, not the current rating of the cable itself. The cable current rating is intentionally set to a higher level given that there are numerous non-standard power chargers that offer more than the Default levels established by the ***USB 2.0*** and ***USB 3.1*** specifications.

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Table 3-2 USB Type-C Legacy Cable Assemblies

Cable Ref	Plug 1[3]	Plug 2[3]	USB Version	Cable Length[2]	Current Rating
AC2-3	***USB 2.0*** Standard-A	***USB 2.0*** Type-C[1]	***USB 2.0***	≤ 4 m	3 A
AC3G1-3	***USB 3.1*** Standard-A	USB Full-Featured Type-C[1]	***USB 3.1*** Gen1	≤ 2 m	3 A
AC3G2-3	***USB 3.1*** Standard-A	USB Full-Featured Type-C[1]	***USB 3.1*** Gen2	≤ 1 m	3 A
CB2-3	***USB 2.0*** Type-C[2]	***USB 2.0*** Standard-B	***USB 2.0***	≤ 4 m	3 A
CB3G2-3	USB Full-Featured Type-C[2]	***USB 3.1*** Standard-B	***USB 3.1*** Gen2	≤ 1 m	3 A
CmB2	***USB 2.0*** Type-C[2]	***USB 2.0*** Mini-B	***USB 2.0***	≤ 4 m	500 mA
CμB2-3	***USB 2.0*** Type-C[2]	***USB 2.0*** Micro-B	***USB 2.0***	≤ 2 m	3 A
CμB3G1-3	USB Full-Featured Type-C[2]	***USB 3.1*** Micro-B	***USB 3.1*** Gen1	≤ 2 m	3 A
CμB3G2-3	USB Full-Featured Type-C[2]	***USB 3.1*** Micro-B	***USB 3.1*** Gen2	≤ 1 m	3 A

Notes:

1. USB Type-C plugs associated with the "B" end of a legacy adapter cable are required to have ***Rp*** (56 kΩ ± 5%) termination incorporated into the plug assembly – see Section 4.5.3.2.2.
2. USB Type-C plugs associated with the "A" end of a legacy adapter cable are required to have ***Rd*** (5.1 kΩ ± 20%) termination incorporated into the plug assembly – see Section 4.5.3.2.1.
3. Refer to Section 3.7.5.3 for the mated resistance and temperature rise required for the legacy plugs.

3.1.4 Compliant USB Type-C to Legacy Adapter Assemblies

Table 3-3 summarizes the USB Type-C legacy adapter assemblies along with the primary differentiating characteristics. The cable lengths listed in the table are ***informative*** and represent the practical length based on cable performance requirements. All USB Type-C to legacy adapter assemblies are only defined specific to ***USB 2.0*** and ***USB 3.2*** as there are no USB Type-C to legacy adapters that are uniquely applicable to ***USB4***.

Table 3-3 USB Type-C Legacy Adapter Assemblies

Cable Ref	Plug	Receptacle[3]	USB Version	Cable Length	Current Rating
CμBR2-3	***USB 2.0*** Type-C[1]	***USB 2.0*** Micro-B	***USB 2.0***	≤ 0.15 m	3 A
CAR3G1-3	USB Full-Featured Type-C[2]	***USB 3.1*** Standard-A	***USB 3.1*** Gen1	≤ 0.15 m	3 A

Notes:

1. USB Type-C plugs associated with the "B" end of a legacy adapter are required to have ***Rp*** (56 kΩ ± 5%) termination incorporated into the plug assembly – see Section 4.5.3.2.2.
2. USB Type-C plugs associated with the "A" end of a legacy adapter are required to have ***Rd*** (5.1 kΩ ± 20%) termination incorporated into the plug assembly – see Section 4.5.3.2.1.
3. Refer to Section 3.7.5.3 for the mated resistance and temperature rise required for the legacy receptacles.

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3.2 USB Type-C Connector Mating Interfaces

This section defines the connector mating interfaces, including the connector interface drawings, pin assignments, and descriptions. All dimensions in figures are in millimeters.

3.2.1 Interface Definition

Figure 3-1 and Figure 3-3 show, respectively, the USB Type-C receptacle and USB Full-Featured Type-C plug interface dimensions.

Figure 3-11 shows the ***USB 2.0*** Type-C plug interface dimensions. The dimensions that govern the mating interoperability are specified. All the REF dimensions are provided for reference only, not hard requirements.

Key features, configuration options, and design areas that need attention:

1. Figure 3-1 shows a vertical-mount receptacle. Other PCB mounting types such as right-angle mount and mid-mount are allowed.
2. A mid-plate is required between the top and bottom signals inside the receptacle tongue to manage crosstalk in full-featured applications. The mid-plate ***shall*** be connected to the PCB ground with at least two grounding points. The mid-plate ***shall*** be designed such that plug pins A4, A5, A6, A7, A8, A9, and B4, B5, B6, B7, B8, B9 do not short to ground during the connector mating process with an effective 6.2 mm receptacle shell implementation. If the receptacle connector has a short shell or no shell, the connector manufacturer ***shall*** provide an effective length shell fixture for compliance testing. A reference design of the mid-plate is provided in Section 3.2.2.1.
3. Retention of the cable assembly in the receptacle is achieved by the side-latches in the plug and features on the sides of the receptacle tongue. Side latches are required for all plugs except plugs used for docking with no cable attached. Side latches ***shall*** be connected to ground inside the plug. A reference design of the side latches is provided in Section 3.2.2.2 along with its grounding scheme. Docking applications ***may not*** have side latches, requiring special consideration regarding EMC (Electromagnetic Compatibility).
4. EMC shielding springs are required inside the cable plug. The shielding spring ***shall*** be connected to the plug shell. No EMC shielding spring finger tip of the USB Full-Featured Type-C plug or ***USB 2.0*** Type-C plug ***shall*** be exposed in the plug housing opening of the unmated USB Type-C plug (see Figure 3-12). Section 3.2.2.3 shows reference designs of the EMC spring.
5. Shorting of any signal or power contact spring to the plug metal shell is not allowed. The spring in the deflected state ***should not*** touch the plug shell. An isolation layer (e.g., Kapton tape placed on the plug shell) is recommended to prevent accidental shorting due to plug shell deformation.
6. The USB Type-C receptacle ***shall*** provide an EMC ground return path through one of the following options:
   - a system of specific points of contact on the receptacle outer shell (e.g., spring fingers or spring fingers and formed solid bumps),
   - internal EMC pads, or
   - a combination of both points of contact on the receptacle outer shell and internal EMC pads.

   If points of contacts are used on the receptacle, then the receptacle points of contact ***shall*** make connection with the mated plug within the contact zones defined in Figure 3-2. A minimum of four separate points of contact are required. Additional points of contact are allowed. See Section 3.2.2.4 for a reference design of receptacle outer shell. The reference design includes four spring fingers as points of contact. Alternate configurations ***may*** include spring fingers on the A contact side or B contact side and formed solid bumps (e.g., dimples) on the B contact side or A contact side, respectively. Spring fingers are required on a minimum of one side to provide a pressure fit on opposing sides of the plug shell. Additional bumps ***may*** be used, but if bumps are on opposing sides of the receptacle shell, the minimum distance between the bumps ***shall*** be greater than the maximum plug shell defined dimension.

   If internal EMC pads are present in the receptacle, then they ***shall*** comply with the requirements defined in Figure 3-1. The shielding pads ***shall*** be connected to the receptacle shell. If no receptacle shell is present, then the receptacle ***shall*** provide a means to connect the shielding pad to ground. See Section 3.2.2.3 for a reference design of the shielding pad and ground connection.
7. This specification defines the USB Type-C receptacle shell length of 6.20 mm as a reference dimension. The USB Type-C receptacle is designed to have shell length of 6.20 ± 0.20 mm to provide proper mechanical and electrical mating of the plug to the receptacle (e.g., full seating of the plug in the receptacle and protection of the receptacle tongue during insertion/withdrawal). The USB Type-C receptacle at the system level ***should*** be implemented such that the USB Type-C receptacle connector mounted in the associated system hardware has an effective shell length equal to 6.20 ± 0.20 mm.

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8. The USB Type-C connector mating interface is defined so that the electrical connection ***may*** be established without the receptacle shell. To prevent excessive misalignment of the plug when it enters or exits the receptacle, the enclosure ***should*** have features to guide the plug for insertion and withdrawal when a modified receptacle shell is present. If the USB Type-C receptacle shell is modified from the specified dimension, then the recommended lead in from the receptacle tongue to the plug point of entry is 1.5 mm minimum when mounted in the system.

   This specification allows receptacle configurations with a conductive shell, a non-conductive shell, or no shell. The following requirements apply to the receptacle contact dimensions shown in SECTION A-A and ALTERNATE SECTION A-A shown in Figure 3-1:

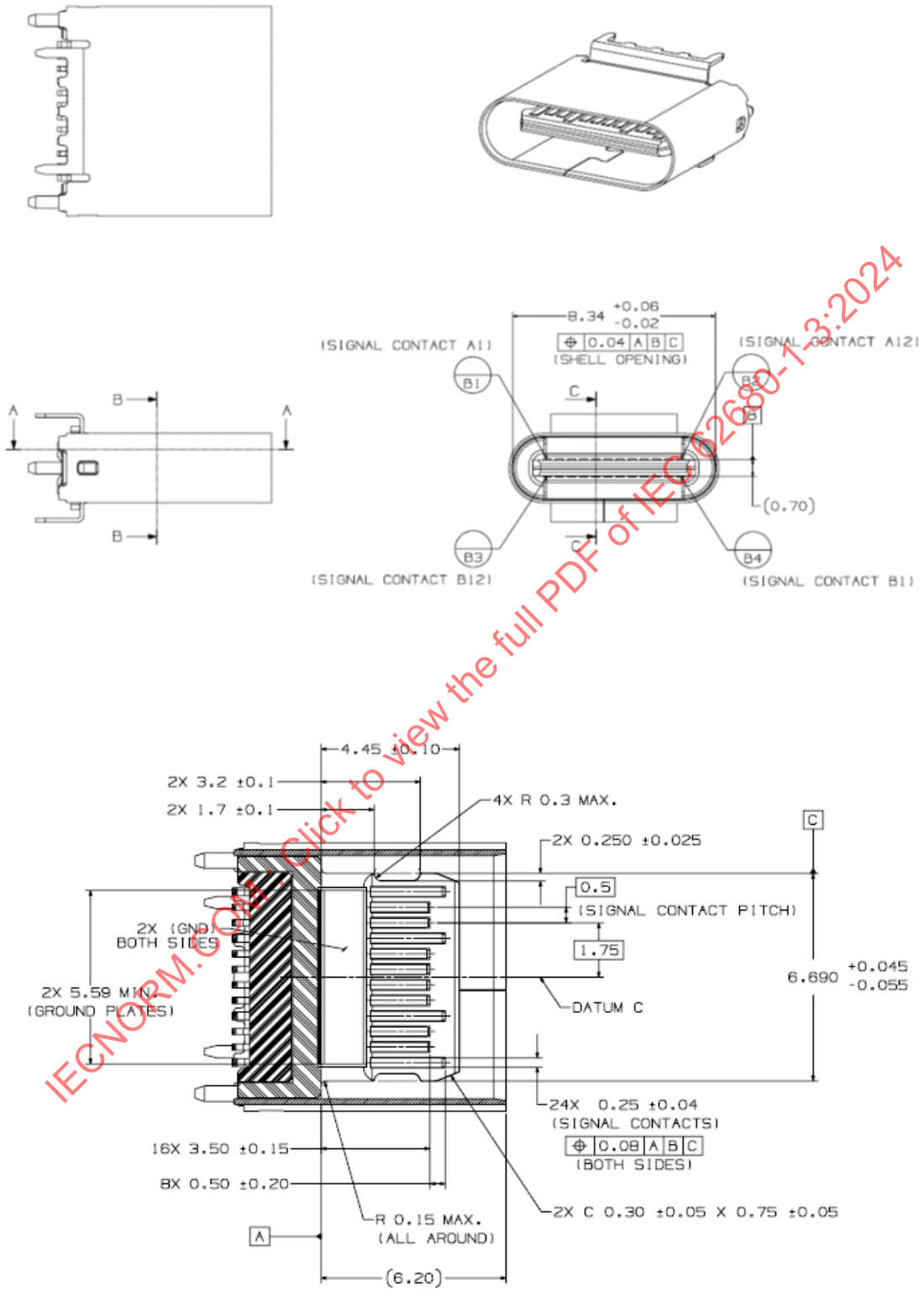
   - If the receptacle shell is conductive, then the receptacle contact dimensions of SECTION A-A or ALTERNATE SECTION A-A shown in Figure 3-1 ***shall*** be used.
   - If the receptacle shell is non-conductive, then the receptacle contact dimensions of ALTERNATE SECTION A-A shown in Figure 3-1 ***shall*** be used. The contact dimensions of SECTION A-A are not allowed.
   - If there is no receptacle shell, then the receptacle contact dimensions of either SECTION A-A or ALTERNATE SECTION A-A shown in Figure 3-1 ***shall*** be used. If there is no receptacle shell and the receptacle is used in an implementation that does not effectively provide a conductive shell, then a receptacle with the contact dimensions of ALTERNATE SECTION A-A shown in Figure 3-1 ***should*** be used.

   Note: If the product that incorporates a USB Type-C receptacle supports ***USB PD*** Extended Power Range (EPR) operation, consideration ***should*** be given to the choice between the contact dimensions shown in SECTION A-A versus ALTERNATE SECTION A-A. ***USB PD*** EPR-compatible Sources and Sinks have to be designed to withstand potential electrical arcing during unplug events when power is being supplied across the connector and having a larger difference in length between the CC and VBUS pins ***may*** be beneficial when implementing detection circuitry intended to help mitigate the damage due to potential arcing. See Section H.3.2 for more information.

9. A paddle card (e.g., PCB) ***may*** be used in the USB Type-C plug to manage wire termination and electrical performance. Section 3.2.2.5 includes the guidelines and a design example for a paddle card.
10. This specification does not define standard footprints. Figure 3-4 shows an example SMT (surface mount) footprint for the vertical receptacle shown in Figure 3-1. Additional reference footprints and mounting configurations are shown in Figure 3-5, Figure 3-6, Figure 3-7, Figure 3-8, Figure 3-9 and Figure 3-10.
11. The receptacle shell ***shall*** be connected to the PCB ground plane.
12. All VBUS pins ***shall*** be connected together in the USB Type-C plug.
13. All Ground return pins ***shall*** be connected together in the USB Type-C plug.
14. All VBUS pins ***shall*** be connected together at the USB Type-C receptacle when it is in its mounted condition (e.g., all VBUS pins bussed together in the PCB).
15. All Ground return pins ***shall*** be connected together at the USB Type-C receptacle when it is in its mounted condition (e.g., all Ground return pins bussed together in the PCB).
16. The USB Type-C Power-Only plug is a depopulated version of the USB Full-Featured Type-C plug or the ***USB 2.0*** Type-C plug. The interface dimensions ***shall*** conform to Figure 3 3 or Figure 3 11. Contacts for CC, VBUS, and GND (i.e., A1, A4, A5, A9, A12, B1, B4, B9, and B12) ***shall*** be present. Physical presence of contacts in the other 15 contact locations is ***optional***. The USB Type-C Power-Only plug ***shall*** only be used on a non-charger captive cable application. Implementation of ***Rd*** or CC communication on pin A5 is required in the application.

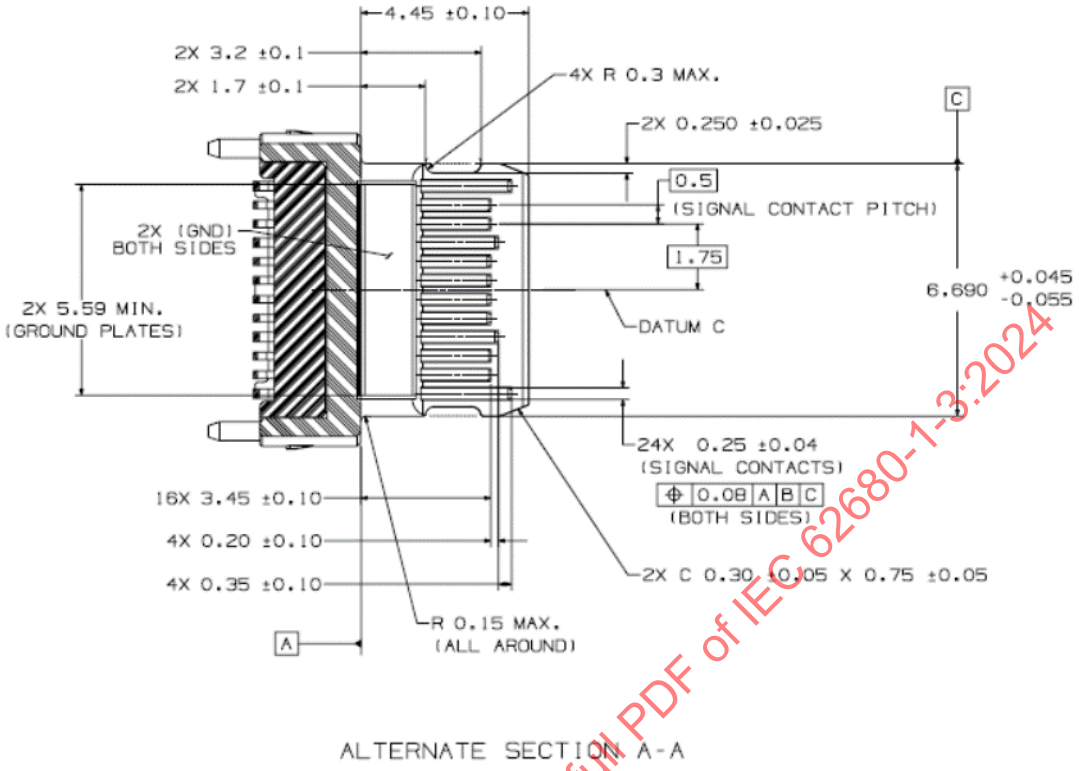
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Figure 3-1 USB Type-C Receptacle Interface Dimensions

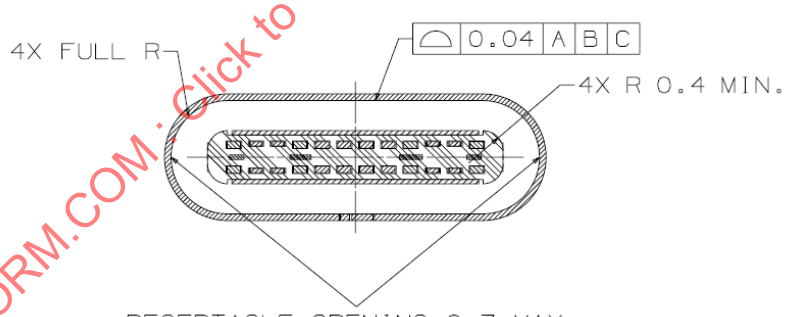


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Figure 3-1 USB Type-C Receptacle Interface Dimensions, cont.



ALTERNATE SECTION A-A

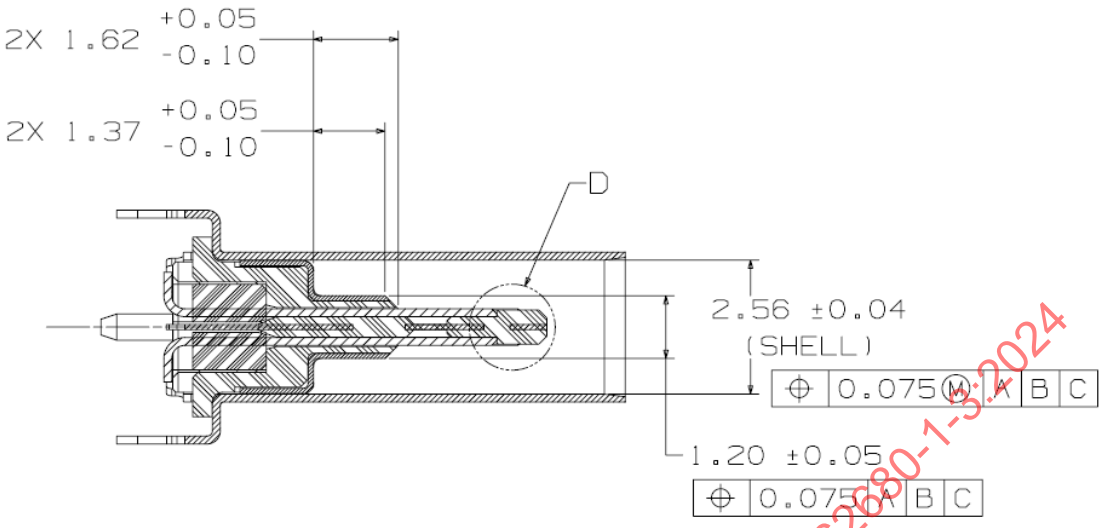


RECEPTACLE OPENING 0.7 MAX.
FLAT SIDES ALLOWED

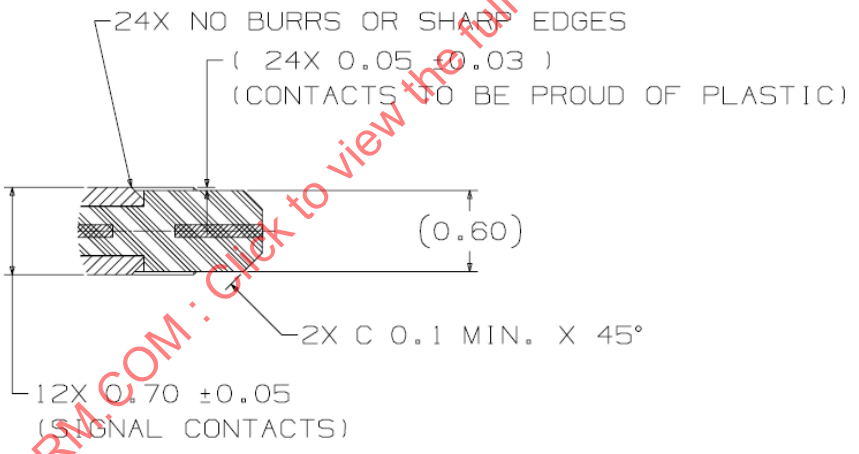
SECTION B-B

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Figure 3-1 USB Type-C Receptacle Interface Dimensions, cont.



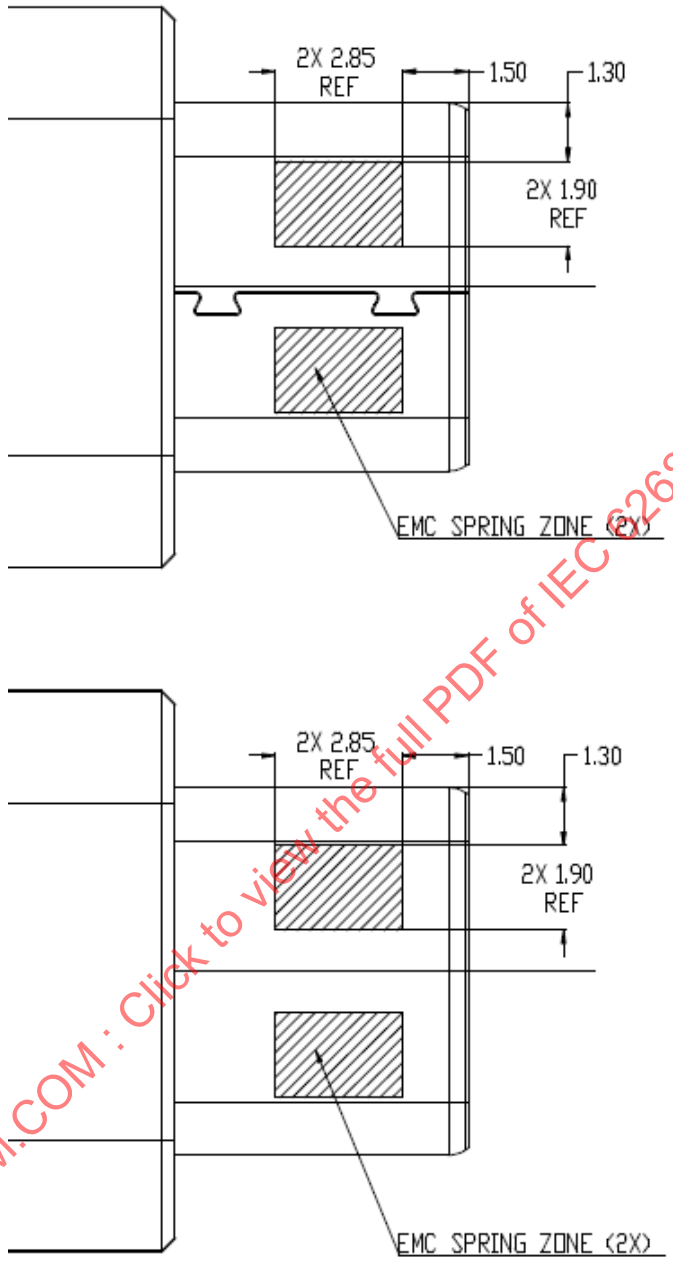
SECTION C-C



DETAIL D

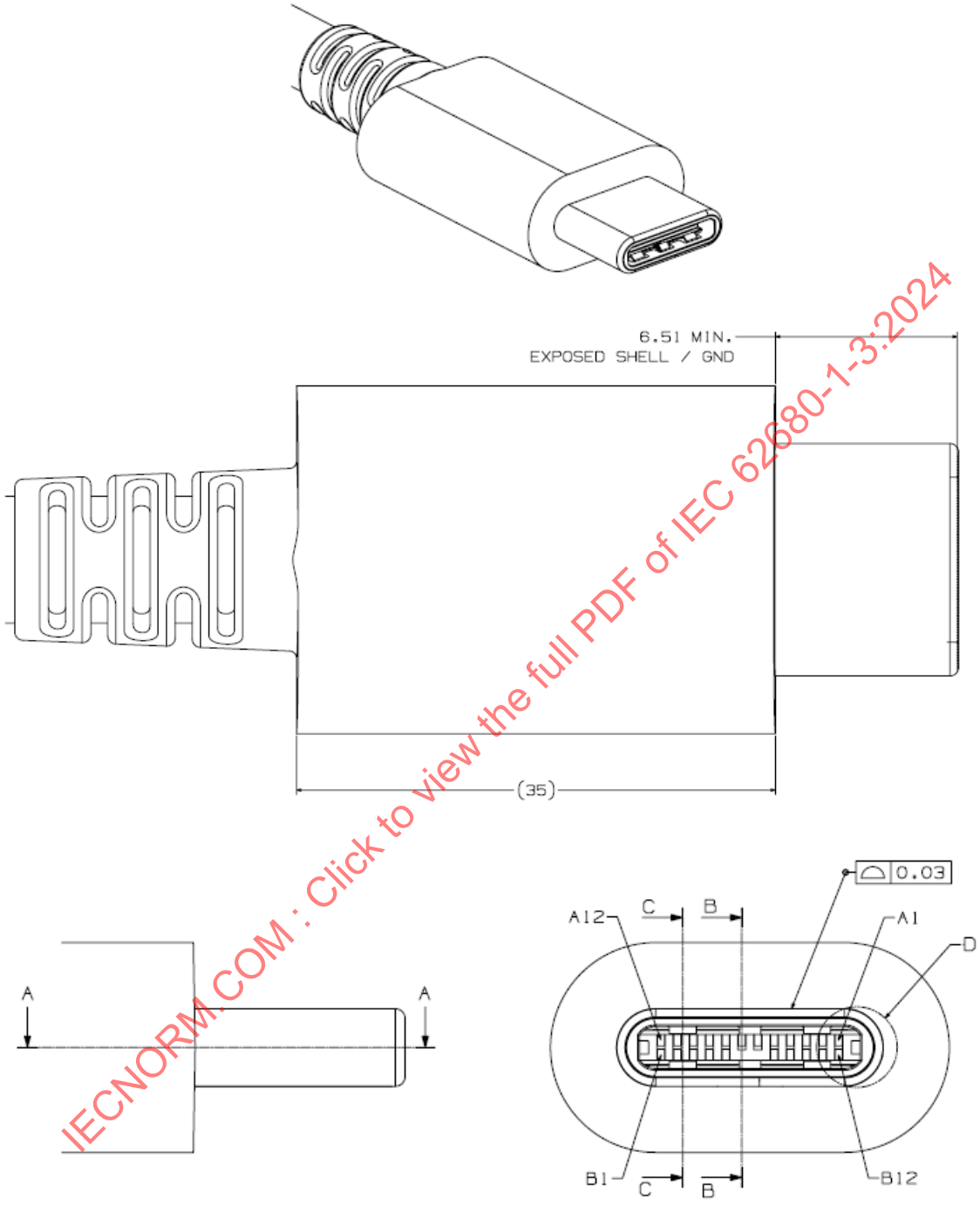
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Figure 3-2 Reference Design USB Type-C Plug External EMC Spring Contact Zones



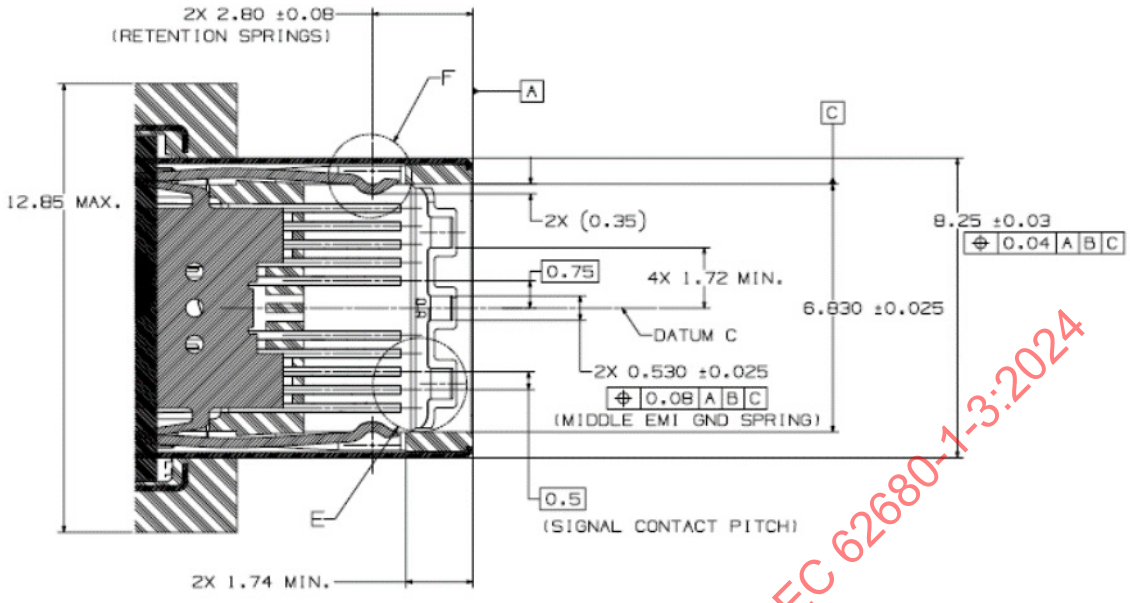
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Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions

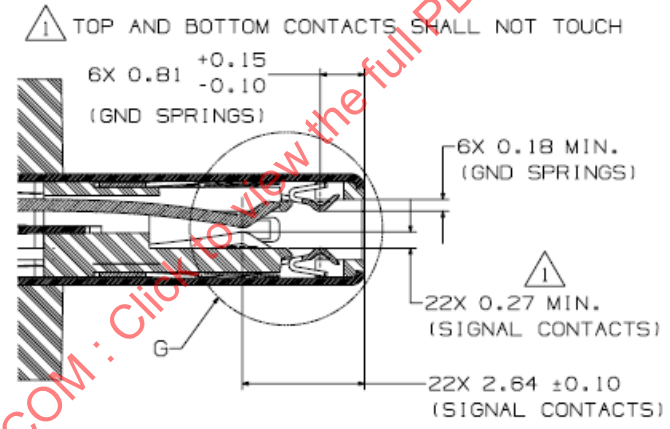


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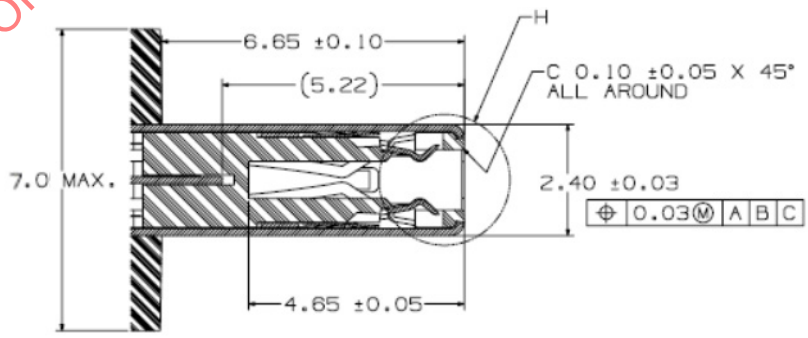
Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions, cont.



SECTION A-A



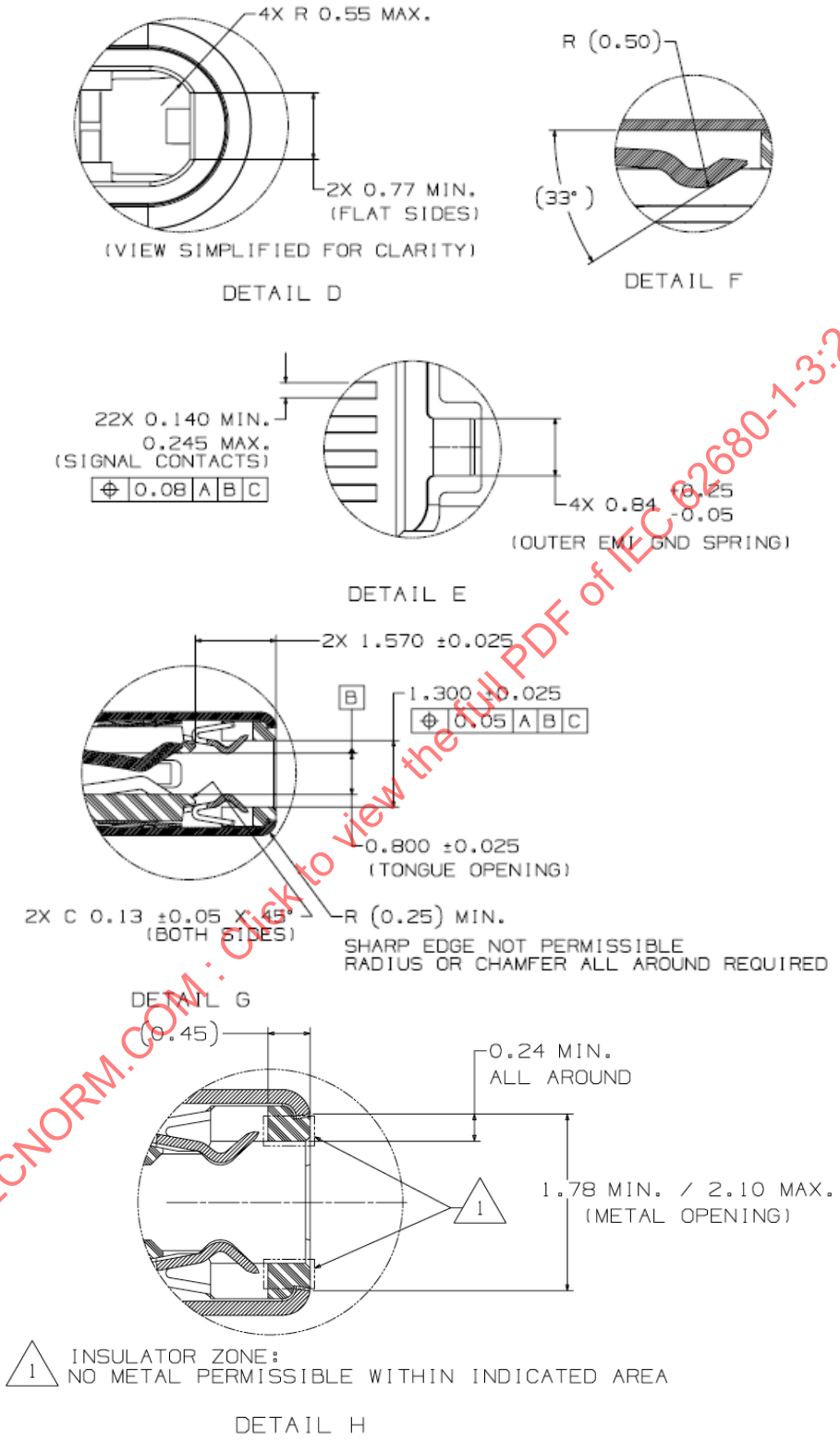
SECTION B-B



SECTION C-C

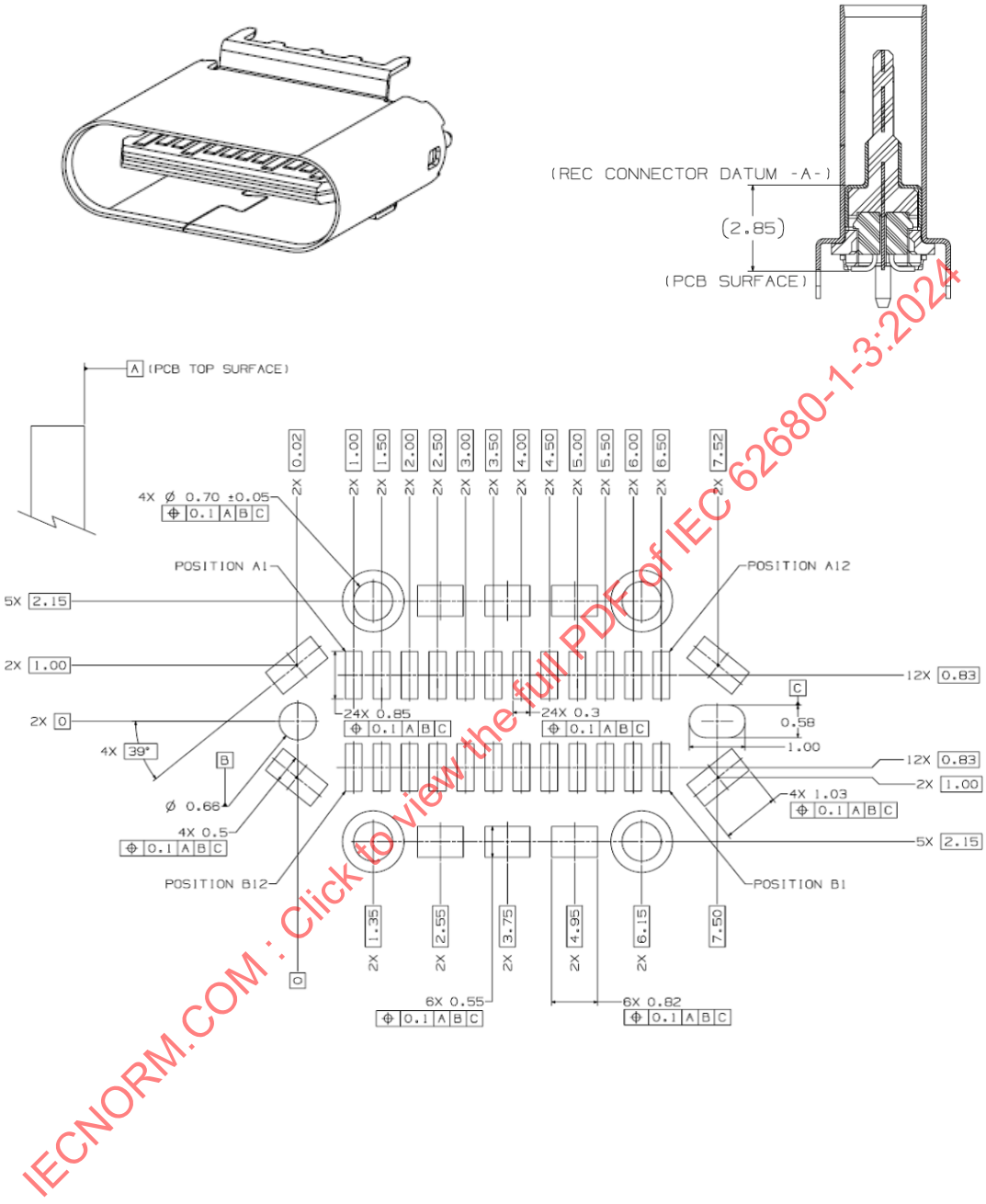
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Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions, cont.



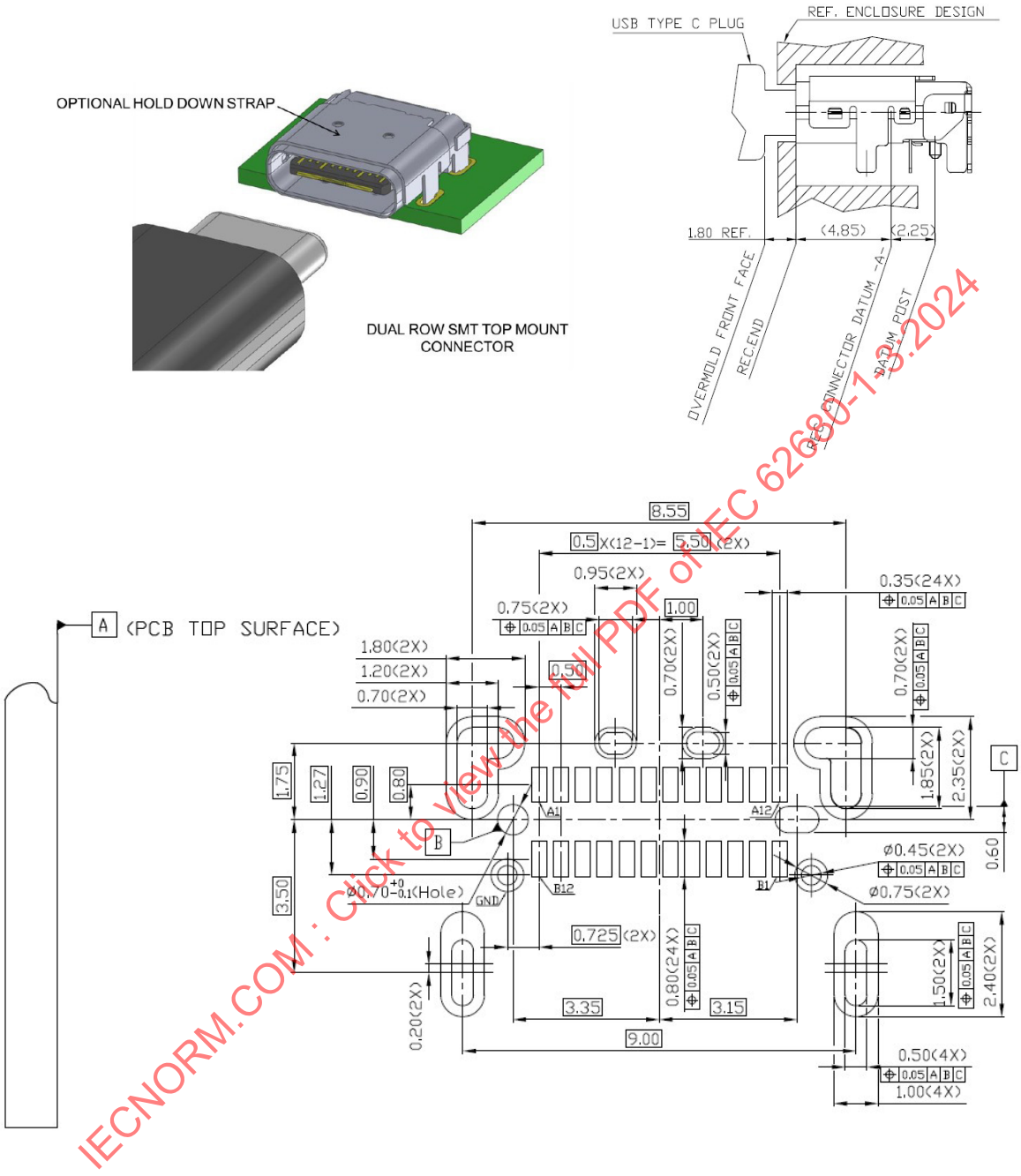
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Figure 3-4 Reference Footprint for a USB Type-C Vertical Mount Receptacle (*Informative*)



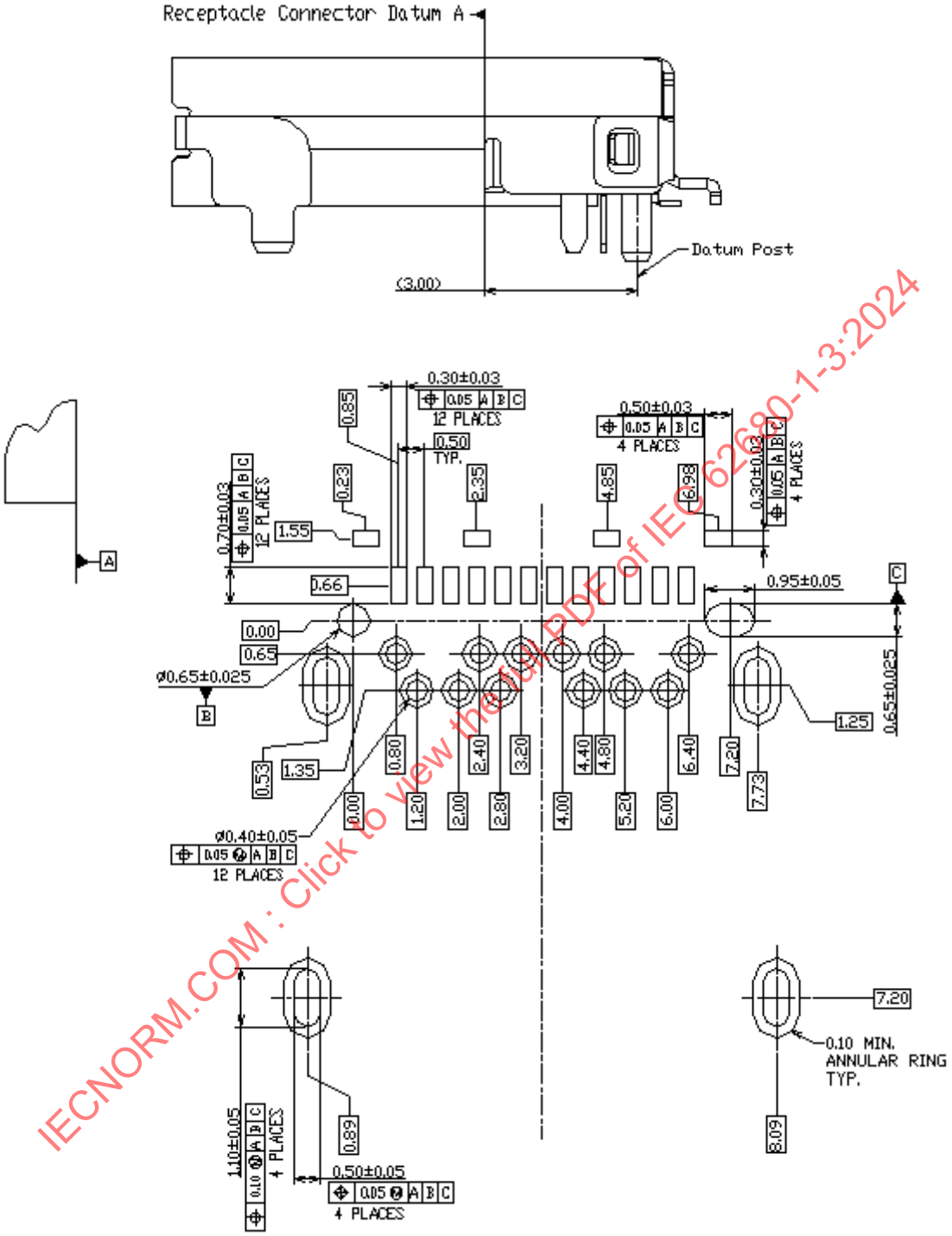
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Figure 3-5 Reference Footprint for a USB Type-C Dual-Row SMT Right-Angle Receptacle (*Informative*)



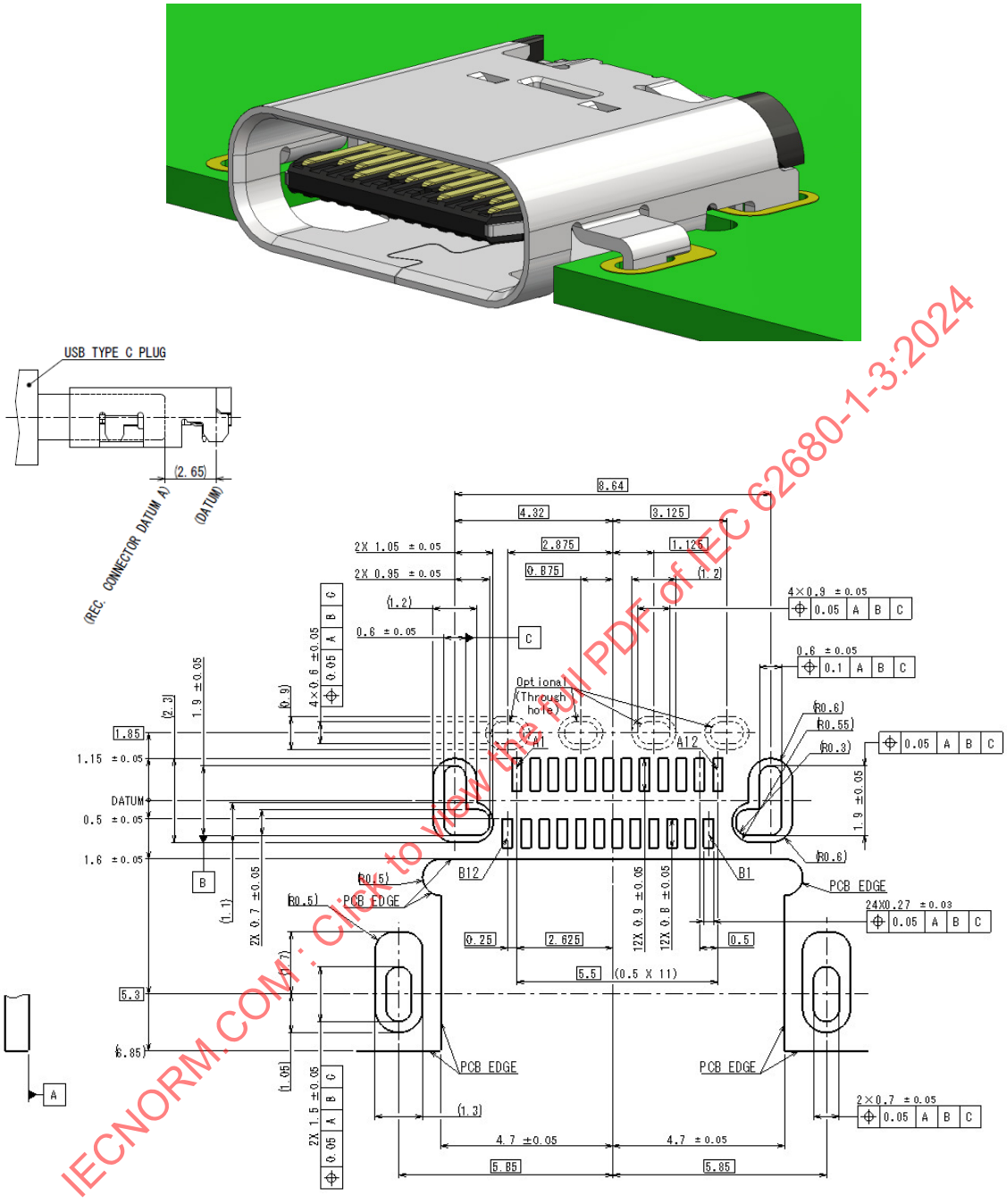
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Figure 3-6 Reference Footprint for a USB Type-C Hybrid Right-Angle Receptacle (*Informative*)



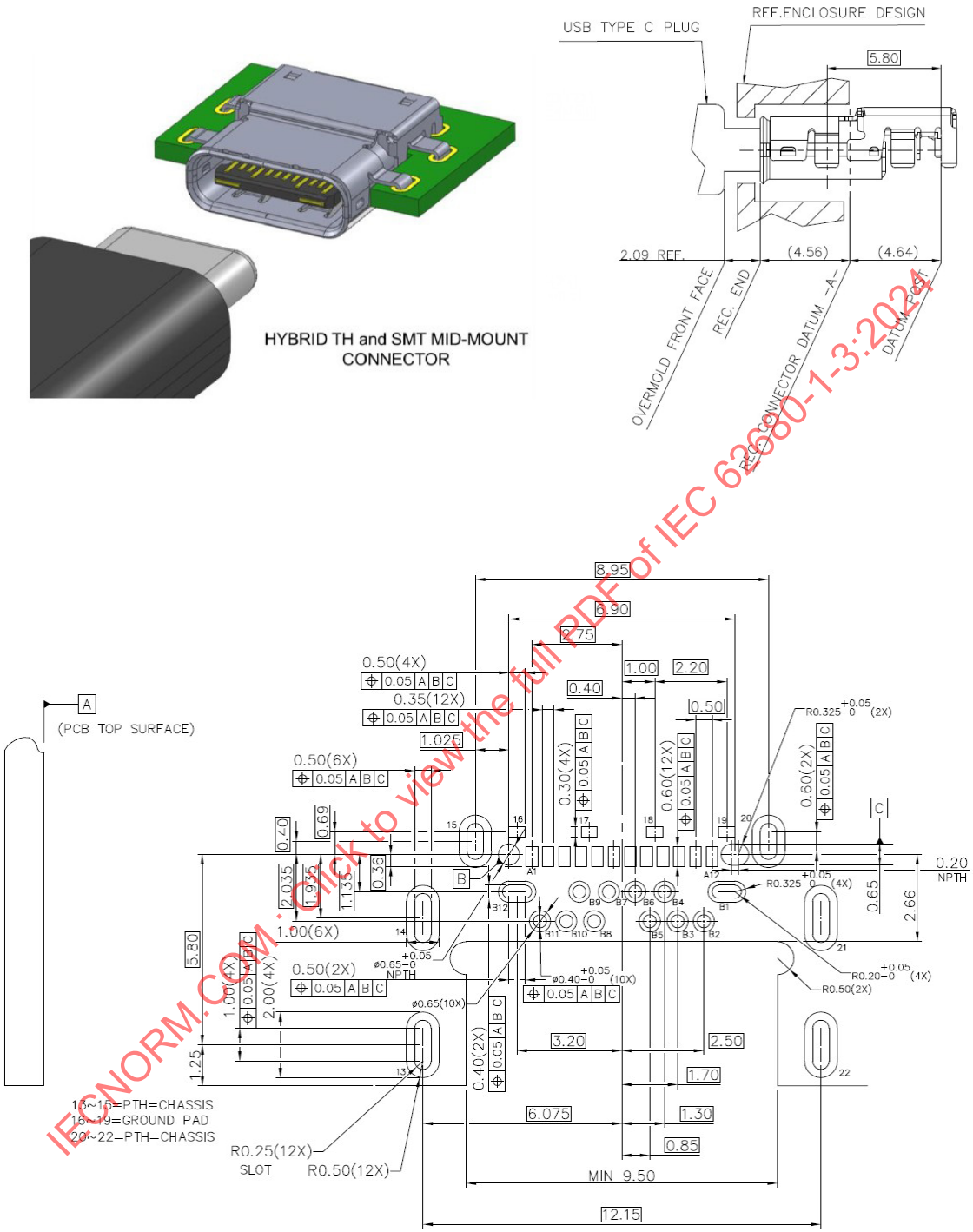
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Figure 3-7 Reference Footprint for a USB Type-C Mid-Mount Dual-Row SMT Receptacle (*Informative*)



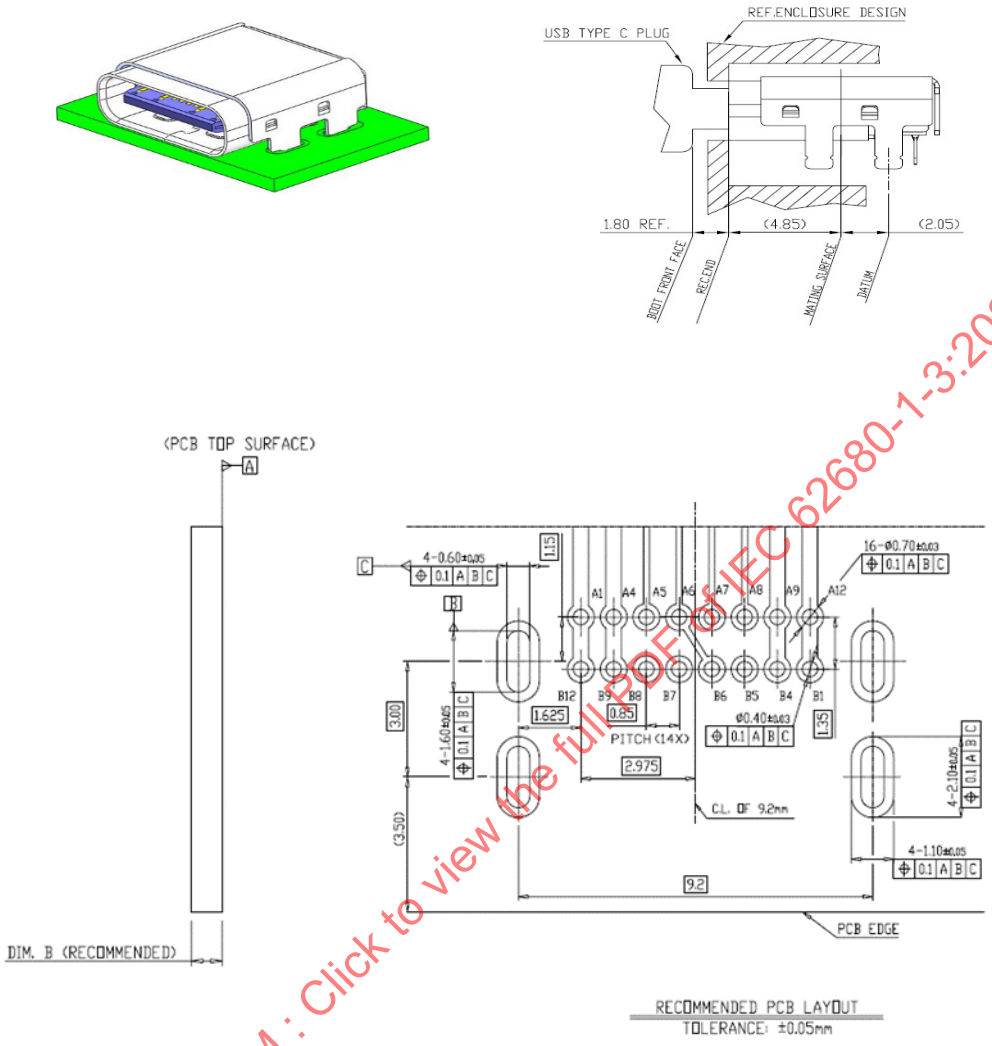
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Figure 3-8 Reference Footprint for a USB Type-C Mid-Mount Hybrid Receptacle (*Informative*)



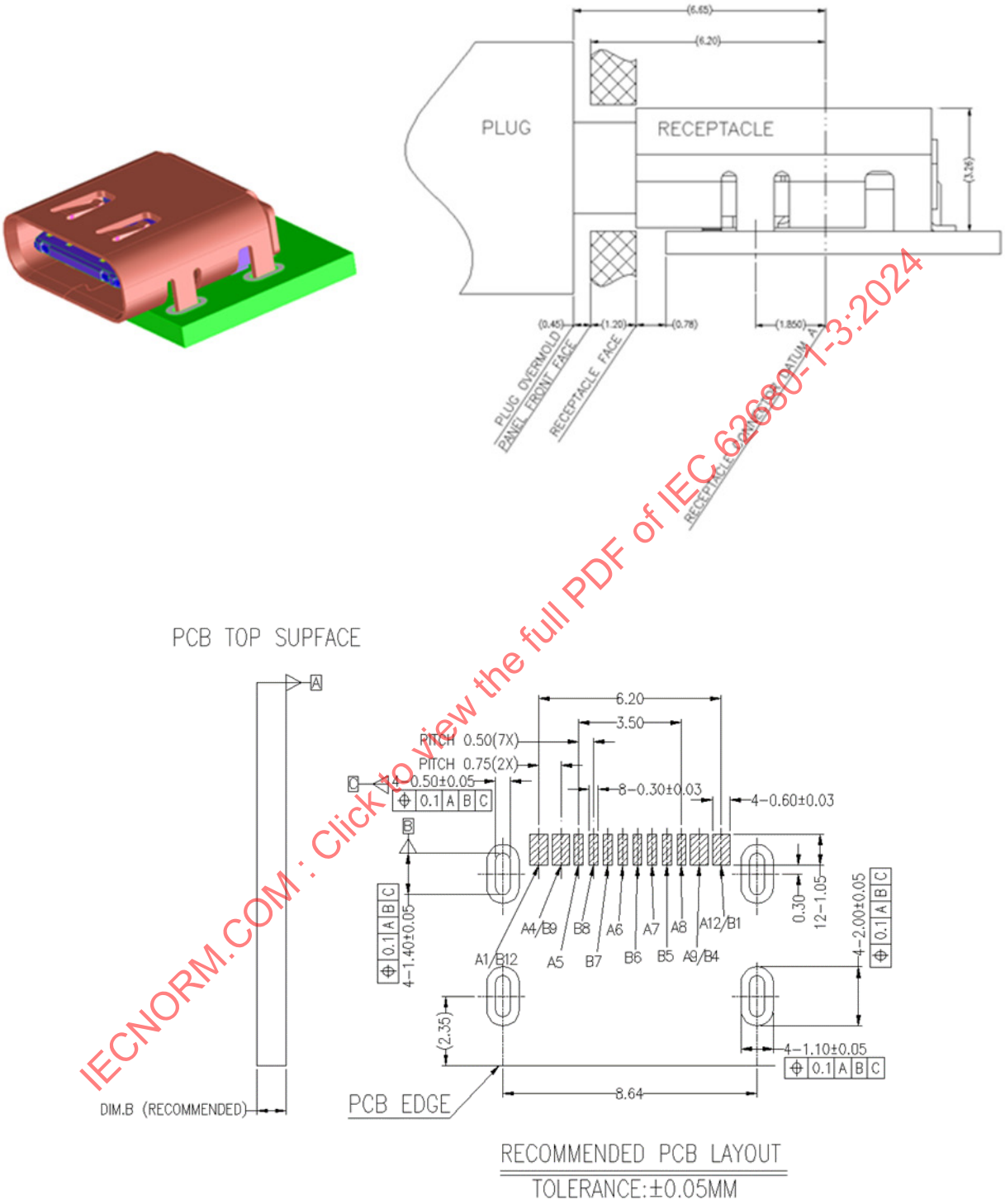
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Figure 3-9 Reference Footprint for a *USB 2.0* Type-C Through Hole Right Angle Receptacle (*Informative*)



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Figure 3-10 Reference Footprint for a *USB 2.0* Type-C Single Row Right Angle Receptacle (*Informative*)

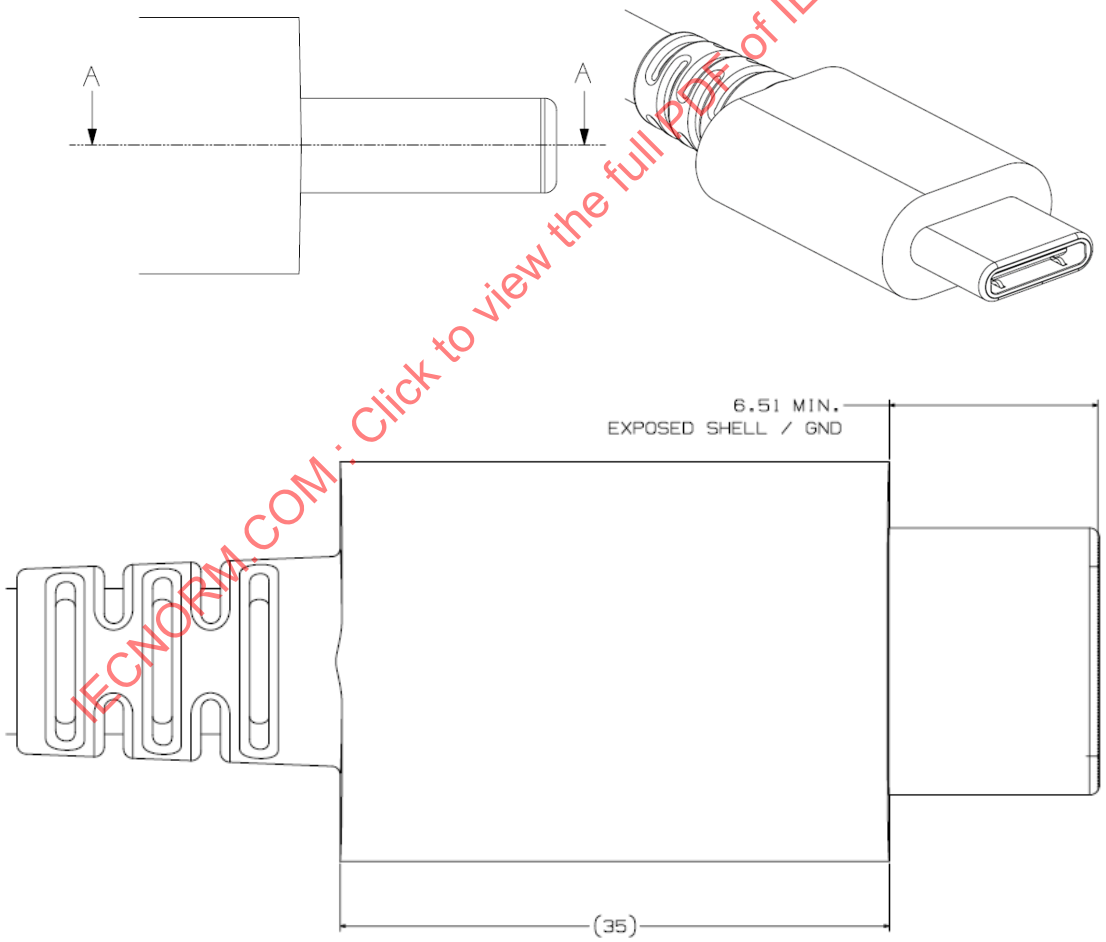


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This specification requires that all contacts be present in the mating interface of the USB Full-Featured Type-C receptacle connector and all contacts except the ***USB 3.2*** or ***USB4*** signals (i.e., A2, A3, A10, A11, B2, B3, B10 and B11) be present in the mating interface of the ***USB 2.0*** Type-C receptacle connector, but allows the plug to include only the contacts required for ***USB PD*** and ***USB 2.0*** functionality for applications that only support ***USB 2.0***. The ***USB 2.0*** Type-C plug is shown in Figure 3-11. The following design simplifications ***may*** be made when only ***USB 2.0*** is supported:

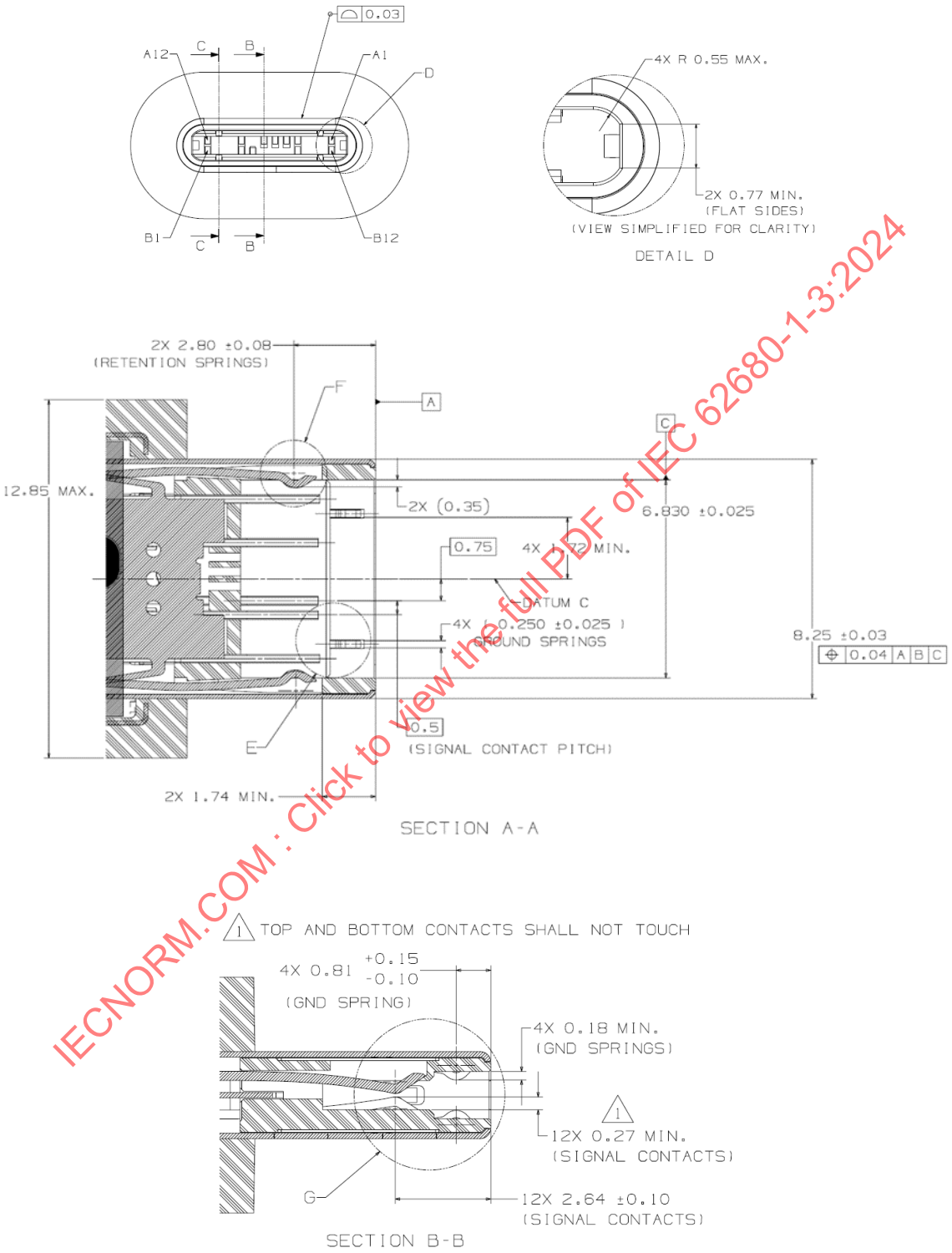
- Only the contacts necessary to support ***USB PD*** and ***USB 2.0*** are required in the plug. All other pin locations ***may*** be unpopulated. See Table 3-5.
- Unlike the USB Full-Featured Type-C plug, the internal EMC springs ***may*** be formed from the same strip as the signal, power, and ground contacts. The internal EMC springs contact the inner surface of the plug shell and mate with the receptacle EMC pads when the plug is seated in the receptacle. Alternately, the ***USB 2.0*** Type-C plug ***may*** use the same EMC spring configuration as defined for the USB Full-Featured Type-C plug. The ***USB 2.0*** Type-C plug four EMC spring locations are defined in Figure 3-11. The alternate configuration using the six spring locations is defined in Figure 3-1. Also refer to the reference designs in 3.2.2.3 for further clarification.
- A paddle card inside the plug ***may not*** be necessary if wires are directly attached to the contact pins.

Figure 3-11 *USB 2.0* Type-C Plug Interface Dimensions



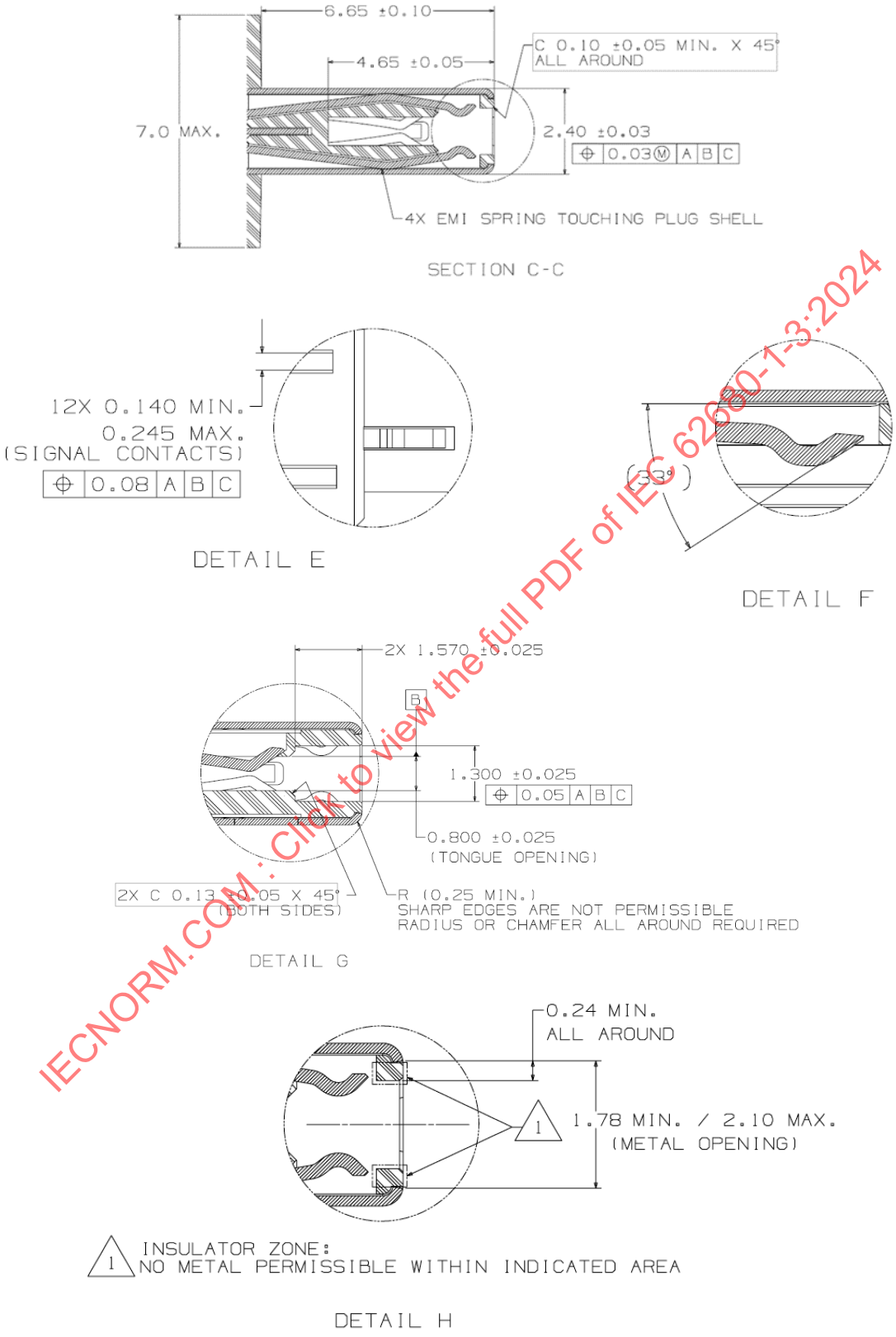
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Figure 3-11 *USB 2.0* Type-C Plug Interface Dimensions, cont.



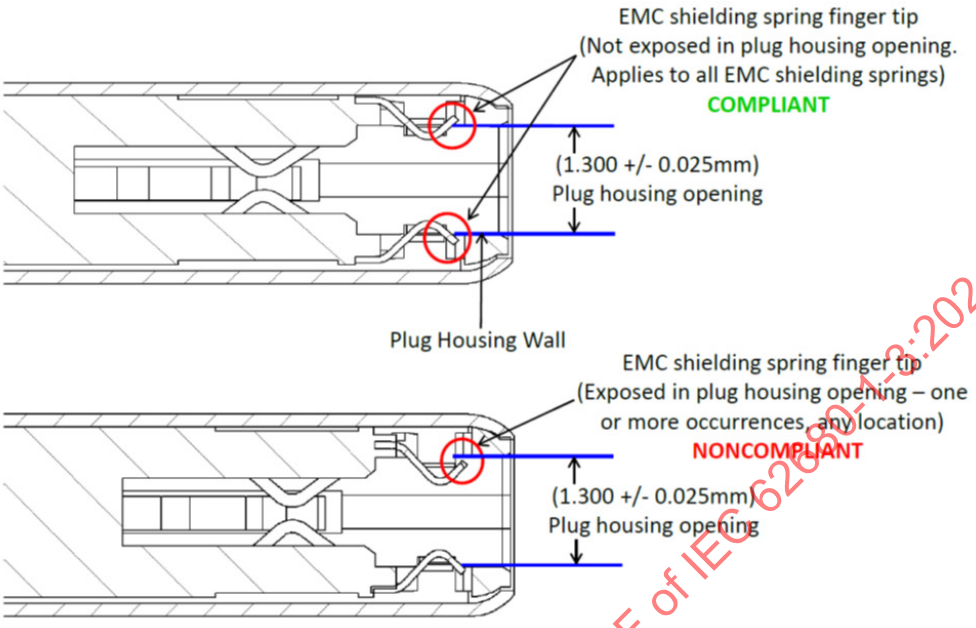
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Figure 3-11 *USB 2.0* Type-C Plug Interface Dimensions, cont.



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Figure 3-12 USB Type-C Plug EMC Shielding Spring Tip Requirements



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3.2.2 Reference Designs

This section provides reference designs for a few key features of the USB Type-C connector. The reference designs are provided as acceptable design examples. They are not ***normative***.

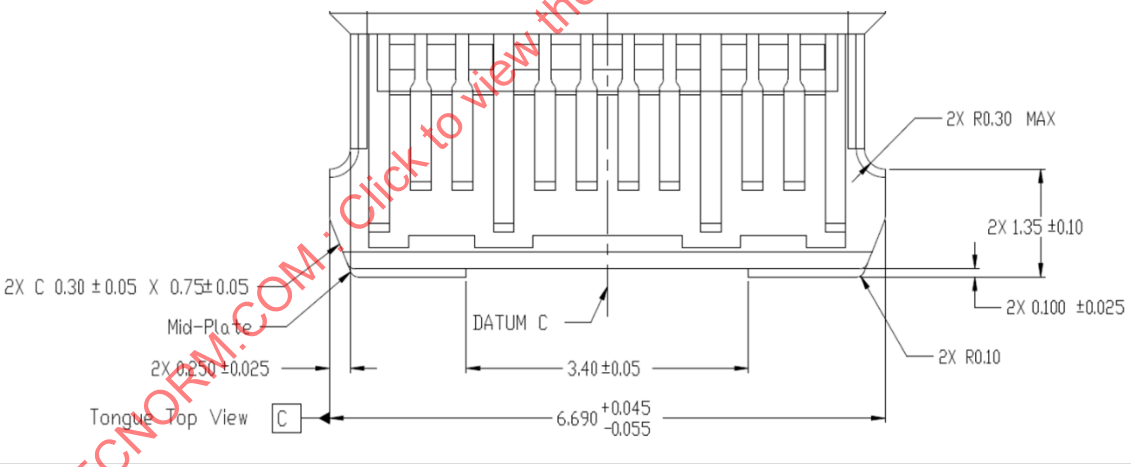
3.2.2.1 Receptacle Mid-Plate (*Informative*)

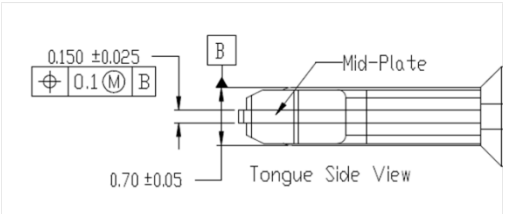
The signals between the top and bottom of the receptacle tongue are isolated by a mid-plate inside the tongue.

Figure 3-13 shows a reference design of the mid-plate. It is important to pay attention to the following features of the middle plate:

- The distance between the signal contacts and the mid-plate ***should*** be accurately controlled since the variation of this distance ***may*** significantly impact impedance of the connector.
- The mid-plate in this particular design protrudes slightly beyond the front surface of the tongue. This is to protect the tongue front surface from damage caused by miss-insertion of small objects into the receptacle.
- The mid-plate is required to be directly connected to the PCB ground with at least two grounding points.
- The sides of the mid-plate mate with the plug side latches, making ground connections to reduce EMC. Proper surface finishes are necessary in the areas where the side latches and mid-plate connections occur.

Figure 3-13 Reference Design of Receptacle Mid-Plate





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3.2.2.2 Side Latch (*Informative*)

The side latches (retention latches) are located in the plug. Figure 3-14 shows a reference design of a blanked side latch. The plug side latches ***should*** contact the receptacle mid-plate to provide an additional ground return path.

Figure 3-14 Reference Design of Retention Latch

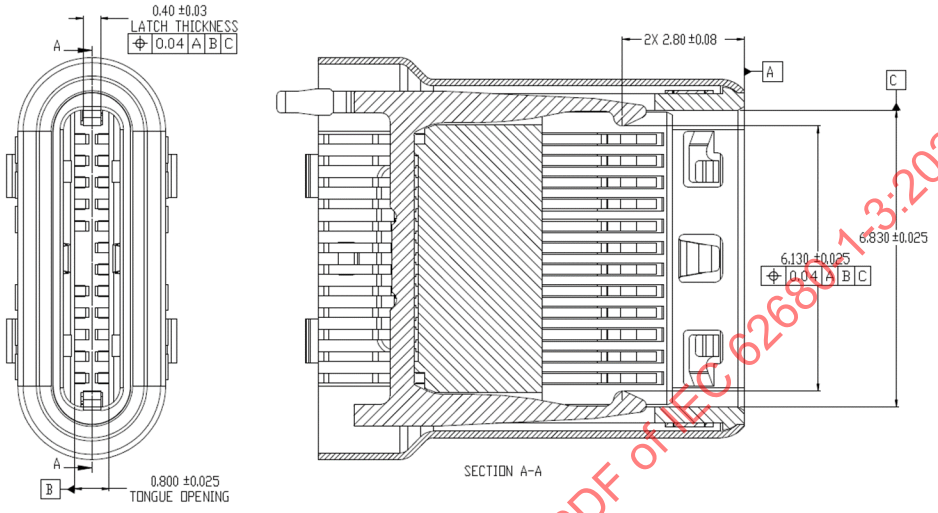
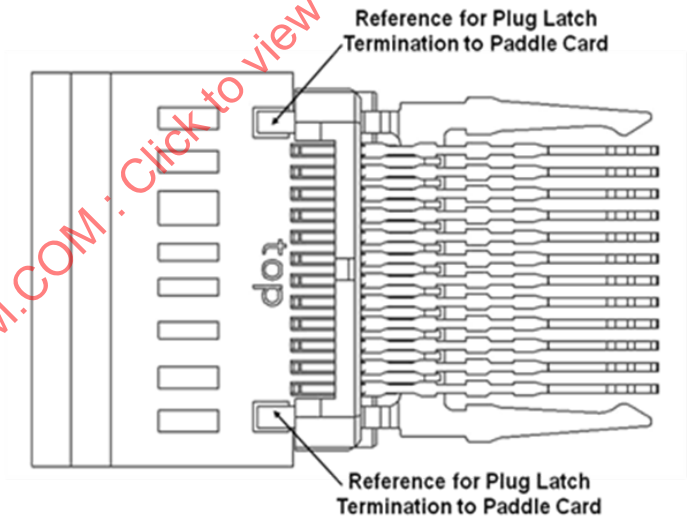


Figure 3-15 Illustration of the Latch Soldered to the Paddle Card Ground

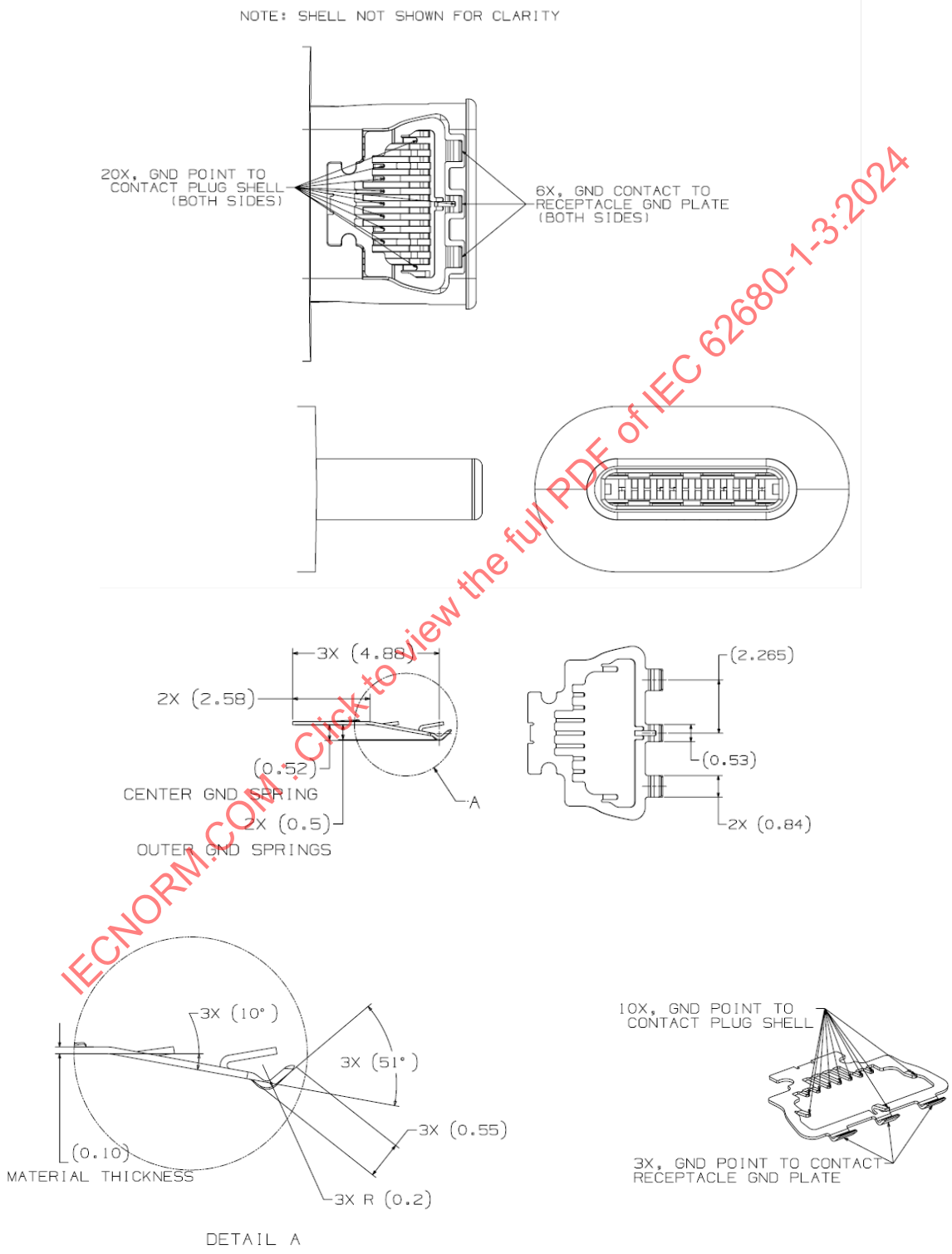


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3.2.2.3 Internal EMC Springs and Pads (*Informative*)

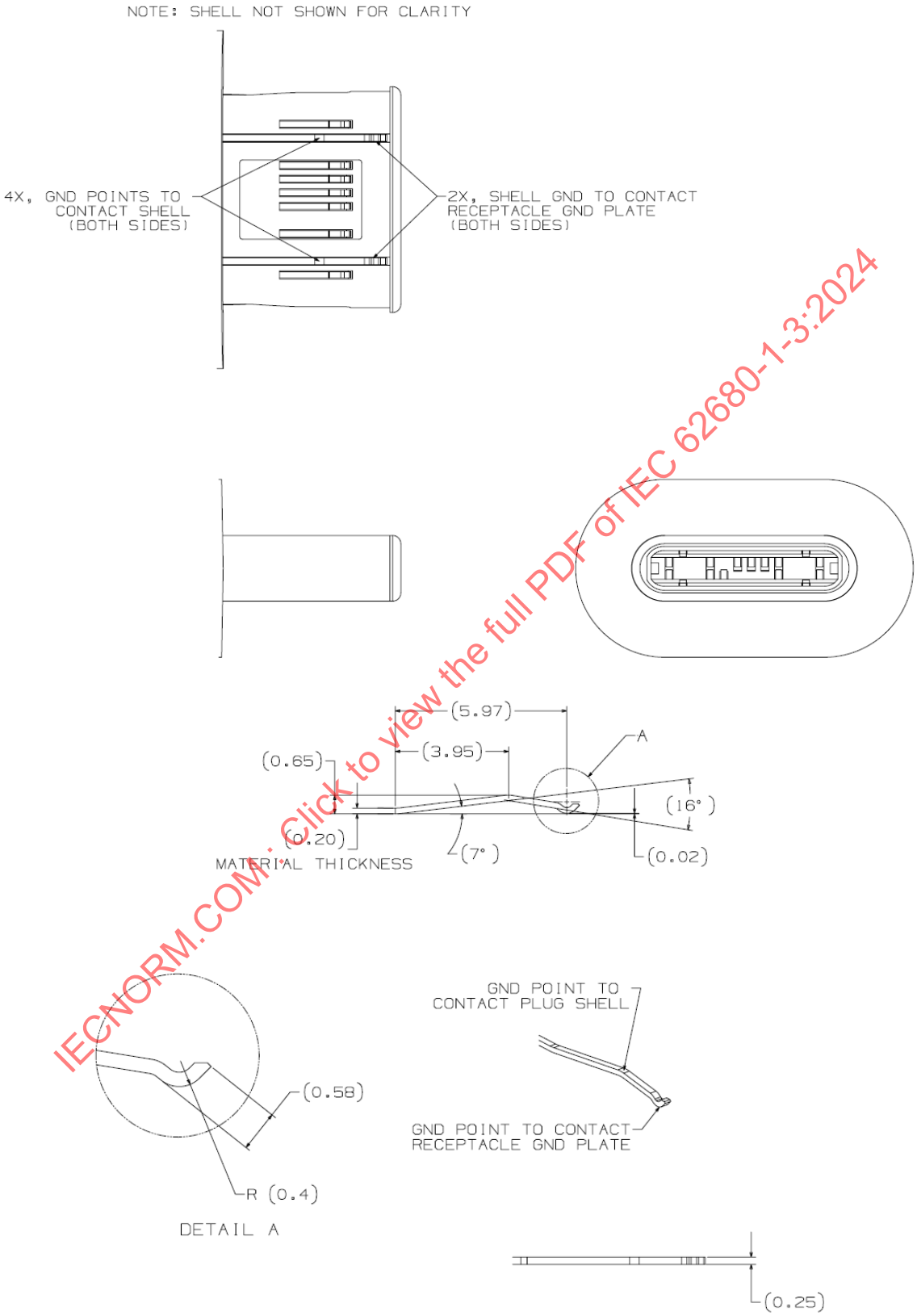
Figure 3-16 is a reference design of the internal EMC spring located inside the USB Full-Featured Type-C plug. Figure 3-17 is a reference design of the internal EMC spring located inside the ***USB 2.0*** Type-C plug.

Figure 3-16 Reference Design of the USB Full-Featured Type-C Plug Internal EMC Spring



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Figure 3-17 Reference Design of the *USB 2.0* Type-C Plug Internal EMC Spring

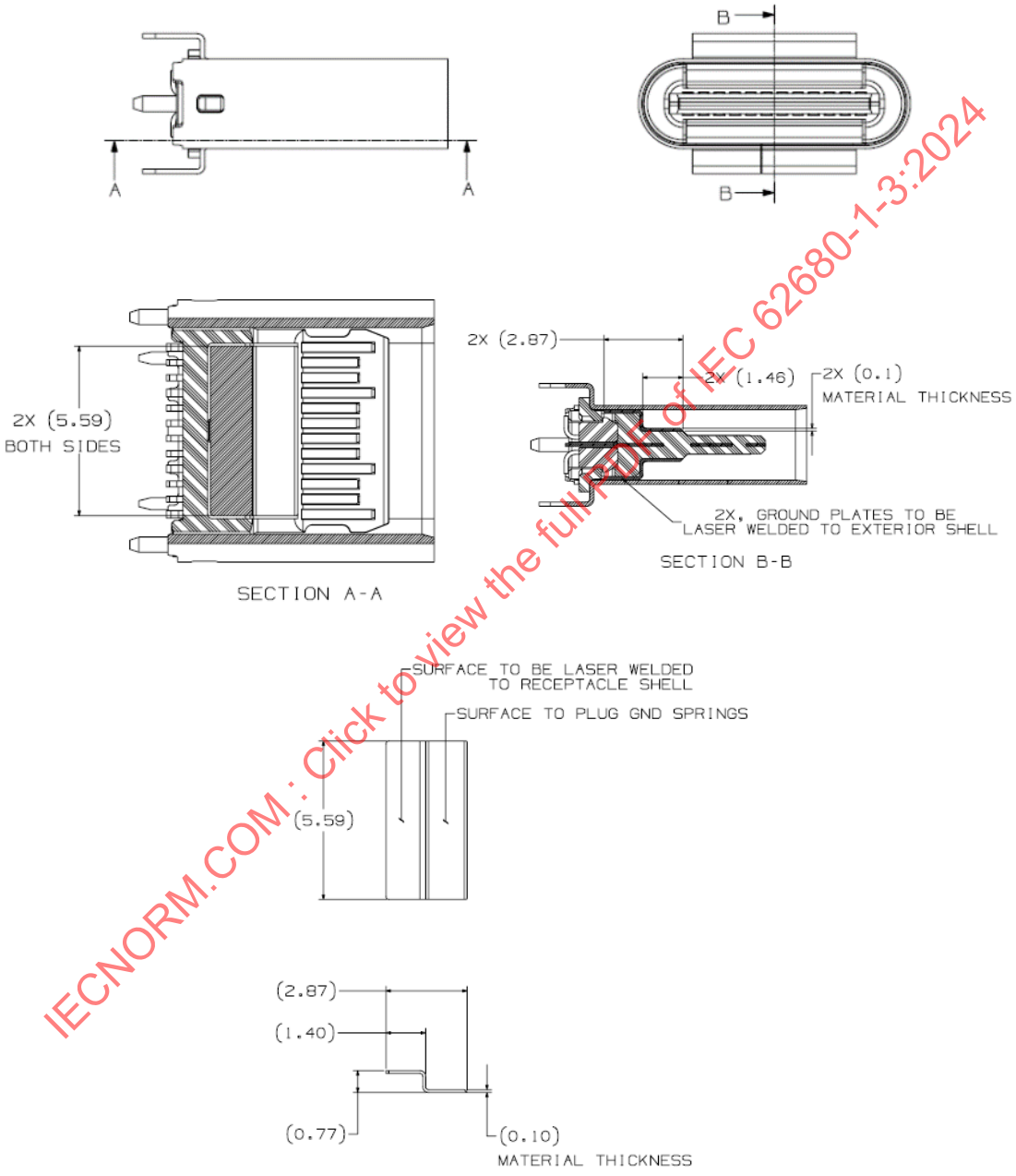


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It is critical that the internal EMC spring contacts the plug shell as close to the EMC spring mating interface as possible to minimize the length of the return path.

The internal EMC pad (i.e., ground plate) shown in Figure 3-18 is inside the receptacle. It mates with the EMC spring in the plug. To provide an effective ground return, the EMC pads ***should*** have multiple connections with the receptacle shell.

Figure 3-18 Reference Design of Internal EMC Pad

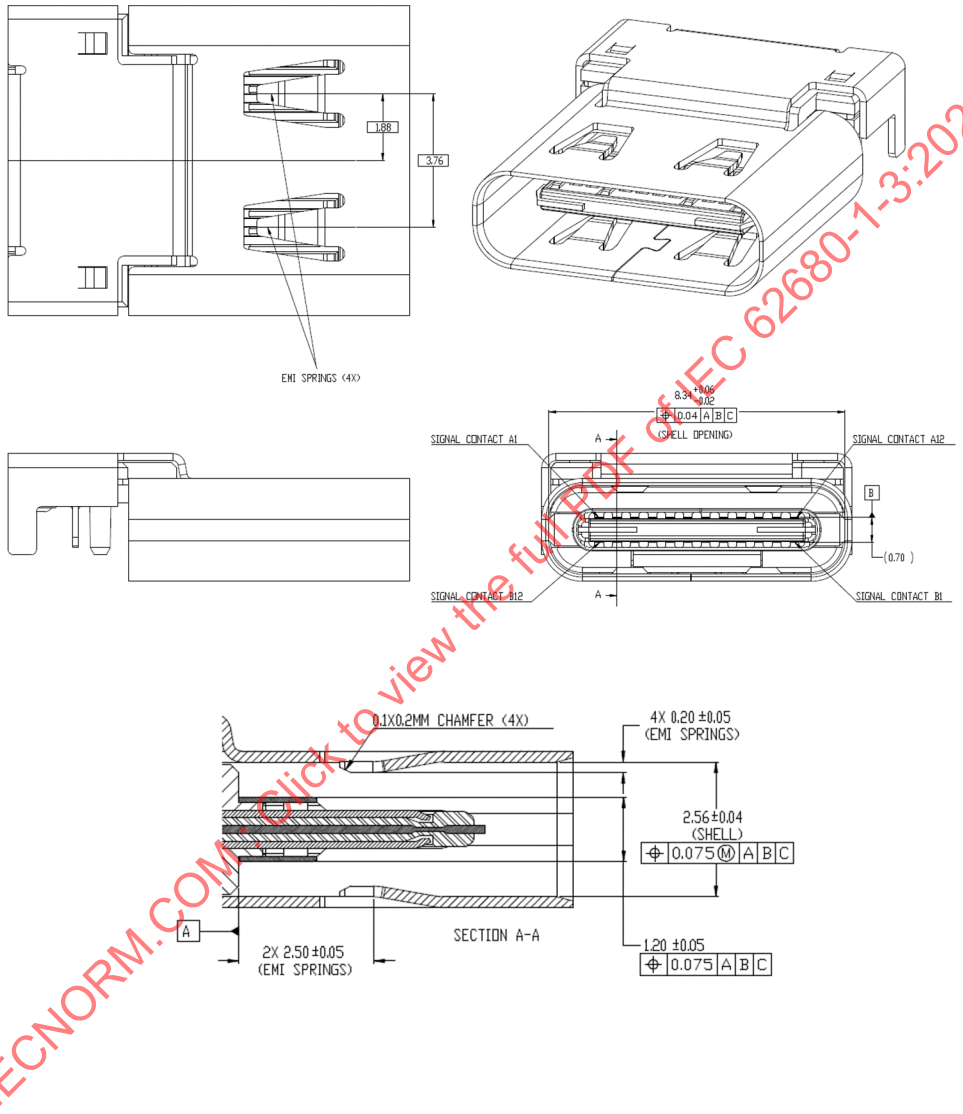


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3.2.2.4 Optional External Receptacle EMC Springs (*Informative*)

Some applications ***may*** use receptacles with EMC springs that contact the outside of the plug shell. Figure 3-19 shows a reference receptacle design with external EMC springs. The EMC spring contact landing zones for the fully mated condition are ***normative*** and defined in Section 3.2.1.

Figure 3-19 Reference Design of a USB Type-C Receptacle with External EMC Springs



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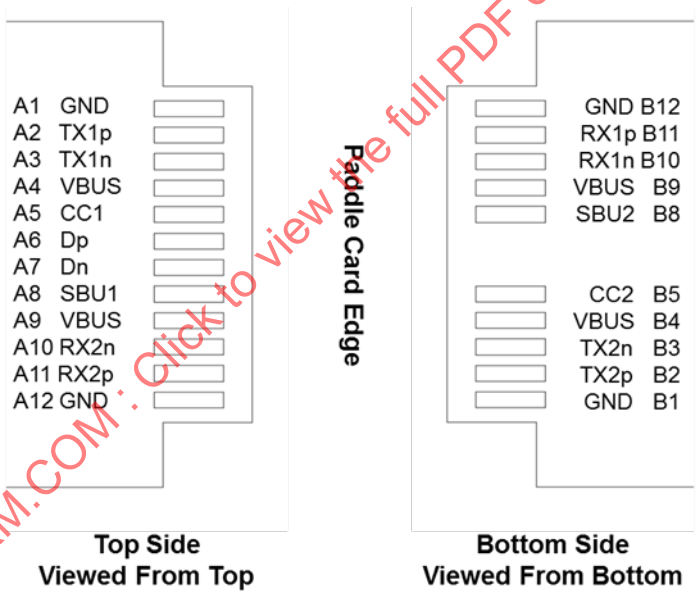
3.2.2.5 USB Full-Featured Type-C Plug Paddle Card (*Informative*)

The use of a paddle card is expected in the USB Full-Featured Type-C Plug.

Figure 3-20 illustrates the paddle card pin assignment and contact spring connection location for a USB Full-Featured Type-C plug. The following guidelines are provided for the paddle card design:

- The paddle card ***should*** use high performance substrate material. The recommended paddle card thickness ***should*** have a tolerance less than or equal to ± 10%.
- The USB TX/RX traces ***should*** be as short as possible and have a nominal differential characteristic impedance of 85 Ω.
- The wire attach ***should*** have two high speed differential pairs on one side and two other high-speed differential pairs on the other side, separated as far as practically allowed.
- It is recommended that a grounded coplanar waveguide (CPWG) system be selected as a transmission line method.
- Use of vias ***should*** be minimized.
- VBUS pins ***should*** be bussed together on the paddle card.
- GND pins ***should*** be bussed together on the paddle card.

Figure 3-20 Reference Design of a USB Full-Featured Type-C Plug Paddle Card



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3.2.3 Pin Assignments and Descriptions

The usage and assignments of the 24 pins for the USB Type-C receptacle interface are defined in Table 3-4.

Table 3-4 USB Type-C Receptacle Interface Pin Assignments

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2	TXp1	Positive half of first TX differential pair	Second	B11	RXp1	Positive half of first RX differential pair	Second
A3	TXn1	Negative half of first TX differential pair	Second	B10	RXn1	Negative half of first RX differential pair	Second
A4	VBUS	Bus Power	First	B9	VBUS	Bus Power	First
A5	CC1	Configuration Channel	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the ***USB 2.0*** differential pair – Position 1	Second	B7	Dn2	Negative half of the ***USB 2.0*** differential pair – Position 2	Second
A7	Dn1	Negative half of the ***USB 2.0*** differential pair – Position 1	Second	B6	Dp2	Positive half of the ***USB 2.0*** differential pair – Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel	Second
A9	VBUS	Bus Power	First	B4	VBUS	Bus Power	First
A10	RXn2	Negative half of second RX differential pair	Second	B3	TXn2	Negative half of second TX differential pair	Second
A11	RXp2	Positive half of second RX differential pair	Second	B2	TXp2	Positive half of second TX differential pair	Second
A12	GND	Ground return	First	B1	GND	Ground return	First

Notes:

1. Contacts B6 and B7 ***should not*** be present in the USB Type-C plug. The receptacle side ***shall*** support the ***USB 2.0*** differential pair present on Dp1/Dn1 or Dp2/Dn2. The plug orientation determines which pair is active. In one implementation, Dp1 and Dp2 ***may*** be shorted on the host/device as close to the receptacle as possible to minimize stub length; Dn1 and Dn2 ***may*** also be shorted. The maximum shorting trace length ***should not*** exceed 3.5 mm.
2. All VBUS pins ***shall*** be connected together within the USB Type-C plug and ***shall*** be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all VBUS pins bussed together on the PCB).
3. All Ground return pins ***shall*** be connected together within the USB Type-C plug and ***shall*** be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all ground return pins bussed together on the PCB).
4. If the contact dimensions shown in Figure 3 1 ALTERNATE SECTION A-A are used, then the VBUS contacts (A4, A9, B4 and B9) mate second, and signal contacts (A2, A3, A5, A6, A7, A8, A10, A11, B2, B3, B5, B6, B7, B8, B10 and B11) mate third.

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The usage and assignments of the signals necessary for the support of only ***USB 2.0*** with the USB Type-C mating interface are defined in Table 3-5.

Table 3-5 USB Type-C Receptacle Interface Pin Assignments for *USB 2.0*-only Support

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2				B11			
A3				B10			
A4	VBUS	Bus Power	First	B9	VBUS	Bus Power	First
A5	CC1	Configuration Channel	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the ***USB 2.0*** differential pair – Position 1	Second	B7	Dn2	Negative half of the ***USB 2.0*** differential pair – Position 2	Second
A7	Dn1	Negative half of the ***USB 2.0*** differential pair – Position 1	Second	B6	Dp2	Positive half of the ***USB 2.0*** differential pair – Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel	Second
A9	VBUS	Bus Power	First	B4	VBUS	Bus Power	First
A10				B3			
A11				B2			
A12	GND	Ground return	First	B1	GND	Ground return	First

Notes:

1. Unused contact locations ***shall*** be electrically isolated from power, ground or signaling (i.e., not connected).
2. Contacts B6 and B7 ***should not*** be present in the USB Type-C plug. The receptacle side ***shall*** support the ***USB 2.0*** differential pair present on Dp1/Dn1 or Dp2/Dn2. The plug orientation determines which pair is active. In one implementation, Dp1 and Dp2 ***may*** be shorted on the host/device as close to the receptacle as possible to minimize stub length; Dn1 and Dn2 ***may*** also be shorted. The maximum shorting trace length ***should not*** exceed 3.5 mm.
3. Contacts A8 and B8 (SBU1 and SBU2) ***shall not*** be connected unless required for a specified purpose.
4. All VBUS pins ***shall*** be connected together within the USB Type-C plug and ***shall*** be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all VBUS pins bussed together on the PCB).
5. All Ground return pins ***shall*** be connected together within the USB Type-C plug and ***shall*** be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all ground return pins bussed together on the PCB).
6. If the contact dimensions shown in Figure 3 1 ALTERNATE SECTION A-A are used then the VBUS contacts (A4, A9, B4 and B9) mate second, and signal contacts (A5, A6, A7, A8, B5, B6, B7 and B8) mate third.

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3.3 Cable Construction and Wire Assignments

This section discusses the USB Type-C cables, including cable construction, wire assignments, and wire gauges.

3.3.1 Cable Construction (*Informative*)

Figure 3-21 illustrates an example of USB Full-Featured Type-C cable cross-section, using micro-coaxial wires for TX/RX pairs. There are four groups of wires: USB D+/D– (typically unshielded twisted pairs (UTP)), TX/RX signal pairs (coaxial wires, twin-axial or shielded twisted pairs), sideband signal wires, and power and ground wires. In this example, the ***optional*** VCONN wire is shown whereas in Figure 3-22 the example is shown with the VCONN wire removed – the inclusion of VCONN or not relates to the implementation approach chosen for Electronically Marked Cables (See Section 4.9).

Figure 3-21 Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example with VCONN

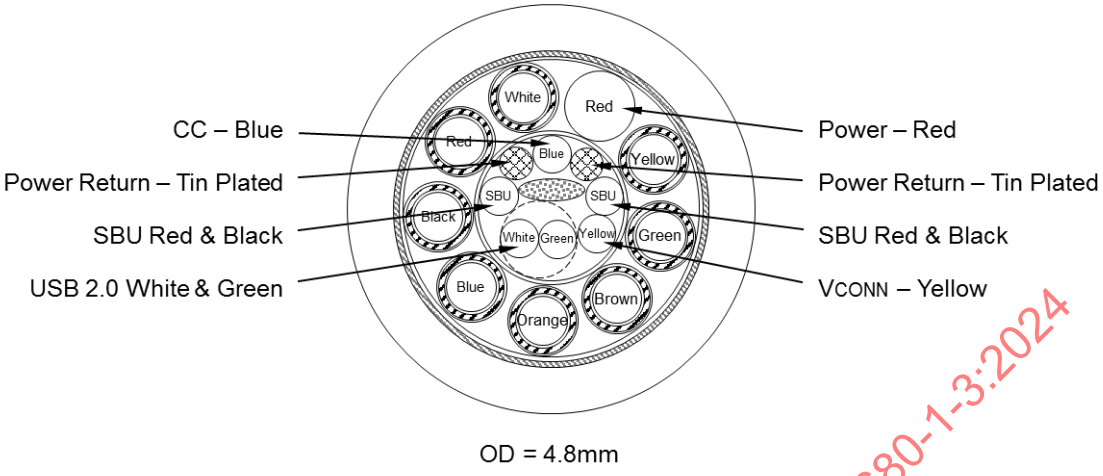
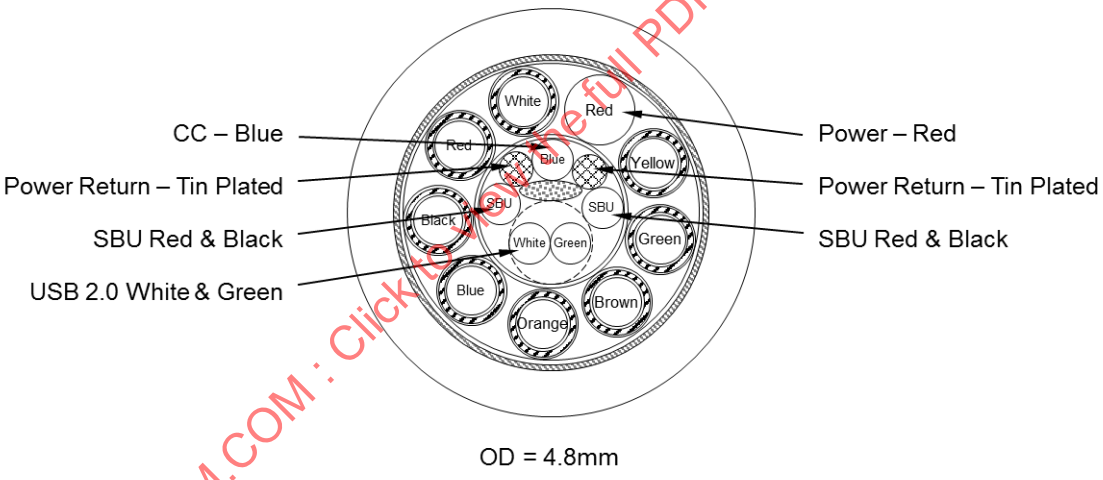


Figure 3-22 Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example without VCONN



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The USB D+/D– signal pair is intended to transmit the ***USB 2.0*** Low-Speed, Full-Speed and High-Speed signaling while the TX/RX signal pairs are used for either ***USB 3.2*** or ***USB4*** signaling. Shielding is needed for the TX/RX differential pairs for signal integrity and EMC performance.

3.3.2 Wire Assignments

Table 3-6 defines the full set of possible wires needed to produce all standard USB Type-C cables assemblies. For some cable assemblies, not all of these wires are used. For example, a USB Type-C cable that only provides ***USB 2.0*** functionality will not include wires 6–15.

Table 3-6 USB Type-C Standard Cable Wire Assignments

Wire Number	Signal Name	Description
1	GND_PWRrt1	Ground for power return
2	PWR_VBUS1	VBUS power
3	CC	Configuration Channel
4	UTP_Dp	Unshielded twist pair, positive
5	UTP_Dn	Unshielded twist pair, negative
6	SDPp1	Shielded differential pair #1, positive
7	SDPn1	Shielded differential pair #1, negative
8	SDPp2	Shielded differential pair #2, positive
9	SDPn2	Shielded differential pair #2, negative
10	SDPp3	Shielded differential pair #3, positive
11	SDPn3	Shielded differential pair #3, negative
12	SDPp4	Shielded differential pair #4, positive
13	SDPn4	Shielded differential pair #4, negative
14	SBU_A	Sideband Use
15	SBU_B	Sideband Use
16	GND_PWRrt2	Ground for power return (***optional***)
17	PWR_VBUS2	VBUS power (***optional***)
18	PWR_VCONN	VCONN power (***optional***, see Section 4.9)
Braid	Shield	Cable external braid

Note:

1. This table assumes that coaxial wire construction is used for all SDP's and there are no drain wires. The signal ground return is through the shields of the coaxial wires. If shielded twisted or twin-axial pairs are used, then drain wires are needed.

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Table 3-7 defines the full set of possible wires needed to produce USB Type-C to legacy cable assemblies. For some cable assemblies, not all of these wires are needed. For example, a USB Type-C to ***USB 2.0*** Standard-B cable will not include wires 5–10.

Table 3-7 USB Type-C Cable Wire Assignments for Legacy Cables/Adapters

Wire Number	Signal Name	Description
1	GND_PWRrt1	Ground for power return
2	PWR_VBUS1	VBUS power
3	UTP_Dp	Unshielded twist pair, positive
4	UTP_Dn	Unshielded twist pair, negative
5	SDPp1	Shielded differential pair #1, positive
6	SDPn1	Shielded differential pair #1, negative
7	SDP1_Drain	Drain wire for SDPp1 and SDPn1
8	SDPp2	Shielded differential pair #2, positive
9	SDPn2	Shielded differential pair #2, negative
10	SDP2_Drain	Drain wire for SDPp2 and SDPn2
Braid	Shield	Cable external braid

Note:
1. This table assumes that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are needed, and the signal ground return is through the shields of the coaxial wires .

3.3.3 Wire Gauges and Cable Diameters (*Informative*)

This specification does not specify wire gauge. Table 3-8 and Table 3-9 list typical wire gauges for reference purposes only. A large gauge wire incurs less loss, but at the cost of cable diameter and flexibility. Multiple wires ***may*** be used for a single wire such as for VBUS or Ground. It is recommended to use the smallest possible wire gauges that meet the cable assembly electrical and mechanical requirements.

To maximize cable flexibility, all wires ***should*** be stranded, and the cable outer diameter ***should*** be minimized as much as possible. A typical USB Full-Featured Type-C cable outer diameter ***may*** range from 4 mm to 6 mm while a typical ***USB 2.0*** Type-C cable outer diameter ***may*** range from 2 mm to 4 mm. A typical USB Type-C to ***USB 3.1*** legacy cable outer diameter ***may*** range from 3 mm to 5 mm.

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Table 3-8 Reference Wire Gauges for standard USB Type-C Cable Assemblies

Wire Number	Signal Name	Wire Gauge (AWG)
1	GND_PWRrt1	20-28
2	PWR_VBUS1	20-28
3	CC	32-34
4	UTP_Dp	28-34
5	UTP_Dn	28-34
6	SDPp1	26-34
7	SDPn1	26-34
8	SDPp2	26-34
9	SDPn2	26-34
10	SDPp3	26-34
11	SDPn3	26-34
12	SDPp4	26-34
13	SDPn4	26-34
14	SBU_A	32-34
15	SBU_B	32-34
16	GND_PWRrt2	20-28
17	PWR_VBUS2	20-28
18	PWR_VCONN	32-34

Table 3-9 Reference Wire Gauges for standard USB Type-C to Legacy Cable Assemblies

Wire Number	Signal Name	Wire Gauge (AWG)
1	GND_PWRrt1	20-28
2	PWR_VBUS1	20-28
3	UTP_Dp	28-34
4	UTP_Dn	28-34
5	SDPp1	26-34
6	SDPn1	26-34
7	SDP1_Drain	28-34
8	SDPp2	26-34
9	SDPn2	26-34
10	SDP2_Drain	28-34

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3.4 Standard USB Type-C Cable Assemblies

Two standard USB Type-C cable assemblies are defined and allowed by this specification. In addition, captive cables are allowed (see Section 3.4.3). Shielding (braid) is required to enclose all the wires in the USB Type-C cable. The shield ***shall*** be terminated to the plug metal shells. The shield ***should*** be physically connected to the plug metal shell as close to 360° as possible, to control EMC.

Note: Up until Release 1.4 of this specification, the TX and RX signals used in this specification were named SSTX and SSRX. With the introduction of ***USB4***, these signals were renamed such that they generically can apply to both SuperSpeed USB and ***USB4*** signaling. It is intended that the TX and RX signal names are synonymous with the original SSTX and SSRX names for implementations prior to Release 2.0 of this specification.

3.4.1 USB Full-Featured Type-C Cable Assembly

Figure 3-23 shows a USB Full-Featured Type-C standard cable assembly.

Figure 3-23 USB Full-Featured Type-C Standard Cable Assembly

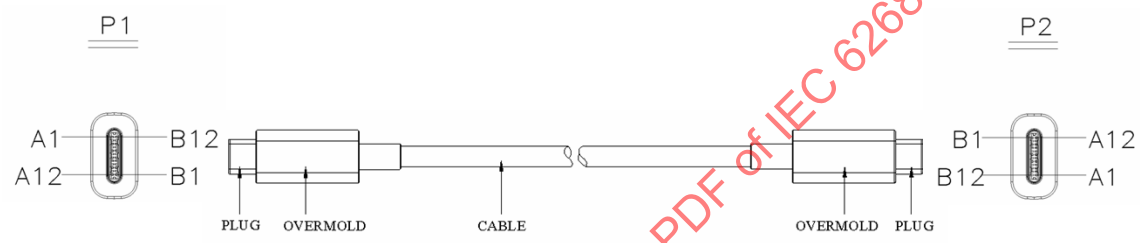


Table 3-10 defines the wire connections for the USB Full-Featured Type-C standard cable assembly.

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Table 3-10 USB Full-Featured Type-C Standard Cable Assembly Wiring

USB Type-C Plug #1		Wire		USB Type-C Plug #2	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 [16]	GND_PWRrt1 [GND_PWRrt2]	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2 [17]	PWR_VBUS1 [PWR_VBUS2]	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (See 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
A2	TXp1	6	SDPp1	B11	RXp1
A3	TXn1	7	SDPn1	B10	RXn1
B11	RXp1	8	SDPp2	A2	TXp1
B10	RXn1	9	SDPn2	A3	TXn1
B2	TXp2	10	SDPp3	A11	RXp2
B3	TXn2	11	SDPn3	A10	RXn2
A11	RXp2	12	SDPp4	B2	TXp2
A10	RXn2	13	SDPn4	B3	TXn2
A8	SBU1	14	SBU_A	B8	SBU2
B8	SBU2	15	SBU_B	A8	SBU1
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. This table assumes that coaxial wire construction is used for all SDP's and there are no drain wires. The shields of the coaxial wires are connected to the ground pins. If shielded twisted pair is used, then drain wires are needed and ***shall*** be connected to the GND pins.
2. Pin B5 (VCONN) of the USB Type-C plug ***shall*** be used in electronically marked versions of this cable. See Section 4.9.
3. Contacts B6 and B7 ***should not*** be present in the USB Type-C plug.
4. All VBUS pins ***shall*** be connected together within the USB Type-C plug. A 10 nF bypass capacitor (minimum recommended voltage rating of 30 V, 63 V if EPR-capable) is required for the VBUS pin in the full-featured cable at each end of the cable. The bypass capacitor ***should*** be placed as close as possible to the power supply pad.
5. All GND pins ***shall*** be connected together within the USB Type-C plug
6. Shield and GND ***shall*** be connected within the USB Type-C plug on both ends of the cable assembly.

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3.4.1.1 Cable Certification and Identification

All USB Full-Featured Type-C cable assemblies ***shall*** be Electronically Marked and include information in the eMarker as defined by the ***USB PD*** specification.

All USB Full-Featured Type-C cable assemblies ***should*** be certified and visibly identified with certified cable identification icons as defined by the ***USB-IF***. This enables end users to be able to confirm visually the functional capabilities of the cable in terms of the cable's power rating, either 60W or 240W, and the cable's data performance, e.g., 5 Gbps, 20 Gbps or higher.

3.4.2 *USB 2.0* Type-C Cable Assembly

A ***USB 2.0*** Type-C standard cable assembly has the same form factor shown in Figure 3-23.

Table 3-11 defines the wire connections for the ***USB 2.0*** Type-C standard cable assembly.

Table 3-11 *USB 2.0* Type-C Standard Cable Assembly Wiring

USB Type-C Plug #1		Wire		USB Type-C Plug #2	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 [16]	GND_PWRrt1 [GND_PWRrt2]	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2 [17]	PWR_VBUS1 [PWR_VBUS2]	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (See Section 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin B5 (VCONN) of the USB Type-C plug ***shall*** be used in electronically marked versions of this cable. See Section 4.9.
2. Contacts B6 and B7 ***should not*** be present in the USB Type-C plug.
3. All VBUS pins ***shall*** be connected together within the USB Type-C plug. A bypass capacitor is not required for the VBUS pin in the ***USB 2.0*** Type-C cable.
4. All GND pins ***shall*** be connected together within the USB Type-C plug.
5. All USB Type-C plug pins that are not listed in this table ***shall*** be open (not connected).
6. Shield and GND grounds ***shall*** be connected within the USB Type-C plug on both ends of the cable assembly.

3.4.2.1 Cable Certification and Identification

All ***USB 2.0*** Type-C cable assemblies that are rated for higher than 3A ***shall*** be Electronically Marked and include information in the eMarker as defined by the ***USB PD*** specification.

All ***USB 2.0*** Type-C cable assemblies ***should*** be certified and visibly identified with certified cable identification icons as defined by the ***USB-IF***. This enables end users to be able to confirm visually the functional capabilities of the cable in terms of the cable's power rating, either 60W or 240W.

3.4.3 USB Type-C Captive Cable Assembly

A captive cable assembly is a cable assembly that is terminated on one end with a USB Type-C plug and has a vendor-specific connect means (hardwired or custom detachable) on the opposite end. The cable assembly that is hardwired is not detachable from the device.

The assembly wiring for captive USB Type-C cables follow the same wiring assignments as the standard cable assemblies (see Table 3-10 and Table 3-11) with the exception that the hardwired attachment on the device side substitutes for the USB Type-C Plug #2 end.

The CC wire in a captive cable ***shall*** be terminated and behave as appropriate to the function of the product to which it is captive (e.g., host or device).

A device (Sink, UFP or DRP) with a captive cable assembly ***shall*** respond to SOP' cable identity inquiries when the device either sinks higher than 3A current or supports ***USB4*** operation. The physical location of the eMarker can be either within the captive cable or the device with the cable.

This specification does not define how the hardware attachment is physically done on the device side.

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3.4.4 USB Type-C Thumb Drive Assembly

A thumb drive assembly is an assembly that incorporates a USB Type-C plug as its primary USB interface. This assembly does not functionally include a cable assembly.

A thumb drive device (Sink, UFP or DRP) ***shall*** respond to SOP' cable identity inquiries when it either sinks higher than 3A current or supports ***USB4*** operation.

3.5 Legacy Cable Assemblies

To enable interoperability between USB Type-C-based products and legacy USB products, the following standard legacy cable assemblies are defined. Only the cables defined within this specification are allowed.

Legacy cable assemblies that source power to a USB Type-C connector (e.g., a USB Type-C to USB Standard-A plug cable assembly and a USB Type-C plug to USB Micro-B receptacle adapter assembly) are required to use the Default ***USB Type-C Current Rp*** resistor (56 kΩ). The value of ***Rp*** is used to inform the Sink how much current the Source can provide. Since the legacy cable assembly does not comprehend the capability of the Source it is connected to, it is only allowed to advertise Default ***USB Type-C Current*** as defined by the ***USB 2.0***, ***USB 3.1,*** and ***USB BC 1.2*** specifications. No other ***Rp*** values are permitted because these ***may*** cause a USB Type-C Sink to overload a legacy power supply.

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3.5.1 USB Type-C to *USB 3.1* Standard-A Cable Assembly

Figure 3-24 shows a USB Type-C to ***USB 3.1*** Standard-A cable assembly.

Figure 3-24 USB Type-C to *USB 3.1* Standard-A Cable Assembly



Table 3-12 defines the wire connections for the USB Type-C to ***USB 3.1*** Standard-A cable assembly.

Table 3-12 USB Type-C to *USB 3.1* Standard-A Cable Assembly Wiring

USB Type-C Plug		Wire		*USB 3.1* Standard-A Plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 2			
B5	VCONN				
A6	Dp1	4	UTP_Dp	3	D+
A7	Dn1	5	UTP_Dn	2	D–
A2	TXp1	6	SDPp1	6	StdA_SSRX+
A3	TXn1	7	SDPn1	5	StdA_SSRX–
B11	RXp1	8	SDPp2	9	StdA_SSTX+
B10	RXn1	9	SDPn2	8	StdA_SSTX–
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. This table assumes that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present, and the shields of the coaxial wires are connected to the ground pins.
2. Pin A5 (CC) of the USB Type-C plug ***shall*** be connected to VBUS through a resistor ***Rp*** (56 kΩ ± 5%). See Section 4.5.3.2.2 and Table 4-27 for the functional description and value of ***Rp***.
3. Contacts B6 and B7 ***should not*** be present in the USB Type-C plug.
4. All VBUS pins ***shall*** be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor ***shall*** be 10nF ± 20% in cables which incorporate a USB Standard-A plug. The bypass capacitor ***shall*** be placed as close as possible to the power supply pad.
5. All Ground return pins ***shall*** be connected together within the USB Type-C plug.
6. Shield and GND grounds ***shall*** be connected within the USB Type-C and ***USB 3.1*** Standard-A plugs on both ends of the cable assembly.
7. All USB Type-C plug pins that are not listed in this table ***shall*** be open (not connected).

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3.5.2 USB Type-C to *USB 2.0* Standard-A Cable Assembly

Figure 3-25 shows a USB Type-C to ***USB 2.0*** Standard-A cable assembly.

Figure 3-25 USB Type-C to *USB 2.0* Standard-A Cable Assembly

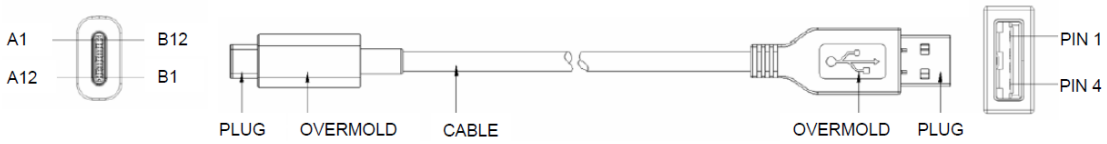


Table 3-13 defines the wire connections for the USB Type-C to ***USB 2.0*** Standard-A cable assembly.

Table 3-13 USB Type-C to *USB 2.0* Standard-A Cable Assembly Wiring

USB Type-C Plug		Wire		*USB 2.0* Standard-A Plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	4	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug ***shall*** be connected to VBUS through a resistor ***Rp*** (56 kΩ ± 5%). See Section 4.5.3.2.2 and Table 4-27 for the functional description and value of ***Rp***.
2. Contacts B6 and B7 ***should not*** be present in the USB Type-C plug.
3. All VBUS pins ***shall*** be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins ***shall*** be connected together within the USB Type-C plug.
5. Shield and GND grounds ***shall*** be connected within the USB Type-C and ***USB 2.0*** Standard-A plugs on both ends of the cable assembly.
6. All USB Type-C plug pins that are not listed in this table ***shall*** be open (not connected).

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3.5.3 USB Type-C to *USB 3.1* Standard-B Cable Assembly

Figure 3-26 shows a USB Type-C to ***USB 3.1*** Standard-B cable assembly.

Figure 3-26 USB Type-C to *USB 3.1* Standard-B Cable Assembly

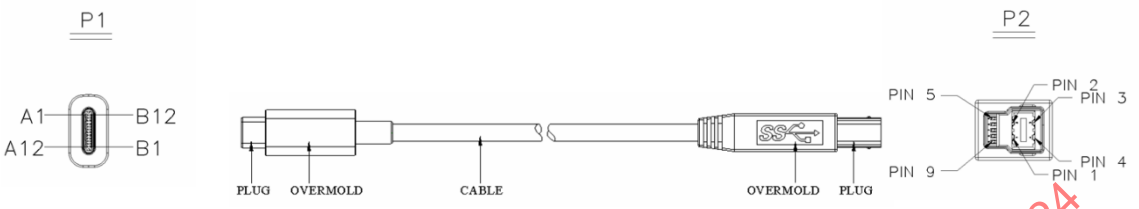


Table 3-14 defines the wire connections for the USB Type-C to ***USB 3.1*** Standard-B cable assembly.

Table 3-14 USB Type-C to *USB 3.1* Standard-B Cable Assembly Wiring

USB Type-C Plug		Wire		*USB 3.1* Standard-B Plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	4	UTP_Dp	3	D+
A7	Dn1	5	UTP_Dn	2	D–
A2	TXp1	6	SDPp1	9	StdB_SSRX+
A3	TXn1	7	SDPn1	8	StdB_SSRX–
B11	RXp1	8	SDPp2	6	StdB_SSTX+
B10	RXn1	9	SDPn2	5	StdB_SSTX–
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug ***shall*** be connected to GND through a resistor ***Rd*** (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-28 for the functional description and value of ***Rd***.
2. This table assumes that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present, and the shields of the coaxial wires are connected to the ground pins.
3. Contacts B6 and B7 ***should not*** be present in the USB Type-C plug.
4. All VBUS pins ***shall*** be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor ***shall*** be 10nF ± 20% in cables which incorporate a USB Standard-B plug. The bypass capacitor ***shall*** be placed as close as possible to the power supply pad.
5. All Ground return pins ***shall*** be connected together within the USB Type-C plug.
6. Shield and GND grounds ***shall*** be connected within the USB Type-C and ***USB 3.1*** Standard-B plugs on both ends of the cable assembly.
7. All USB Type-C plug pins that are not listed in this table ***shall*** be open (not connected).

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3.5.4 USB Type-C to *USB 2.0* Standard-B Cable Assembly

Figure 3-27 shows a USB Type-C to ***USB 2.0*** Standard-B cable assembly.

Figure 3-27 USB Type-C to *USB 2.0* Standard-B Cable Assembly

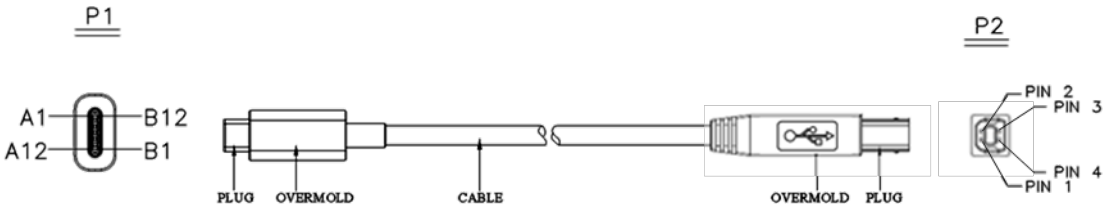


Table 3-15 defines the wire connections for the USB Type-C to ***USB 2.0*** Standard-B cable assembly.

Table 3-15 USB Type-C to *USB 2.0* Standard-B Cable Assembly Wiring

USB Type-C Plug		Wire		*USB 2.0* Standard-B Plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	4	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug ***shall*** be connected to GND through a resistor ***Rd*** (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-28 for the functional description and value of ***Rd***.
2. Contacts B6 and B7 ***should not*** be present in the USB Type-C plug.
3. All VBUS pins ***shall*** be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins ***shall*** be connected together within the USB Type-C plug.
5. Shield and GND grounds ***shall*** be connected within the USB Type-C and ***USB 2.0*** Standard-B plugs on both ends of the cable assembly.
6. All USB Type-C plug pins that are not listed in this table ***shall*** be open (not connected).

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3.5.5 USB Type-C to *USB 2.0* Mini-B Cable Assembly

Figure 3-28 shows a USB Type-C to ***USB 2.0*** Mini-B cable assembly.

Figure 3-28 USB Type-C to *USB 2.0* Mini-B Cable Assembly

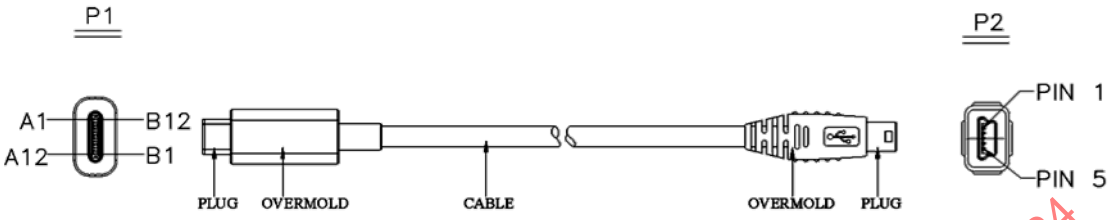


Table 3-16 defines the wire connections for the USB Type-C to ***USB 2.0*** Mini-B cable assembly.

Table 3-16 USB Type-C to *USB 2.0* Mini-B Cable Assembly Wiring

USB Type-C Plug		Wire		*USB 2.0* Mini-B Plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
				4	ID
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug ***shall*** be connected to GND through a resistor ***Rd*** (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-28 for the functional description and value of ***Rd***.
2. Contacts B6 and B7 ***should not*** be present in the USB Type-C plug.
3. All VBUS pins ***shall*** be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins ***shall*** be connected together within the USB Type-C plug.
5. Pin 4 (ID) of the ***USB 2.0*** Mini-B plug ***shall*** be terminated as defined in the applicable specification for the cable type.
6. Shield and GND grounds ***shall*** be connected within the USB Type-C and ***USB 2.0*** Mini-B plugs on both ends of the cable assembly.
7. All USB Type-C plug pins that are not listed in this table ***shall*** be open (not connected).

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3.5.6 USB Type-C to *USB 3.1* Micro-B Cable Assembly

Figure 3-29 shows a USB Type-C to ***USB 3.1*** Micro-B cable assembly.

Figure 3-29 USB Type-C to *USB 3.1* Micro-B Cable Assembly

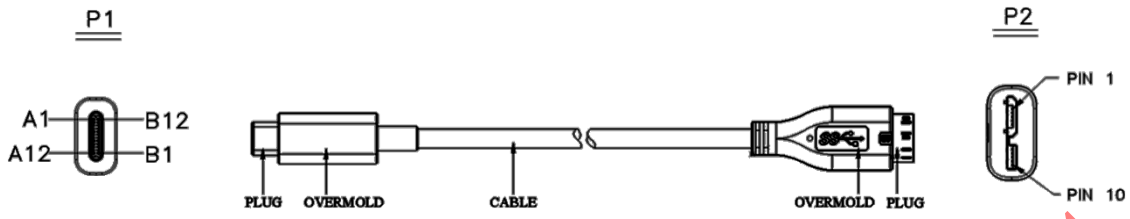


Table 3-17 defines the wire connections for the USB Type-C to ***USB 3.1*** Micro-B cable assembly.

Table 3-17 USB Type-C to *USB 3.1* Micro-B Cable Assembly Wiring

USB Type-C Plug		Wire		*USB 3.1* Micro-B Plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	5 8	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	4	UTP_Dp	3	D+
A7	Dn1	5	UTP_Dn	2	D–
A2	TXp1	6	SDPp1	10	MicB_SSRX+
A3	TXn1	7	SDPn1	9	MicB_SSRX–
B11	RXp1	8	SDPp2	7	MicB_SSTX+
B10	RXn1	9	SDPn2	6	MicB_SSTX–
				4	ID
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug ***shall*** be connected to GND through a resistor ***Rd*** (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-28 for the functional description and value of ***Rd***.
2. This table assumes that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present, and the shields of the coaxial wires are connected to the ground pins.
3. Contacts B6 and B7 ***should not*** be present in the USB Type-C plug.
4. All VBUS pins ***shall*** be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor ***shall*** be 10nF ± 20% in cables which incorporate a USB Micro-B plug. The bypass capacitor ***shall*** be placed as close as possible to the power supply pad.
5. All Ground return pins ***shall*** be connected together within the USB Type-C plug.
6. Pin 4 (ID) of the ***USB 3.1*** Micro-B plug ***shall*** be terminated as defined in the applicable specification for the cable type.
7. Shield and GND grounds ***shall*** be connected within the USB Type-C and ***USB 3.1*** Micro-B plugs on both ends of the cable assembly.
8. All USB Type-C plug pins that are not listed in this table ***shall*** be open (not connected).

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3.5.7 USB Type-C to *USB 2.0* Micro-B Cable Assembly

Figure 3-30 shows a USB Type-C to ***USB 2.0*** Micro-B cable assembly.

Figure 3-30 USB Type-C to *USB 2.0* Micro-B Cable Assembly

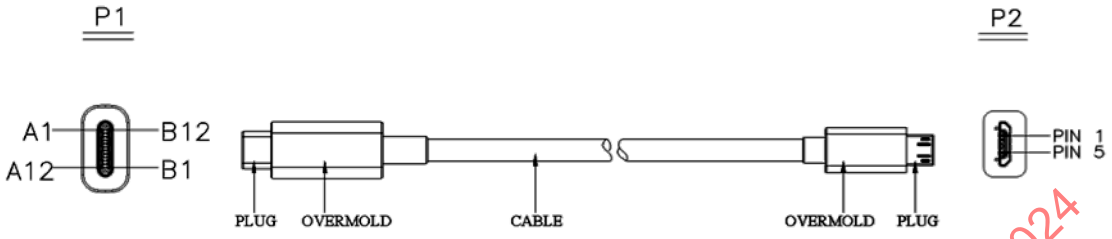


Table 3-18 defines the wire connections for the USB Type-C to ***USB 2.0*** Micro-B cable assembly.

Table 3-18 USB Type-C to *USB 2.0* Micro-B Cable Assembly Wiring

USB Type-C Plug		Wire		*USB 2.0* Micro-B Plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWR1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
				4	ID
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug ***shall*** be connected to GND through a resistor ***Rd*** (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-28 for the functional description and value of ***Rd***.
2. Contacts B6 and B7 ***should not*** be present in the USB Type-C plug.
3. All VBUS pins ***shall*** be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins ***shall*** be connected together within the USB Type-C plug.
5. Pin 4 (ID) of the ***USB 2.0*** Micro-B plug ***shall*** be terminated as defined in the applicable specification for the cable type.
6. Shield and GND grounds ***shall*** be connected within the USB Type-C and ***USB 2.0*** Micro-B plugs on both ends of the cable assembly.
7. All USB Type-C plug pins that are not listed in this table ***shall*** be open (not connected).

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3.6 Legacy Adapter Assemblies

To enable interoperability between USB Type-C-based products and legacy USB products, the following standard legacy adapter assemblies are defined. Only the adapter assemblies defined in this specification are allowed.

3.6.1 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly

Figure 3-31 shows a USB Type-C to ***USB 3.1*** Standard-A receptacle adapter assembly. This cable assembly is defined for direct connect to a USB device (e.g., a thumb drive). System functionality of using this adaptor assembly together with another USB cable assembly is not guaranteed.

Figure 3-31 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly

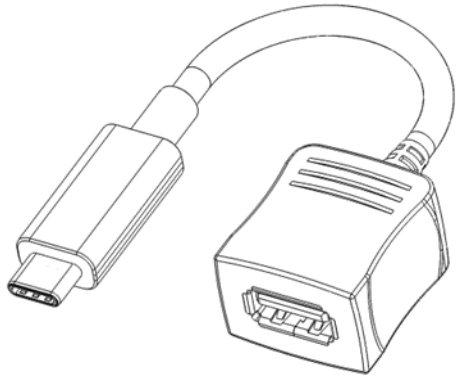


Table 3-19 defines the wire connections for the USB Type-C to ***USB 3.1*** Standard-A receptacle adapter assembly.

Table 3-19 USB Type-C to *USB 3.1* Standard-A Adapter Assembly Wiring

USB Type-C Plug		**Wire (Optional – See Note 7)**		***USB 3.1* Standard-A Receptacle**	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	4	UTP_Dp	3	D+
A7	Dn1	5	UTP_Dn	2	D–
A2	TXp1	6	SDPp1	9	StdB_SSTX+
A3	TXn1	7	SDPn1	8	StdB_SSTX–
B11	RXp1	8	SDPp2	6	StdB_SSRX+
B10	RXn1	9	SDPn2	5	StdB_SSRX–
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug ***shall*** be connected to GND through a resistor ***Rd*** (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-28 for the functional description and value of ***Rd***.
2. This table assumes that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present, and the shields of the coaxial wires are connected to the ground pins.
3. Contacts B6 and B7 ***should not*** be present in the USB Type-C plug.
4. All VBUS pins ***shall*** be connected together within the USB Type-C plug. A 10 nF bypass capacitor is required for the VBUS pin in the USB Type-C plug end of the cable. The bypass capacitor ***should*** be placed as close as possible to the power supply pad. A bypass capacitor is not required for the VBUS pin in the Standard-A receptacle.
5. Shield and GND grounds ***shall*** be connected within the USB Type-C plug and ***USB 3.1*** Standard-A receptacle on both ends of the adapter assembly.
6. All USB Type-C plug pins that are not listed in this table ***shall*** be open (not connected).
7. This adapter assembly ***may*** or ***may not*** include a cable between the USB Type-C plug and ***USB 3.1*** Standard-A receptacle. Wire information provided here is when a cable is part of the assembly.

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3.6.2 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly

Figure 3-32 shows a USB Type-C to ***USB 2.0*** Micro-B receptacle adapter assembly.

Figure 3-32 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly

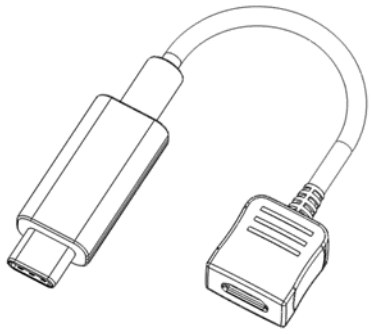


Table 3-20 defines the wire connections for the USB Type-C to ***USB 2.0*** Micro-B receptacle adapter assembly.

Table 3-20 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly Wiring

USB Type-C Plug		Wire (Optional – See Note 6)		*USB 2.0* Micro-B Receptacle	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
				4	ID
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug ***shall*** be connected to VBUS through a resistor ***Rp*** (56 kΩ ± 5%). See Section 4.5.3.2.2 and Table 4-27 for the functional description and value of ***Rp***.
2. Contacts B6 and B7 ***should not*** be present in the USB Type-C plug.
3. All VBUS pins ***shall*** be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins at the Micro-B receptacle end of this cable.
4. Shield and GND grounds ***shall*** be connected within the USB Type-C plug and ***USB 2.0*** Micro-B receptacle on both ends of the adapter assembly.
5. All USB Type-C plug pins that are not listed in this table ***shall*** be open (not connected).
6. This adapter assembly ***may*** or ***may not*** include a cable between the USB Type-C plug and ***USB 2.0*** Micro-B receptacle. Wire information provided here is when a cable is part of the assembly.

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3.7 Electrical Characteristics

This section defines the USB Type-C raw cable, connector, and cable assembly electrical requirements, including signal integrity, shielding effectiveness, and DC requirements. Section 3.11.1 defines additional requirements regarding functional signal definition, host/device discovery and configuration, and power delivery.

Unless otherwise specified, all measurements are made at a temperature of 15° to 35° C, a relative humidity of 25% to 85%, and an atmospheric pressure of 86 to 106 kPa and all S-parameters are normalized with an 85 Ω differential impedance.

3.7.1 Raw Cable (*Informative*)

Informative raw cable electrical performance targets are provided to help cable assembly manufacturers manage the procurement of raw cable. These targets are not part of the USB Type-C compliance requirements. The ***normative*** requirement is that the cable assembly meets the performance characteristics specified in Sections 3.7.2 and 3.7.5.3.

The differential characteristic impedance for shielded differential pairs is recommended to be 90 Ω ± 5 Ω. The single-ended characteristic impedance of coaxial wires is recommended to be 45 Ω ± 3 Ω. The impedance ***should*** be evaluated using a 200 ps (10%-90%) rise time; a faster rise time is not necessary for raw cable since it will make cable test fixture discontinuities more prominent.

3.7.1.1 Intra-Pair Skew (*Informative*)

The intra-pair skew for a differential pair is recommended to be less than 10 ps/m. It ***should*** be measured with a Time Domain Transmission (TDT) in a differential mode using a 200 ps (10%-90%) rise time with a crossing at 50% of the input voltage.

3.7.1.2 Differential Insertion Loss (*Informative*)

Cable loss depends on wire gauges, plating, and dielectric materials. Table 3-21 and Table 3-22 show examples of differential insertion losses.

Table 3-21 Differential Insertion Loss Examples for USB TX/RX with Twisted Pair Construction

Frequency	34AWG	32AWG	30AWG	28AWG
0.625 GHz	−1.8 dB/m	−1.4 dB/m	−1.2 dB/m	−1.0 dB/m
1.25 GHz	−2.5 dB/m	−2.0 dB/m	−1.7 dB/m	−1.4 dB/m
2.50 GHz	−3.7 dB/m	−2.9 dB/m	−2.5 dB/m	−2.1 dB/m
5.00 GHz	−5.5 dB/m	−4.5 dB/m	−3.9 dB/m	−3.1 dB/m
7.50 GHz	−7.0 dB/m	−5.9 dB/m	−5.0 dB/m	−4.1 dB/m
10.00 GHz	−8.4 dB/m	−7.2 dB/m	−6.1 dB/m	−4.8 dB/m
12.50 GHz	−9.5 dB/m	−8.2 dB/m	−7.3 dB/m	−5.5 dB/m
15.00 GHz	−11.0 dB/m	−9.5 dB/m	−8.7 dB/m	−6.5 dB/m

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Table 3-22 Differential Insertion Loss Examples for USB TX/RX with Coaxial Construction

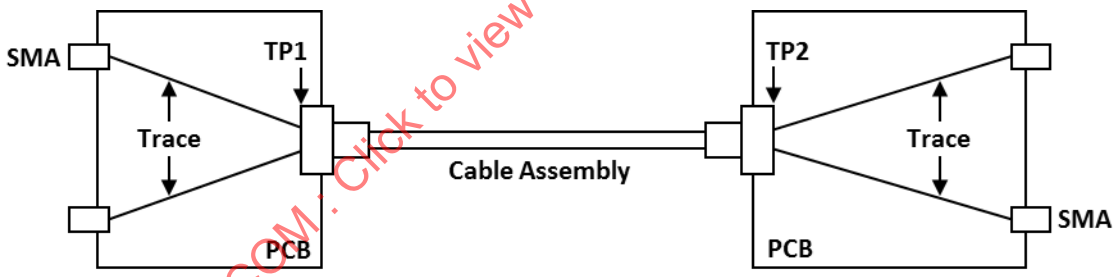
Frequency	34AWG	32AWG	30AWG	28AWG
0.625 GHz	−1.8 dB/m	−1.5 dB/m	−1.2 dB/m	−1.0 dB/m
1.25 GHz	−2.8 dB/m	−2.2 dB/m	−1.8 dB/m	−1.3 dB/m
2.50 GHz	−4.2 dB/m	−3.4 dB/m	−2.7 dB/m	−1.9 dB/m
5.00 GHz	−6.1 dB/m	−4.9 dB/m	−4.0 dB/m	−3.1 dB/m
7.50 GHz	−7.6 dB/m	−6.5 dB/m	−5.2 dB/m	−4.2 dB/m
10.0 GHz	−8.8 dB/m	−7.6 dB/m	−6.1 dB/m	−4.9 dB/m
12.5 GHz	−9.9 dB/m	−8.6 dB/m	−7.1 dB/m	−5.7 dB/m
15.0 GHz	−12.1 dB/m	−10.9 dB/m	−9.0 dB/m	−6.5 dB/m

3.7.2 USB Type-C to USB Type-C Passive Cable Assemblies

A USB Type-C to Type-C cable assembly ***shall*** be tested using a test fixture with the receptacle tongue fabricated in the test fixture. This is illustrated in Figure 3-33. The USB Type-C receptacles are not present in the test fixture. Hosts and devices ***should*** account for the additional signal degradation the receptacle introduces.

The requirements are for the entire signal path of the cable assembly mated with the fixture PCB tongues, not including lead-in PCB traces. As illustrated in Figure 3-33, the measurement is between TP1 (test point 1) and TP2 (test point 2). Refer to documentation located at Cables and Connectors page on the ***USB-IF*** website for a detailed description of a standardized test fixture.

Figure 3-33 Illustration of Test Points for a Mated Cable Assembly



The cable assembly requirements are divided into ***informative*** and ***normative*** requirements. The ***informative*** requirements are provided as design targets for cable assembly manufacturers. The ***normative*** requirements are the pass/failure criteria for cable assembly compliance.

3.7.2.1 Recommended TX/RX Passive Cable Assembly Characteristics (*USB 3.2* Gen2 and *USB4* Gen2)

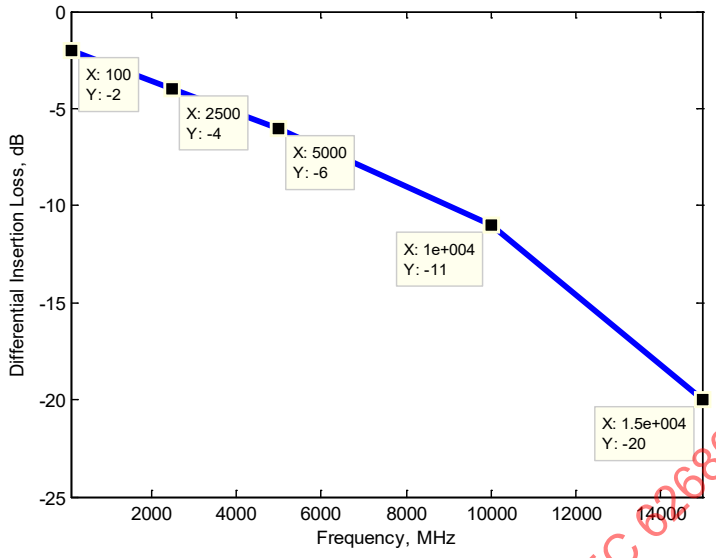
The recommended electrical characteristics defined in this section are ***informative*** design guidelines. Cable assemblies that do not meet these recommended electrical characteristics ***may*** still pass USB certification testing. Similarly, cable assemblies that meet these recommended electrical characteristics ***may*** or ***may not*** pass USB certification testing.

3.7.2.1.1 Differential Insertion Loss (*Informative – USB 3.2* Gen2 and *USB4* Gen2)

Figure 3-34 shows the differential insertion loss limit for a ***USB 3.2*** Gen2 or a ***USB4*** Gen2 Type-C cable assembly, which is defined by the following vertices: (100 MHz, −2 dB), (2.5 GHz, −4 dB), (5.0 GHz, −6 dB), (10 GHz, −11 dB) and (15 GHz, −20 dB).

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Figure 3-34 Recommended Differential Insertion Loss Requirement (*USB 3.2* Gen2 and *USB4* Gen2)

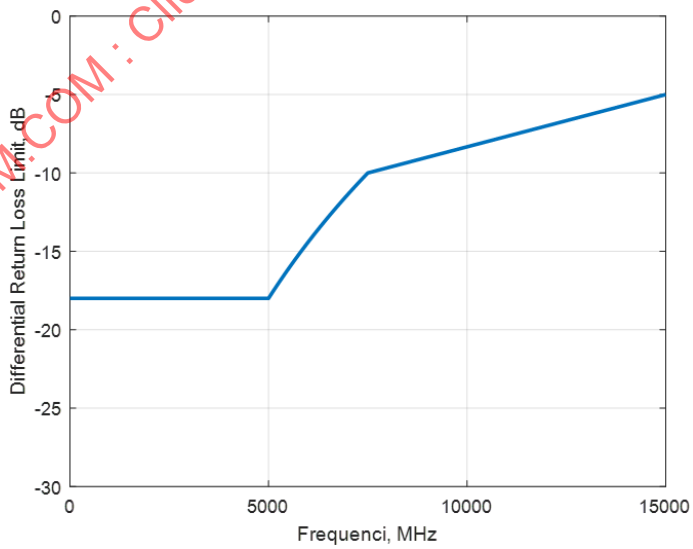


3.7.2.1.2 Differential Return Loss (*Informative – USB 3.2* Gen2 and *USB4* Gen2)

Figure 3-35 shows the differential return loss limit, which is defined by the following equation:

$$RL\ mask = \begin{cases} -18\ dB,\ f < 5\ Ghz \\ -18 + 45.43 \times \log_{10}\left(\frac{f}{5}\right)\ dB\ ,\ 5\ Ghz < f\ \leq 7.5\ Ghz \\ -15 + \frac{2}{3} \times f\ dB,\ 7.5\ Ghz < f \leq 15\ Ghz \end{cases}$$

Figure 3-35 Recommended Differential Return Loss Requirement

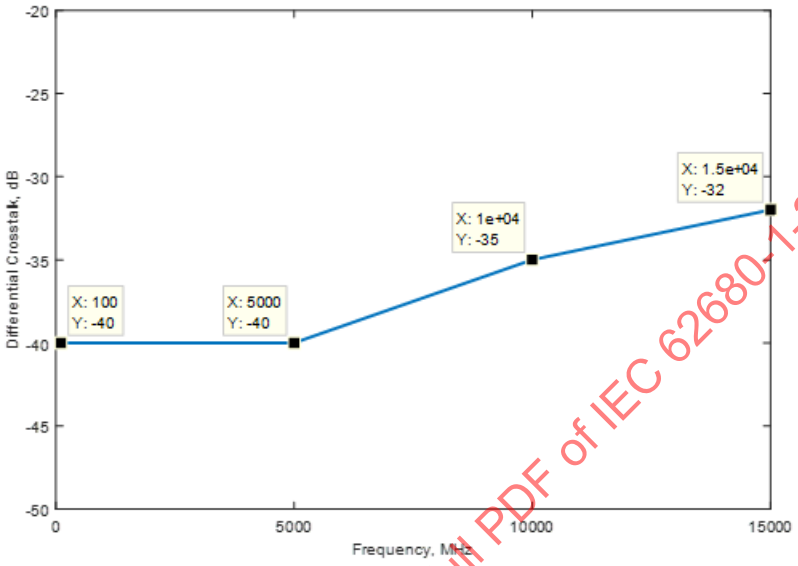


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3.7.2.1.3 Differential Near-End and Far-End Crosstalk between TX/RX Pairs (*Informative – USB 3.2* Gen2 and *USB4* Gen2)

Both the near-end crosstalk (DDNEXT) and far-end crosstalk (DDFEXT) are specified, as shown in Figure 3-36. The DDNEXT/DDFEXT limits are defined by the following vertices: (100 MHz, −40 dB), (5 GHz, −40 dB), (10 GHz, −35 dB), and (15 GHz, −32 dB).

Figure 3-36 Recommended Differential Crosstalk Requirement



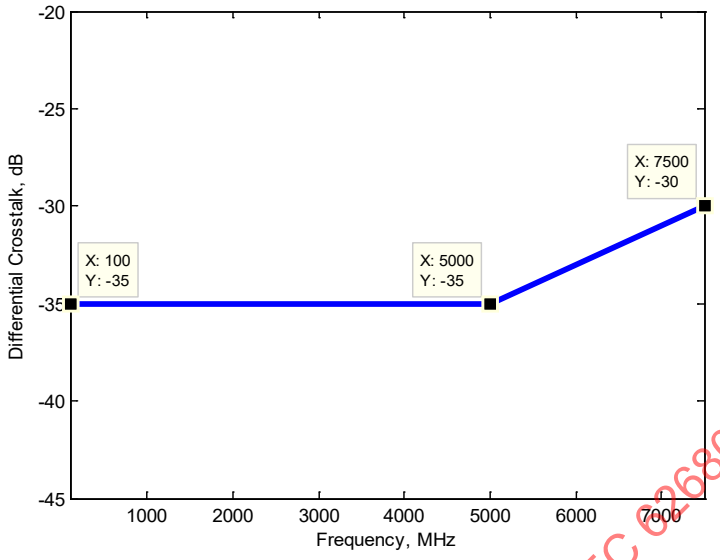
3.7.2.1.4 Differential Crosstalk between USB D+/D− and TX/RX Pairs (*Informative – USB 3.2* Gen2 and *USB4* Gen2)

The differential near-end and far-end crosstalk between the USB D+/D− pair and the TX/RX pairs ***should*** be managed not to exceed the limits shown in Figure 3-37. The USB D+/D− pair and the TX/RX pairs ***should*** be considered in the context of both an aggressor and a victim. It ***should*** also be considered that the D+/D− pair maximum frequency for similar tests is

1.2 GHz (see Table 3-31), but in this case the crosstalk on the D+/D− pair is extended to 7.5 GHz. The limits are defined by the following points: (100 MHz, −35 dB), (5 GHz, −35 dB), and (7.5 GHz, −30 dB).

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Figure 3-37 Recommended Differential Near-End and Far-End Crosstalk Requirement between USB D+/D– Pair and TX/RX Pair



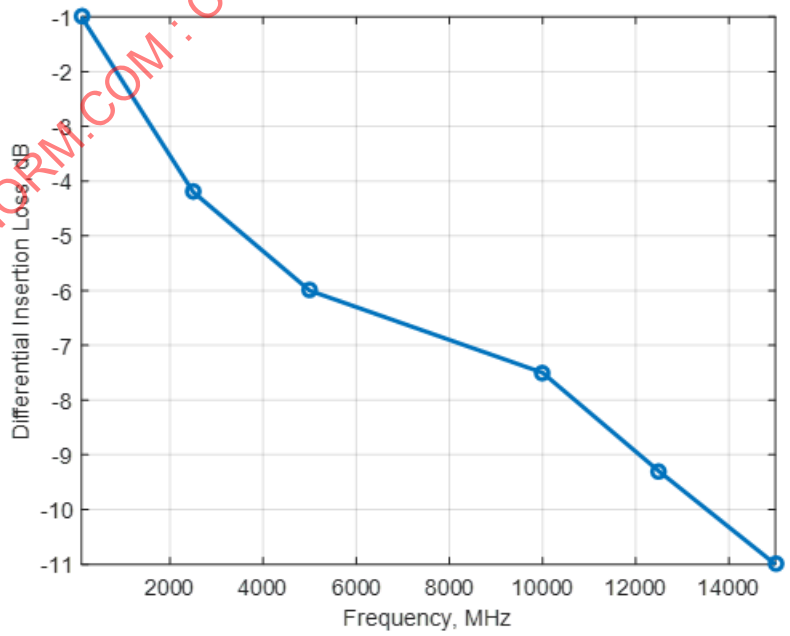
3.7.2.2 Recommended TX/RX Passive Cable Assembly Characteristics (*USB4* Gen3/Gen4)

Note: While the recommended characteristics in this section are defined in terms of ***USB4*** Gen3, these characteristics apply also to ***USB4*** Gen4 passive cable assemblies as these are electrically equivalent to ***USB4*** Gen3 passive cable assemblies.

3.7.2.2.1 Differential Insertion Loss (*Informative – USB4* Gen3/Gen4)

Figure 3-38 shows the recommended differential insertion loss limit for a ***USB4*** Gen3 Type-C cable assembly, which is defined by the following vertices: (100 MHz, −1 dB), (2.5 GHz, −4.2 dB), (5.0 GHz, −6 dB), (10 GHz, −7.5 dB), (12 GHz, −9.3 dB), and (15 GHz, −11 dB).

Figure 3-38 Recommended Differential Insertion Loss Requirement (*USB4* Gen3/Gen4)



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3.7.2.2.2 Differential Return Loss (*Informative – USB4* Gen3/Gen4)

The ***informative*** differential return loss mask is identical in Section 3.7.2.1.2.

3.7.2.2.3 Differential Near-End and Far-End Crosstalk between TX/RX Pairs (*Informative – USB4* Gen3/Gen4)

The recommended near-end crosstalk (DDNEXT) and far-end crosstalk (DDFEXT) are defined in Section 3.7.2.1.3. To minimize crosstalk, it is important to optimize the paddle card and wire termination designs inside the cable plug.

3.7.2.2.4 Differential Crosstalk between USB D+/D– and TX/RX Pairs (*Informative – USB4* Gen3/Gen4)

The ***informative*** near-end and far-end crosstalk between the USB D+/D– pair and the TX/RX pairs are the same as in Section 3.7.2.1.4.

3.7.2.3 *Normative* TX/RX Passive Cable Assembly Requirements for *USB 3.2* Gen2 and *USB4* Gen2

The integrated parameters are used for cable assembly compliance (except for insertion loss and differential-to-common-mode conversion) to avoid potential rejection of a functioning cable assembly that ***may*** fail the traditional S-parameters spec at a few frequencies.

3.7.2.3.1 Insertion Loss Fit at Nyquist Frequencies (*Normative – USB 3.2* Gen2 and *USB4* Gen2)

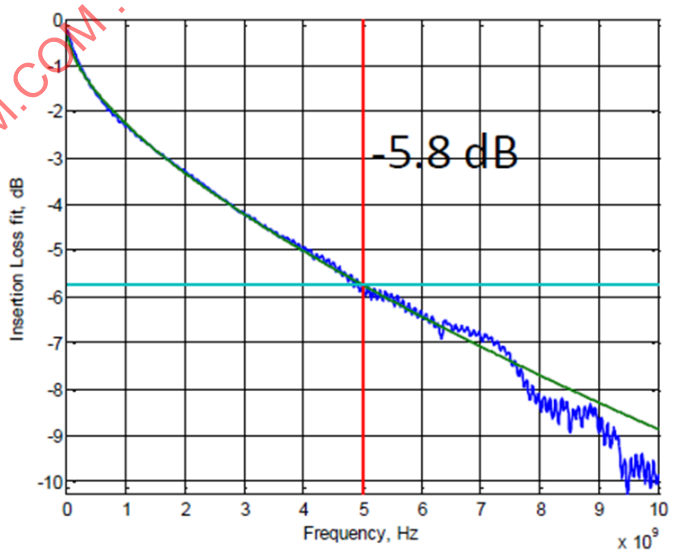
The insertion loss fit at Nyquist frequency measures the attenuation of the cable assembly. To obtain the insertion loss fit at Nyquist frequency, the measured cable assembly differential insertion loss is fitted with a smooth function. A standard fitting algorithm and tool ***shall*** be used to extract the insertion loss fit at Nyquist frequencies. The fitting equation is defined by the following equation:

$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3}$$

where f is the frequency and a, b, c, and d are the fitting coefficients.

Figure 3-39 illustrates an example of a measured cable assembly insertion loss fitted with a smooth function; the insertion loss fit at the Nyquist frequency of SuperSpeed USB Gen2 (5.0 GHz) is –5.8 dB.

Figure 3-39 Illustration of Insertion Loss Fit at Nyquist Frequency



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The insertion loss fit at Nyquist frequency (ILfitatNq) ***shall*** meet the following requirements:

- ≥ −4 dB at 2.5 GHz,
- ≥ −6 dB at 5 GHz, and
- ≥ −11 dB at 10 GHz.

2.5 GHz, 5.0 GHz and 10 GHz are the Nyquist frequencies for SuperSpeed USB Gen1, SuperSpeed USB Gen2, and ***USB4*** Gen3 data rate, respectively.

3.7.2.3.2 Integrated Multi-Reflection (*Normative – USB 3.2* Gen2 and *USB4* Gen2)

The insertion loss deviation, ILD, is defined as:

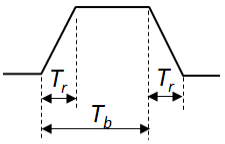
$$ILD(f) = IL(f) - ILfit(f)$$

It measures the ripple of the insertion loss, caused by multiple reflections inside the cable assembly (mated with the fixture). The integration of *ILD(f)* is called the integrated multi-reflection (IMR):

$$IMR = dB\left(\sqrt{\frac{\int_0^{fmax}|ILD(f)|^2|Vin(f)|^2df}{\int_0^{fmax}|Vin(f)|^2df}}\right)$$

where f_{max} = 12.5 GHz and *Vin(f)* is the input trapezoidal pulse spectrum, defined in Figure 3-40.

Figure 3-40 Input Pulse Spectrum



$$|V_{in}(f)| = \left|\frac{\sin(\pi f T_r)}{\pi f T_r} \cdot \frac{\sin(\pi f T_b)}{\pi f T_b}\right|$$

T_b=Unit interval=100 ps
T_r=0 to 100% rise time=0.4T_b

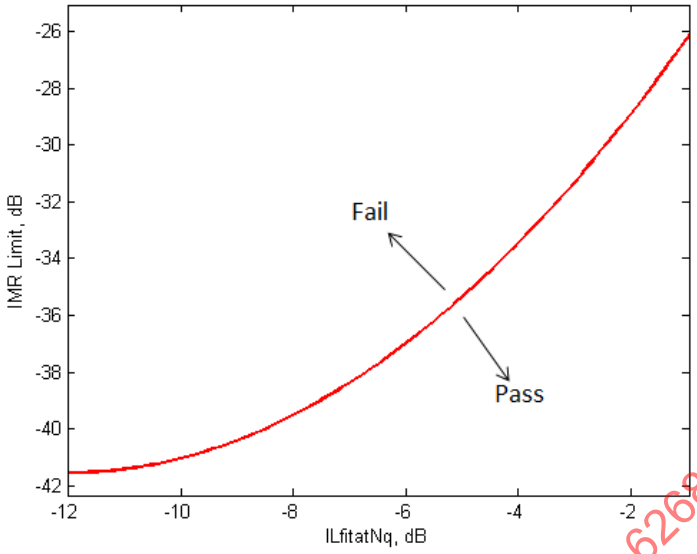
IMR has dependency on ILfitatNq. More IMR ***may*** be tolerated when ILfitatNq decreases. The IMR limit is specified as a function of ILfitatNq:

$$IMR \leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 23.392$$

This is plotted in Figure 3-41.

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Figure 3-41 IMR Limit as Function of ILfitatNq



3.7.2.3.3 Integrated Crosstalk between TX/RX Pairs (*Normative – USB 3.2* Gen2 and *USB4* Gen2)

The integrated crosstalk between all TX/RX pairs is calculated with the following equations:

$$INEXT = dB\left(\sqrt{\frac{\int_0^{fmax}(|Vin(f)|^2(|NEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2\,|NEXTd(f)|^2)df}{\int_0^{fmax}|Vin(f)|^2 df}}\right)$$

$$IFEXT = dB\left(\sqrt{\frac{\int_0^{fmax}(|Vin(f)|^2(|FEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2\,|FEXTd(f)|^2)df}{\int_0^{fmax}|Vin(f)|^2 df}}\right)$$

where *NEXT(f)*, *FEXT(f)*, and *C2D(f)* are the measured near-end and far-end crosstalk between TX/RX pairs, and the common-mode-to-differential conversion, respectively. The factor of 0.1252 accounts for the assumption that the common mode amplitude is 12.5% of the differential amplitude. *NEXTd(f)* and *FEXTd(f)* are, respectively, the near-end and far-end crosstalk from the D+/D− pair to TX/RX pairs. *Vdd(f)* is the input pulse spectrum evaluated using the equation in Figure 3-40 with Tb=2.08 ns.

The integration ***shall*** be done for each NEXT and FEXT between all differential pairs. The largest values of INEXT and IFEXT ***shall*** meet the following requirements:

- INEXT ≤ −40 dB to 12.5GHz, for TX1 to RX1, TX2 to RX2, TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2,
- IFEXT ≤ −40 dB to 12.5GHz, for TX1 to RX1, TX2 to RX2, TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2.

The port-to-port crosstalk (TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2) is specified to support the usages in which all the four pairs transmit or receive signals simultaneously, for example in SuperSpeed USB dual-lane operation.

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3.7.2.3.4 Integrated Crosstalk from TX/RX Pairs to USB D+/D– (*Normative – USB 3.2* Gen2 and *USB4* Gen2)

Crosstalk from the TX/RX pairs to ***USB 2.0*** D+/D– ***shall*** be controlled to ensure the robustness of the ***USB 2.0*** link. Since USB Type-C to Type-C Full-Featured cable assemblies ***may*** support the usage of ***USB 3.2***, ***USB4*** or an ***Alternate Mode*** (e.g., ***DisplayPort***), the crosstalk from the four high speed differential pairs to D+/D– ***may*** be from near-end crosstalk, far-end crosstalk, or a combination of the two. The integrated crosstalk to D+/D– is calculated with the following equations:

$$\text{IDDXT_1NEXT + FEXT } = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2(|NEXT1(f)|^2 + |FEXT(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2df}}\right)$$

where:

NEXT = Near-end crosstalk from TX pair to D+/D–,

FEXT = Far-end crosstalk from RX pair to D+/D–, and

f_{max} = 1.2 GHz.

$$\text{IDDXT_2NEXT } = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2(|NEXT1(f)|^2 + |NEXT2(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2df}}\right)$$

where:

NEXT1 = Near-end crosstalk from TX pair to D+/D–,

NEXT2 = Near-end crosstalk from RX (the RX functioning in TX mode) pair to D+/D–, and

f_{max} = 1.2 GHz.

The integration ***shall*** be done for NEXT + FEXT and 2NEXT on D+/D– from the two differential pairs located at A2, A3, B10 and B11 (see Figure 2-2) and for NEXT + FEXT and 2NEXT on D+/D– from the two differential pairs located at B2, B3 A10 and A11 (see Figure 2-2). Measurements are made in two sets to minimize the number of ports required for each measurement. The integrated differential crosstalk on D+/D– ***shall*** meet the following requirements:

- IDDXT_1NEXT + FEXT ≤ –34.5 dB, and
- IDDXT_2NEXT ≤ –33 dB.

3.7.2.3.5 Integrated Return Loss (*Normative – USB 3.2* Gen2 and *USB4* Gen2)

The integrated return loss (IRL) manages the reflection between the cable assembly and the rest of the system (host and device). It is defined as:

$$IRL = dB\left(\sqrt{\frac{\int_0^{fmax}|Vin(f)|^2|SDD21(f)|^2(|SDD11(f)|^2 + |SDD22(f)|^2)df}{\int_0^{fmax}|Vin(f)|^2df}}\right)$$

where *SDD21(f)* is the measured cable assembly differential insertion loss, *SDD11(f)* and *SDD22(f)* are the measured cable assembly return losses on the left and right sides, respectively, of a differential pair.

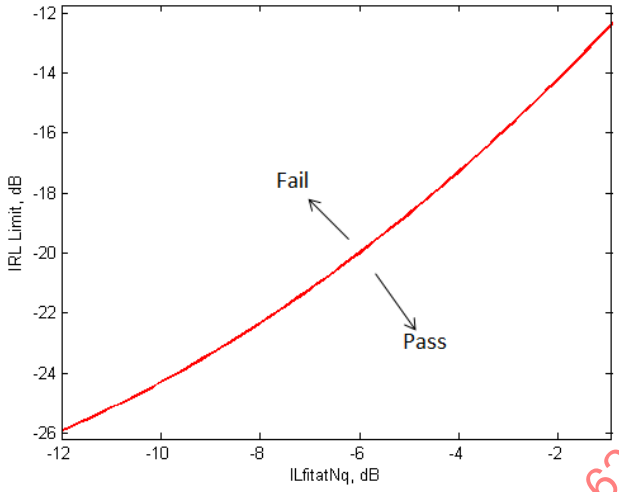
The IRL also has a strong dependency on ILfitatNq, and its limit is specified as a function of ILfitatNq:

$$IRL \leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 10.784.$$

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It is shown in Figure 3-42.

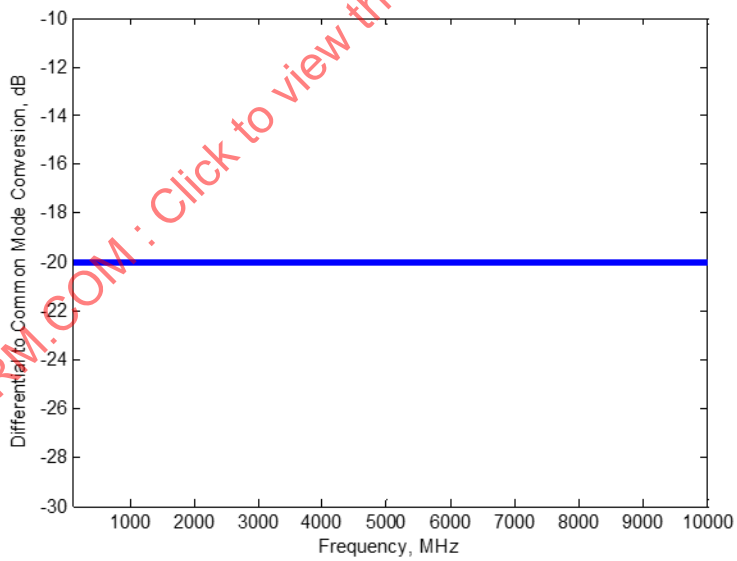
Figure 3-42 IRL Limit as Function of ILfitatNq



3.7.2.3.6 Differential-to-Common-Mode Conversion (*Normative – USB 3.2* Gen2 and *USB4* Gen2)

The differential-to-common-mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Figure 3-43 illustrates the differential-to-common mode conversion (SCD12/SCD21) requirement. A mated cable assembly passes if its SCD12/SCD21 is less than or equal to −20 dB from 100 MHz to 10 GHz.

Figure 3-43 Differential-to-Common Mode Conversion Requirement



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3.7.2.4 *Normative* TX/RX Passive Cable Assembly Requirements for *USB 3.2* Gen1 and *USB4* Gen2

3.7.2.4.1 Insertion Loss Fit at Nyquist Frequencies (*Normative – USB 3.2* Gen1 and *USB4* Gen2)

The integrated S-parameter requirements for ***USB 3.2*** Gen1 and ***USB4*** Gen2 follow the same methodology as defined in Section 3.7.2.3. There are parameter adjustments made to suit the ***USB4*** Gen2 data rate. Unless otherwise specified, the following parameters ***shall*** be used to calculate insertion loss fit and integrated parameters:

- T_b, the unit interval, is set to 100 ps, reflecting the ***USB4*** Gen2 data rate.
- T_r, the rise time, remains at 0.4 * T_b.
- f_{max}, the maximum frequency over which the integration or fitting is performed is increased to 12.5 GHz.
- The fitting equation is defined by the following equation:

$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3}$$

where *f* is the frequency and *a*, *b*, *c*, and *d* are the fitting coefficients.

The insertion loss fit at Nyquist frequency (ILfitatNq) ***shall*** meet the following requirements:

- ≥ −7.0 dB at 2.5 GHz, and
- > −11.5 dB at 5 GHz.

3.7.2.4.2 Integrated Multi-Reflection (*Normative – USB 3.2* Gen1 and *USB4* Gen2)

The insertion loss deviation, ILD, is defined as:

$$ILD(f) = IL(f) - ILfit(f)$$

It measures the ripple of the insertion loss, caused by multiple reflections inside the cable assembly (mated with the fixture). The integration of ILD(f) is called the integrated multi- reflection (IMR):

$$IMR = dB\left(\sqrt{\frac{\int_0^{f_{max}} |ILD(f)|^2 |Vin(f)|^2 df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

where f_{max} = 12.5 GHz and *Vin(f)* is the input trapezoidal pulse spectrum.

For ***USB 3.2*** Gen1 and ***USB4*** Gen2 cable assemblies, IMR limit is specified as:

$$IMR \leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 24.792$$

3.7.2.4.3 Integrated Crosstalk between TX/RX Pairs (*Normative – USB 3.2* Gen1 and *USB4* Gen2)

The integrated crosstalk between all TX/RX pairs is calculated with the following equations:

$$INEXT = dB\left(\sqrt{\frac{\int_0^{f_{max}} (|Vin(f)|^2 (|NEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2 \, |NEXTd(f)|^2) df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

$$IFEXT = dB\left(\sqrt{\frac{\int_0^{f_{max}} (|Vin(f)|^2 (|FEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2 \, |FEXTd(f)|^2) df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

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where *NEXT(f)*, *FEXT(f)*, and *C2D(f)* are the measured near-end and far-end crosstalk between TX/RX pairs, and the common-mode-to-differential conversion, respectively. The factor of 0.1252 accounts for the assumption that the common mode amplitude is 12.5% of the differential amplitude. *NEXTd(f)* and *FEXTd(f)* are, respectively, the near-end and far-end crosstalk from the D+/D− pair to TX/RX pairs. *Vdd(f)* is the input pulse spectrum with Tb=2.08 ns.

The largest values of INEXT and IFEXT ***shall*** meet the following requirements:

- INEXT ≤ −40 dB to 12.5GHz, for TX1 to RX1, TX2 to RX2, TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2,
- IFEXT ≤ −40 dB to 12.5GHz, for TX1 to RX1, TX2 to RX2, TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2.

The port-to-port crosstalk (TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2) is specified to support the usages in which all the four high speed pairs transmit or receive signals simultaneously (e.g., USB dual-lane operation).

3.7.2.4.4 Integrated Crosstalk from TX/RX Pairs to USB D+/D− (*Normative – USB 3.2* Gen1 and *USB4* Gen2)

Crosstalk from the TX/RX pairs to ***USB 2.0*** D+/D− ***shall*** be controlled to ensure the robustness of the ***USB 2.0*** link. Since USB Type-C to Type-C Full-Featured cable assemblies ***may*** support the usage of ***USB 3.2***, ***USB4*** or an ***Alternate Mode*** (e.g., ***DisplayPort***), the crosstalk from the four high speed differential pairs to D+/D− ***may*** be from near-end crosstalk, far-end crosstalk, or a combination of the two. The integrated crosstalk to D+/D− is calculated with the following equations:

$$\text{IDDXT_1NEXT + FEXT } = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2(|NEXT1(f)|^2 + |FEXT(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2df}}\right)$$

where:

NEXT = Near-end crosstalk from TX pair to D+/D−,

FEXT = Far-end crosstalk from RX pair to D+/D−, and

f_{max} = 1.2 GHz.

$$\text{IDDXT}_{\text{2NEXT}} = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2(|NEXT1(f)|^2 + |NEXT2(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2df}}\right)$$

where:

NEXT1 = Near-end crosstalk from TX pair to D+/D−,

NEXT2 = Near-end crosstalk from RX (the RX functioning in TX mode) pair to D+/D−, and

f_{max} = 1.2 GHz.

The integration ***shall*** be done for NEXT + FEXT and 2NEXT on D+/D− from the two differential pairs located at A2, A3, B10 and B11 (see Figure 2-2) and for NEXT + FEXT and 2NEXT on D+/D− from the two differential pairs located at B2, B3 A10 and A11 (see Figure 2-2). Measurements are made in two sets to minimize the number of ports required for each measurement.

The integrated differential crosstalk on D+/D− ***shall*** meet the following requirements:

- IDDXT_1NEXT + FEXT ≤ −34.5 dB,

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- IDDXT_2NEXT ≤ −33 dB.

3.7.2.4.5 Integrated Return Loss (*Normative – USB 3.2* Gen1 and *USB4* Gen2)

The integrated return loss (IRL) manages the reflection between the cable assembly and the rest of the system (host and device). It is defined as:

$$IRL = dB\left(\sqrt{\frac{\int_0^{f_{max}} |Vin(f)|^2 |SDD21(f)|^2 (|SDD11(f)|^2 + |SDD22(f)|^2) df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

where *SDD21(f)* is the measured cable assembly differential insertion loss, *SDD11(f)* and *SDD22(f)* are the measured cable assembly return losses on the left and right sides, respectively, of a differential pair.

For ***USB 3.2*** Gen 1 and ***USB4*** Gen 2 cable assemblies, IRL limit is specified as:

$$IRL \leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 9.784$$

3.7.2.4.6 Differential-to-Common-Mode Conversion (*Normative – USB 3.2* Gen1 and *USB4* Gen2)

The differential-to-common-mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. A mated cable assembly passes if its SCD12/SCD21 is less than or equal to −17 dB from 100 MHz to 10 GHz.

3.7.2.5 *Normative* TX/RX Passive Cable Assembly Requirements for *USB4* Gen3/Gen4

Note: While the ***normative*** requirements in this section are defined in terms of ***USB4*** Gen3, these requirements apply also to ***USB4*** Gen4 passive cable assemblies as these are electrically equivalent to ***USB4*** Gen3 passive cable assemblies.

The integrated S-parameter requirements for ***USB4*** Gen3 follow the same methodology as defined in Section 3.7.2.3. There are parameter adjustments made to suit the ***USB4*** Gen3 data rate. Unless otherwise specified, the following parameters ***shall*** be used to calculate insertion loss fit and integrated parameters:

- T_b, the unit interval, is set to 50 ps, reflecting the ***USB4*** Gen3 data rate.
- T_r, the rise time, remains at 0.4 * T_b.
- f_{max}, the maximum frequency over which the integration or fitting is performed is increased to 20 GHz.
- An f-square term is added to the insertion loss fit equation to improve fitting quality:

$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3} + e * \sqrt{f^4}$$

USB4 Gen3 introduces a system-level COM (Channel Operating Margin) specification for the cable assembly. The details are defined in Section 3.7.2.5.7.

3.7.2.5.1 Insertion Loss Fit at Nyquist Frequencies (*Normative – USB4* Gen3/Gen4)

The insertion loss fit at Nyquist frequency (ILfitatNq) ***shall*** meet the following requirements:

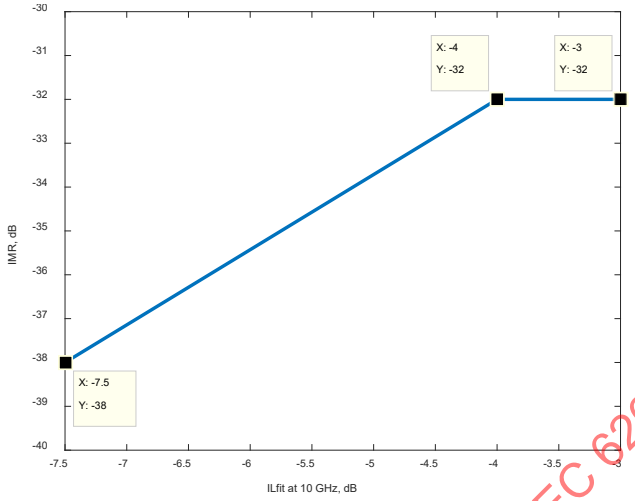
- ≥ −1 dB at 100 MHz,
- ≥ −4.2 dB at 2.5 GHz,
- ≥ −6 dB at 5 GHz,
- ≥ −7.5 dB at 10 GHz,
- ≥ −9.3 dB at 12.5 GHz, and
- ≥ −11 dB at 15 GHz.

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3.7.2.5.2 Integrated Multi-Reflection (*Normative – USB4* Gen3/Gen4)

The IMR limit is plotted in Figure 3-44.

Figure 3-44 IMR Limit as Function of ILfit at 10 GHz (*USB4* Gen3/Gen4)



3.7.2.5.3 Integrated Crosstalk between TX/RX Pairs (*Normative – USB4* Gen3/Gen4)

The integrated crosstalk within a port for TX1 to RX1 and TX2 to RX2 is recommended to meet the following ***informative*** requirements:

- INEXT ≤ −43 dB and
- IFEXT ≤ −43 dB.

The recommended ***informative*** requirement for the integrated port-to-port crosstalk for TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2) are defined as:

- INEXT_p2p ≤ −50 dB and
- IFEXT_p2p ≤ −50 dB.

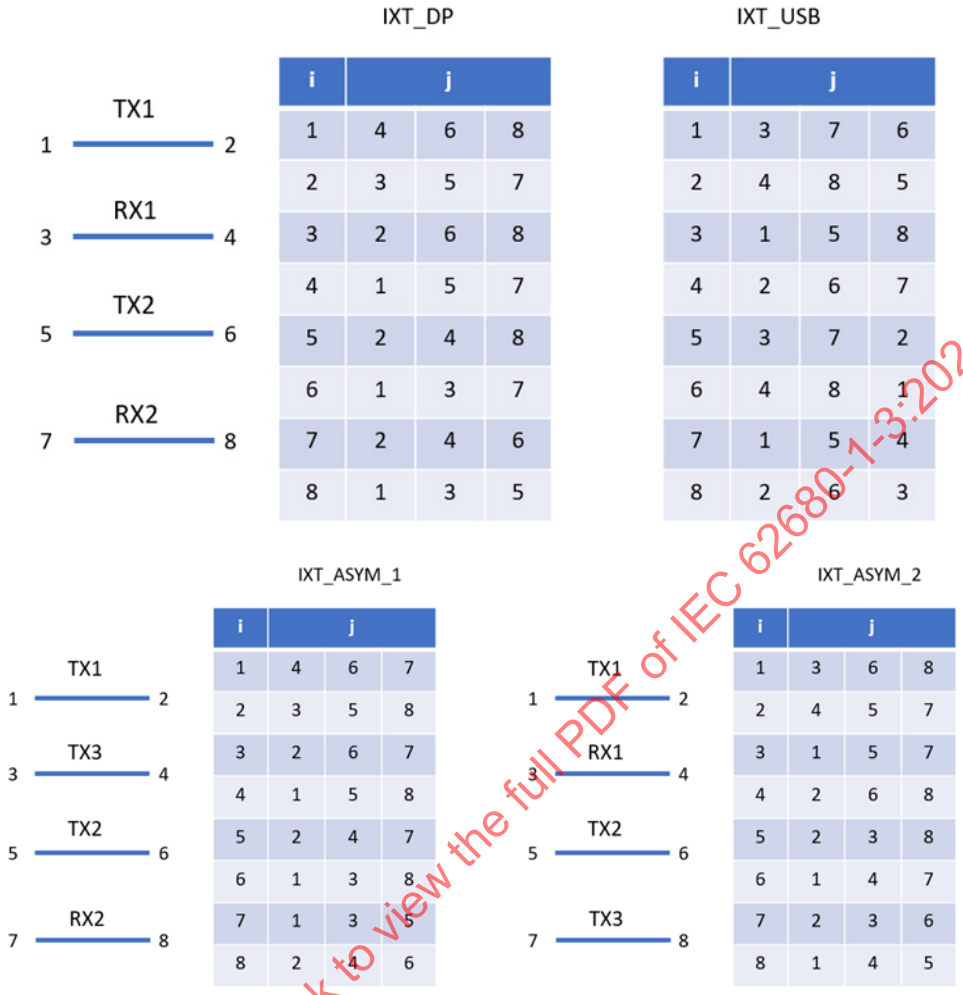
The total crosstalk is defined for the ***DP Alternate Mode***, ***USB4*** symmetric, and ***USB4*** asymmetric operation. In ***DP Alternate Mode***, all crosstalk is FEXT, while in ***USB4*** symmetric and asymmetric operation both FEXT and NEXT exist. The total crosstalk is defined in the equation below:

$$\text{IXTi_DP or IXTi_USB or IXTi_ASYM} = dB\left(\sqrt{\frac{\int_0^{f_{max}} |Vin(f)|^2 \sum_j |SDDij|^2 df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

where the victims i = 1 to 8 and the aggressors j are defined in Figure 3-45.

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Figure 3-45 Definition of Port, Victim, and Aggressor



i	j		
1	4	6	8
2	3	5	7
3	2	6	8
4	1	5	7
5	2	4	8
6	1	3	7
7	2	4	6
8	1	3	5

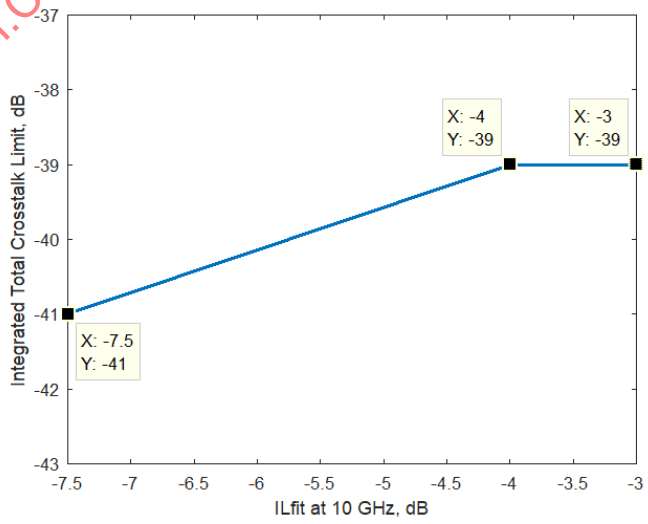
i	j		
1	3	7	6
2	4	8	5
3	1	5	8
4	2	6	7
5	3	7	2
6	4	8	1
7	1	5	4
8	2	6	3

i	j		
1	4	6	7
2	3	5	8
3	2	6	7
4	1	5	8
5	2	4	7
6	1	3	8
7	1	3	5
8	2	4	6

i	j		
1	3	6	8
2	4	5	7
3	1	5	7
4	2	6	8
5	2	3	8
6	1	4	7
7	2	3	6
8	1	4	5

The total crosstalk for the ***DP Alternate Mode***, ***USB4*** symmetric, and ***USB4*** asymmetric operation ***shall*** be controlled. Its ***normative*** limit is defined in Figure 3-46.

Figure 3-46 IXT_DP and IXT_USB Limit as Function of ILfit at 10 GHz (*USB4* Gen3/Gen4)



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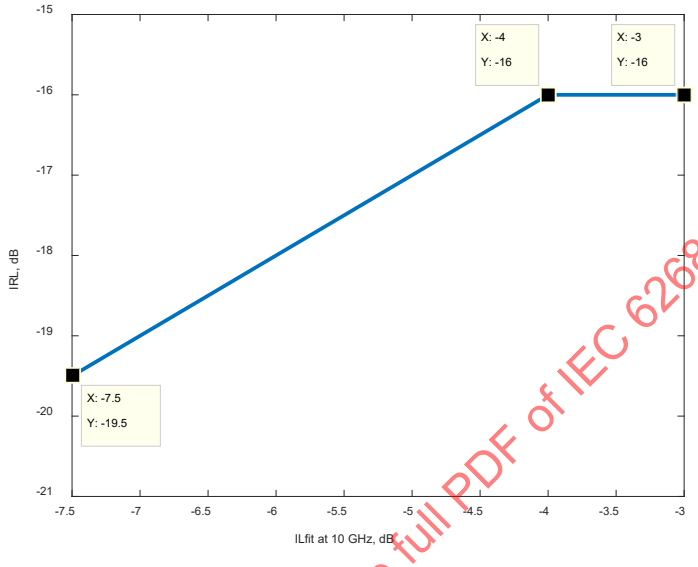
3.7.2.5.4 Integrated Crosstalk from TX/RX Pairs to USB D+/D– (*Normative – USB4* Gen3/Gen4)

The requirements for the integrated crosstalk from the TX/RX pairs to ***USB 2.0*** D+/D– are defined in Section 3.7.2.3.4.

3.7.2.5.5 Integrated Return Loss (*Normative – USB4* Gen3/Gen4)

The IRL limit is shown in Figure 3-47.

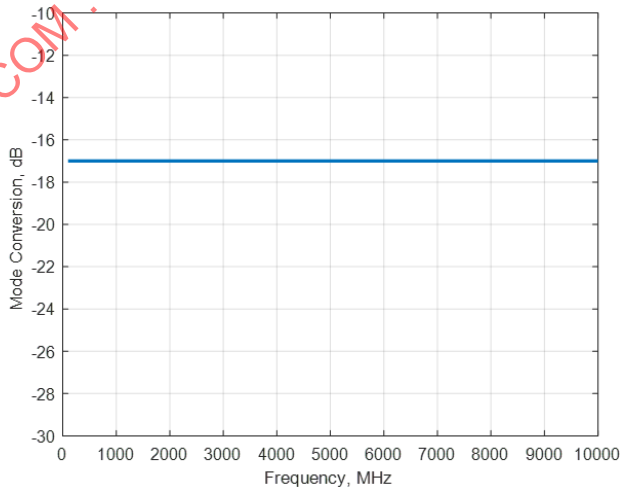
Figure 3-47 IRL Limit as Function of ILfit at 10 GHz (*USB4* Gen3/Gen4)



3.7.2.5.6 Differential-to-Common-Mode Conversion (*Normative – USB4* Gen3/Gen4)

Figure 3-48 illustrates the differential-to-common mode conversion (SCD12/SCD21) requirement. A mated cable assembly passes if its SCD12/SCD21 is less than or equal to −17 dB from 100 MHz to 10 GHz. Note that −17 dB is the worst-case limit; no ***USB4*** Gen3/Gen4 Type-C cable is allowed to exceed it.

Figure 3-48 Differential-to-Common Mode Conversion Requirement (*USB4* Gen3/Gen4)



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3.7.2.5.7 COM Requirement (*Normative – USB4* Gen3/Gen4)

Channel Operating Margin (COM) is a figure of merit to measure the channel electrical quality. The technical detail of COM may be found in IEEE Std 802.3bj™-2014 Clause 93a.

COM is essentially the channel signal-to-noise ratio:

$$COM = 20log10(\frac{A}{N})$$

where A is the signal amplitude and N is the combined noise at BER (bit-error-ratio), which includes the noise sources from ISI (inter-symbol-interference), crosstalk, transmitter jitter, etc.

To calculate COM, reference hosts/devices, which represent the worst-case hosts/devices, ***shall*** be defined and the reference TX and RX ***shall*** be used. As illustrated in Figure 3-49, the measured cable assembly S-parameters are cascaded with the reference host and reference device models to form the complete channel; the TX and RX die-loading and equalizers are then applied to the channel to calculate COM.

Figure 3-49 Cable Assembly in System

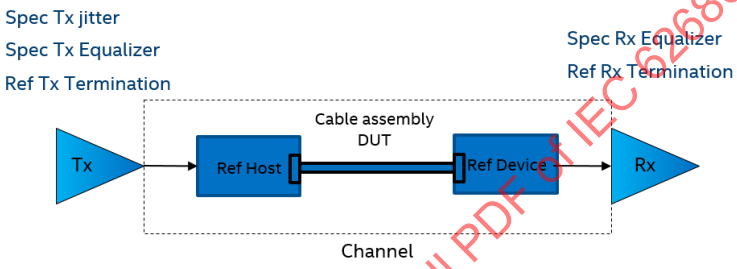


Table 3-23 defines the key parameters in the COM configuration file. It uses the standard COM notations. Note that all the TX and RX equalization settings follow the ***USB4*** specification.

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Table 3-23 Key Parameters in COM Configuration File

Parameter	Setting	Unit	Information
f_b	20	GBd	***USB4*** Gen 3 data rate
C_d	[0 0]	nF	TX and RX capacitive loading. It is set to zeros as the die-loading is treated as part of the channel
R_d	[42.5 42.5]	Ohm	TX and RX termination resistance
ffe_preset	Table 3-4 of ***USB4*** Specification		TX equalization presets
g_DC	[–9:1:0]	dB	CTLE DC gain
f_p1	5	GHz	CTLE pole 1
f_p2	10	GHz	CTLE pole 2
f_z	3.55	GHz	CTLE zero
A_v	0.4	V	Signal swing
A_fe	0.4	V	FEXT aggressor swing
A_ne	0.6	V	NEXT aggressor swing
N_b	1		Number of DFE tap
b_max(1)	0.7		DFE bound, ratio to cursor
Sigma_RJ	0.01	UI	TX random jitter, rms.
A_DD	0.085	UI	TX deterministic jitter, mean-to-peak
DER_0	1e-12		Target raw bit-error-rate
eta_0	3.3e-8	V^2/GHz	One sided noise spectral density
SNR_TX	40	dB	TX signal to noise ratio
COM Threshold	3	dB	Pass/fail criterion

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To support the calculation of the cable assembly COM, the following collaterals is provided and may be obtained from ***USB-IF*** website:

- Reference host/device S-parameter models,
- Reference TX and RX die-loading S-parameter models,
- COM configuration file, and
- Tool to compute COM.

3.7.2.6 Low-Speed Signal Requirements (*Normative*)

This section specifies the electrical requirements for CC and SBU wires and the coupling among CC, USB D+/D–, VBUS and SBU.

The CC and SBU wires ***may*** be unshielded or shielded and ***shall*** have the properties specified in Table 3-24.

Table 3-24 Electrical Requirements for CC and SBU Wires

Name	Description	Min	Max	Units
zCable_CC	Cable characteristic impedance on the CC wire	32	93	Ω
rCable_CC	Cable DC resistance on the CC wire		15	Ω
tCableDelay_CC	Cable propagation delay on the CC wire		26	ns
cCablePlug_CC	Capacitance for each cable plug on the CC wire		25	pF
zCable_SBU	Cable characteristic impedance on the SBU wires	32	53	Ω
tCableDelay_SBU	Cable propagation delay on the SBU wires		26	ns
rCable_SBU	DC resistance of SBU wires in the cable		5	Ω
SBU SE Insertion Loss	Cable SBU single-ended insertion loss		2.0 @ 0.5 MHz 4.0 @ 1 MHz 9.0 @ 10 MHz 10.7 @ 25 MHz 11.9 @ 50 MHz 13.0 @ 100 MHz	dB

Coupling or crosstalk, both near-end and far-end, among the low speed signals ***shall*** be controlled. Table 3-25 shows the matrix of couplings specified.

Table 3-25 Coupling Matrix for Low Speed Signals

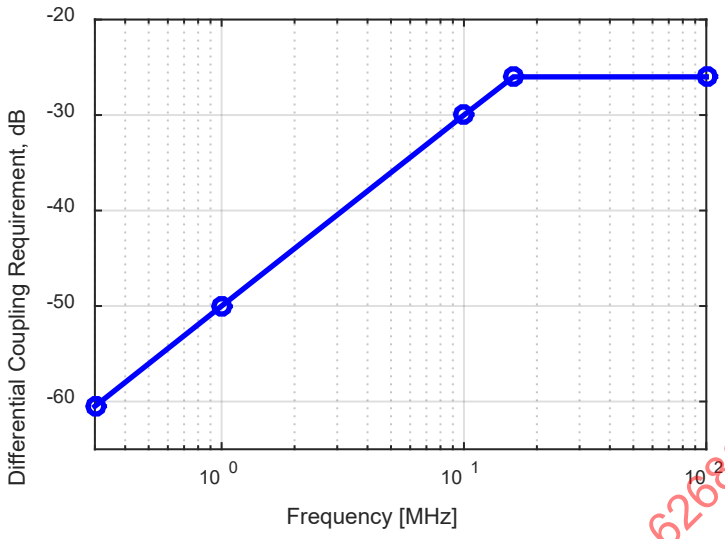
Coupling Matrix	D– (SE)	D+/D– (DF)	VBUS	SBU_B/SBU_A (SE)
CC	FF, CT	FF, CT	FF, CT, CTVPD	FF
D+/D– (DF)	***N/A***	***N/A***	FF, CT	FF
SBU_A/SBU_B	***N/A***	FF	FF	FF
DF: Differential; FF: Full-featured cable; CT: Charge-through cable (including ***USB 2.0*** function); ***CTVPD***: Charge-Through ***VCONN-Powered USB Device***.				

3.7.2.6.1 Coupling between CC to USB D+/D– (*Normative*)

The differential coupling between the CC and D+/D– ***shall*** be below the limit shown in Figure 3-50. The limit is defined with the vertices of (0.3 MHz, -60.5 dB), (1 MHz, −50 dB), (10 MHz, −30 dB), (16 MHz, −26 dB) and (100 MHz, −26 dB).

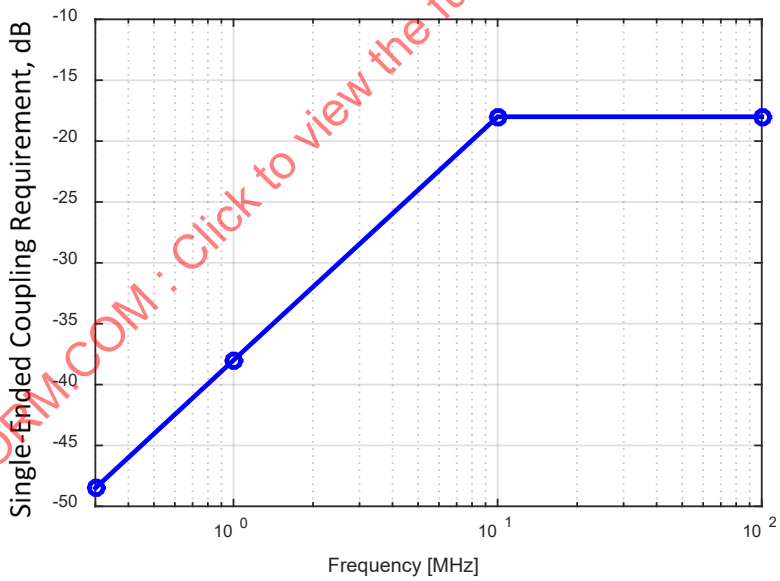
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Figure 3-50 Requirement for Differential Coupling between CC and D+/D–



For ***USB 2.0*** Type-C cables, the singled-ended coupling between the CC and D– ***shall*** be below the limit shown in Figure 3-51. The limit is defined with the vertices of (0.3 MHz, −48.5 dB), (1 MHz, −38 dB), (10 MHz, −18 dB) and (100 MHz, −18 dB).

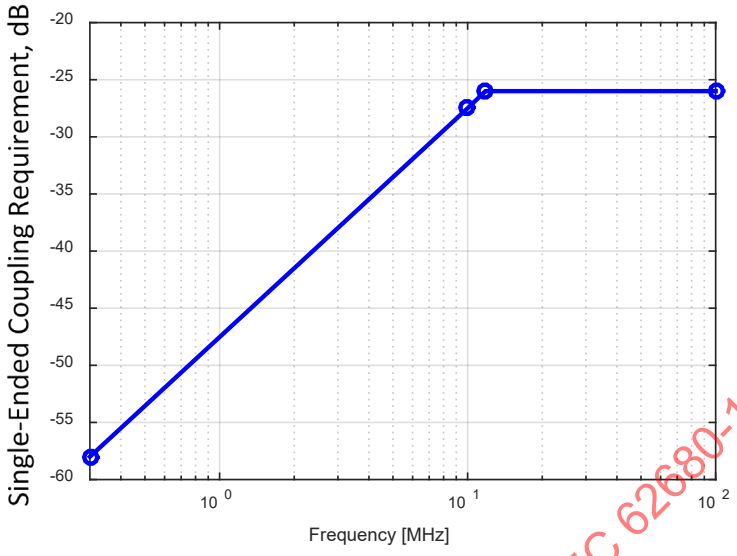
Figure 3-51 Requirement for Single-Ended Coupling between CC and D– in *USB 2.0* Type-C Cables



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For USB Full-Featured Type-C cables, the singled-ended coupling between the CC and D– ***shall*** be below the limit shown in Figure 3-52. The limit is defined with the vertices of (0.3 MHz, −58 dB), (10 MHz, −27.5 dB), (11.8 MHz, −26 dB) and (100 MHz, −26 dB).

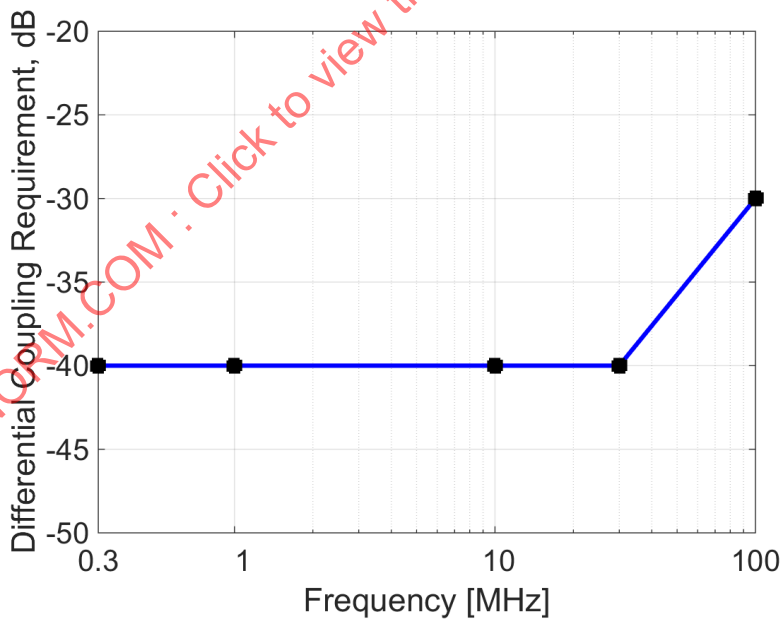
Figure 3-52 Requirement for Single-Ended Coupling between CC and D– in USB Full-Featured Type-C Cables



3.7.2.6.2 VBUS Coupling to SBU_A/SBU_B, CC, and USB D+/D– (*Normative*)

The differential coupling between VBUS and USB D+/D– ***shall*** be less than the limit shown in Figure 3-53. The limit is defined by the following vertices: (0.3 MHz, –40 dB), (1 MHz, –40 dB), (30 MHz, –40 dB), and (100 MHz, –30 dB).

Figure 3-53 Requirement for Differential Coupling between VBUS and D+/D–



The maximum VBUS loop inductance ***shall*** be 900 nH and the maximum mutual inductance (M) between VBUS and low speed signal lines (CC, SBU_A, SBU_B, D+, D–) ***shall*** be as specified in Table 3-26 to limit VBUS inductive noise coupling on low speed signal lines. For full-featured cables, the range of VBUS bypass capacitance ***shall*** be 8nF up to 500nF as any of the values in the range is equally effective for high-speed return-path bypassing.

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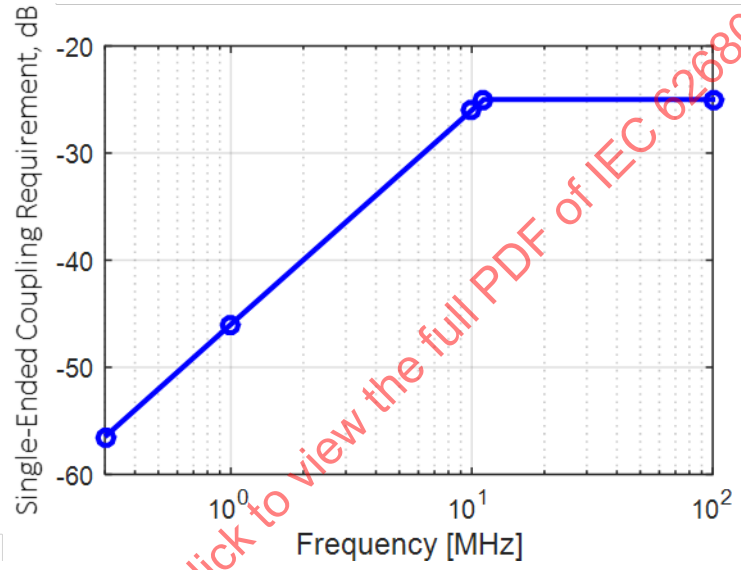
Table 3-26 Maximum Mutual Inductance (M) between VBUS and Low Speed Signal Lines

Low Speed Wire	Maximum Mutual Inductance (nH)
CC	350
SBU_A/SBU_B	330
D+/D–	330

3.7.2.6.3 Coupling between SBU_A and SBU_B (*Normative*)

The single-ended coupling between SBU_A and SBU_B ***shall*** be less than the limit shown in Figure 3-54. The limit is defined with the vertices of (0.3 MHz, −56.5 dB), (1 MHz, −46 dB), (10 MHz, −26 dB), (11.2 MHz, −25 dB), and (100 MHz, −25 dB).

Figure 3-54 Requirement for Single-Ended Coupling between SBU_A and SBU_B

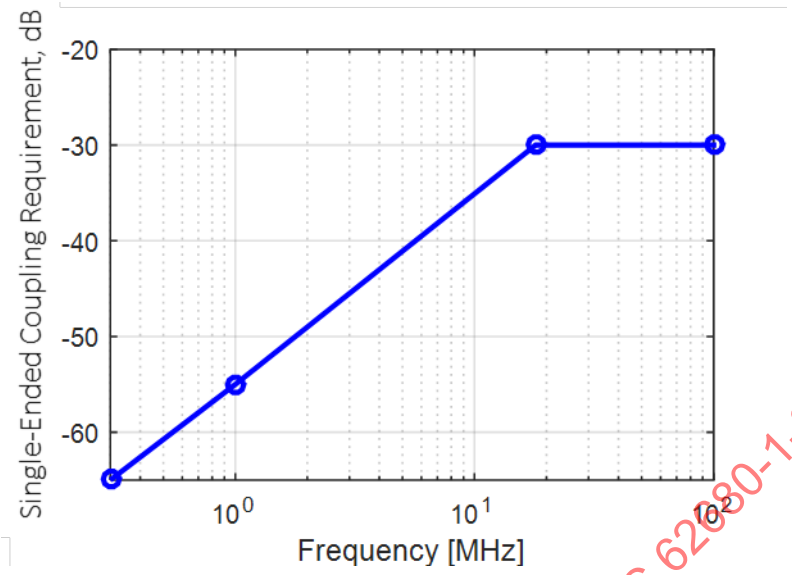


3.7.2.6.4 Coupling between SBU_A/SBU_B and CC (*Normative*)

The single-ended coupling between SBU_A and CC, and between SBU_B and CC ***shall*** be less than the limit shown in Figure 3-55. The limit is defined with the vertices of (0.3 MHz, −65 dB), (1 MHz, −55 dB), (18 MHz, −30 dB), and (100 MHz, −30 dB).

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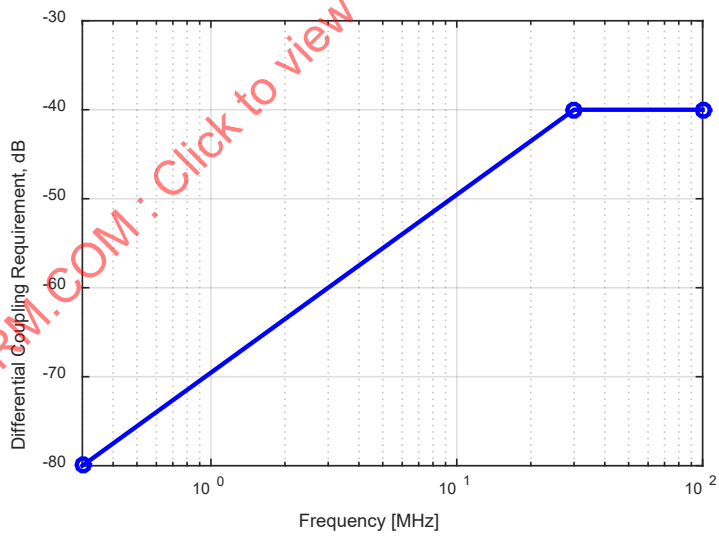
Figure 3-55 Requirement for Single-Ended Coupling between SBU_A/SBU_B and CC



3.7.2.6.5 Coupling between SBU_A/SBU_B and USB D+/D– (*Normative*)

The coupling between SBU_A and differential D+/D–, and between SBU_B and differential D+/D– ***shall*** be less than the limit shown in Figure 3-56. The limit is defined with the vertices of (0.3 MHz, –80 dB), (30 MHz, –40 dB), and (100 MHz, –40 dB).

Figure 3-56 Requirement for Coupling between SBU_A and differential D+/D–, and SBU_B and differential D+/D–



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3.7.2.7 USB D+/D– Signal Requirements (*Normative*)

The USB D+/D– lines of the USB Type-C to USB Type-C passive cable assembly ***shall*** meet the requirements defined in Table 3-27.

Table 3-27 USB D+/D– Signal Integrity Requirements for USB Type-C to USB Type-C Passive Cable Assemblies

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D– lines of the cable assembly have the proper impedance. For the entire cable assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20%-80%).
Propagation Delay	EIA 364-103 The purpose of the test is to verify the end-to-end propagation of the D+/D– lines of the cable assembly.	26 ns max. 400 ps rise time (20%-80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D– lines of cable assembly arrive at the receiver at the same time.	100 ps max. 400 ps rise time (20%-80%).
D+/D– Pair Attenuation	EIA 364 – 101 This test ensures the D+/D– pair of a cable assembly is able to provide adequate signal strength to the receiver in order to maintain a low error rate.	≥ –1.52 dB @ 50 MHz ≥ –2.03 dB @ 100 MHz ≥ –2.91 dB @ 200 MHz ≥ –4.35 dB @ 400 MHz
D+ or D– DC Resistance	This test ensures the D+/D– has the proper DC resistance range in order to predict the EOP level and set the ***USB 2.0*** disconnect level.	3.5 ohms max.

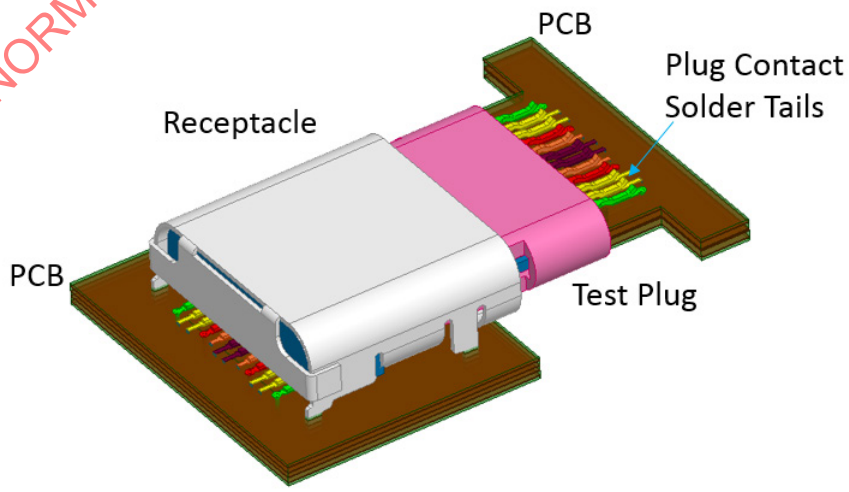
3.7.2.8 VBUS DC Voltage Tolerance (*Normative*)

A USB Type-C to USB Type-C cable assembly ***shall*** tolerate a VBUS voltage of 21 V DC at the cable rated current (i.e., 3 A or 5 A) applied for one hour as a pre-condition of the testing of the electrical aspects of the cable assembly.

3.7.3 Mated Connector (*Informative – USB 3.2* Gen2 and *USB4* Gen2)

The mated connector as defined in this specification for USB Type-C consists of a receptacle mounted on a PCB, representing how the receptacle is used in a product, and a test plug also mounted on a PCB (paddle card) without cable. This is illustrated in Figure 3-57. Note that the test plug is used in host/device TX/RX testing also.

Figure 3-57 Illustration of USB Type-C Mated Connector

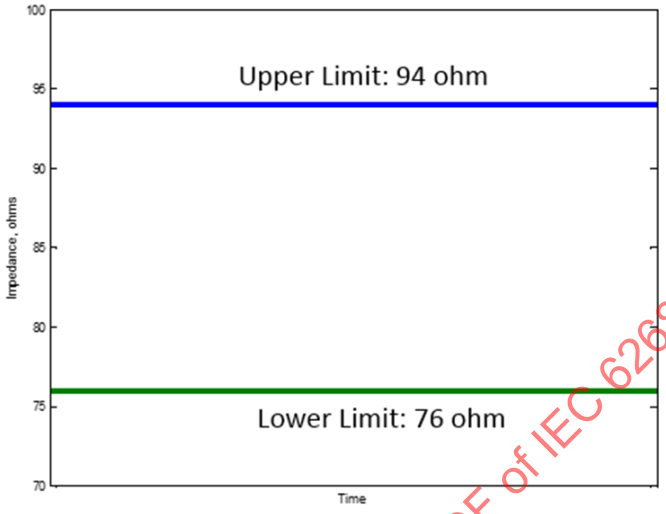


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3.7.3.1 Differential Impedance (*Informative*)

The mated connector impedance target is specified to minimize reflection from the connector. The differential impedance of a mated connector ***should*** be within 85 Ω ± 9 Ω, as seen from a 40 ps (20% – 80%) rise time. The impedance profile of a mated connector ***should*** fall within the limits shown in Figure 3-58.

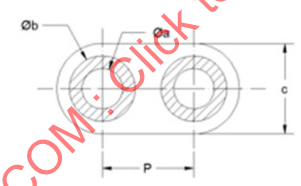
Figure 3-58 Recommended Impedance Limits of a USB Type-C Mated Connector



The PCB stack up, lead geometry, and solder pad geometry ***should*** be modeled in 3D field-solver to optimize electrical performance. Example ground voids under signal pads are shown in Figure 3-59 based on pad geometry, mounting type, and PCB stack-up shown.

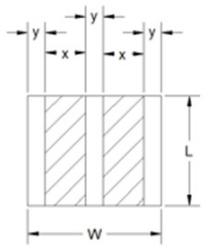
Figure 3-59 Recommended Ground Void Dimensions for USB Type-C Receptacle

PTH



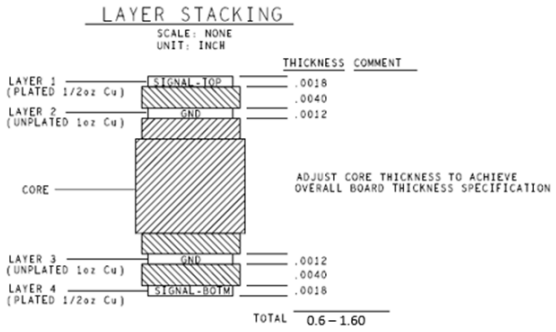
a	Finish hole diameter	0.40
b	Annular ring diameter	0.65
c	Antipad diameter	1.00
P	Antipad center to center distance	0.80

SMT



x	SMT pad width	0.35
y	Gap to SMT pad edge	0.15
L	Ground void length	0.7~0.95
W	Ground void width	1.15

Unit: mm



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3.7.3.2 Mated Connector Recommended Differential S-Parameter and Signal Integrity Characteristics

The recommended signal integrity characteristics of USB Type-C mated connector pair are listed in Table 3-28.

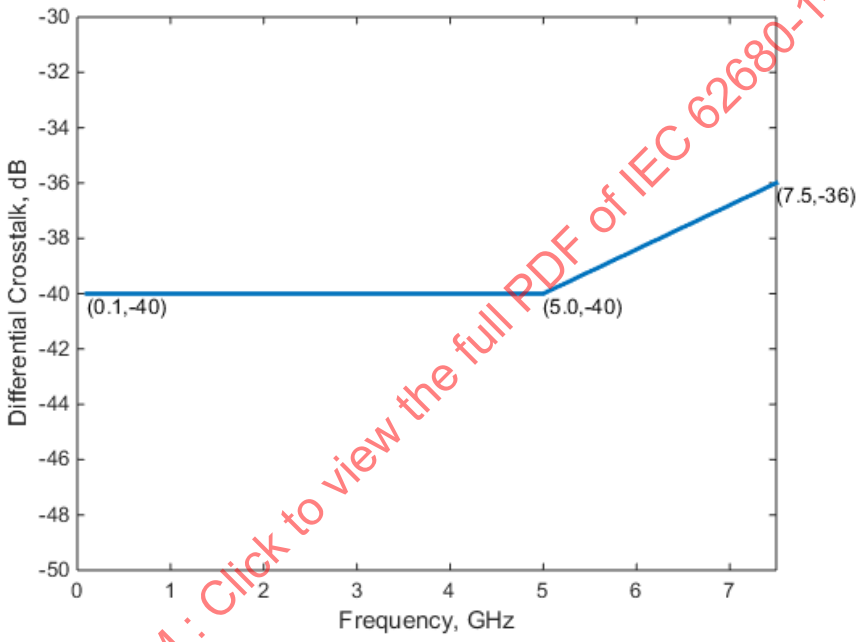
Table 3-28 USB Type-C Mated Connector Recommended Signal Integrity Characteristics (*Informative*)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at the TX/RX Gen1, Gen2 and Gen3 generation Nyquist frequencies.	≥ −0.6 dB @ 2.5 GHz ≥ −0.8 dB @ 5.0 GHz ≥ −1.0 dB @ 10 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −40 dB ≤ −39 dB (with fmax = 20 GHz and Vin(f) defined with Tb (UI) = 50 ps; ***USB4*** Gen3)
Integrated Differential Near-end Crosstalk on TX/RX (INEXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + 0.125^2\cdot\lvert C2D(f)\rvert^2)df + \int_0^{f_{max}}\lvert Vdd(f)\rvert^2\ \lvert NEXTd(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXT* = NEXT between TX/RX pairs *NEXTd* = NEXT between D+/D− and TX/RX pairs	≤ −44 dB
Integrated Differential Far-end Crosstalk on TX/RX (IFEXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2 + 0.125^2\cdot\lvert C2D(f)\rvert^2)df + \int_0^{f_{max}}\lvert Vdd(f)\rvert^2\ \lvert FEXTd(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: *FEXT* = FEXT between TX/RX pairs *FEXTd* = FEXT between D+/D− and TX/RX pairs	≤ −44 dB
Differential Crosstalk of TX/RX on D+/D−	The differential near-end and far-end crosstalk of the TX/RX pairs on the D+/D− pair in mated connectors.	See Figure 3-60
Differential Crosstalk of D+/D− on TX/RX	The differential near-end and far-end crosstalk of the D+/D− pair on the TX/RX pairs in mated connectors.	See Figure 3-60
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2 + \lvert SDD22(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −18 dB

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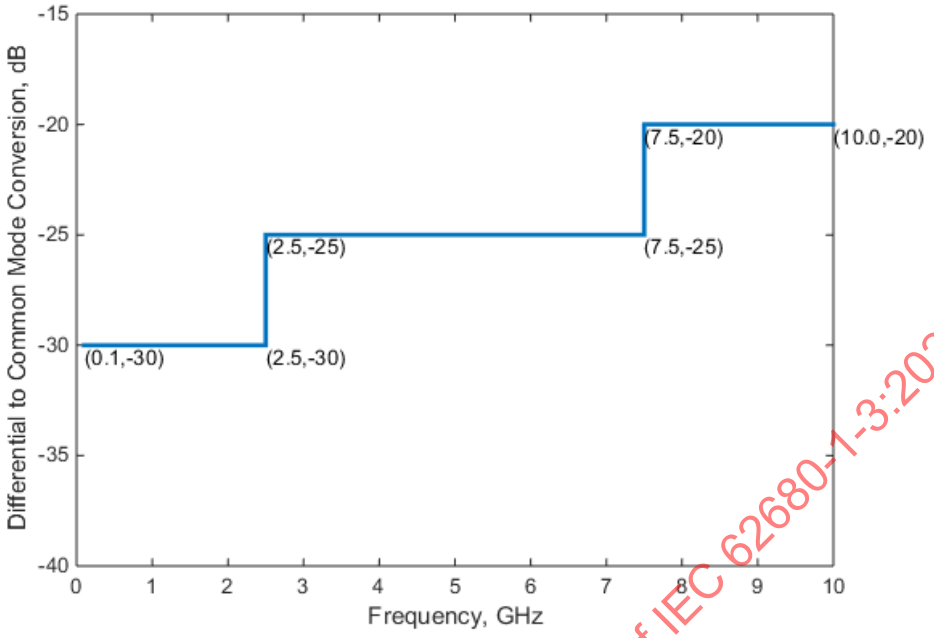
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	See Figure 3-61
Note: *fmax* = 12.5 GHz (unless otherwise specified); *Vin(f)* is defined in Figure 3-40 with Tb (UI) = 100 ps (unless otherwise specified); *Vdd(f)* is also defined in Figure 3-40 with Tb (UI) = 2.08 ns. *C2D(f)* =measured near-end and far-end crosstalk between TX/RX pairs, and the common-mode-to-differential conversion, respectively. The factor of 0.125^2 accounts for the assumption that the common mode amplitude is 12.5% of the differential amplitude.		

Figure 3-60 Recommended Differential Near-End and Far-End Crosstalk Limits between D+/D– Pair and TX/RX Pairs



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Figure 3-61 Recommended Limits for Differential-to-Common-Mode Conversion



3.7.4 Receptacle Connector SI Requirements and Testing (*Normative* – *USB4* Gen3/Gen4)

Note: While the ***normative*** requirements in this section are defined in terms of ***USB4*** Gen3, these requirements apply also to ***USB4*** Gen4 passive cable assemblies as these are electrically equivalent to ***USB4*** Gen3 passive cable assemblies.

The USB Type-C receptacle connector requirements for ***USB4*** Gen3 are ***normative*** and listed in Table 3-29. Unless otherwise specified, the items to be specified are identical to what is defined in Section 3.7.3 and the parameters used to calculate the integrated parameters are the same as defined in Section 3.7.2.4 for the ***USB4*** Gen3 cable assembly.

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Table 3-29 USB Type-C Receptacle Connector Signal Integrity Characteristics for *USB4* Gen3 (*Normative*)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at a few different frequencies.	≥ −0.6 dB @ 2.5 GHz ≥ −0.8 dB @ 5.0 GHz ≥ −1.0 dB @ 10 GHz ≥ −1.25 dB @ 12.5 GHz ≥ −1.5 dB @ 15 GHz
Integrated Differential Near-end Crosstalk on TX/RX (INEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXT* = NEXT between TX1and RX1, and TX2 and RX2.	≤ −43 dB
Integrated Differential Far-end Crosstalk on TX/RX (IFEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *FEXT* = FEXT between TX1 and RX1, and TX2 and RX2.	≤ −43 dB
Differential Crosstalk of TX/RX on D+/D− Differential Crosstalk of D+/D− on TX/RX	The differential near-end and far-end crosstalk of the TX/RX pairs on the D+/D− pair in mated connectors, and the differential near-end and far-end crosstalk of the D+/D− pair on the TX/RX pairs in mated connectors. $dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2+\lvert NEXT(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *FEXT* = Far-end crosstalk between TX/RX and D+/D− pairs *NEXT* = Near-end crosstalk between TX/RX and D+/D− pairs *fmax* = 1.2 GHz	≤ −50 dB
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −15 dB
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	≤ −20 dB
Note: *fmax* = 20 GHz (unless otherwise specified); *Vin(f)* is defined with Tb (UI) = 50 ps.		

The requirements defined in this section do not apply to the USB Type-C plug connector, as the limits Table 3-29 factor in the electrical characteristics of test fixture that includes a USB Type-C plug connector specifically selected for testing of the USB Type-C receptacle. The USB Type-C plug connector does not have a set of requirements defined at the mated connector level as there are tradeoffs allowed to achieve acceptable performance at the finished cable assembly level.

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3.7.5 USB Type-C to USB Legacy Cable Assemblies (*Normative*)

The USB Type-C to legacy cable assemblies ***may*** support ***USB 2.0*** only or ***USB 3.1***.

3.7.5.1 *USB 2.0*-only Cable Assemblies (*Normative*)

The ***USB 2.0***-only Type-C to legacy USB cable assemblies include:

- USB Type-C plug to ***USB 2.0*** Standard-A plug
- USB Type-C plug to ***USB 2.0*** Standard-B plug
- USB Type-C plug to ***USB 2.0*** Micro-B plug
- USB Type-C plug to ***USB 2.0*** Mini-B plug

The USB D+/D− signal integrity requirements are specified in Table 3-30.

Table 3-30 USB D+/D− Signal Integrity Requirements for USB Type-C to Legacy USB Cable Assemblies (*Normative*)

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D− lines of the cable assembly have the proper impedance. For the entire cable assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20% – 80%).
Propagation Delay	EIA 364-103 The purpose of the test is to verify the end-to-end propagation of the D+/D− lines of the cable assembly.	10 ns max for USB Type-C to Micro-B cable assembly; 20 ns max for all other USB Type-C to legacy USB cable assemblies. 400 ps rise time (20% – 80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D− lines of cable assembly arrive at the receiver at the same time.	100 ps max. 400 ps rise time (20% – 80%).
D+/D− Pair Attenuation	EIA 364 – 101 This test ensures the D+/D− pair of a cable assembly is able to provide adequate signal strength to the receiver in order to maintain a low error rate.	≥ −1.52 dB @ 50 MHz ≥ −2.03 dB @ 100 MHz ≥ −2.91 dB @ 200 MHz ≥ −4.35 dB @ 400 MHz
D+ or D− DC Resistance	This test ensures the D+/D− has the proper DC resistance range in order to predict the EOP level and set the ***USB 2.0*** disconnect level.	3.5 ohms max.

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3.7.5.2 *USB 3.1* Gen2 Cable Assemblies (*Normative*)

The USB Type-C to ***USB 3.1*** Gen2 legacy cable assemblies include:

- USB Type-C plug to ***USB 3.1*** Standard-A plug
- USB Type-C plug to ***USB 3.1*** Standard-B plug
- USB Type-C plug to ***USB 3.1*** Micro-B plug

The ***informative*** design targets for these cables are provided in Table 3-31.

Table 3-31 Design Targets for USB Type-C to *USB 3.1* Gen2 Legacy Cable Assemblies (*Informative*)

Items	Design Targets
Differential Impedance	76 ohms min and 96 ohms max. 40 ps rise time (20%-80%).
Differential Insertion Loss	≥ −2 dB @ 100 MHz ≥ −4 dB @ 2.5 GHz, except for the USB Type-C plug to ***USB 3.1*** Standard-A plug cable assembly which is ≥−3.5 dB @ 2.5 GHz −6.0 dB max @ 5.0 GHz
Differential NEXT between SuperSpeed Pairs	≤ −34 dB to 5 GHz
Differential NEXT and FEXT between D+/D- and SuperSpeed Pairs	≤ −30 dB to 5 GHz

The ***normative*** requirements include the USB D+/D− signaling as specified in Table 3-30, and the SuperSpeed USB parameters specified in Table 3-32.

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Table 3-32 USB Type-C to *USB 3.1* Gen2 Legacy Cable Assembly Signal Integrity Requirements (*Normative*)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at both the SuperSpeed Gen1 and Gen2 Nyquist frequencies.	≥ −4 dB @ 2.5 GHz, except for the USB Type-C plug to ***USB 3.1*** Standard-A plug cable assembly which is ≥ −3.5 dB @ 2.5 GHz ≥ −6.0 dB at 5.0 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	$\leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 21.392$ See Figure 3-62.
Integrated Differential Crosstalk on SuperSpeed (ISSXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}(\lvert Vin(f)\rvert^2\lvert NEXTs(f)\rvert^2 + \lvert Vdd(f)\rvert^2\lvert NEXTd(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXTs* = NEXT between SuperSpeed pairs *NEXTd* = NEXT between D+/D− and SuperSpeed pairs *Vdd(f)* = Input pulse spectrum on D+/D− pair, evaluated using equation shown in Figure 3-40 with Tb (UI) = 2.08 ns.	≤ −38 dB
Integrated Differential Crosstalk on D+/D- (IDDXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + \lvert FEXT(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXT* = Near-end crosstalk from SuperSpeed to D+/D− *FEXT* = Far-end crosstalk from SuperSpeed to D+/D− *fmax* = 1.2 GHz	≤ −28.5 dB
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2 + \lvert SDD22(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	$\leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 9.784$ See Figure 3-63.
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	≤ −20 dB
Note: *fmax* = 10 GHz (unless otherwise specified); *Vin(f)* is defined in Figure 3-40 with Tb (UI) = 100 ps; and *Vdd(f)* is also defined in Figure 3-40 with Tb (UI) = 2.08 ns.		

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Figure 3-62 IMR Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly

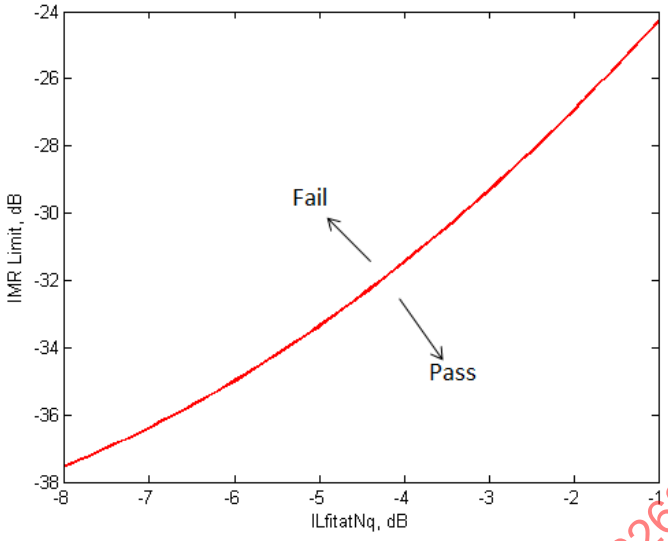
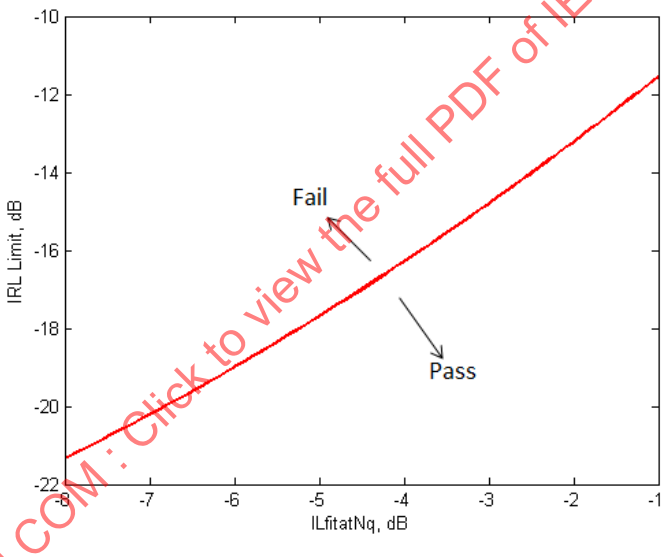


Figure 3-63 IRL Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly



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3.7.5.3 Compliant USB Legacy Plugs used in USB Type-C to USB Legacy Cable Assemblies

The following requirements are incremental to the existing requirements for legacy connectors when used in compliant USB Type-C to legacy cable assemblies.

3.7.5.3.1 Contact Material Requirements for USB Type-C to USB Micro-B Assemblies

For USB Type-C to USB Micro-B assemblies, change the contact material in the USB Micro-B connector to achieve the following Low-Level Contact Resistance (EIA 364-23B):

- 20 milliohms (Max) initial for V_{BUS} and GND contacts, and
- Maximum change (delta) of +10 milliohms after environmental stresses.

3.7.5.3.2 Contact Current Ratings for USB Standard-A, USB Standard-B and USB Micro-B Connector Mated Pairs (EIA 364-70, Method 2)

When a current of 3 A is applied to the VBUS pin and its corresponding GND pin (i.e., pins 1 and 4 in a USB Standard-A or USB Standard-B connector or pins 1 and 5 in a USB Micro-B connector), the delta temperature ***shall not*** exceed +30° C at any point on the connectors under test, when measured at an ambient temperature of 25° C.

3.7.6 USB Type-C to USB Legacy Adapter Assemblies (*Normative*)

Only the following standard legacy adapter assemblies are defined:

- ***USB 2.0*** Type-C plug to ***USB 2.0*** Micro-B receptacle, and
- USB Full-Featured Type-C plug to ***USB 3.1*** Standard-A receptacle.

3.7.6.1 *USB 2.0* Type-C Plug to *USB 2.0* Micro-B Receptacle Adapter Assembly

This adapter assembly supports only the ***USB 2.0*** signaling. It ***shall not*** exceed 150 mm in total length, measured from end to end. Table 3-33 defines the electrical requirements.

Table 3-33 USB D+/D– Signal Integrity Requirements for USB Type-C to Legacy USB Adapter Assemblies (*Normative*)

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D– lines of the adapter assembly have the proper impedance. For the entire adapter assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20% – 80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D– lines of adapter assembly arrive at the receiver at the same time.	20 ps max. 400 ps rise time (20% – 80%).
Differential Insertion Loss	EIA 364 – 101 This test ensures the D+/D– pair of an adapter assembly can provide adequate signal strength to the receiver.	–0.7 dB max @ 400 MHz
D+ or D– DC Resistance	This test ensures the D+/D– has the proper DC resistance range in order to predict the EOP level and set the ***USB 2.0*** disconnect level.	2.5 ohms max.

3.7.6.2 USB Full-Featured Type-C Plug to *USB 3.1* Standard-A Receptacle Adapter Assembly

The USB Full-Featured Type-C plug to ***USB 3.1*** Standard–A receptacle adapter assembly is intended to be used with a direct-attach device (e.g., USB thumb drive). A system is not guaranteed to function when using an adapter assembly together with a Standard USB cable assembly.

To minimize the impact of the adapter assembly to system signal integrity, the adapter assembly ***should*** meet the ***informative*** design targets in Table 3-34.

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Table 3-34 Design Targets for USB Type-C to *USB 3.1* Standard-A Adapter Assemblies (*Informative*)

Items	Design Targets
Differential Return Loss	≤ −15 dB to 5 GHz Normalized with 85 ohms.
Differential Insertion Loss	≥ −2.4 dB to 2.5 GHz, ≥ −3.5 dB to 5 GHz
Differential NEXT between SuperSpeed Pairs	≤ −40 dB to 2.5 GHz ≤ −34 dB at 5 GHz
Differential NEXT and FEXT between D+/D− and SuperSpeed Pairs	≤ −30 dB to 2.5 GHz

The ***normative*** requirements for the adapter assembly are defined in Table 3-33 and Table 3-35. The adapter assembly total length is limited to 150 mm max.

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Table 3-35 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly Signal Integrity Requirements (*Normative*)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequency (ILfitatNq)	ILfitatNq is evaluated at the SuperSpeed Gen1 Nyquist frequency.	≥ −2.4 dB at 2.5 GHz ≥ −3.5 dB at 5 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −38 dB, Tb = 200 ps ≤ −27 dB, Tb = 100 ps
Integrated Differential Crosstalk on SuperSpeed (ISSXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}(\lvert Vin(f)\rvert^2\lvert NEXTs(f)\rvert^2 + \lvert Vdd(f)\rvert^2\lvert NEXTd(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXTs* = NEXT between SuperSpeed pairs *NEXTd* = NEXT between D+/D− and SuperSpeed pairs *Vdd(f)* = Input pulse spectrum on D+/D− pair, evaluated using equation shown in Figure 3-40 with Tb (UI) = 2.08 ns.	≤ −37 dB
Integrated Differential Crosstalk on D+/D- (IDDXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + \lvert FEXT(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXT* = Near-end crosstalk from SuperSpeed to D+/D− *FEXT* = Far-end crosstalk from SuperSpeed to D+/D− *fmax* = 1.2 GHz	≤ −30 dB
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2 + \lvert SDD22(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −14.5 dB, Tb = 200 ps ≤ −12.0 dB, Tb = 100 ps
Diff to Comm mode	Differential to Common Mode conversion (SCD12, SCD21)	≤ −15 dB
Note: *fmax* = 7.5 GHz; *Vin(f)* is defined in Figure 3 40 with Tb (UI) = 200 ps; and *Vdd(f)* is also specified in Figure 3-40 with Tb (UI) = 2.08 ns.		

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3.7.6.3 Compliant USB Legacy Receptacles used in USB Type-C to USB Legacy Adapter Assemblies

3.7.6.3.1 Contact Material Requirements

Refer to Section 3.7.5.3.1 for contact material requirements as these apply to legacy USB Standard-A and USB Micro-B receptacles used in USB Type-C to Legacy Adapter Assemblies.

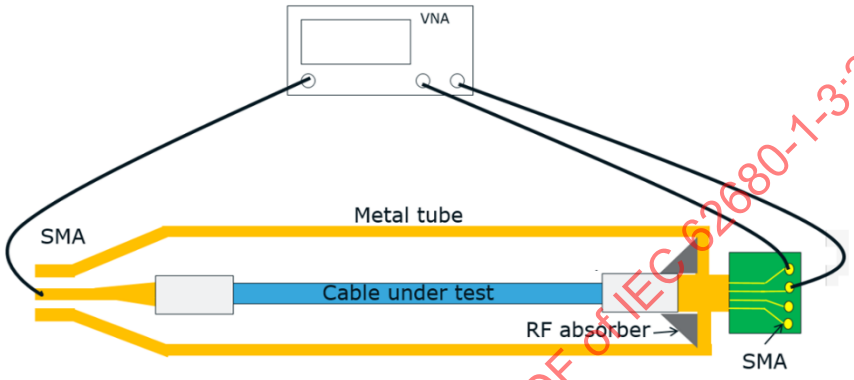
3.7.6.3.2 Contact Current Ratings

Refer to Section 3.7.5.3.2 for contact current rating requirements as these apply to legacy USB Standard-A and USB Micro-B receptacles used in USB Type-C to Legacy Adapter Assemblies.

3.7.7 Shielding Effectiveness Requirements (*Normative*)

The cable assembly shielding effectiveness (SE) test measures the EMI and RFI levels from the cable assembly. To perform the measurement, the cable assembly ***shall*** be installed in the cable SE test fixture as shown in Figure 3-64. The coupling factors from the cable to the fixture are characterized with a VNA.

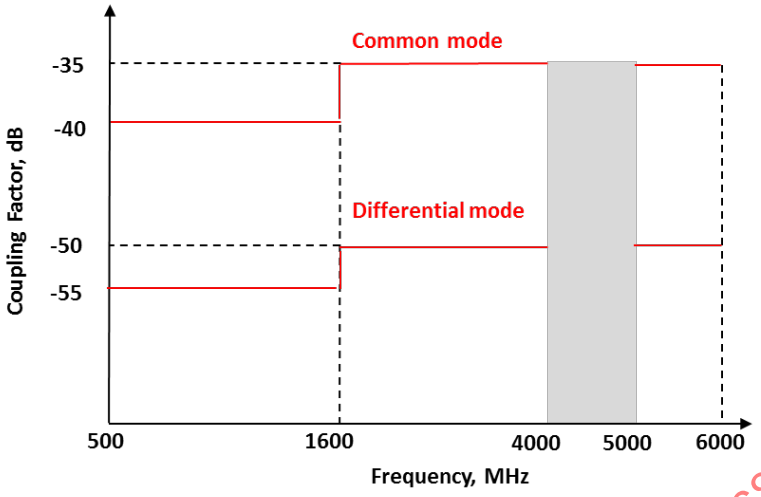
Figure 3-64 Cable Assembly Shielding Effectiveness Testing



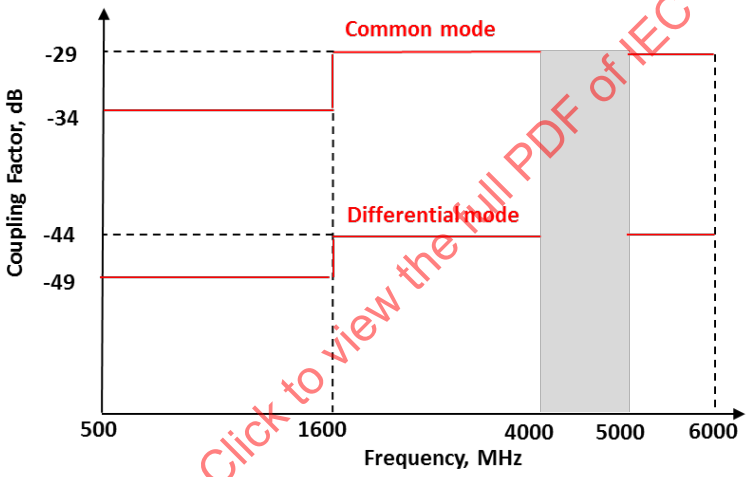
All USB Type-C cable assemblies ***shall*** pass the shielding effectiveness test for compliance. Figure 3-65 shows the pass/fail criteria for (a) USB Type-C to USB Type-C cable assemblies, (b) USB Type-C to legacy USB cable assemblies, and (c) the USB Type-C to ***USB 3.1*** Standard-A Receptacle Adapter assembly. Note that the shielding effectiveness for the frequency band from 4 GHz to 5 GHz is not specified since there is no antenna operating in this frequency range.

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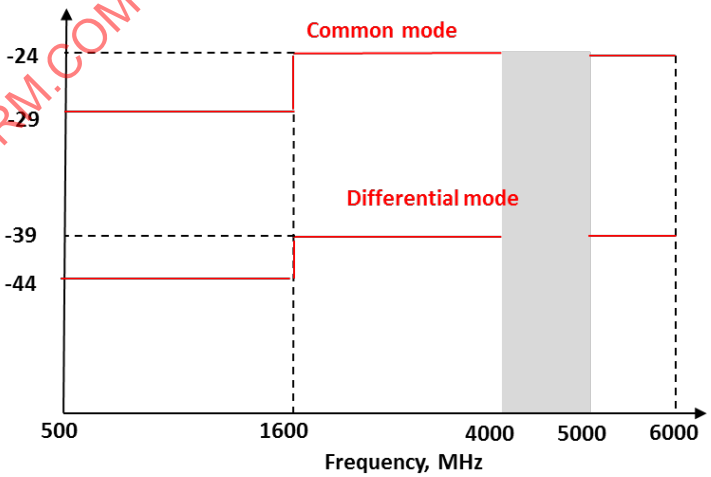
Figure 3-65 Shielding Effectiveness Pass/Fail Criteria



(a) For USB Type-C to USB Type-C Cable Assemblies



(b) For USB Type-C to legacy USB Cable Assemblies



(c) For USB Type-C to USB3.1 Standard-A Receptacle Adapter Assembly

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3.7.8 DC Electrical Requirements (*Normative*)

Unless otherwise stated, the tests in this section are performed on mated connector pairs.

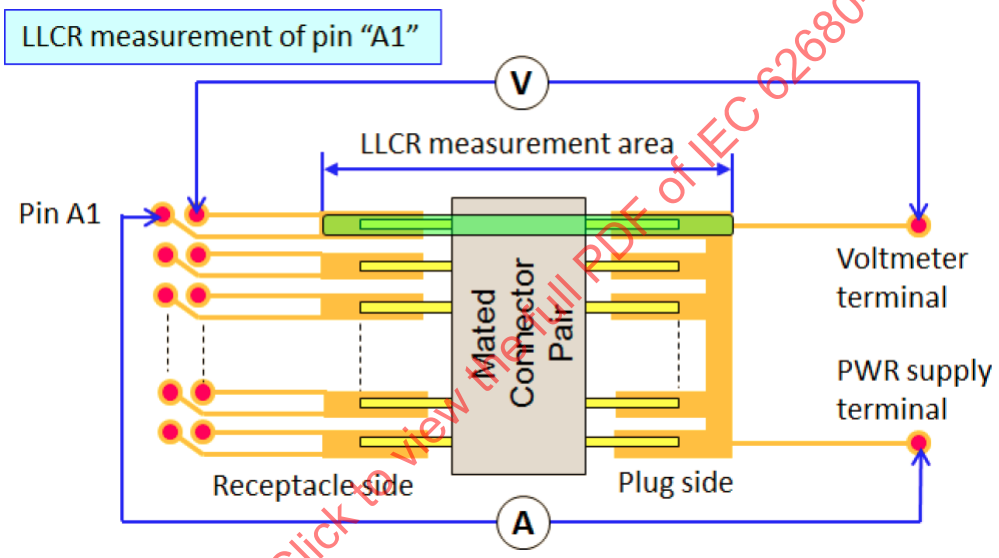
3.7.8.1 Low Level Contact Resistance (EIA 364-23B)

The low-level contact resistance (LLCR) measurement is made across the plug and receptacle mated contacts and does not include any internal paddle cards or substrates of the plug or receptacle. See Figure 3-66. The following apply to the power and signal contacts:

- 40 mΩ (Max) initial for VBUS, GND and all other contacts.
- 50 mΩ (Max) after environmental stresses.
- Measure at 20 mV (Max) open circuit at 100 mA.

Refer to Section 3.8 for environmental requirements and test sequences.

Figure 3-66 LLCR Measurement Diagram



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3.7.8.2 Dielectric Strength (EIA 364-20)

No breakdown ***shall*** occur when 100 Volts AC (RMS) is applied between adjacent contacts of unmated and mated connectors.

3.7.8.3 Insulation Resistance (EIA 364-21)

A minimum of 100 MΩ insulation resistance is required between adjacent contacts of unmated and mated connectors.

3.7.8.4 Contact Current Rating

The current rating testing for the USB Type-C connector (plug and receptacle) ***shall*** be conducted per the following set up and procedures:

- A current of 5 A ***shall*** be applied collectively to VBUS pins (i.e., pins A4, A9, B4, and B9) and 1.25 A ***shall*** be applied to the VCONN pin (i.e., B5) as applicable, terminated through the corresponding GND pins (i.e., pins A1, A12, B1, and B12). A minimum current of 0.25 A ***shall*** also be applied individually to all the other contacts, as applicable. When current is applied to the contacts, the temperature of the connector pair ***shall*** be allowed to stabilize. The temperature rise of the outside shell surface of

the mated pair above the VBUS and GND contacts ***shall not*** exceed 30 °C above the ambient temperature. Figure 3-67 provides an illustration of the measurement location.

- The measurement ***shall*** be done in still air.
- The connectors ***shall*** be oriented such that the accessible outer shell surface is on top and horizontal to the ground.
- The plug and receptacle ***may*** require modification to access solder tails or cable attachment points.
- Either thermocouple or thermo-imaging (preferred) method ***may*** be used for temperature measurement
- For certification, the connector manufacturer ***shall*** provide the receptacle and plug samples under test mounted on a current rating test PCB with no copper planes. A cable plug ***may*** use short wires to attach the cable attachment points together rather than using a current rating test PCB.

The current rating test PCBs ***shall*** be of a 2-layer construction. If 2-layer construction is not possible due to the solder tail configuration, VBUS and ground traces ***shall*** be located on the outer layers with the inner layers reserved for signal traces, as required; VCONN traces ***may*** be routed either on internal or external layers. Table 3-36 defines the requirements for the test PCB thickness and traces. The trace length applies to each PCB (receptacle PCB and plug PCB) and is from the contact terminal to the current source tie point.

- Figure 3-68 provides an ***informative*** partial trace illustration of the current rating test PCB.
- If short wires are used instead of a current rating test PCB, the wire length ***shall not*** exceed 70 mm, measured from the plug contact solder point to the other end of the wire. There ***shall*** be no paddle card or overmold included in the test set-up. Each plug solder tail ***shall*** be attached with a wire with the wire gauge of AWG 36 for signals, AWG 32 for power (VBUS and VCONN), and AWG 30 for ground.

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Figure 3-67 Temperature Measurement Point

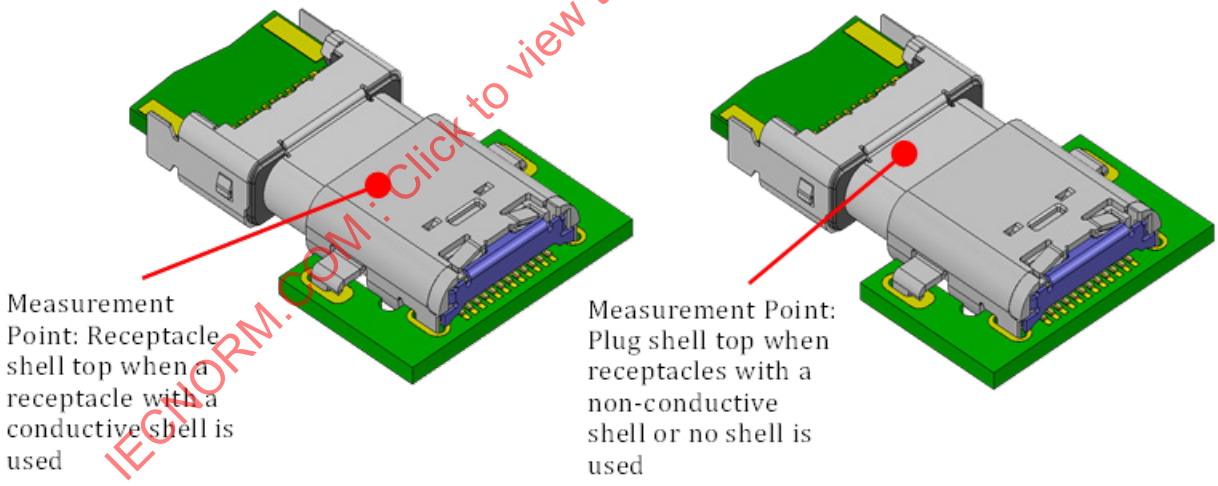
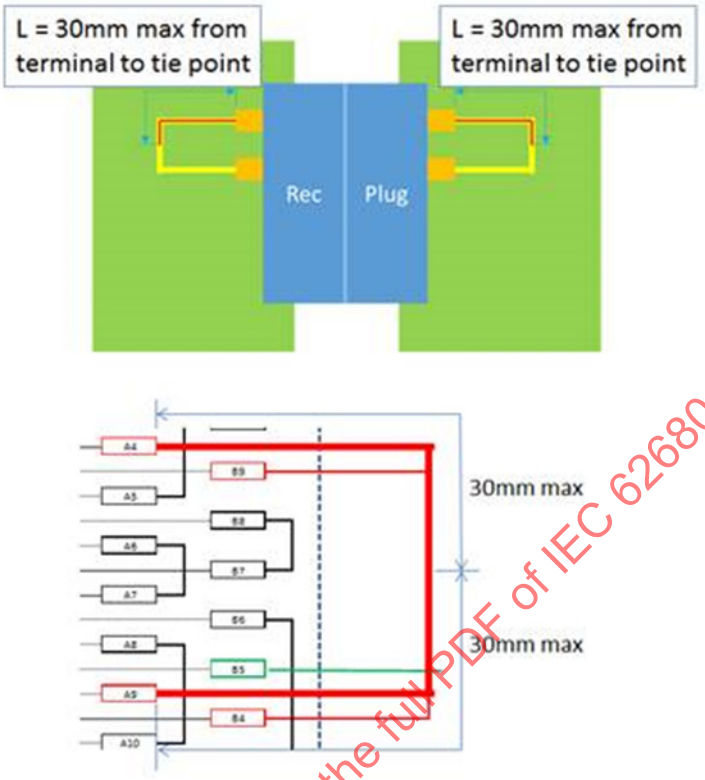


Table 3-36 Current Rating Test PCB

Items	Trace Width (mm)	Trace Length (mm) on each PCB	Thickness
Signal trace	0.25 max.	13 max.	35 µm (1 oz. copper)
Ground trace	1.57 max.	38 max.	35 µm (1 oz. copper)
VBUS and VCONN	1.25 max.	30 max.	35 µm (1 oz. copper)
PCB	***N/A***	***N/A***	0.80 – 1.20 mm

Figure 3-68 Example Current Rating Test Fixture Trace Configuration



3.7.8.5 DC Resistance of D+ and D–

The DC Resistance of the D+ and D– in ***USB 2.0*** High-Speed capable USB Type-C devices and ***USB 2.0*** High-Speed capable USB Type-C Captive devices ***shall*** be equal or less than the maximum value specified in Table 3-37. The D+ and D– DC Resistance is the series combination of any resistance in switches, multiplexers, and the USB PHY.

Table 3-37 Maximum DC Resistance Requirement (*Normative*)

	Maximum DC Resistance
USB Type-C Hosts, Hubs, or Dual-Role Host/Device (*USB 2.0* High-speed capable)	13 Ω
USB Type-C Device only (*USB 2.0* High-speed capable)	17 Ω
USB Type-C Captive Device (*USB 2.0* High-speed capable)	23 Ω

A USB Type-C Host operating in ***USB 2.0*** High-Speed mode ***shall*** implement a disconnect threshold voltage (V_{HSDSC}) level as defined in the ***USB 2.0*** DCR ECN.

3.8 Mechanical and Environmental Requirements (*Normative*)

The requirements in this section apply to all USB Type-C connectors and/or cable assemblies unless otherwise specified. For USB Type-C plug connectors and cable assemblies, the test methods assume that the cable exits the overmold in line with mating direction to a USB Type-C receptacle (i.e., straight out the back of the overmold). For USB Type-C plug connectors and cable assemblies with the cable exiting the overmold in a different direction than straight out the back (e.g., right angle to the mating direction), test fixtures and procedures ***shall*** be modified as required to accomplish the measurement.

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3.8.1 Mechanical Requirements

3.8.1.1 Insertion Force (EIA 364-13)

The initial connector insertion force ***shall*** be within the range from 5 N to 20 N at a maximum rate of 12.5 mm (0.492") per minute. This requirement does not apply when the connectors are used in a docking application.

It is recommended to use a non-silicone-based lubricant on the latching mechanism to reduce wear. The effects of lubricants ***should*** be restricted to insertion and extraction characteristics and ***should not*** increase the resistance of the mated connection.

3.8.1.2 Extraction Force (EIA 364-13)

The initial connector extraction force ***shall*** be within the range of 8 N to 20 N, measured after a preconditioning of five insertion/extraction cycles (i.e., the sixth extraction). After an additional twenty-five insertion/extraction cycles, the extraction force ***shall*** be measured again (i.e., the thirty-second extraction) and the extraction force ***shall*** be:

a. within 33% of the initial reading, and

b. within the range of 8 N to 20 N.

The extraction force ***shall*** be within the range of 6 N to 20 N after 10,000 insertion/ extraction cycles. The extraction force measurement ***shall*** be performed at a maximum speed of 12.5 mm (0.492”) per minute. The extraction force requirement does not apply when the connectors are used in a mechanical docking application.

It is recommended to use a non-silicone-based lubricant on the latching mechanism to reduce wear. The effects of lubricants ***should*** be restricted to insertion and extraction characteristics and ***should*** not increase the resistance of the mated connection.

3.8.1.3 Durability or Insertion/Extraction Cycles (EIA 364-09)

The durability rating ***shall*** be 10,000 cycles minimum for the USB Type-C connector family. The durability test ***shall*** be done at a rate of 500 ± 50 cycles per hour and no physical damage to any part of the connector and cable assembly ***shall*** occur.

3.8.1.4 Cable Flexing (EIA 364-41, Condition 1)

No physical damage or discontinuity over 1 ms during flexing ***shall*** occur to the cable assembly with Dimension X = 22 mm and 500 cycles in each of two planes.

3.8.1.5 Cable Pull-Out (EIA 364-38, Method A)

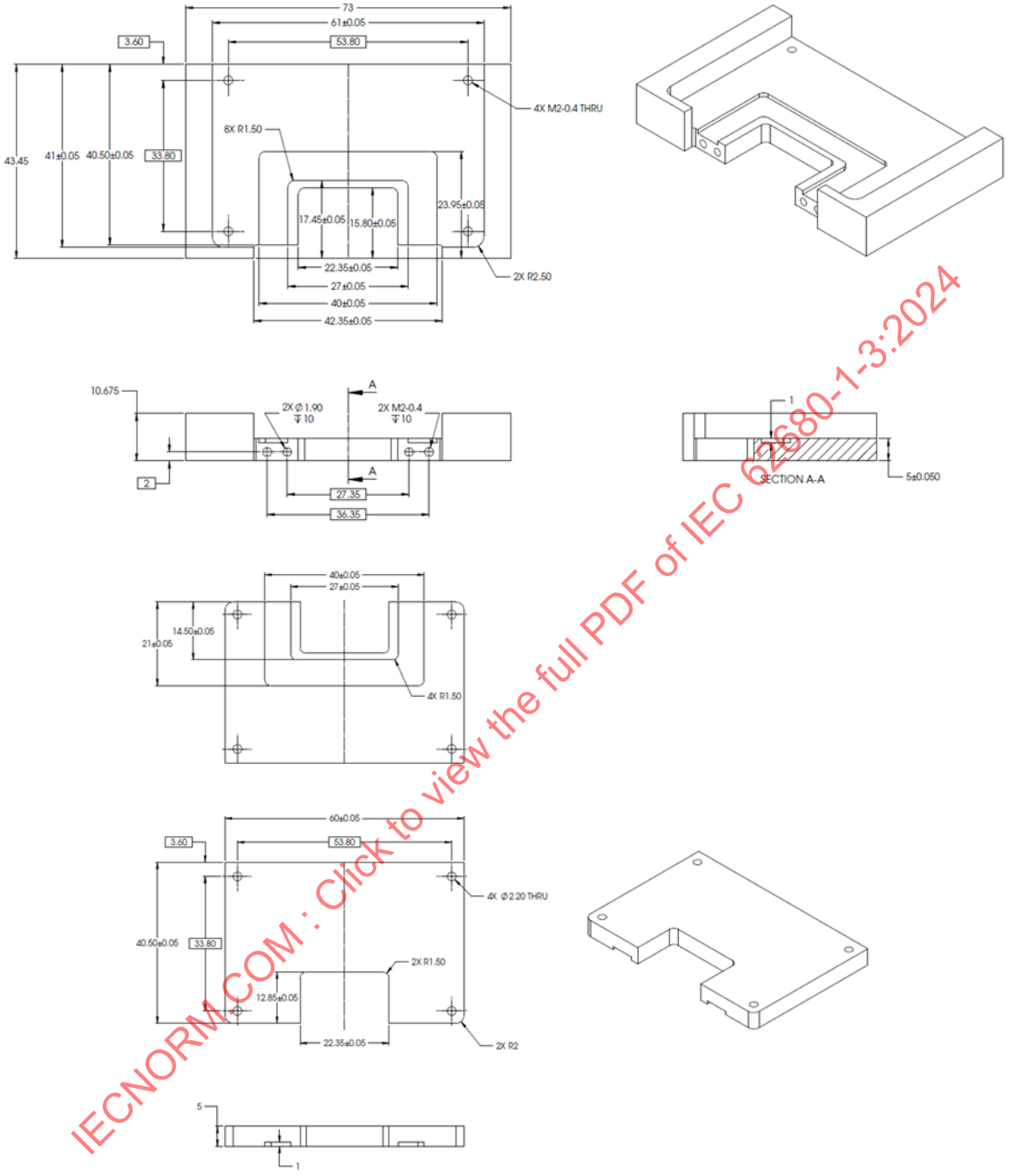
No physical damage to the cable assembly ***shall*** occur when it is subjected to a 40 N axial load for a minimum of 1 minute while clamping one end of the cable plug.

3.8.1.6 4-Axis Continuity Test

The USB Type-C connector family ***shall*** be tested for continuity under stress using a test fixture shown in Figure 3-69 or equivalent.

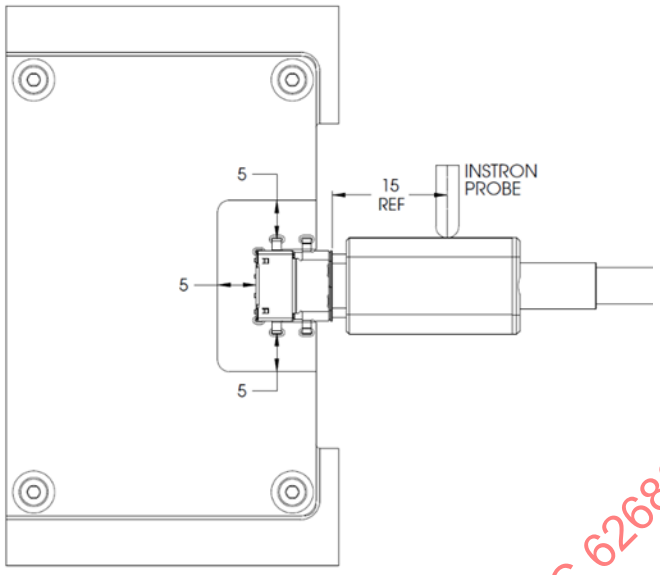
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Figure 3-69 Example of 4-Axis Continuity Test Fixture



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Figure 3-69 Example of 4-Axis Continuity Test Fixture, cont.



Plugs ***shall*** be supplied with a representative overmold or mounted on a 2-layer printed circuit board (PCB) between 0.8 mm and 1.0 mm thickness as applicable. A USB Type-C receptacle ***shall*** be mounted on a 2-layer PCB between 0.8 mm and 1.0 mm thickness. The PCB ***shall*** be clamped on three sides of the receptacle no further than 5 mm away from the receptacle outline. The receptacle PCB ***shall*** initially be placed in a horizontal plane, and a perpendicular moment ***shall*** be applied to the plug with a 5 mm ball tipped probe for a period of at least 10 seconds at a distance of 15 mm from the mating edge of the receptacle shell in a downward direction, perpendicular to the axis of insertion. See Table 3-38 for the force and moment to be applied. Any configuration of non-conductive shell receptacles ***shall*** be tested at the values specified for the vertical receptacle configuration.

Table 3-38 Force and Moment Requirements

Receptacle configuration with respect to mounting surface	Force at 15 mm from receptacle shell mating edge (N)	Moment with respect to receptacle shell mating edge (Nm)
Right angle	20	0.30
Vertical[1]	8	0.12

Notes:
1. Any configuration of non-conductive shell receptacles ***shall*** be tested at the values specified for the vertical receptacle configuration.

The continuity across each contact ***shall*** be measured throughout the application of the tensile force. Each non-ground contact ***shall*** also be tested to confirm that it does not short to the shell during the stresses. The PCB ***shall*** then be rotated 90 degrees such that the cable is still inserted horizontally and the tensile force in Table 3-38 ***shall*** be applied again in the downward direction and continuity measured as before. This test is repeated for 180 degree and 270 degree rotations. Passing parts ***shall not*** exhibit any discontinuities or shorting to the shell greater than 1 µs duration in any of the four orientations.

One method for measuring the continuity through the contacts is to short all the wires at the end of the cable pigtail and apply a voltage through a pull-up to each of VBUS, USB D+,

USB D−, SBU, CC, and TX/RX pins, with the GND pins connected to ground.

Alternate methods are allowed to verify continuity through all pins.

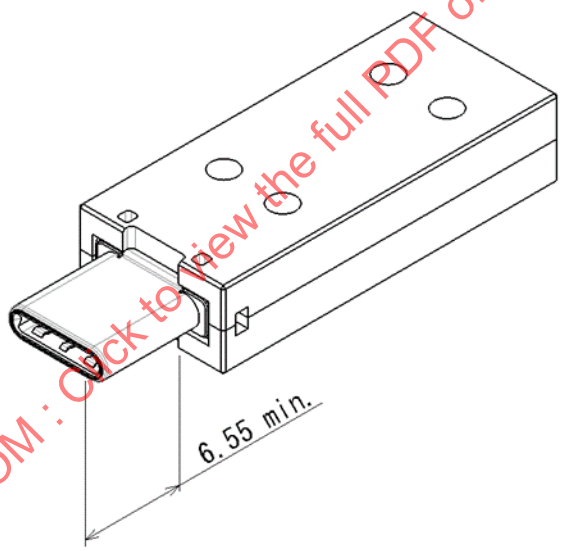
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3.8.1.7 Wrenching Strength

USB Type-C plugs on cable assemblies and fixture plugs without overmold (including PCB-mount USB Type-C plugs) ***shall*** be tested using the mechanical wrenching test fixture defined in the Universal Serial Bus Type-C Connectors and Cable Assemblies Compliance Document. For plug without overmold, the supplier ***shall*** provide a plug test fixture that conforms to the specified plug overmold dimensions for the USB Type-C plug (see Figure 3-70). The fixture ***may*** be metal or other suitable material. Perpendicular moments are applied to the plug with a 5 mm ball tipped probe for a period of at least 10 seconds when inserted in the test fixture to achieve the defined moments in four directions of up or down (i.e., perpendicular to the long axis of the plug opening) and left or right (i.e., in the plane of the plug opening). Compliant connectors ***shall*** meet the following force thresholds:

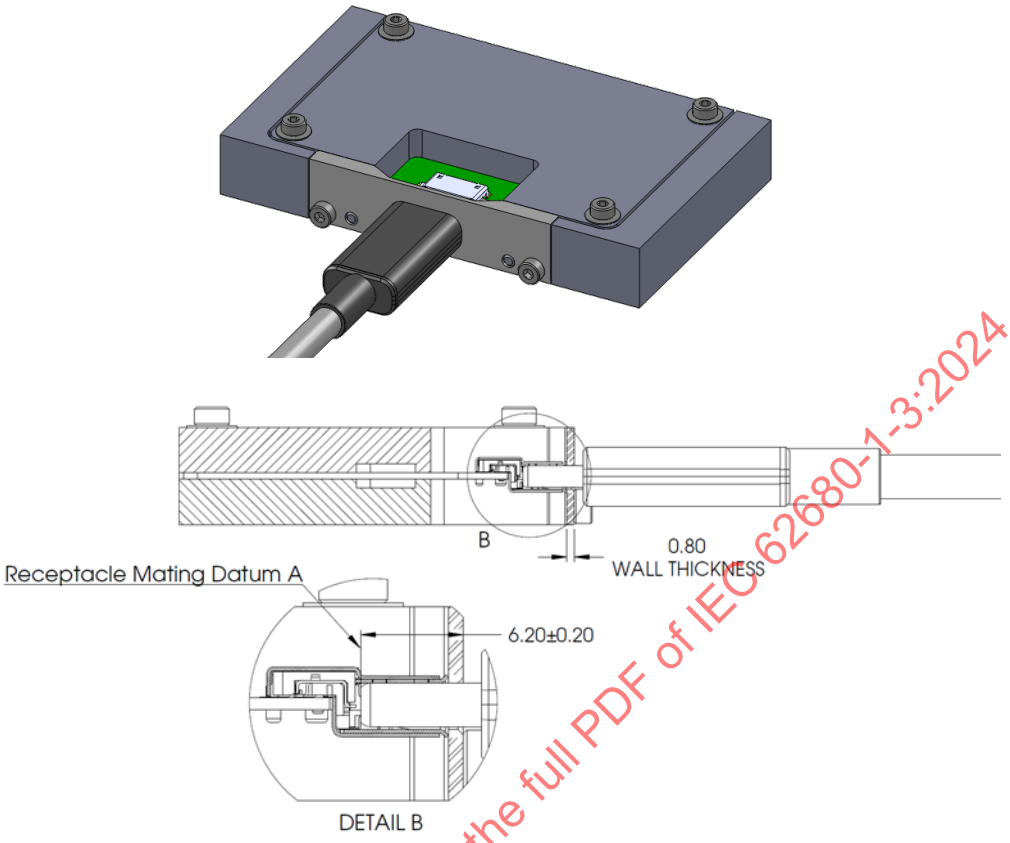
- A moment of 0-0.75 Nm (e.g., 50 N at 15 mm from the edge of the receptacle) is applied to a plug inserted in the test fixture in each of the four directions. A single plug ***shall*** be used for this test. Some mechanical deformation ***may*** occur. The plug ***shall*** be mated with the continuity test fixture after the test forces have been applied to verify no damage has occurred that causes discontinuity or shorting. The continuity test fixture ***shall*** provide a planar surface on the mating side located 6.20 ± 0.20 mm from the receptacle Datum A, perpendicular to the direction of insertion. No moment forces are applied to the plug during this continuity test. Figure 3-71 illustrates an example continuity test fixture to perform the continuity test. The Dielectric Withstanding Voltage test ***shall*** be conducted after the continuity test to verify plug compliance.

Figure 3-70 Example Wrenching Strength Test Fixture for Plugs without Overmold



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Figure 3-71 Reference Wrenching Strength Continuity Test Fixture



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- The plug ***shall*** disengage from the test fixture or demonstrate mechanical failure (i.e., the force applied during the test procedure peaks and drops off) when a moment of 2.0 Nm is applied to the plug in the up and down directions and a moment 3.5 Nm is applied to the plug in the left and right directions. A new plug is required for each of the four test directions. An example of the mechanical failure point and an illustration of the wrenching test fixture are shown in Figure 3-72 and Figure 3-73, respectively.

Figure 3-72 Example of Wrenching Strength Test Mechanical Failure Point

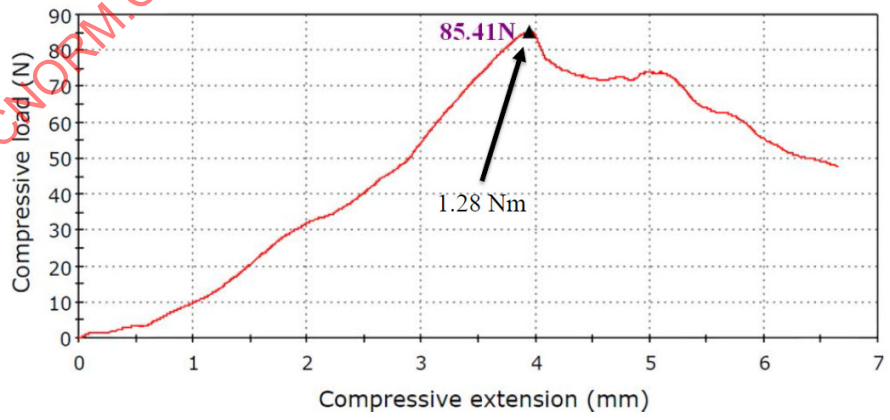
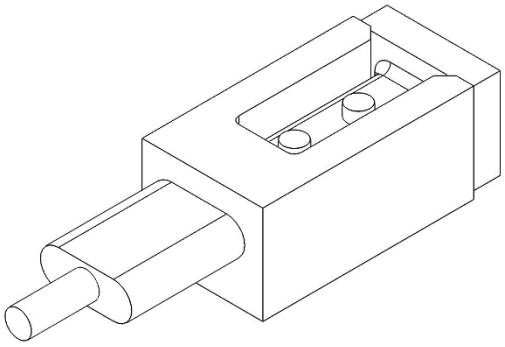


Figure 3-73 Wrenching Strength Test with Cable in Fixture



3.8.1.8 Restriction of Hazardous Substances

It is recommended that components be RoHS compliant.

3.8.2 Environmental Requirements

The connector interface environmental tests ***shall*** follow EIA 364-1000.01, Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications.

Since the connector defined has more than 0.127 mm wipe length, Test Group 6 in EIA 364-1000.01 is not required. The temperature life test duration and the mixed flowing gas test duration values are derived from EIA 364-1000.01 based on the field temperature per the following.

Table 3-39 Environmental Test Conditions

Temperature Life test temperature and duration	105 °C for 120 hours
Temperature Life test temperature and duration for preconditioning	105 °C for 72 hours
Mixed flowing gas test duration	7 days

The pass/fail criterion for the low-level contact resistance (LLCR) is as defined in Section 3.7.8.1. The durability ratings are defined in Section 3.8.1.3.

3.8.2.1 Reference Materials (*Informative*)

This specification does not specify materials for connectors and cables. Connector and cable manufacturers ***should*** select appropriate materials based on performance requirements. The information below is provided for reference only.

Note: Connector and cable manufacturers ***should*** comply with contact plating requirements per the following options:

Option I

Receptacle: Contact area: (Min) 0.05 µm Au + (Min) 0.75 µm Ni-Pd on top of (Min) 2.0 µm Ni

Plug: Contact area: (Min) 0.05 µm Au + (Min) 0.75 µm Ni-Pd on top of (Min) 2.0 µm Ni

Option II

Receptacle: Contact area: (Min) 0.75 µm Au on top of (Min) 2.0 µm Ni

Plug: Contact area: (Min) 0.75 µm Au on top of (Min) 2.0 µm Ni

Other reference materials that connector and cable manufacturers select based on performance parameters listed in Table 3-40 are for reference only.

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Table 3-40 Reference Materials

Component	Material
Cable	Conductor: copper with tin or silver plating
	SDP Shield: AL foil or AL/mylar foil
	Coaxial shield: copper strand
	Braid: Tin plated copper or aluminum
	Jacket: PVC or halogen free substitute material
Cable Overmold	Thermoset or thermoplastic
Connector Shells	Stainless steel or phosphor bronze
Plug Side Latches	Stainless steel
Receptacle Mid-Plate	Stainless steel
Plug Internal EMC Spring	Stainless steel or high yield strength copper alloy
Receptacle EMC Pad	Stainless steel or phosphor bronze
Receptacle Shell	Stainless steel or phosphor bronze
Receptacle Tongue	Glass-filled nylon
Housing	Thermoplastics capable of withstanding lead-free soldering temperature
Note: Halogen-free materials ***should*** be considered for all plastics	

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3.9 Docking Applications (*Informative*)

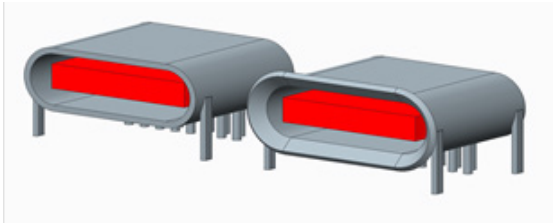
In this specification, docking refers to plugging a device directly into a dock without using a cable assembly. The USB Type-C connector is defined to support such applications.

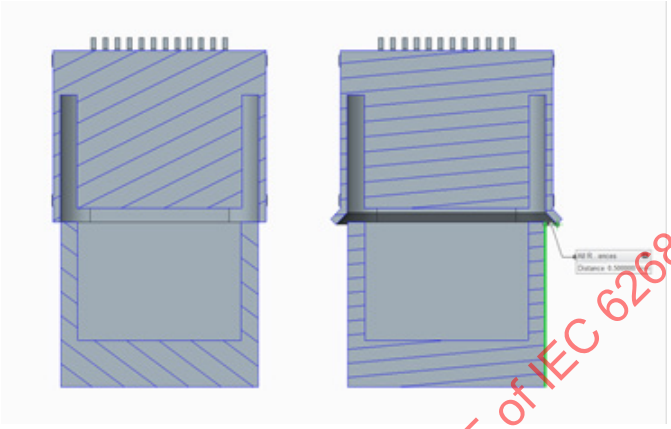
The connector is only part of a docking solution. A complete docking solution at the system level ***may*** also include retention or locking mechanisms, alignment mechanisms, docking plug mounting solutions, and protocols supported through the connector. This specification does not attempt to standardize system docking solutions, therefore there is no interoperability requirement for docking solutions.

The following list includes the requirements and guidelines when using the USB Type-C connector for docking:

1. The USB Type-C plug used for docking ***shall*** work with compliant USB Type-C receptacle. It ***shall*** comply with all dimensional, electrical, and mechanical requirements.
2. If the plug on the dock does not include the side latches, then the dock ***should*** provide a retention or locking mechanism to secure the device to the plug. The retention latches also serve as one of the ground return paths for EMC. The docking design ***should*** ensure adequate EMC performance without the side latches if they are not present.
3. The internal EMC fingers are not required for the docking plug as long as the receptacle and plug shells have adequate electrical connection.
4. Alignment is critical for docking. Depending on system design, standard USB Type-C connectors alone ***may not*** provide adequate alignment for mating. System level alignment is highly recommended. Alignment solutions are implementation-specific.
5. Fine alignment is provided by the connector. The receptacle front face ***may*** have lead-in features for fine alignment. Figure 3-74 shows an example of a USB Type-C receptacle with a lead-in flange compared to a receptacle without the flange.

Figure 3-74 USB Type-C Cable Receptacle Flange Example





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3.10 Implementation Notes and Design Guides

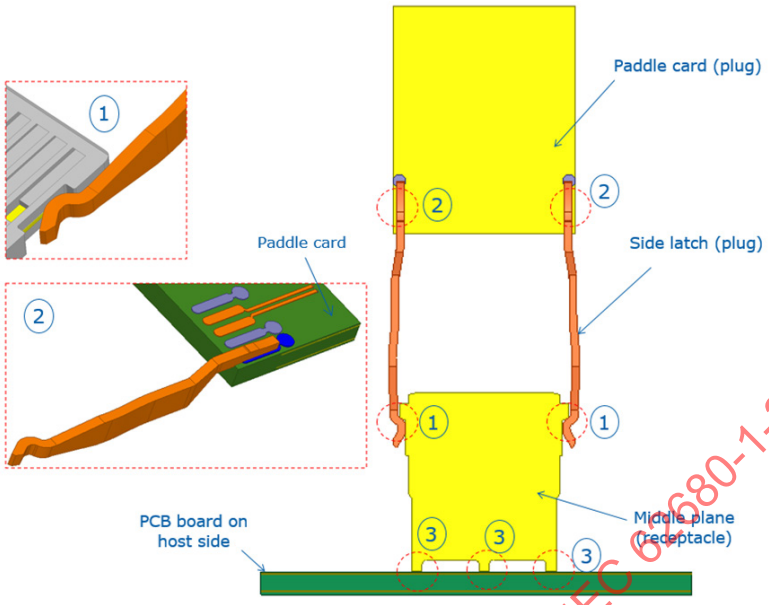
This section discusses a few implementation notes and design guides to help users design and use the USB Type-C connectors and cables.

3.10.1 EMC Management (*Informative*)

Connector and cable assembly designers, as well as system implementers ***should*** pay attention to receptacle and cable assembly shielding to ensure a low-impedance grounding path. The following are guidelines for EMC management:

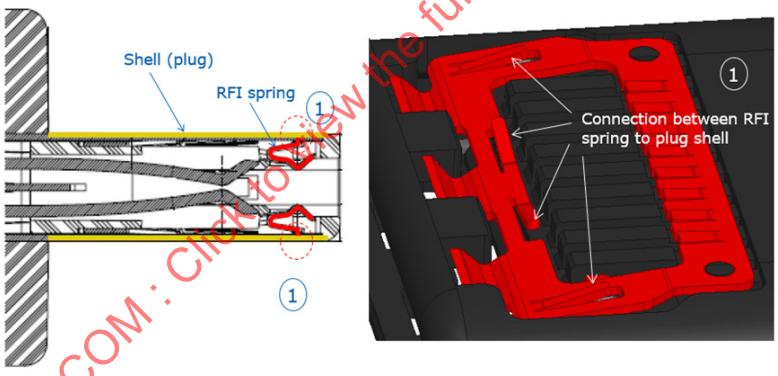
- The quality of raw cables ***should*** be ensured. The intra-pair skew or the differential to common mode conversion of the TX/RX pairs has a significant impact on cable EMC and ***should*** be controlled within the limits of this specification.
- The cable external braid ***should*** be physically connected to the plug metal shell as close to 360° as possible to control EMC. Without appropriate shielding termination, even a perfect cable with zero intra-pair skew ***may*** not meet EMC requirements. Copper tape ***may*** be needed to shield off the braid termination area.
- The wire termination contributes to common-mode noise. The breakout distance for the wire termination ***should*** be kept as small as possible to optimize EMC and signal integrity performance. If possible, symmetry ***should*** be maintained for the two lines within a differential pair.
- Besides the mechanical function, the side latches on the plug and the mid-plate in the receptacle also play a role for EMC. This is illustrated in Figure 3-75:
    1. The side latch ***should*** have electrical connection to the receptacle mid-plate (a docking plug ***may not*** have side latches).
    2. The side latches ***should*** be terminated to the paddle card GND plane inside the plug.
    3. The mid-plate ***should*** be directly connected to system PCB GND plane with three or more solder leads/tails.

Figure 3-75 EMC Guidelines for Side Latch and Mid-Plate



- The internal RFI finger inside the plug ***should*** have adequate connection points to the inner surface of the plug shell. Four or more connection points are recommended as illustrated in Figure 3-76.

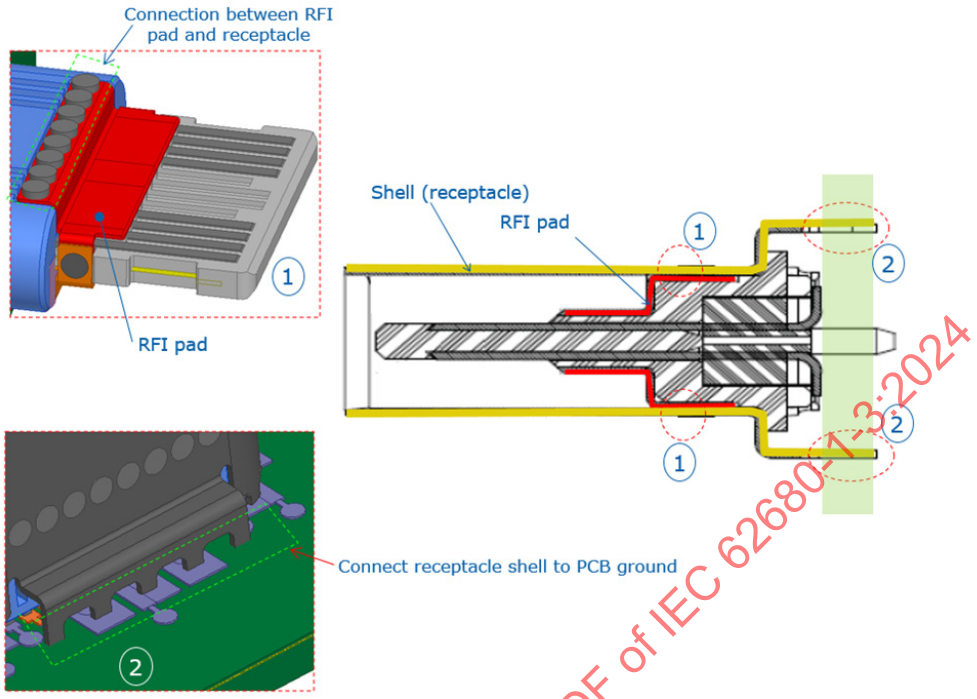
Figure 3-76 EMC Finger Connections to Plug Shell



- The EMC fingers inside the plug mates with the EMC pad in the receptacle. It is important for the EMC pad to have adequate connections to the receptacle shell. As illustrated in Figure 3-77, there are multiple laser welding points between the EMC pads and the receptacle shell, top and bottom.
- The receptacle shell ***should*** have sufficient connection points to the system PCB GND plane with apertures as small as possible. Figure 3-77 illustrates an example with multiple solder tails to connect the receptacle shell to system PCB GND.

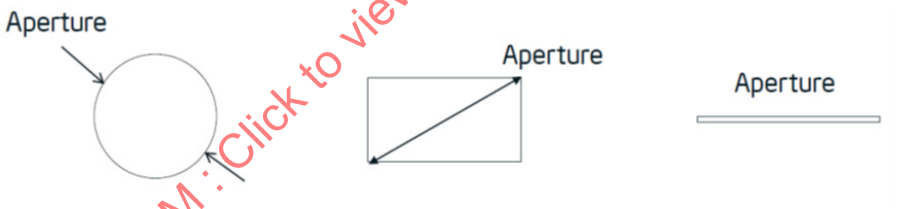
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Figure 3-77 EMC Pad Connections to Receptacle Shell



- Apertures in the receptacle and plug shells ***should*** be minimized. If apertures are unavoidable, a maximum aperture size of 1.5 mm is recommended. See Figure 3-78 for aperture illustrations. Copper tape ***may*** be applied to seal the apertures inside the cable plug.

Figure 3-78 Examples of Connector Apertures



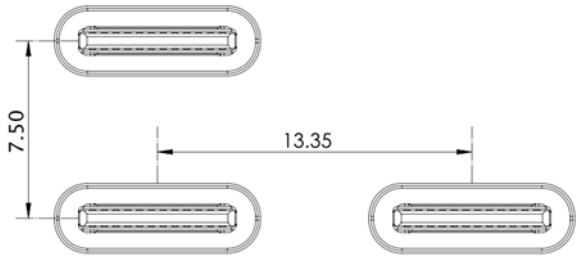
- The receptacle connectors ***should*** be connected to metal chassis or enclosures through grounding fingers, screws, or any other way to manage EMC.

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3.10.2 Stacked and Side-by-Side Connector Physical Spacing (*Informative*)

Stacked and side-by-side USB connectors are commonly used in PC systems. Figure 3-79 illustrates the recommended spacing between connectors for stacked and side-by-side configurations.

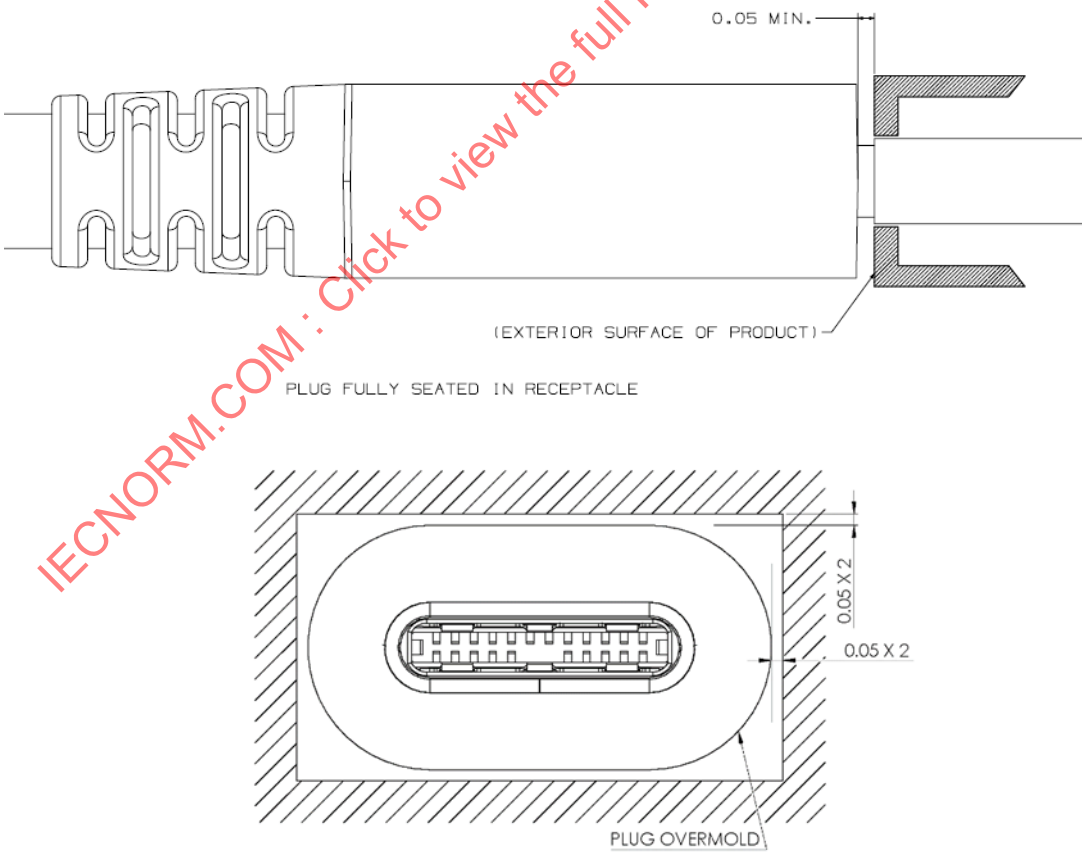
Figure 3-79 Recommended Minimum Spacing between Connectors



3.10.3 Cable Mating Considerations (*Informative*)

The receptacle mounting location, exterior product surfaces, cable overmold, and plug mating length need to be considered to ensure the USB Type-C plug is allowed to fully engage the USB Type-C receptacle. Figure 3-80 illustrates the recommended minimum plug overmold clearance to avoid interference between the plug overmold and enclosure opening, allowing the cable plug to fully seat in the product receptacle.

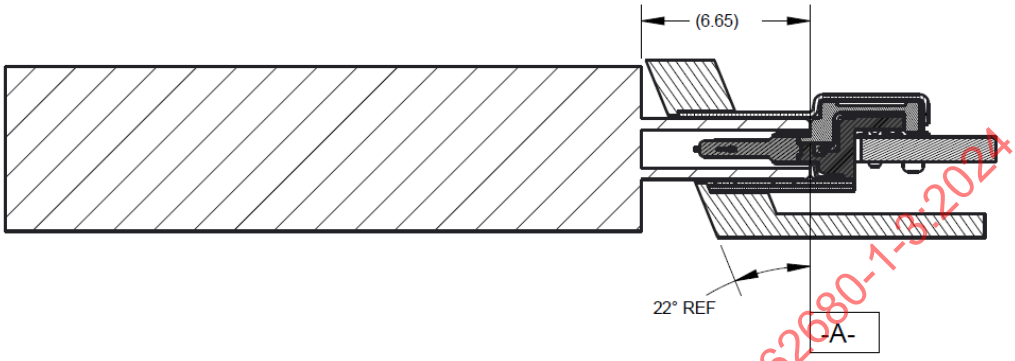
Figure 3-80 Recommended Minimum Plug Overmold Clearance



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Figure 3-81 illustrates special considerations required when external walls are angled. For such applications, the USB Type-C receptacle shell ***may not*** provide as much mechanical alignment protection to the receptacle tongue as in the full shell design. Design options to allow the receptacle to pass mechanical test requirements include relief in the exterior wall surface to allow use of a full shell receptacle or use of a receptacle specifically designed for the application.

Figure 3-81 Cable Plug Overmold and an Angled Surface



3.11 Extended Power Range (EPR) Cables

3.11.1 Electrical Requirements

Extended Power Range cables have additional requirements to assure that these cables can deliver the full defined voltage and current range for ***USB PD*** EPR operation.

EPR cables ***shall*** functionally support a reported 50 V and 5 A operation. The minimum functional voltage that a cable ***shall*** support is 50.9 V. The electrical components potentially in the path of V_{BUS} in an EPR cable, e.g., bypass capacitors, ***should*** be minimally rated for 63 V.

See Appendix H for information about ***USB PD*** high-voltage design and mitigating arcing damage during cable withdrawal.

3.11.2 EPR Cable Identification Requirements

All EPR cables ***shall*** be Electronically Marked and include EPR-specific information in the eMarker as defined by the ***USB PD*** specification. As defined in the ***USB PD*** specification, EPR cables are marked as 50 V and 5 A capable.

Refer to Sections 3.4.1.1 and 3.4.2.1 regarding cable certification and identification.

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4 Functional

This chapter covers the functional requirements for the signaling across the USB Type-C® cables and connectors. This includes functional signal definition, discovery and configuration processes, and power delivery.

4.1 Signal Summary

Table 4-1 summarizes the list of signals used on the USB Type-C connectors.

Table 4-1 USB Type-C List of Signals

Signal Group	Signal	Description
USB 3.2 / ***USB4***	**TXp1, TXn1** **RXp1, RXn1** **TXp2, TXn2** **RXp2, RXn2**	Both the ***USB 3.2*** SuperSpeed USB and ***USB4*** serial data interfaces defines 1 differential transmit pair and 1 differential receive pair per lane. On a USB Type-C receptacle, two sets of signal pins are defined to support dual-lane operation and enable plug flipping feature.
USB 2.0	**Dp1, Dn1** **Dp2, Dn2**	***USB 2.0*** serial data interface defines a differential pair. On a USB Type-C receptacle, two set of ***USB 2.0*** signal pins are defined to enable plug flipping feature.
Configuration	**CC1, CC2** (receptacle) **CC** (plug)	CC channel in the plug used for connection detect, interface configuration and VCONN.
Auxiliary signals	**SBU1, SBU2**	Sideband Use. For ***USB4***, these signals are used for SBTX and SBRX.
Power	**VBUS**	USB cable bus power
	VCONN (plug)	USB plug power
	GND	USB cable return current path

4.2 Signal Pin Descriptions

4.2.1 *USB 3.2*/*USB4* Pins

TXp1, TXn1
TXp2, TXn2

These pins are required to implement the system's transmit path of either a ***USB 3.2*** SuperSpeed or ***USB4*** TX/RX interface. The transmitter differential pair in a port are routed to the receiver differential pair in the port at the opposite end of the path. Depending on the established connection, the ***USB 3.2*** Specification or ***USB4*** Specification defines all electrical characteristics, enumeration, protocol, and management features for this interface.

Two pairs of pins are defined to enable dual-lane operation – see Section 4.5.1.1 for further definition.

RXp1, RXn1
RXp2, RXn2

These pins are required to implement the system's receive path of a ***USB 3.2*** SuperSpeed or ***USB4*** TX/RX interface. The receiver differential pair in a port are routed to the transmitter differential pair in the port at the opposite end of the path. Depending on the established connection, the ***USB 3.2*** Specification or ***USB4*** Specification defines all electrical characteristics, enumeration, protocol, and management features for this interface.

Two pairs of pins are defined to enable dual-lane operation – see Section 4.5.1.1 for further definition.

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4.2.2 *USB 2.0* Pins

Dp1, Dn1 (Dp2, Dn2)	These pins are required to implement ***USB 2.0*** functionality. ***USB 2.0*** in all three modes (LS, FS, and HS) is supported. The ***USB 2.0*** Specification defines all electrical characteristics, enumeration, and bus protocol and bus management features for this interface. Two pairs of pins are defined to enable the plug flipping feature – see Section 4.5.1.1 for further definition.

4.2.3 Auxiliary Signal Pins

SBU1, SBU2	These pins are assigned to sideband use. For ***USB4***, these signals are used for SBTX and SBRX. Refer to Section 4.3 for the functional requirements.

4.2.4 Power and Ground Pins

VBUS	These pins are for USB cable bus power as defined by the USB specifications. VBUS is only present when a Source-to-Sink connection across the CC channel is present – see Section 4.5.1.2.1. Refer to Section 4.4.2 for the functional requirements for VBUS.
VCONN	VCONN is applied to the unused CC pin to supply power to the local plug. Refer to Section 4.4.3 for the functional requirements for VCONN.
GND	Return current path.

4.2.5 Configuration Pins

CC1, CC2, CC	These pins are used to detect connections and configure the interface across the USB Type-C cables and connectors. Refer to Section 4.5 for the functional definition. Once a connection is established, CC1 or CC2 will be reassigned for providing power over the VCONN pin of the plug – see Section 4.5.1.2.1.

4.3 Sideband Use (SBU)

The Sideband Use pins (SBU1 and SBU2) are limited to the uses as defined by this specification and additional functionality defined in the ***USB4*** Specification. See Appendix E for use of the SBU pins in ***Alternate Modes***.

The SBU pins on a port ***shall*** either be open circuit or have a weak pull-down to ground no stronger than ***zSBUTermination*** when in ***USB 3.2*** or ***USB 2.0***.

These pins are pre-wired in the standard USB Full-Featured Type-C cable as individual single-ended wires (SBU_A and SBU_B). Note that SBU1 and SBU2 are cross-connected in the cable.

When operating in ***USB4***, these pins are used as the ***USB4*** Sideband Channel with SBU1 mapping to SBTX and SBU2 mapping to SBRX. SBTX and SBRX functional requirements are as defined in the ***USB4*** specification. When a port determines that the locally-inserted plug is flipped (i.e., CC1 is open, CC2 is terminated), the ***USB4*** specification (reference Sideband Channel Lane Reversal) dictates that the port flip the SBTX and SBRX mappings to SBU1 and SBU2 in order to assure proper sideband transmit-to-receive end-to-end operation.

4.4 Power and Ground

4.4.1 IR Drop

The maximum allowable cable IR drop for ground (including ground on a captive cable) ***shall*** be 250 mV and for VBUS ***shall*** be 500 mV through the cable to the cable's maximum rated VBUS current capacity. When VCONN

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is being sourced, the IR drop for the ground ***shall*** still be met considering any additional VCONN return current.

Figure 4-1 illustrates what parameters contribute to the IR drop and where it ***shall*** be measured. The IR drop includes the contact resistance of the mated plug and receptacles at each end.

Figure 4-1 Cable IR Drop

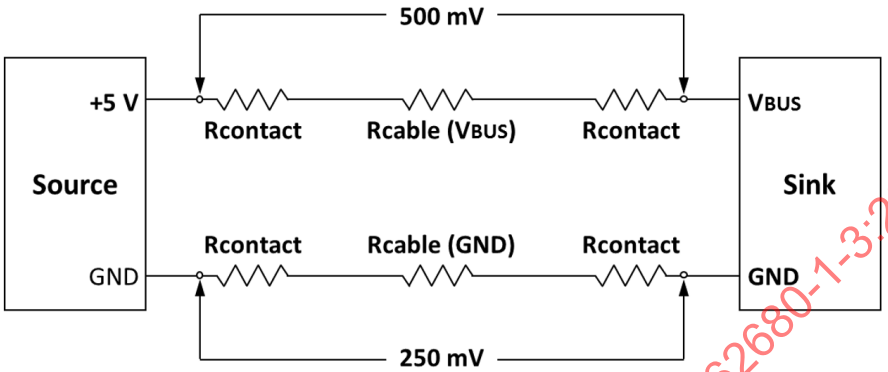
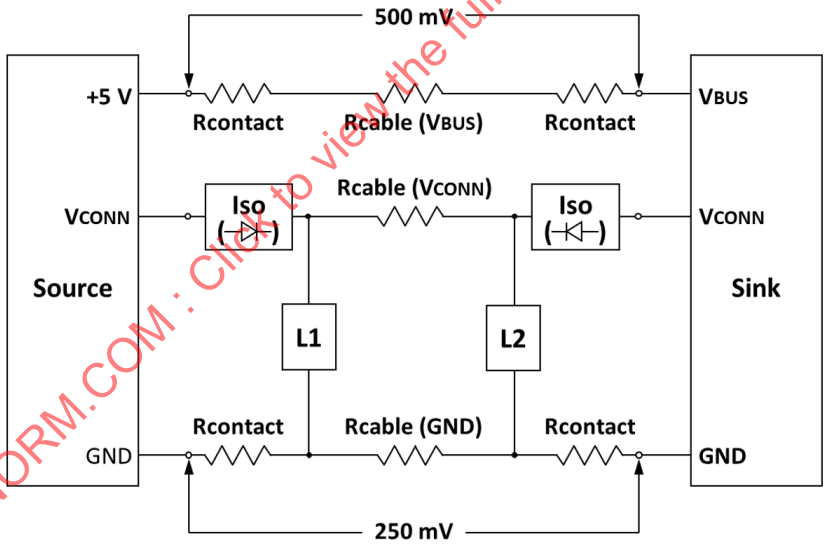


Figure 4-2 illustrates what parameters contribute to the IR drop for a powered cable and where it ***shall*** be measured. Note that the powered cable includes isolation elements (Iso) and loads (L1 and L2) for the functions in the powered cable such as ***USB PD*** controllers. The IR drop ***shall*** remain below 250 mV in all cases.

Figure 4-2 Cable IR Drop for powered cables



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4.4.2 VBUS

The allowable default range for VBUS as measured at the Source receptacle ***shall*** be as defined by the ***USB 2.0*** and ***USB 3.2*** specifications. For ***USB4***, the ***USB 3.2*** specification is used for this requirement. NOTE that due to higher currents allowed, legacy devices ***may*** experience a higher voltage (up to 5.5V maximum) at light loads.

The Source's USB Type-C receptacle VBUS pin ***shall*** remain unpowered and ***shall*** limit the capacitance between VBUS and GND as specified in Table 4-2 until a Sink is attached. The VBUS pin ***shall*** return to the unpowered state when the Sink is detached. See Table 4-32 for VBUS timing values. Legacy hosts/chargers

that by default source VBUS when connected using any legacy USB connector (Standard-A, Micro-B, etc.) to USB Type-C cable or adapter are exempted from these two requirements.

A DRP or Source (or device with Accessory Support) implementing an ***Rp*** pull-up as its method of connection detection ***shall*** provide an impedance between VBUS and GND on its receptacle pins as specified in Table 4-2 when not sourcing power on VBUS (i.e., when in states ***Unattached.SRC*** or ***Unattached.Accessory***).

Table 4-2 VBUS Source Characteristics

	Minimum	Maximum	Notes
VBUS Leakage Impedance	72.4 kΩ		Leakage between VBUS pins and GND pins on receptacle when VBUS is not being sourced.
VBUS Capacitance		3000 µF	Capacitance for source-only ports between VBUS and GND pins on receptacle when VBUS is not being sourced.
		10 µF	Capacitance for DRP ports between VBUS and GND pins on receptacle when VBUS is not being sourced.

Table 4-3 specifies VBUS Sink characteristics with regard to disconnect behavior based on monitoring VBUS. Sinks ***may*** monitor the CC pin for the removal of ***Rp*** by the Source as an additional indication of disconnect.

Table 4-3 VBUS Sink Characteristics

	Minimum	Maximum	Notes
tSinkDisconnect		40 ms	Time limit for transition from ***Attached.SNK*** to ***Unattached.SNK***
vSinkDisconnect[1]	0.8 V	3.67 V	Threshold used for transition from ***Attached.SNK*** to ***Unattached.SNK*** when VBUS is 5 V. This also applies for ***USB PD*** contracts at 5 V. For ***USB PD*** contracts at 5 V, the Sink ***shall*** take IR drop and margin into account when selecting this threshold.
		PPS_APDO_Min_Voltage * 0.95	Threshold used for transition from ***Attached.SNK*** to ***Unattached.SNK***. This applies for ***USB PD*** PPS contracts for RDO Output Voltage less than or equal to 5 V. This also applies for ***USB PD*** PPS contracts operating in the Current Limit mode. The Sink ***shall*** take IR drop and margin into account when selecting this threshold.
vSinkPD_min[1]		vNew – 750 mV + vValid	The minimum valid VBUS voltage seen by sink when negotiated through ***USB PD***. vNew = vSrcNew (min) or vPpsNew (min) as defined in ***USB PD***. 750 mV= 500 mV + 250 mV (maximum IR drop) vValid = vSrcValid (min) or vPpsValid (min) as defined in ***USB PD***.
vSinkDisconnectPD[1]	90% of ***vSinkPD_min***	***vSinkPD_min***	VBUS disconnect threshold when VBUS voltage was negotiated through ***USB PD*** to a value above 5 V. This applies for ***USB PD*** PPS contracts for RDO Output Voltage above 5 V. This also applies for ***USB PD*** PPS contracts operating in the Constant Voltage mode.
VBUS Capacitance		10 µF	Capacitance between VBUS and GND pins on receptacle when not in ***Attached.SNK***.

Note 1: See Section 4.5.2.2.5.2 with regard to applicability of this requirement.

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4.4.3 VCONN

VCONN is provided by the Source to power cables with electronics in the plug. VCONN is provided over the CC pin that is determined not to be connected to the CC wire of the cable.

Initially, VCONN is sourced on Source USB Type-C receptacles based on the ***Attached.SRC*** requirements in Section 4.5.2.2.9.1. Subsequently, if VCONN is not explicitly required by the cable or device as indicated in its eMarker, VCONN ***may*** be removed as described in Table 4-4. ***USB PD VCONN_Swap*** command also provides the Source a means to request that the attached Sink source VCONN.

Table 4-4 USB Type-C Source Port's VCONN Requirements Summary

D+/D–	TX/RX, VPD	> 3 A	VCONN Requirements
No	No	No	Not required to source VCONN
Yes	No	No	Not required to source VCONN
Yes	Yes	No	Required to source 1 W for x1 implementations and 1.5 W for x2 implementations. If after reading the cable's eMarker, the Source has determined that the cable is not a ***VPD*** and the Cable Termination Type field is 00b, it ***may*** remove VCONN power.
No	No	Yes	Required to source 100 mW. VCONN power ***may*** be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity.
Yes	No	Yes	Required to source 100 mW. VCONN power ***may*** be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity.
Yes	Yes	Yes	Required to source 1 W for x1 implementations and 1.5 W for x2 implementations. If after reading the cable's eMarker, the Source has determined the cable's current carrying capacity and the cable is not a ***VPD*** and the Cable Termination Type field is 00b, it ***may*** remove VCONN power.

Table 4-5 provides the voltage and power requirements that ***shall*** be met for VCONN. See Section 4.9 for more details about Electronically Marked Cables. See Appendix E regarding ***optional*** support for an increased VCONN power range in ***Alternate Modes***.

Table 4-5 VCONN Source Characteristics

	Minimum	Maximum	Notes
vVCONNValid	3.0 V	5.5 V	The voltage range over which VCONN is considered valid.
Power for Sources with TX/RX Signals	x1 1 W		Source ***may*** latch-off VCONN if excessive power is drawn beyond the specified inrush and mode wattage. Source ***may*** disable VCONN per Table 4-4. Alternate modes ***may*** require higher power.
	x2 1.5 W		
Power for Sources with VPD support	1 W		Source ***may*** latch-off VCONN if excessive power is drawn beyond the specified inrush and mode wattage.
Power for Sources in USB Suspend or without TX/RX Signals	100 mW		Minimum power Source must provide in USB Suspend or without TX/RX signals.[1] Source ***may*** disable VCONN per Table 4-4.
Rdch	30 Ω	6120 Ω	Discharge resistance applied in ***UnattachedWait.SRC*** between the CC pin being discharged and GND.

Note 1: During transition from U3 to U0, VCONN Source ***shall*** provide up to max U0 power.

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To aid in reducing the power associated with supplying VCONN, a Source is allowed to either not source VCONN or turn off VCONN under any of the following conditions:

- ***Ra*** is not detected on the CC pin after ***tCCDebounce*** when the other CC pin is in the ***SRC.Rd*** state, or
- if there is no GoodCRC response to ***USB PD Discover Identity*** messages sent to SOP'.

If the power source used to supply VCONN power is a shared power source for other USB VCONN and VBUS outputs, it must be bypassed with capacitance identical to the VBUS capacitance requirements of ***USB 3.2*** Section 11.4.4 – Dynamic Attach and Detach. Any VCONN power source bypass capacitance must be isolated from the CC pins when VCONN is not being provided.

Table 4-6 provides the requirements that ***shall*** be met for cables that consume VCONN power.

Table 4-6 Cable VCONN Sink Characteristics

	Minimum	Maximum	Notes
Voltage	3.0 V	5.5 V	Voltage range (vVCONNValid) when VCONN is valid.
Inrush Capacitance		10 µF	A cable ***shall not*** present more than the equivalent inrush capacitance to the VCONN source. The active cable is responsible for discharging its capacitance.
Power for Electronically Marked Passive Cables		20 mW	See Section 4.9. Measured with no ***USB PD*** traffic at least ***tRaWeaken*** after VCONN applied. Note: 75mW max allowed for the first ***tRaWeaken*** after VCONN applied.
***USB 3.2* Power for Active Cables in U-states**		See Table 6-6	U0, U1, U2, U3, Rx.Detect, and eSS.Disabled.
tVCONNDischarge		230 ms	Time from cable disconnect to ***vVCONNDischarge*** met.
vVCONNDischarge		800 mV	VCONN voltage after ***tVCONNDischarge***
vVCONNDisconnect	1 V	2.4 V	Threshold used to detect VCONN disconnect.
iRaDetect		10 mA	The maximum current drawn from VCONN when the voltage is below vVCONNValid. Note: This current is below the 75 mW allowance for the first 500 ms at 5.5 V.
tRaReconnect		1 ms	Time from VCONN falling below ***vVCONNDisconnect*** at the cable plug until the cable has re-applied ***Ra***.
tRaWeaken	21 ms	1.2 s	Time from VCONN exceeding ***vVCONNDisconnect*** until the cable removes or weakens ***Ra***.
tVCONNSwitch		***tVCONNStable***	Cables that ***optionally*** use VBUS ***shall*** power from VCONN within ***tVCONNStable***.

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The cable ***shall*** remove or weaken ***Ra*** according to the state diagram behavior in 4.5.2.5. The cable ***shall*** reapply ***Ra*** according to the state diagram behavior in 4.5.2.5. The cable ***shall*** discharge VCONN to below ***vVCONNDischarge*** on a cable disconnect. The cable ***shall*** control ***Ra*** at each of its ends independently based on the VCONN on that end.

Implementation Note: Increasing ***Ra*** to 20KΩ will meet both the power dissipation for electronically marked passive cables and discharge 10µF to less than ***vVCONNDischarge*** in ***tVCONNDischarge***.

Table 4-7 VCONN-Powered Accessory (VPA) Sink Characteristics

	Minimum	Maximum	Notes
Voltage	3.0 V	5.5V	Voltage range (vVCONNValid) when VCONN is valid.
Inrush Capacitance		10 µF	An accessory ***shall not*** present more than the equivalent inrush capacitance to the VCONN source. The accessory is responsible for discharging its capacitance.
Power before Alternate Mode Entry		35 mW	Maximum power in USB suspend. Note: Power ***shall*** be reduced 5 seconds after VCONN is applied if no ***Alternate Mode*** Entry has occurred. A VCONN power cycle ***may*** be required to re-enable ***USB PD*** communication. Note: 75 mW max allowed for the first 500 ms after VCONN is applied.
tVCONNDischarge		230 ms	Time from ***VPA*** disconnect to ***vVCONNDischarge*** met.
vVCONNDischarge		800 mV	VCONN voltage after ***tVCONNDischarge***.
iRaDetect		10 mA	The maximum current drawn from VCONN when the voltage is below vVCONNValid. Note: This current is below the 75 mW allowance for the first 500 ms at 5.5 V.
vRaReconnect	800 mV		Voltage at which the ***VPA shall*** reapply ***Ra*** on the falling edge of VCONN.
tRaWeaken		1.2 s	Time from VCONN exceeding ***vVCONNDisconnect*** until the ***VPA*** removes or weakens ***Ra***.
vVCONNDisconnect	1 V	2.4 V	Threshold used to detect VCONN disconnect.

The ***VPA shall*** remove or weaken ***Ra*** within ***tRaWeaken*** (as defined in Table 4-7) after VCONN enters the valid voltage range (***vVCONNValid***).

The ***VPA shall*** reapply ***Ra*** when VCONN falls below vRaReconnect as defined in Table 4-7. The ***VPA shall*** discharge VCONN to below ***vVCONNDischarge*** within ***tVCONNDischarge*** on a cable disconnect. The ***VPA shall*** consider the VCONN capacitance present in the accessory when discharging VCONN.

The maximum power consumption while in an ***Alternate Mode*** is defined by the specification specific to the ***Alternate Mode*** being used.

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Table 4-8 VCONN-Powered Device (VPD) Sink Characteristics

	Minimum	Maximum	Notes
Voltage	3.0 V	5.5V	Voltage range (vVCONNValid) when VCONN is valid.
Inrush Capacitance		10 µF	A device ***shall not*** present more than the equivalent inrush capacitance to the VCONN source. The device is responsible for discharging its capacitance.
Power before USB enumeration		35 mW	Maximum power in USB suspend. Note: 75 mW max allowed for the first 500 ms after VCONN is applied.
Power when active		500 mW (***USB 2.0***) 750 mW (***USB 3.2***)	A ***VPD*** ***shall*** only expose a low-power interface over USB.
tVCONNDischarge		230 ms	Time from ***VPD*** disconnect to ***vVCONNDischarge*** met.
vVCONNDischarge		800 mV	VCONN voltage after ***tVCONNDischarge***.
iRaDetect		10 mA	The maximum current drawn from VCONN when the voltage is below vVCONNValid. Note: This current is below the 75 mW allowance for the first 500 ms at 5.5 V.
vRaReconnect	800 mV		Voltage at which the ***VPD*** ***shall*** reapply ***Ra*** on the falling edge of VCONN.
tRaWeaken		1.2 s	Time from VCONN exceeding ***vVCONNDisconnect*** until the ***VPD*** removes or weakens ***Ra***.
vVCONNDisconnect	1 V	2.4 V	Threshold used to detect VCONN disconnect.

The ***VPD*** ***shall*** remove or weaken ***Ra*** within ***tRaWeaken*** (as defined in Table 4-8) after VCONN enters the valid voltage range (***vVCONNValid***).

The ***VPD*** ***shall*** reapply ***Ra*** when VCONN falls below vRaReconnect as defined in Table 4-8. The ***VPD*** ***shall*** discharge VCONN to below ***vVCONNDischarge*** within ***tVCONNDischarge*** on a cable disconnect. The ***VPD*** ***shall*** consider the VCONN capacitance present in the device when discharging VCONN.

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4.5 Configuration Channel (CC)

4.5.1 Architectural Overview

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection. When the device is connected through a hub, the connection between a Sink (UFP) on the hub and the Source (host port) and the connection between the Sink (device port) and a Source (DFP on the hub), are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes:

- Detect attach of USB ports, e.g., a Source to a Sink,
- Resolve cable orientation and twist connections to establish USB data bus routing,
- Establish data roles between two attached ports,
- Discover and configure VBUS: ***USB Type-C Current*** modes or ***USB Power Delivery***,
- Configure VCONN, and
- Discover and configure ***optional*** Alternate and Accessory modes.

4.5.1.1 USB Data Bus Interface and USB Type-C Plug Flip-ability

Since the USB Type-C plug can be inserted in either right-side-up or upside-down position, the hosts and devices that support USB data bus functionality must operate on the signal pins that are actually connected end-to-end. In the case of ***USB 2.0***, this is done by shorting together the two D+ signal pins and the two D– signal pins in the host and device receptacles. In the case of ***USB 3.2*** SuperSpeed USB or ***USB4*** TX/RX signals in a single-lane implementation, it requires the functional equivalent of a switch in both the host and device to appropriately route the TX and RX signal pairs to the connected path through the cable. For a ***USB 3.2*** SuperSpeed USB or ***USB4*** dual-lane implementation, the host and/or device resolves the lane ordering.

Figure 4-3 illustrates the logical data bus model for a USB Type-C-based Host connected to a USB Type-C-based Device that is only capable of SuperSpeed USB single-lane operation. The USB cable that sits between a host and device can be in one of four possible connected states when viewed by the host:

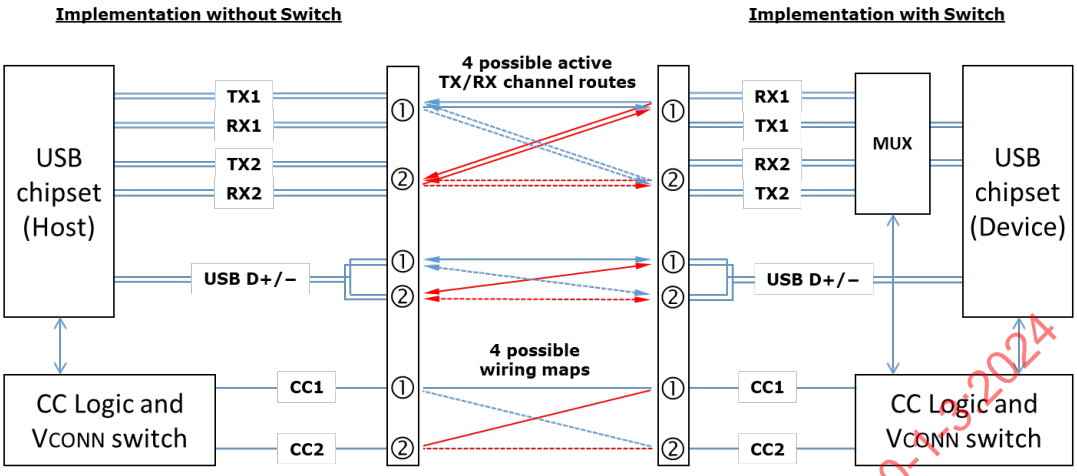
- Un-flipped straight through – Position ① ⇔ Position ①
- Un-flipped twisted through – Position ① ⇔ Position ②
- Flipped straight through – Position ② ⇔ Position ②
- Flipped twisted through – Position ② ⇔ Position ①

To establish the proper routing of the active USB data bus from host to device, the standard USB Type-C cable is wired such that a single CC wire is position aligned with the first TX/RX signal pairs (TXp1/TXn1 and RXp1/RXn1) – in this way, the CC wire and TX/RX data bus wires that are used for single-lane operational signaling within the cable track with regard to the orientation and twist of the cable. By being able to detect which of the CC pins (CC1 or CC2) at the receptacle is terminated by the device, the host is able to determine which TX/RX signals are to be used for the single-lane connection and the host can use this to control the functional switch for routing the TX/RX signal pairs. Similarly in the device, detecting which of the CC pins at the receptacle is terminated by the host allows the device to control the functional switch that routes its TX/RX signal pairs.

For a dual-lane implementation, the TX/RX signal pairs in the cable/plug aligned with the CC wire/pin is Lane 0 and in reference to ***USB 3.2***, ***shall*** be identified as the Configuration Lane. The second TX/RX signal pairs (TXp2/TXn2 and RXp2/RXn2) in the cable/plug is Lane 1 of a dual-lane configuration.

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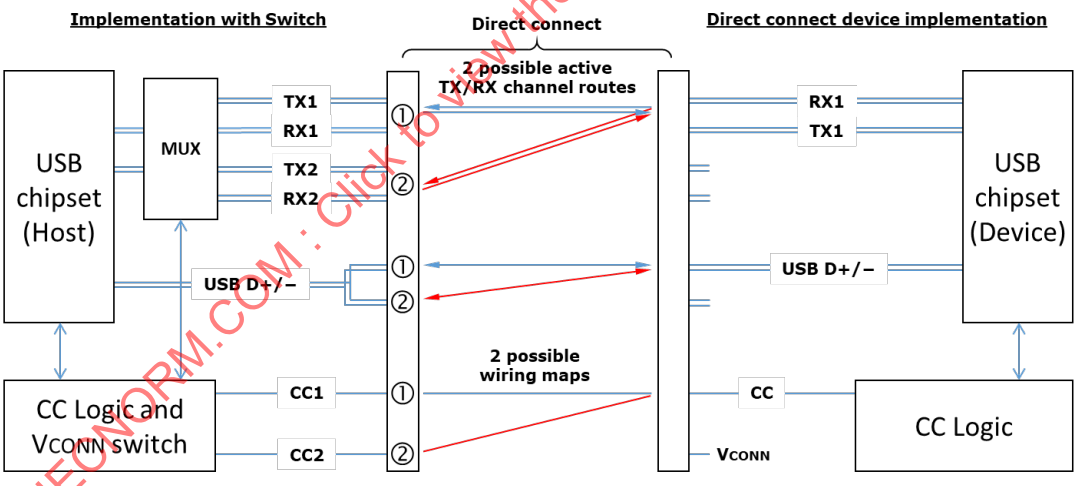
Figure 4-3 Logical Model for Single-Lane Data Bus Routing across USB Type-C-based Ports



While Figure 4-3 illustrates the functional model as a host connected to a device, this model equally applies to a USB hub's downstream ports as well.

Figure 4-4 illustrates the logical data bus model for a single-lane USB Type-C-based Device (implemented with a USB Type-C plug either physically incorporated into the device or permanently attached as a captive cable) connected directly to a USB Type-C-based Host. For the device, the location of the TX/RX data bus, ***USB 2.0*** data bus, CC and VCONN pins are fixed by design. Given that the device pin locations are fixed, only two possible connected states exist when viewed by the host.

Figure 4-4 Logical Model for USB Type-C-based Ports for a Single-Lane Direct Connect Device



The functional requirements for implementing TX/RX data bus routing for the USB Type-C receptacle are not included in the scope of this specification. There are multiple host, device and hub architectures that can be used to accomplish this which could include either discrete or integrated switching and could include merging this functionality with other ***USB 3.2*** or ***USB4*** design elements, e.g., a bus repeater.

The functional requirements for addressing SBU1 and SBU2 routing are not included in the scope of this specification. For ***USB4***, where SBTX and SBRX are mapped to SBU1 and SBU2, the adjustment to the mapping of these signals based on the connection state (flipped and/or twisted) of the cable is defined by the ***USB4*** Specification (reference Sideband Channel Lane Reversal).

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4.5.1.2 Connecting Sources and Sinks

Given that the USB Type-C receptacle and plug no longer differentiate host and device roles based on connector shape, e.g., as was the case with USB Type-A and Type-B connectors, any two ports that have USB Type-C receptacles can be connected together with a standard USB Type-C cable. Table 4-9 summarizes the expected results when interconnecting Source, Sink and DRP ports.

Table 4-9 USB Type-C Port Interoperability

	Source-Only	**Sink-Only**	**DRP (Dual-Role-Power)**
Source-Only	Non-functional	Functional	Functional
Sink-Only	Functional	Non-functional	Functional
DRP (Dual-Role-Power)	Functional	Functional	Functional[1]
Note 1: Resolution of roles ***may*** be automatic or manually driven.			

In the cases where no function results, neither port ***shall*** be harmed by this connection. The user has to independently realize the invalid combination and take appropriate action to resolve. While these two invalid combinations mimic traditional USB where host-to-host and device-to-device connections are not intended to work, the non-keyed USB Type-C solution does not prevent the user from attempting such interconnects. VBUS and VCONN ***shall not*** be applied by a Source (host) in these cases.

The typical flow for the configuration of the interface in the general USB case of a Source (Host) to a Sink (Device) is as follows:

1. Detect a valid connection between the ports (including determining cable orientation, Source/Sink and DFP/UFP relationship).
2. ***Optionally*** discover the cable's capabilities.
3. ***Optionally*** establish alternatives to traditional USB power (See Section 4.6.2).
    a. ***USB PD*** communication over CC for advanced power delivery negotiation.
    b. ***USB Type-C Current*** modes.
    c. ***USB BC 1.2***.
4. USB Device Enumeration.

For cases of Dual-Role-Power (DRP) ports connecting to either Source-only, Sink-only or another DRP, the process is essentially the same except that during the detecting a valid connection step, the DRP alternates between operating as a Source for detecting an attached Sink and presenting as a Sink to be detected by an attached Source. Ultimately this results in a Source-to-Sink connection.

4.5.1.2.1 Detecting a Valid Source-to-Sink Connection

The general concept for setting up a valid connection between a Source and Sink is based on being able to detect terminations residing in the product being attached.

To aid in defining the functional behavior of CC, a pull-up (***Rp***) and pull-down (***Rd***) termination model is used – actual implementation in hosts and devices ***may*** vary, for example, the pull-up termination could be replaced by a current source. Figure 4-5 and Figure 4-6 illustrates two models, the first based on a pull-up resistor in the Source and the second replacing this with a current source.

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Figure 4-5 Pull-Up/Pull-Down CC Model

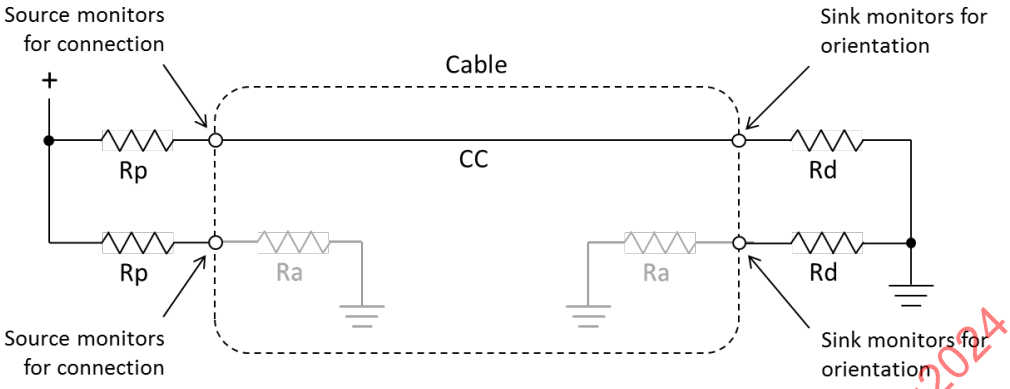
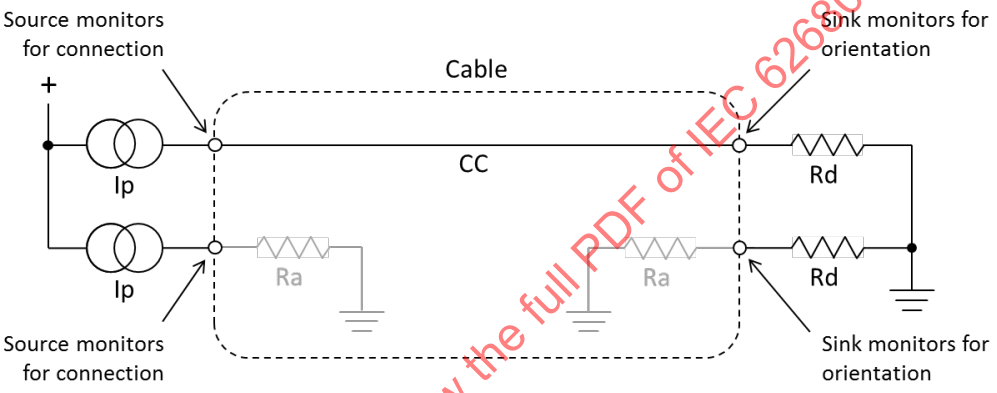


Figure 4-6 Current Source/Pull-Down CC Model



Initially, a Source exposes independent ***Rp*** terminations on its CC1 and CC2 pins, and a Sink exposes independent ***Rd*** terminations on its CC1 and CC2 pins, the Source-to-Sink combination of this circuit configuration represents a valid connection. To detect this, the Source monitors CC1 and CC2 for a voltage lower than its unterminated voltage – the choice of ***Rp*** is a function of the pull-up termination voltage and the Source's detection circuit. This indicates that either a Sink, a powered cable, or a Sink connected via a powered cable has been attached.

Prior to application of VCONN, a powered cable exposes ***Ra*** on its VCONN pin. ***Ra*** represents the load on VCONN plus any resistive elements to ground. In some cable plugs it might be purely resistive and in others it ***may*** be simply the load.

The Source has to be able to differentiate between the presence of ***Rd*** and ***Ra*** to know whether there is a Sink attached and where to apply VCONN. The Source is not required to source VCONN unless ***Ra*** is detected.

Two special termination combinations on the CC pins as seen by a Source are defined for specific modes: ***Ra***/***Ra*** for ***Liquid Corrosion Mitigation Mode*** (Appendix A) and ***Rd***/***Rd*** for ***Debug Accessory Mode*** (Appendix B).

The Source uses de-bounce timers to reliably detect states on the CC pins to de-bounce the connection (***tCCDebounce***) and hide ***USB PD*** BMC communications (***tPDDebounce***).

Table 4-10 summarizes the port state from the Source's perspective.

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Table 4-10 Source Perspective

CC1	CC2	State	Position
Open	**Open**	Nothing attached	***N/A***
Rd	**Open**	Sink attached	①
Open	**Rd**		②
Open	**Ra**	Powered cable without Sink attached or for ***Liquid Corrosion Mitigation Mode*** attached (Appendix A)	①
Ra	**Open**		②
Rd	**Ra**	Powered cable with Sink, ***VCONN-Powered Accessory*** (***VPA***), or ***VCONN-Powered USB Device*** (***VPD***) attached	①
Ra	**Rd**		②
Rd	**Rd**	***Debug Accessory Mode*** attached (Appendix B)	***N/A***
Ra	**Ra**	***Liquid Corrosion Mitigation Mode*** attached (Appendix A)	***N/A***

Once the Sink is powered, the Sink monitors CC1 and CC2 for a voltage greater than its local ground. The CC pin that is at a higher voltage (i.e., pulled up by ***Rp*** in the Source) indicates the orientation of the plug.

Table 4-11 summarizes the typical behaviors for simple Sources (Hosts) and Sinks (Devices) for each state in Table 4-10.

Table 4-11 Source (Host) and Sink (Device) Behaviors by State

State	Source Behavior	Sink Behavior
Nothing attached	• Sense CC pins for attach • Do not apply VBUS or VCONN	• Sense VBUS for attach
Sink attached	• Sense CC for orientation • Sense CC for detach • Apply VBUS and VCONN	• Sense CC pins for orientation • Sense loss of VBUS for detach
Powered cable without Sink attached	• Sense CC pins for attach • Do not apply VBUS or VCONN	• Sense VBUS for attach
Powered cable with Sink, *VCONN-Powered Accessory* (*VPA*), or *VCONN-Powered USB Device* (*VPD*) attached	• Sense CC for orientation • Sense CC for detach • Apply VBUS and VCONN • Detect ***VPD*** and remove VBUS	• If accessories or ***VPD***s are supported, see Source Behavior with exception that VBUS is not applied., otherwise, ***N/A***.
Debug Accessory Mode **attached**	• Sense CC pins for detach • Reconfigure for debug	• Sense VBUS for detach • Reconfigure for debug
Liquid Corrosion Mitigation Mode **attached**	• Sense CC pins for detach • Reconfigure for analog audio	• If accessories are supported, see Source Behavior, otherwise, ***N/A***

Figure 4-3 shows how the inserted plug orientation is detected at the Source's receptacle by noting on which of the two CC pins in the receptacle an ***Rd*** termination is sensed. Now that the Source (Host) has recognized

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that a Sink (Device) is attached and the plug orientation is determined, it configures the TX/RX data bus routing to the receptacle.

The Source (Host) then turns on VBUS. For the CC pin that does not connect Source-to-Sink through the cable, the Source supplies VCONN and ***may*** remove the termination. With the Sink (Device) now powered, it configures the USB data path. This completes the Host-to-Device connection.

The Source monitors the CC wire for the loss of pull-down termination to detect detach. If the Sink is removed, the Source port removes any voltage applied to VBUS and VCONN, resets its interface configuration and resumes looking for a new Sink attach.

Once a valid Source-to-Sink connection is established, alternatives to traditional USB power (VBUS as defined by either ***USB 2.0*** or ***USB 3.2*** specifications) ***may*** be available depending on the capabilities of the host and device. These include ***USB Type-C Current***, ***USB Battery Charging 1.2***, and ***USB Power Delivery***.

In the case where ***USB PD PR_Swap*** is used to swap the Source and Sink of VBUS, the supplier of VCONN remains unchanged during and after the VBUS power swap. The new Source monitors the CC wire and the new Sink monitors VBUS to detect detach. When a detach event is detected, any voltages applied to VBUS and VCONN are removed, each port resets its interface configuration and resumes looking for an attach event.

In the case where ***USB PD DR_Swap*** is used to swap the data roles (DFP and UFP), the source of VBUS and VCONN do not change after the data role swap.

In the case where ***USB PD VCONN_Swap*** is used to swap the VCONN source, the VBUS Source/Sink and DFP/UFP roles are maintained during and after the VCONN swap.

The last step in the normal USB Type-C connect process is for the USB device to be attached and enumerated per standard ***USB 2.0*** and ***USB 3.2*** processes.

4.5.1.3 Configuration Channel Functional Models

The functional models for the configuration channel behavior based on the CC1 and CC2 pins are described in this section for each port type: Source, Sink and Dual-Role-Power (DRP).

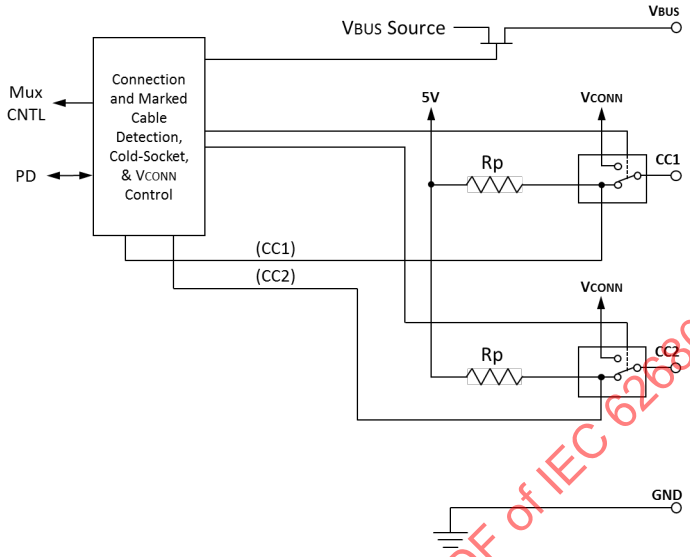
The figures in the following sections illustrate the CC1 and CC2 routing after the CC detection process is complete. In these figures, VBUS and VCONN ***may*** or ***may not*** actually be available.

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4.5.1.3.1 Source Configuration Channel Functional Model

Figure 4-7 illustrates the functional model for CC1 and CC2 for a Source port prior to attach. This illustration includes consideration for ***USB PD***.

Figure 4-7 Source Functional Model for CC1 and CC2



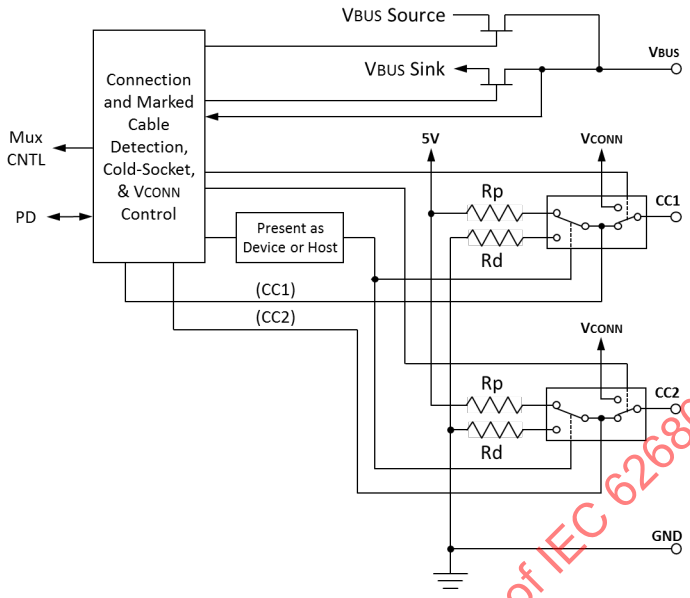
Referring to Figure 4-7, a port that behaves as a Source has the following functional characteristics:

1. The Source uses a FET to enable/disable power delivery across VBUS and initially the Source has VBUS disabled.
2. The Source supplies pull-up resistors (***Rp***) on CC1 and CC2 and monitors both to detect a Sink. The presence of an ***Rd*** pull-down resistor on either pin indicates that a Sink is being attached. The value of ***Rp*** indicates the initial ***USB Type-C Current*** level supported by the host.
3. The Source can ***optionally*** clamp the voltage on either of its CC pins. The minimum clamping voltage ***shall*** be ***vCC-Clamp***. The clamp is intended to protect the Source circuitry associated with CC functionality.
4. The Source uses the CC pin pull-down characteristic to detect and establish the correct routing for the USB TX/RX data path and determine which CC pin is intended for supplying VCONN.
5. Once a Sink is detected, the Source enables VBUS and VCONN.
6. The Source can dynamically adjust the value of ***Rp*** to indicate a change in available ***USB Type-C Current*** to a Sink.
7. The Source monitors the continued presence of ***Rd*** to detect Sink detach. When a detach event is detected, the Source removes, if supplied, VBUS and VCONN, and returns to step 2.
8. If the Source supports advanced functions (e.g., ***USB Power Delivery, USB4***, and ***Alternate Modes***), ***USB PD*** communication is required.

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Figure 4-8 illustrates the functional model for CC1 and CC2 for a Source that supports ***USB PD PR_Swap***.

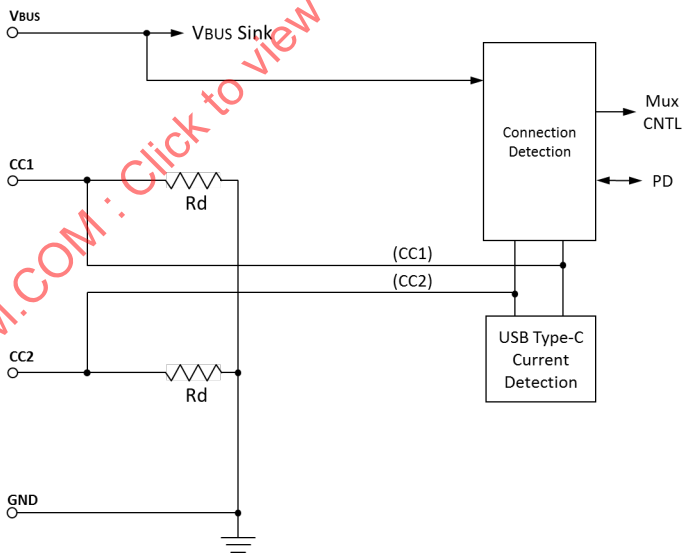
Figure 4-8 Source Functional Model Supporting *USB PD* PR_Swap



4.5.1.3.2 Sink Configuration Channel Functional Model

Figure 4-9 illustrates the functional model for CC1 and CC2 for a Sink. This illustration includes consideration for both ***USB Type-C Current*** and ***USB PD***.

Figure 4-9 Sink Functional Model for CC1 and CC2



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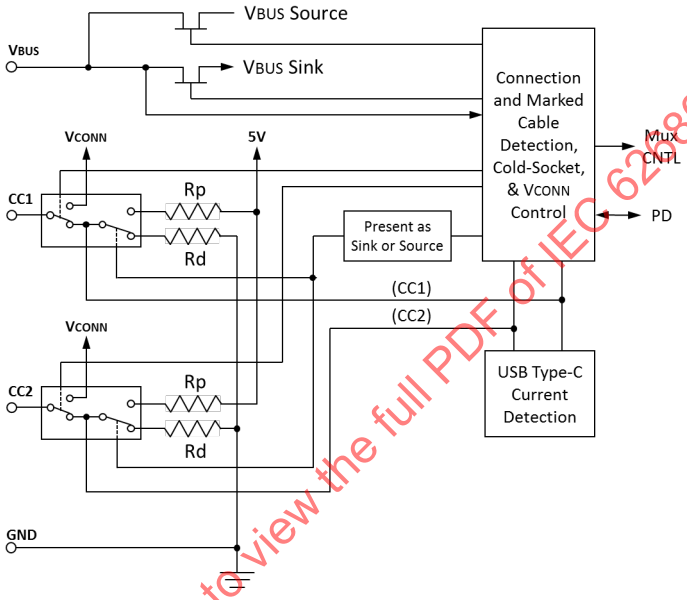
Referring to Figure 4-9, a port that behaves as a Sink has the following functional characteristics:

1. The Sink terminates both CC1 and CC2 to GND using pull-down resistors.
2. The Sink determines that a Source is attached by the presence of power on VBUS.
3. The Sink uses the CC pin pull-up characteristic to detect and establish the correct routing for the USB TX/RX data path.

4. The Sink can ***optionally*** monitor CC to detect an available higher ***USB Type-C Current*** from the Source. The Sink ***shall*** manage its load to stay within the detected Source current limit.
5. The Sink can ***optionally*** clamp the voltage on either of its CC pins. The minimum clamping voltage ***shall*** be ***vCC-Clamp***. The clamp is intended to protect the Sink circuitry associated with CC functionality.
6. If the Sink supports advanced functions (e.g., ***USB Power Delivery, USB4***, and ***Alternate Modes***), ***USB PD*** communication is required.

Figure 4-10 illustrates the functional model for CC1 and CC2 for a Sink that supports ***USB PD PR_Swap*** and supports ***USB PD VCONN_Swap*** prior to attach.

Figure 4-10 Sink Functional Model Supporting *USB PD* PR_Swap and VCONN_Swap

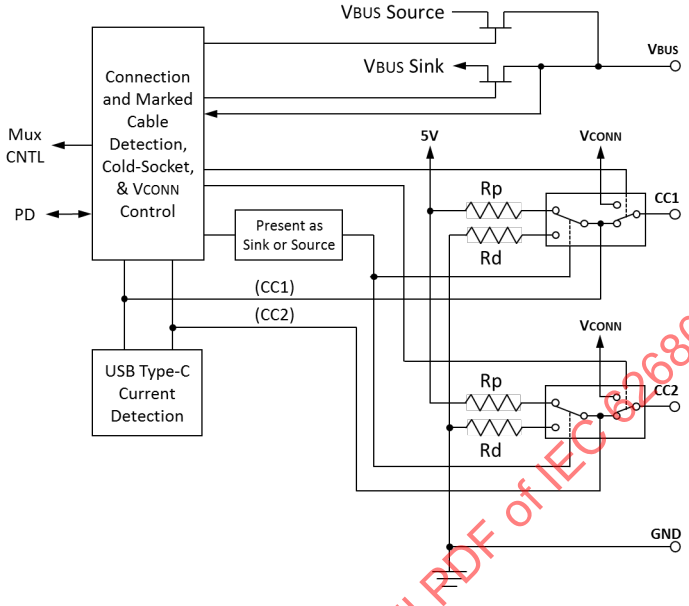


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4.5.1.3.3 Dual-Role-Power (DRP) Configuration Channel Functional Model

Figure 4-11 illustrates the functional model for CC1 and CC2 for a DRP presenting as a Source prior to attach. This illustration includes consideration for both the ***USB Type-C Current*** and the ***USB PD*** features.

Figure 4-11 DRP Functional Model for CC1 and CC2



Referring to Figure 4-11, a port that can alternate between DFP and UFP behaviors has the following functional characteristics:

1. The DRP uses a FET to enable/disable power delivery across VBUS and initially when in Source mode has VBUS disabled.
2. The DRP uses switches for presenting as a Source or Sink.
3. The DRP has logic used during initial attach to toggle between Source and Sink operation:
    a. Until a specific stable state is established, the DRP alternates between exposing itself as a Source and Sink. The timing of this process is dictated by a period (***tDRP***), percentage of time that a DRP exposes ***Rp*** (***dcSRC.DRP***) and role transition time (***tDRPTransition***).
    b. When the DRP is presenting as a Source, it follows Source operation to detect an attached Sink – if a Sink is detected, it applies VBUS, VCONN, and continues to operate as a Source (e.g., cease alternating).
    c. When the DRP is presenting as a Sink, it monitors VBUS to detect that it is attached to a Source – if a Source is detected, it continues to operate as a Sink (cease alternating).
4. If the DRP supports advanced functions (e.g., ***USB Power Delivery, USB4***, and ***Alternate Modes***), ***USB PD*** communication is required.

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4.5.1.4 USB Type-C Port Power Roles and Role Swapping Mechanisms

USB Type-C ports on products (USB hosts, USB devices, USB chargers, etc.) can be generally characterized as implementing one of seven power role behavioral models:

- Source-only
- Source (Default) – strong preference toward being a Source but subsequently capable of becoming a Sink using ***USB PD*** swap mechanisms.
- Sink-only

- Sink (Default) – strong preference toward being a Sink but subsequently capable of becoming a Source using ***USB PD*** swap mechanisms.
- DRP: Toggling (Source/Sink)
- DRP: Sourcing Device
- DRP: Sinking Host

Two independent sets of swapping mechanisms are defined for USB Type-C port implementations, one based on role swapping within the initial state machine connection process and the other based on subsequent use of ***USB PD***-based swapping mechanisms.

4.5.1.4.1 USB Type-C State-Machine-Based Role Swapping

During the initial USB Type-C state machine connection process, the products being connected end up in one of the two following roles associated with the termination of its port:

- ***Rp*** → VBUS and VCONN source and behaving as a downstream facing port (USB Host)
- ***Rd*** → VBUS sink and behaving as an upstream facing port (USB Device)

A USB Type-C DRP-based product ***may*** incorporate either or both the ***Try.SRC*** and ***Try.SNK*** swap mechanisms to affect the resulting role. ***Try.SRC*** allows a DRP that has a policy-based preference to be a Source when connecting to another DRP to affect a transition from a destined Sink role to the Source role. Alternately, ***Try.SNK*** allows a DRP that has a policy-based preference to be a Sink when connecting to another DRP to affect a transition from a destined Source role to the Sink role. Connection timing and other factors are involved in this process as defined in the USB Type-C state machine operation (see Section 4.5.2). It is important to note that these mechanisms, ***Try.SRC*** and ***Try.SNK***, can only be used once as part of the initial connection process. If both sides support ***USB PD***, the appropriate roles ***may*** then be further refined or swapped as per the ***USB PD*** specification.

A USB Type-C DRP-based product that does not support ***USB PD*** ***should*** implement either ***Try.SRC*** or ***Try.SNK*** depending on its preference to ensure predictable power and data roles. For example, a small mobile device that prefers being a Sink or UFP ***should*** implement ***Try.SNK***, so that when attached to a DRP system such as a laptop, the mobile device will always be the power sink. If the mobile device is connected to a Sink-only port partner, the ***Try.SNK*** method will fail, and the mobile device will end up in the Source role. If the mobile device is connected to a port partner that also implements ***Try.SNK***, the mobile device will randomly end up in either a Source or Sink role. Similarly, a DRP host such as a desktop PC that doesn't consume power over the port ***should*** implement ***Try.SRC*** to ensure it always ends up being a DFP when attached to DRPs.

A USB Type-C DRP-based product, independent of if that product supports ***USB PD***, ***may*** also implement either ***Try.SRC*** or ***Try.SNK*** in order to ensure a preferred data role when connecting to another DRP that doesn't support ***USB PD***. If that product only supports one specific data role, DFP or UFP, it ***should*** implement either ***Try.SRC*** or ***Try.SNK*** as appropriate in order to ensure a usable data role when connecting to another DRP that doesn't support ***USB PD***. In this latter case, the use of the Try mechanism to correctly align a product's data role ***should*** take precedence over the use of the Try mechanism to align on a preferred power role as the Try mechanism might be the only opportunity for the product to get into a useable functional role.

Table 4-12 summarizes the recommended implementation of ***Try.SRC*** and ***Try.SNK*** by USB Type-C dual-role ports with preferred power or data roles. For dual-role ports where only one data role is relevant to its functional purpose, that data role ***should*** be its preferred data role, e.g., a USB storage device would have a preferred data role of UFP on its port.

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Table 4-12 Recommended Implementation of Try.SRC and Try.SNK for Dual-Role Ports with Preferred Roles

Current Preferred Roles of the Dual-Role Port:	Recommendation
Source / No DR preference	Enable ***Try.SRC*** (to become Source)
Source / DFP	Enable ***Try.SRC***
Source / UFP	Enable ***Try.SNK*** (to become UFP)
Sink / No DR preference	Enable ***Try.SNK*** (to become Sink)
Sink / DFP	Enable ***Try.SRC*** (to become DFP)
Sink / UFP	Enable ***Try.SNK***
No PR preference / DFP	Enable ***Try.SRC*** (to become DFP)
No PR preference / UFP	Enable ***Try.SNK*** (to become UFP)

4.5.1.4.2 *USB PD*-based Power Role, Data Role and VCONN Swapping

Following the completion of the initial USB Type-C state machine connection process, products ***may*** use ***USB PD***-based swapping mechanisms to command a change in power roles, data roles and which end of the cable will supply VCONN. These mechanisms are:

- ***USB PD PR_Swap*** : swaps Source (***Rp***) and Sink (***Rd***)
- ***USB PD DR_Swap*** : swaps DFP (host data) and UFP (device data) roles
- ***USB PD VCONN_Swap*** : swaps which port supplies VCONN

Table 4-13 summarizes the behaviors of a port in response to the three ***USB PD*** swap commands.

Table 4-13 *USB PD* Swapping Port Behavior Summary

	DFP/UFP Data Roles	Rp/Rd	VBUS Source/Sink	VCONN Source
PR_Swap	Unchanged	Swapped	Swapped	Unchanged
DR_Swap	Swapped	Unchanged	Unchanged	Unchanged
VCONN_Swap	Unchanged	Unchanged	Unchanged	Swapped[1]
Note 1: Swapping of VCONN Source Port				

A USB Type-C dual-role product that supports ***USB PD should*** use ***USB PD PR_Swap*** and ***DR_Swap*** to ensure that it gets into its preferred power and/or data roles. For example, a hub's UFP or a monitor's UFP that prefers being in the Source role ***should*** initiate ***PR_Swap*** if needed to switch from being in the Sink role to the preferred Source role. Similarly, a small mobile device that prefers the Sink role ***should*** initiate ***PR_Swap*** to switch from being in the Source role to the preferred Sink role.

Table 4-14 summarizes the recommended use of power or data role swaps by USB Type-C dual-role ports that have preferred power or data roles. For dual-role ports where only one data role is relevant to its functional purpose, that data role ***should*** be its preferred data role, e.g., the physical upstream port of a hub would have a preferred data role of UFP on that port.

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Table 4-14 Use of Power and Data Role Swaps for Dual-Role Ports with Preferred Roles

Preferred Roles of the Dual-Role Port:	When initially connected to a:	
	Source / DFP	Sink / UFP
Source / No DR preference	Issue ***PR_Swap***	
Source / DFP	Issue ***PR_Swap*** and ***DR_Swap***	
Source / UFP	Issue ***PR_Swap***	Issue ***DR_Swap***
Sink / No DR preference		Issue ***PR_Swap***
Sink / DFP	Issue ***DR_Swap***	Issue ***PR_Swap***
Sink / UFP		Issue ***PR_Swap*** and ***DR_Swap***
No PR preference / DFP	Issue ***DR_Swap***	
No PR preference / UFP		Issue ***DR_Swap***

4.5.1.4.3 Power Role Behavioral Model Summary

Table 4-15 provides a summary of the defining characteristics of the seven fundamental power roles.

Table 4-15 Power Role Behavioral Model Summary

Power Role		Toggles	PR_Swap	USB Host	USB Device	DFP	UFP	DR_Swap	Try.SRC/ Try.SNK	Connects with
Source-Only		No	NA	Opt.	Opt.[1]	Req.	Opt.	Opt.	NA	Sink or DRP
Source (Default)		No	Req.	Opt.	Opt.[1]	Req.	Opt.	Opt.	NA	Sink or DRP
Sink-Only		No	NA	Opt.[1]	Opt.	Opt.	Req.	Opt.	NA	Source or DRP
Sink (Default)		No	Req.	Opt.[1]	Opt.	Opt.	Req.	Opt.	NA	Source or DRP
DRP	**Toggling (Source/ Sink)**	Req.	Req.	Opt.	Opt.	Req.	Req.	Req.	Opt.	Source, Sink or DRP
	Sourcing Device	Req.	Req.	NA	Req.	Req.	Req.	Req.	Opt.	
	Sinking Host	Req.	Req.	Req.	NA	Req.	Req.	Req.	Opt.	

Note 1: Requires use of ***DR_Swap***.

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4.5.2 CC Functional and Behavioral Requirements

This section provides the functional and behavioral requirements for implementing CC. The first sub-section provides connection state diagrams that are the basis for the remaining sub-sections.

The terms Source (SRC) and Sink (SNK) used in this section refer to the port's power role while the terms DFP and UFP refer to the port's data role. A DRP (Dual-Role-Power) port is capable of acting as either a Source or Sink. Typically, Sources are found on hosts and supply VBUS while a Sink is found on a device and consumes power from VBUS. When a connection is initially made, the port's initial power state and data role are established. ***USB PD*** introduces three swap commands that ***may*** alter a port's power or data role:

- The ***PR_Swap*** command changes the port's power state as reflected in the following state machines. ***PR_Swap*** does not change the port sourcing VCONN.

- The ***DR_Swap*** command has no effect on the following state machines or VCONN as it only changes the port's data role.
- ***VCONN_Swap*** command changes the port sourcing VCONN. The ***PR_Swap*** command and ***DR_Swap*** command have no effect on the port sourcing VCONN.

Note: A ***VCONN-Powered USB Device*** that supports the ***optional*** Charge-Through capability, once detected via ***USB PD*** messaging, will also change the Host-side port's power state without changing the port sourcing VCONN.

Note: ***USB PD*** defines another ***optional*** swapping mechanism (***FR_Swap***) that is used in a special case where a user interaction could inadvertently trigger a need to change the source of VBUS. A variant of ***PR_Swap***, ***FR_Swap*** similarly swaps Source (***Rp***) and Sink (***Rd***) between two connected ports. For purposes of this specification, only ***PR_Swap*** is explicitly considered in the behavior requirements and implementations that support ***FR_Swap should***, where applicable, apply ***PR_Swap***-related behaviors to ***FR_Swap***. See the ***USB PD*** specification for further details regarding ***FR_Swap***.

The connection state diagrams and CC behavior descriptions in this section describe the behavior of receptacle-based ports. The plug on a direct connect device or a device with a captive cable ***shall*** behave as a plug on a cable that is attached at its other end in normal orientation to a receptacle, These devices ***shall*** apply and sense CC voltage levels on pin A5 only and pin B5 ***shall*** have an impedance above ***zOPEN***, unless it is a ***VCONN-Powered Accessory***, in which case B5 ***shall*** have an impedance ***Ra***.

4.5.2.1 Connection State Diagrams

This section provides reference connection state diagrams for CC-based behaviors.

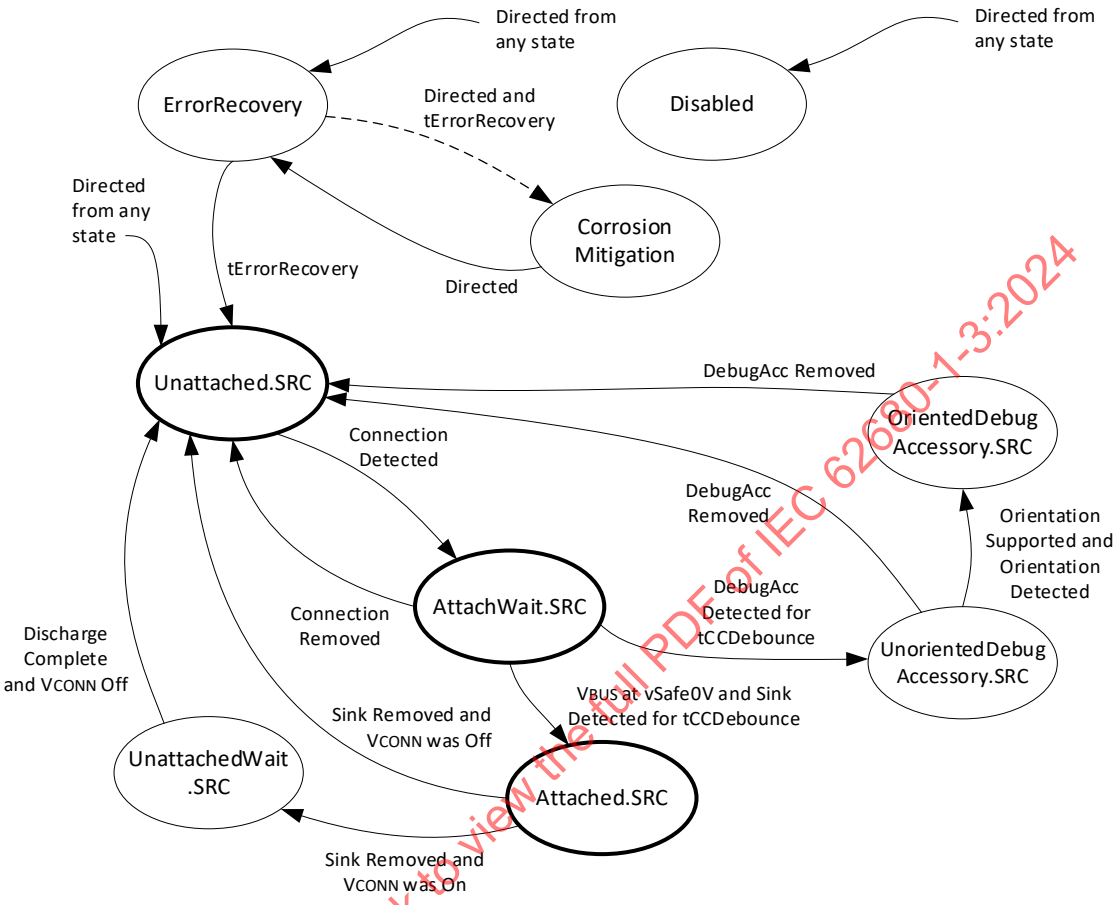
Refer to Section 4.5.2.2 for the specific state transition requirements related to each state shown in the diagrams.

Refer to Section 4.5.2.6 for a description of which states are mandatory for each port type, and a list of states where ***USB PD*** communication is permitted.

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Figure 4-12 illustrates a connection state diagram for a Source (Host/Hub DFP).

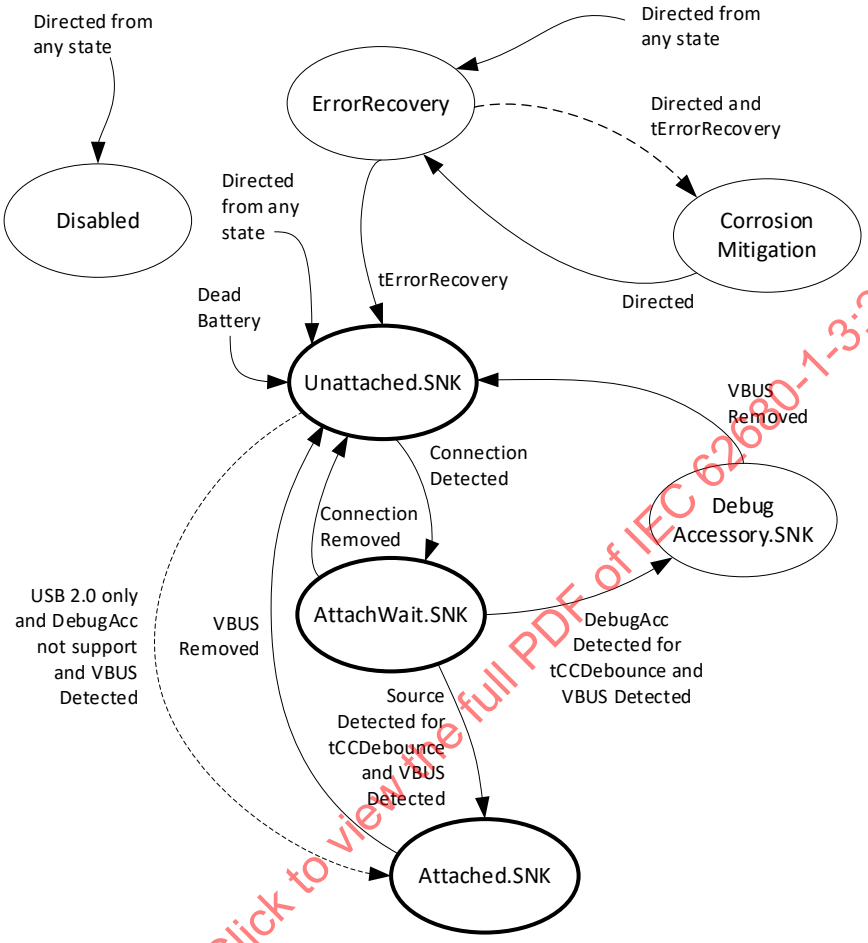
Figure 4-12 Connection State Diagram: Source



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Figure 4-13 illustrates a connection state diagram for a simple Sink (Device/Hub UFP).

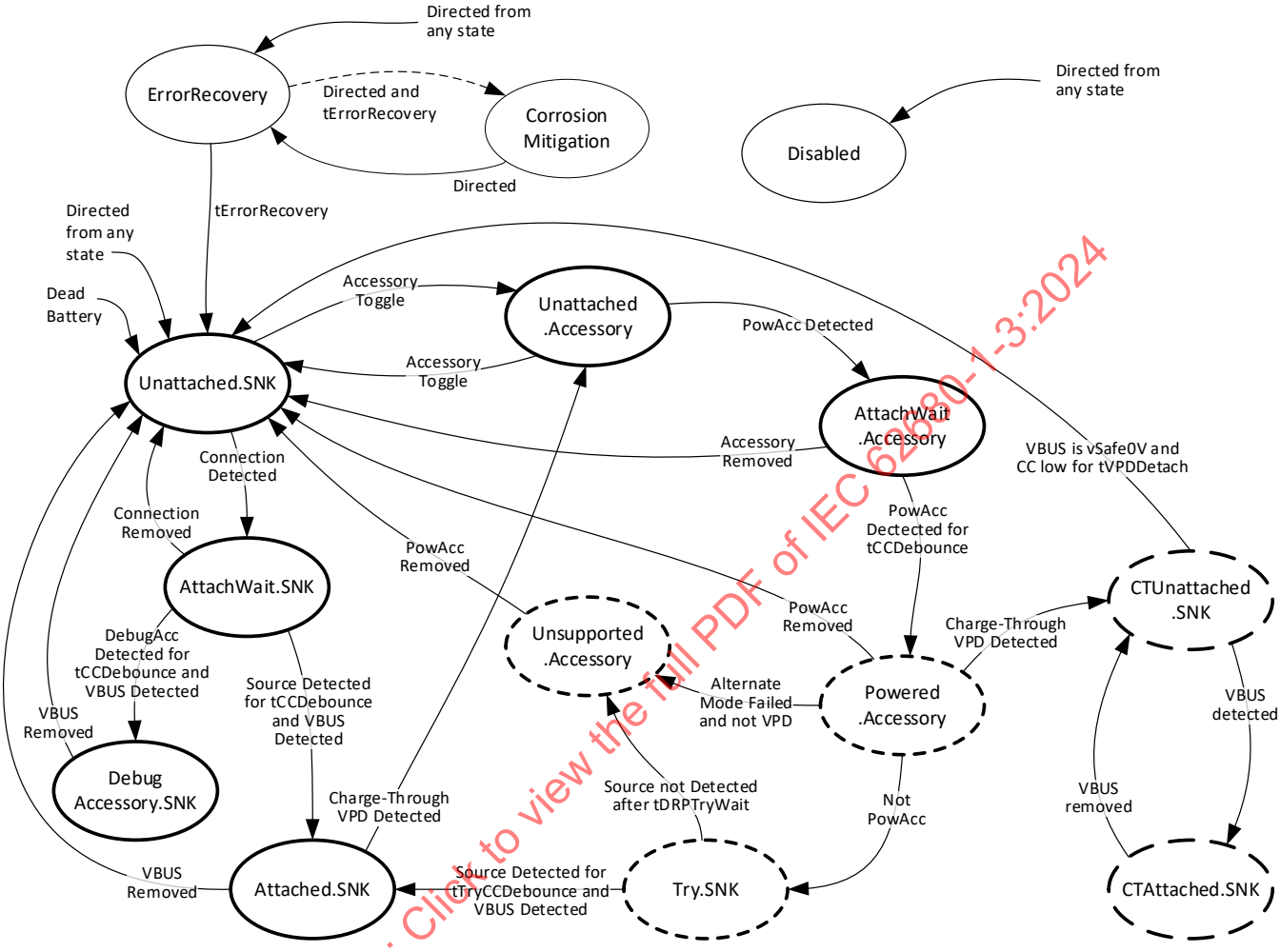
Figure 4-13 Connection State Diagram: Sink



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Figure 4-14 illustrates a connection state diagram for a Sink that supports Accessory Modes.

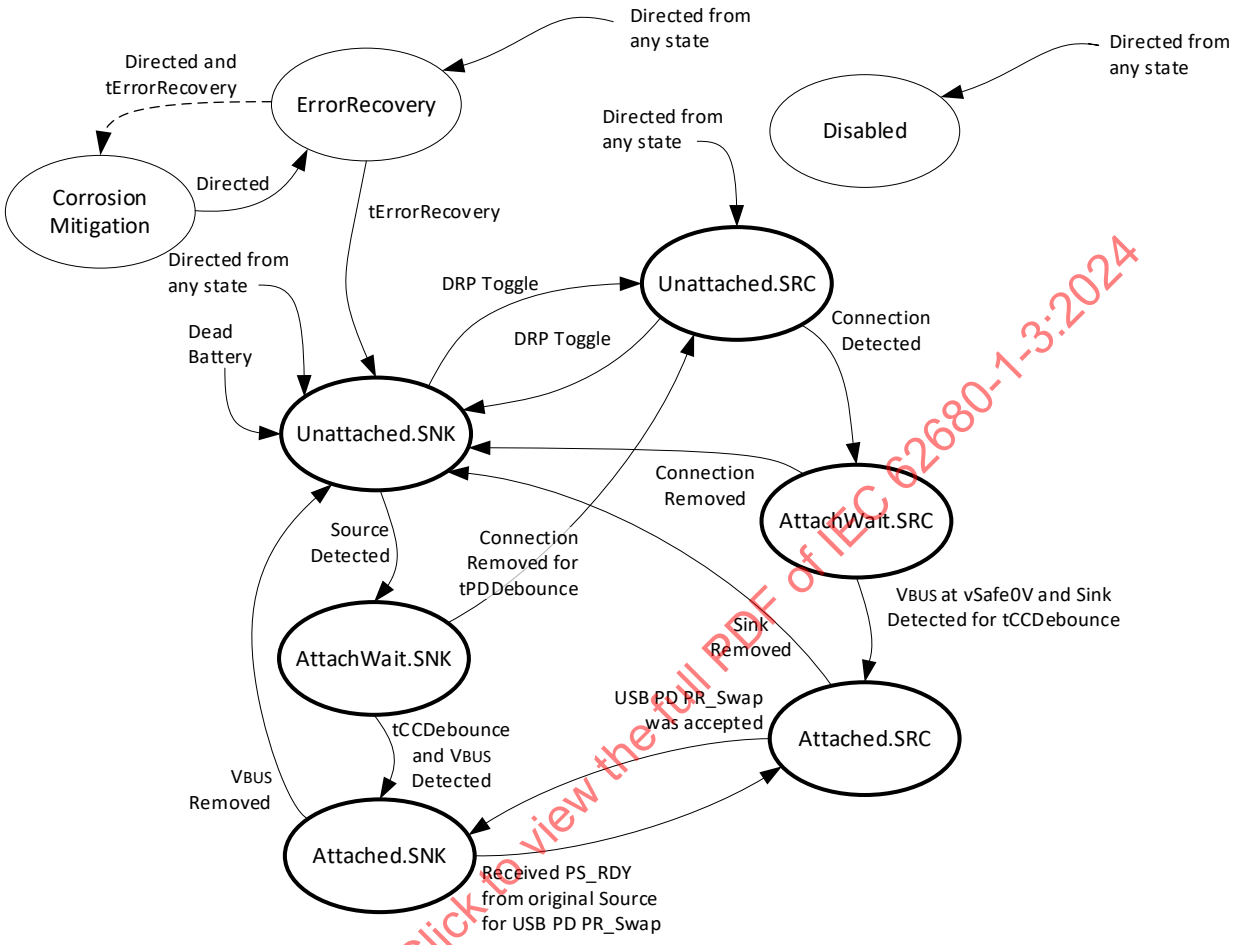
Figure 4-14 Connection State Diagram: Sink with Accessory Support



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Figure 4-15 illustrates a connection state diagram for a simple DRP (Dual-Role-Power) port.

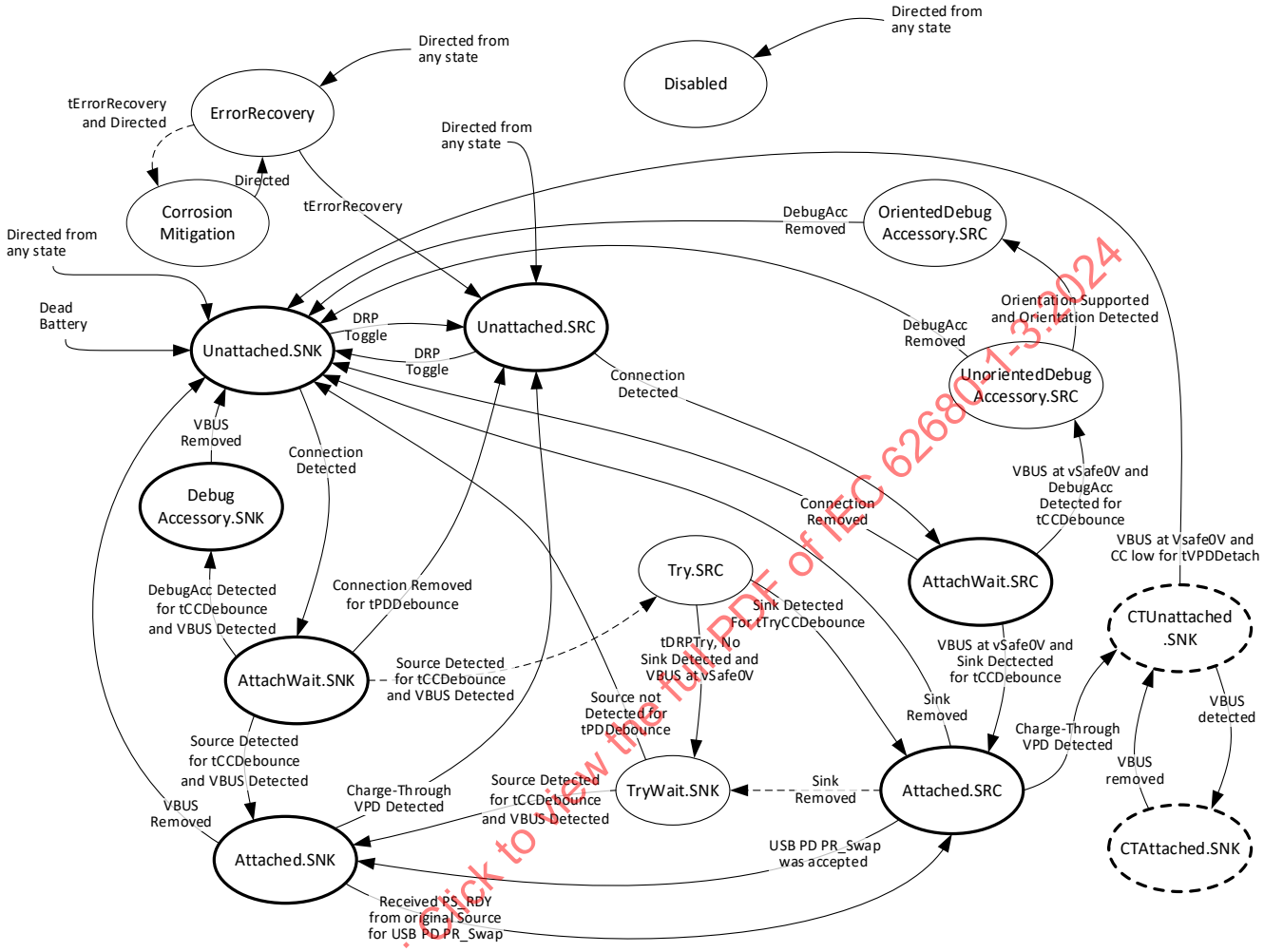
Figure 4-15 Connection State Diagram: DRP



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Figure 4-16 illustrates a connection state diagram for a DRP that supports ***Try.SRC*** and Accessory Modes.

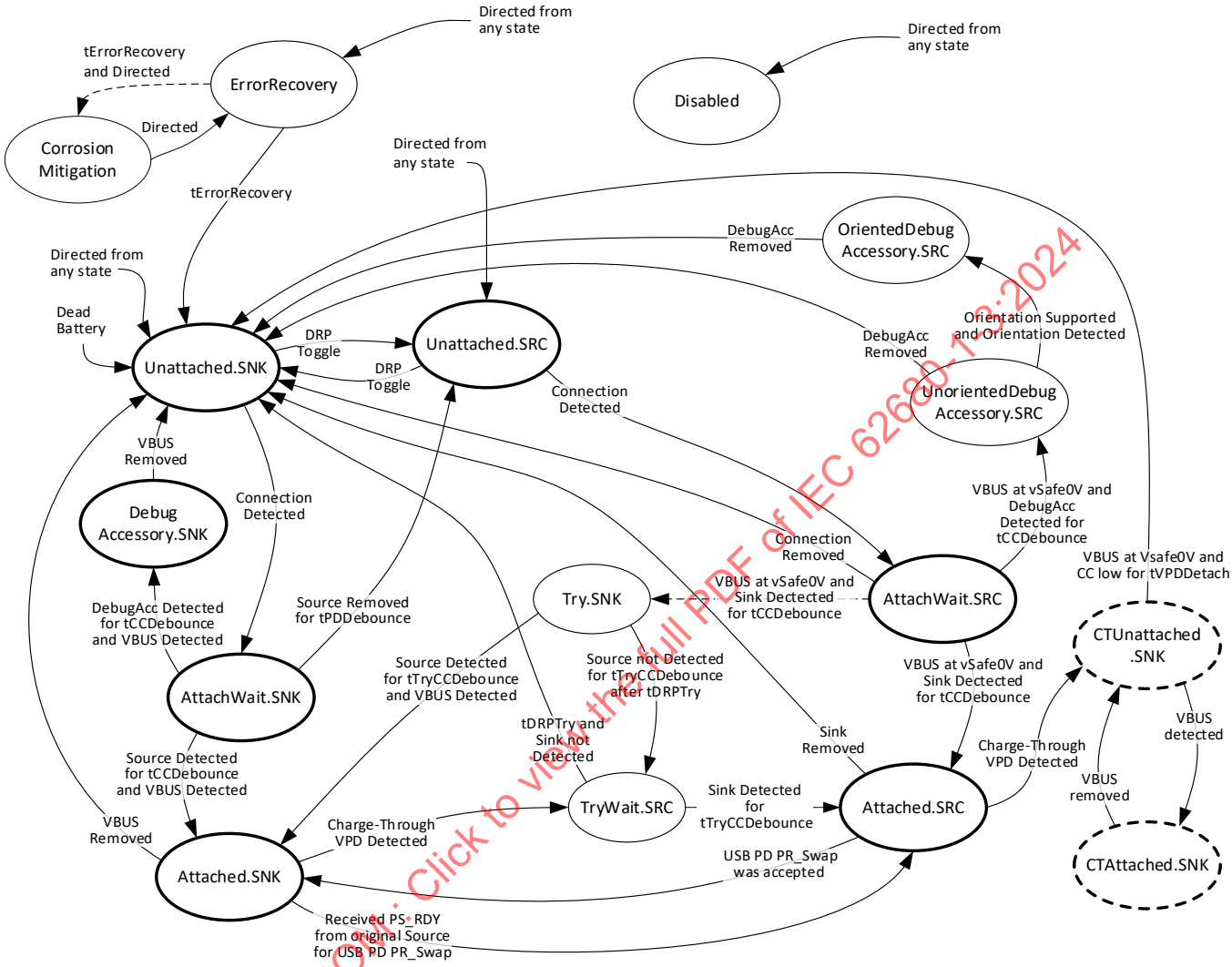
Figure 4-16 Connection State Diagram: DRP with Accessory and Try.SRC Support



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Figure 4-17 illustrates a connection state diagram for a DRP that supports ***Try.SNK*** and Accessory Modes.

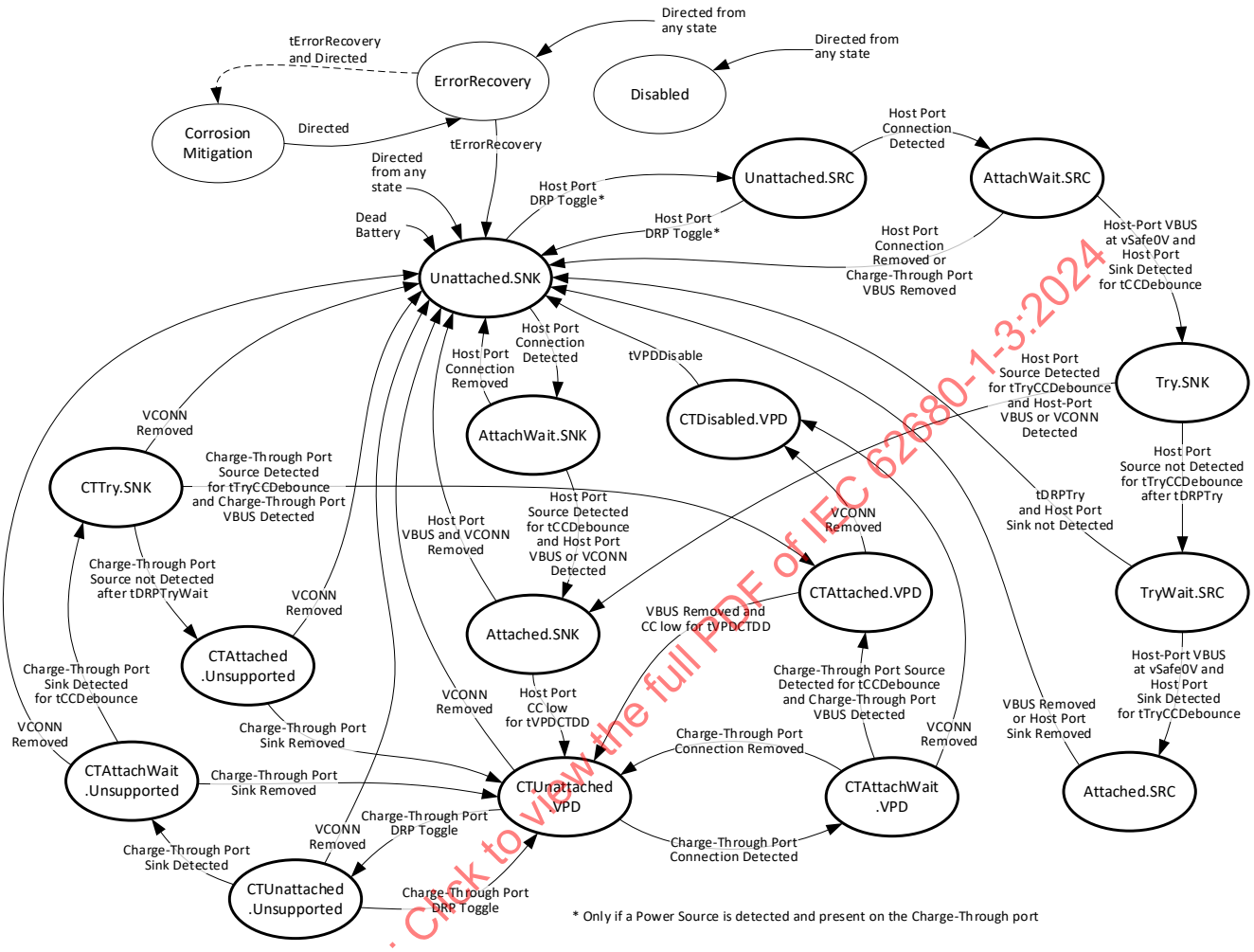
Figure 4-17 Connection State Diagram: DRP with Accessory and Try.SNK Support



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Figure 4-18 illustrates a connection state diagram for a Charge-Through ***VCONN-Powered USB Device***.

Figure 4-18 Connection State Diagram: Charge-Through VPD



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4.5.2.2 Connection State Machine Requirements

Entry into any unattached state when “directed from any state” ***shall not*** be used to override ***tDRP*** toggle.

A DRP or a Sink ***may*** consume default power from VBUS in any state where it is not required to provide VBUS.

The following two tables define the electrical states for a CC pin in both a Source and a Sink. Every port has CC1 and CC2 pins, each with its own individual CC pin state. The combination of a port’s CC1 and CC2 pin states are used to define the conditions under which a port transitions from one state to another.

Table 4-16 Source Port CC Pin State

CC Pin State	Port Partner CC Termination	Voltage Detected on CC when port asserts Rp
SRC.Open	**Open, Rp**	Above ***vOPEN***
SRC.Rd	**Rd**	Within the ***vRd*** range (i.e., between minimum ***vRd*** and maximum ***vRd***)
SRC.Ra	**Ra**	Below maximum ***vRa***

Table 4-17 Sink Port CC Pin State

CC Pin State	Port Partner CC Termination	Voltage Detected on CC when port asserts Rd
SNK.Rp	**Rp**	Above minimum ***vRd-Connect***
SNK.Open	**Open, Ra, Rd**	Below maximum ***vRa***

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4.5.2.2.1 Disabled State

This state appears in Figure 4-12, Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

The ***Disabled*** state is where the port prevents connection from occurring by removing all terminations from the CC pins.

The port ***should*** transition to the ***Disabled*** state from any other state when directed. When the port transitions to the ***Disabled*** state from ***Attached.SNK***, it ***shall*** keep all terminations on the CC pins removed for a minimum of ***tErrorRecovery***.

A port ***may*** choose not to support the ***Disabled*** state. If the ***Disabled*** state is not supported, the port ***shall*** be directed to either the ***Unattached.SNK*** or ***Unattached.SRC*** states after power-on.

4.5.2.2.1.1 Disabled State Requirements

The port ***shall not*** drive VBUS or VCONN and ***shall*** present a high-impedance to ground (above ***zOPEN***) on its CC1 and CC2 pins.

4.5.2.2.1.2 Exiting from Disabled State

A Sink ***shall*** transition to ***Unattached.SNK*** when directed.

A Source ***shall*** transition to ***Unattached.SRC*** when directed.

A DRP ***shall*** transition to either ***Unattached.SNK*** or ***Unattached.SRC*** when directed.

4.5.2.2.2 ErrorRecovery State

This state appears in Figure 4-12, Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

The ***ErrorRecovery*** state is where the port removes the terminations from the CC1 and CC2 pins for ***tErrorRecovery*** followed by transitioning to the appropriate ***Unattached.SNK*** or ***Unattached.SRC*** state based on port type. This is the equivalent of forcing a detach event and looking for a new attach. The port may alternately transition from ***ErrorRecovery*** to ***CorrosionMitigation*** if directed.

Ports that support ***USB Power Delivery shall*** support the ***ErrorRecovery*** state.

Ports that support the ***ErrorRecovery*** state ***shall*** transition to the ***ErrorRecovery*** state from any other state when directed.

A port that does not support ***USB Power Delivery may*** choose not to support the ***ErrorRecovery*** state. If the ***ErrorRecovery*** state is not supported, the port ***shall*** be directed to the ***Disabled*** state if supported. If the ***Disabled*** state is not supported, the port ***shall*** be directed to either the ***Unattached.SNK*** or ***Unattached.SRC*** states.

4.5.2.2.2.1 ErrorRecovery State Requirements

The port ***shall not*** drive VBUS or VCONN AND ***shall*** present a high-impedance to ground (above ***zOPEN***) on its CC1 and CC2 pins.

4.5.2.2.2.2 Exiting from ErrorRecovery State

A Sink ***shall*** transition to ***Unattached.SNK*** after ***tErrorRecovery*** or ***shall*** transition to ***CorrosionMitigation*** after ***tErrorRecovery*** if directed.

A Source ***shall*** transition to ***Unattached.SRC*** after ***tErrorRecovery*** or ***shall*** transition to ***CorrosionMitigation*** after ***tErrorRecovery*** if directed.

A DRP (Figure 4-15) and a DRP with Accessory and ***Try.SNK*** Support (Figure 4-17) ***shall*** transition to ***Unattached.SNK*** after ***tErrorRecovery*** or ***shall*** transition to ***CorrosionMitigation*** after ***tErrorRecovery*** if directed.

A DRP with Accessory and ***Try.SRC*** Support (Figure 4-16) ***shall*** transition to ***Unattached.SRC*** after ***tErrorRecovery*** or ***shall*** transition to ***CorrosionMitigation*** after ***tErrorRecovery*** if directed.

A Charge-Through ***VCONN-Powered USB Device*** (Figure 4-18) ***shall*** transition to ***Unattached.SNK*** after ***tErrorRecovery*** or ***shall*** transition to ***CorrosionMitigation*** after ***tErrorRecovery*** if directed.

4.5.2.2.3 Unattached.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the ***Unattached.SNK*** state, the port is waiting to detect the presence of a Source.

A port with a dead battery ***shall*** enter this state while unpowered.

4.5.2.2.3.1 Unattached.SNK State Requirements

The port ***shall not*** drive VBUS or VCONN.

Both CC1 and CC2 pins ***shall*** be independently terminated to ground through ***Rd***.

A Charge-Through ***VCONN-Powered USB Device*** ***shall*** isolate its Host-side port from its Charge-Through port, including CCs and VBUS, and independently terminate its Charge-Through port's CC1 and CC2 pins and Host-side port's CC pin to ground through ***Rd***.

4.5.2.2.3.2 Exiting from Unattached.SNK State

If the port supports ***USB PD*** or accessories, the port ***shall*** transition to ***AttachWait.SNK*** when the ***SNK.Rp*** state is present on at least one of its CC pins.

The maximum times that a Port ***shall*** take to transition to ***AttachWait.SNK*** are the following:

- ***tNoToggleConnect*** when neither Port Partner is toggling

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- ***tOnePortToggleConnect*** when one Port Partner only is toggling

When both Port Partners are toggling, a Port ***should*** transition to ***AttachWait.SNK*** within ***tTwoPortToggleConnect***. When both Port Partners are DRPs it is indeterminate whether the local port will transition to ***AttachWait.SRC*** or ***AttachWait.SNK***.

Note: The times ***tOnePortToggleConnect*** and ***tTwoPortToggleConnect*** relate to how long toggling ports ***may*** take to sync and detect a connection.

A ***USB 2.0*** only Sink that doesn't support accessories and is self-powered or requires only default power and does not support ***USB PD may*** transition directly to ***Attached.SNK*** when VBUS is detected.

A DRP ***shall*** transition to ***Unattached.SRC*** within ***tDRPTransition*** after the state of both CC pins is ***SNK.Open*** for ***tDRP*** – ***dcSRC.DRP*** · ***tDRP***, or if directed.

A Sink with Accessory support ***shall*** transition to ***Unattached.Accessory*** within ***tDRPTransition*** after the state of both the CC1 and CC2 pins is ***SNK.Open*** for ***tDRP*** – ***dcSRC.DRP*** · ***tDRP***, or if directed.

A Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***Unattached.SRC*** within ***tDRPTransition*** after the state of the Host-side port's CC pin is ***SNK.Open*** for ***tDRP*** – ***dcSRC.DRP*** · ***tDRP*** and both of the following is detected on the Charge-Through port.

- ***SNK.Rp*** state is detected on exactly one of the CC1 or CC2 pins for at least ***tCCDebounce***
- VBUS is detected

A Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***Attached.SNK*** when a Source connection is detected, as indicated by the ***SNK.Rp*** state on its Host-side port's CC pin.

4.5.2.2.4 AttachWait.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the ***AttachWait.SNK*** state, the port has detected the ***SNK.Rp*** state on at least one of its CC pins and is waiting for VBUS.

When in the ***AttachWait.SNK*** state, the Charge-Through ***VCONN-Powered USB Device*** has detected the ***SNK.Rp*** state on its Host-side port's CC pin and is waiting for host-side VBUS.

4.5.2.2.4.1 AttachWait.SNK State Requirements

The port ***shall not*** drive VBUS or VCONN.

Both the CC1 and CC2 pins ***shall*** be independently terminated to ground through ***Rd***.

A Charge-Through ***VCONN-Powered USB Device*** ***shall*** isolate its Host-side port from its Charge-Through port, including CCs and VBUS, and independently terminate its Charge-Through port's CC1 and CC2 pins and Host-side port's CC pin to ground through ***Rd***.

It is strongly recommended that a ***USB 3.2*** SuperSpeed device holds off VBUS detection to the device controller until the ***Attached.SNK*** state or the ***DebugAccessory.SNK*** state is reached, i.e., at least one CC pin is in the ***SNK.Rp*** state. Otherwise, it ***may*** connect as ***USB 2.0*** when attached to a legacy host or hub's DFP.

4.5.2.2.4.2 Exiting from AttachWait.SNK State

A Sink ***shall*** transition to ***Unattached.SNK*** when the state of both the CC1 and CC2 pins is ***SNK.Open*** for at least ***tPDDebounce***.

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A DRP ***shall*** transition to ***Unattached.SRC*** when the state of both the CC1 and CC2 pins is ***SNK.Open*** for at least ***tPDDebounce***.

The port ***shall*** transition to ***Attached.SNK*** after the state of only one of the CC1 or CC2 pins is ***SNK.Rp*** for at least ***tCCDebounce*** and VBUS is detected. Note the Source ***may*** initiate ***USB PD*** communications which will cause brief periods of the ***SNK.Open*** state on one of the CC pins with the state of the other CC pin remaining ***SNK.Open***, but this event will not exceed ***tPDDebounce***.

If the port is a ***VCONN-Powered Accessory*** or a ***VCONN-Powered USB Device***, the port ***shall*** transition to ***Attached.SNK*** when either VCONN or VBUS is detected. The port ***may*** transition without waiting ***tCCDebounce*** on CC.

If the port supports ***Debug Accessory Mode***, the port ***shall*** transition to ***DebugAccessory.SNK*** if the state of both the CC1 and CC2 pins is ***SNK.Rp*** for at least ***tCCDebounce*** and VBUS is detected. Note the DAM Source ***may*** initiate ***USB PD*** communications which will cause brief periods of the ***SNK.Open*** state on one of the CC pins with the state of the other CC pin remaining ***SNK.Rp***, but this event will not exceed ***tPDDebounce***.

A Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***Attached.SNK*** after the state of the Host-side port's CC pin is ***SNK.Rp*** for at least ***tCCDebounce*** and either host-side VCONN or VBUS is detected.

A DRP that strongly prefers the Source role ***may optionally*** transition to ***Try.SRC*** instead of ***Attached.SNK*** when the state of only one CC pin has been ***SNK.Rp*** for at least ***tCCDebounce*** and VBUS is detected.

4.5.2.2.5 Attached.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the ***Attached.SNK*** state, the port is attached and operating as a Sink. When the port initially enters this state it is also operating as a UFP. The power and data roles can be changed using ***USB PD*** commands.

A port that entered this state directly from ***Unattached.SNK*** due to detecting VBUS ***shall not*** determine orientation or availability of higher than Default USB Power and ***shall not*** use ***USB PD***.

4.5.2.2.5.1 Attached.SNK State Requirements

If the port needs to determine the orientation of the connector, it ***shall*** do so only upon entry to this state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the ***SNK.Rp*** state).

If the port supports signaling on USB TX/RX pairs, it ***shall*** functionally connect the USB TX/RX pairs and maintain the connection during and after a ***USB PD PR_Swap***.

If the port has entered the ***Attached.SNK*** state from the ***AttachWait.SNK*** or ***TryWait.SNK*** states, only one the CC1 or CC2 pins will be in the ***SNK.Rp*** state. The port ***shall*** continue to terminate this CC pin to ground through ***Rd***.

If the port has entered the ***Attached.SNK*** state from the ***Attached.SRC*** state following a ***USB PD PR_Swap***, the port ***shall*** terminate the connected CC pin to ground through ***Rd***.

The port ***shall*** meet the ***Sink Power Sub-State*** requirements specified in Section 4.5.2.3.

If the port is a ***VCONN-Powered USB Device***, it ***shall*** respond to ***USB PD*** cable identity queries on SOP'. It ***shall not*** send or respond to messages on SOP. It ***shall*** ensure there is sufficient capacitance on CC to meet cReceiver as defined in ***USB PD***.

A Charge-Through ***VCONN-Powered USB Device*** ***shall*** isolate its Host-side port from its Charge-Through port, including CCs and VBUS, present a high-impedance to ground (above ***zOPEN***) on its Charge-Through port's CC1 and CC2 pins and terminate its Host-side port's CC pin to ground through ***Rd***.

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A Charge-Through ***VCONN-Powered USB Device*** ***shall*** start a Charge-Through Support Timer when it enters the ***Attached.SNK*** state. If a Charge-Through ***VCONN-Powered USB Device*** fails to exit the ***Attached.SNK*** state before the Charge-Through Support Timer exceeds ***tAMETimeout***, it ***shall*** present a ***USB Billboard Device Class*** interface indicating that it does not support Charge-Through.

A Charge-Through ***VCONN-Powered USB Device*** ***shall*** reset the Charge-Through Support Timer when it first receives any ***USB PD*** Structured VDM Command it supports. If a Charge-Through ***VCONN-Powered USB Device*** receives a Structured VDM Command multiple times, it ***shall*** only reset the Charge-Through Support Timer once. This ensures a Charge-Through ***VCONN-Powered USB Device*** will present a ***USB Billboard Device Class*** interface if it fails to exit ***Attached.SNK*** while receiving repeated or continuous Structured VDM Commands (e.g., ***Discover Identity***).

A Charge-Through ***VCONN-Powered USB Device*** ***shall*** reset the Charge-Through Support Timer when it receives any Data Message it supports. A Charge-Through ***VCONN-Powered USB Device*** ***shall*** hold the Charge-Through Support Timer in reset while it is in any ***USB PD*** BIST mode.

Except for a ***VCONN-Powered USB Device*** or Charge-Through ***VCONN-Powered USB Device***, the port ***may*** negotiate a ***USB PD PR_Swap***, ***DR_Swap*** or ***VCONN_Swap***.

If the port supports Charge-Through ***VCONN-Powered USB Device***, and an explicit ***USB PD*** contract has failed to be negotiated, the port ***shall*** query the identity of the cable via ***USB PD*** on SOP'.

By default, upon entry from ***AttachWait.SNK*** or ***Unattached.SNK***, VCONN ***shall not*** be supplied in the ***Attached.SNK*** state. If ***Attached.SNK*** is entered from ***Attached.SRC*** as a result of a ***USB PD PR_Swap***, it ***shall*** maintain VCONN supply state, whether on or off, and its data role connections. A ***USB PD DR_Swap*** has no effect on which port sources VCONN.

The port ***may*** negotiate a ***USB PD VCONN_Swap***. When the port successfully executes ***USB PD VCONN_Swap*** operation and is not sourcing VCONN, it ***shall*** start sourcing VCONN within ***tVCONNON***. The port ***shall*** execute the ***VCONN_Swap*** in a make-before-break sequence in order to keep active USB Type-C to USB Type-C cables powered. When the port successfully executes ***USB PD VCONN_Swap*** operation and was sourcing VCONN, it ***shall*** stop sourcing VCONN within ***tVCONNOFF***.

4.5.2.2.5.2 Exiting from Attached.SNK State

A port that is not a ***VCONN-Powered USB Device*** and is not in the process of a ***USB PD PR_Swap*** or a ***USB PD*** Hard Reset or a ***USB PD FR_Swap*** ***shall*** transition to ***Unattached.SNK*** within ***tSinkDisconnect*** when VBUS falls below ***vSinkDisconnect*** for VBUS operating at or below 5 V or below ***vSinkDisconnectPD*** when negotiated by ***USB PD*** to operate above 5 V.

A ***VCONN-Powered USB Device*** ***shall*** return to ***Unattached.SNK*** when VBUS has fallen below ***vSinkDisconnect*** and VCONN has fallen below ***vVCONNDisconnect***.

A port that has entered into ***USB PD*** communications with the Source and has seen the CC voltage exceed ***vRd-USB*** ***may*** monitor the CC pin to detect cable disconnect in addition to monitoring VBUS.

A port that is monitoring the CC voltage for disconnect (but is not in the process of a ***USB PD PR_Swap*** or ***USB PD FR_Swap***) ***shall*** transition to ***Unattached.SNK*** within ***tSinkDisconnect*** after the CC voltage remains below ***vRd-USB*** for ***tPDDebounce***.

If supplying VCONN, the port ***shall*** cease to supply it within ***tVCONNOFF*** of exiting ***Attached.SNK***.

A Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTUnattached.VPD*** if VCONN is present and the state of its Host-side port's CC pin is ***SNK.Open*** for ***tVPDCTDD***.

A port that via SOP' has detected an attached Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***TryWait.SRC*** if implemented, or transition to ***Unattached.SRC*** or ***Unattached.Accessory*** if ***TryWait.SRC*** is

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not supported. This transition ***may*** be delayed until the device has sufficient battery charge needed to remain powered until it reaches the ***CTAttached.SNK*** state.

After receiving a ***USB PD*** PS_RDY from the original Source during a ***USB PD PR_Swap***, the port ***shall*** transition directly to the ***Attached.SRC*** state (i.e., remove ***Rd*** from CC, assert ***Rp*** on CC and supply VBUS), but ***shall*** maintain its VCONN supply state, whether off or on, and its data role/connections.

4.5.2.2.6 UnattachedWait.SRC State

This state appears in Figure 4-12.

When in the ***UnattachedWait.SRC*** state, the port is discharging the CC pin that was providing VCONN in the previous ***Attached.SRC*** state.

4.5.2.2.6.1 UnattachedWait.SRC State Requirements

The port ***shall not*** enable VBUS or VCONN.

The port ***shall*** complete the VCONN turn off initiated when leaving the previous ***Attached.SRC*** state.

The port ***shall*** continue to provide an ***Rp*** termination, as specified in Table 4-27, on the CC pin not being discharged.

The port ***shall not*** provide an ***Rp*** termination on the CC pin being discharged.

The port ***shall*** provide an ***Rdch*** termination on the CC pin being discharged.

The port ***shall*** discharge the CC pin being discharged below ***vVCONNDischarge***.

4.5.2.2.6.2 Exiting from UnattachedWait.SRC State

The port ***shall*** transition to ***Unattached.SRC*** when VCONN is below ***vVCONNDischarge***. The port ***may*** delay this transition to allow the cable plug more time to reapply ***Ra***.

4.5.2.2.7 Unattached.SRC State

This state appears in Figure 4-12, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the ***Unattached.SRC*** state, the port is waiting to detect the presence of a Sink or an Accessory.

When in the ***Unattached.SRC*** state, the Charge-Through ***VCONN-Powered USB Device*** has detected a Source on its Charge-Through port and is independently monitoring its Host-side port to detect the presence of a Sink.

4.5.2.2.7.1 Unattached.SRC State Requirements

The port ***shall not*** drive VBUS or VCONN.

The port ***shall*** source current on both the CC1 and CC2 pins independently.

The port ***shall*** provide a separate ***Rp*** termination on the CC1 and CC2 pins as specified in Table 4-27. Note: A Source with a captive cable or just a plug presents a single ***Rp*** termination on its CC pin (A5).

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through ***VCONN-Powered USB Device*** ***shall*** ensure that it is powered by VBUS from the Charge-Through port.

Upon entry into this state, the Charge-Through ***VCONN-Powered USB Device*** ***shall*** remove its ***Rd*** termination to ground on the Host-side port CC and provide an ***Rp*** termination instead advertising Default USB Power, as specified in Table 4-27, and continue to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through ***Rd***.

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4.5.2.2.7.2 Exiting from Unattached.SRC State

The port ***shall*** transition to ***AttachWait.SRC*** when:

- The ***SRC.Rd*** state is present on either the CC1 or CC2 pin or
- The ***SRC.Ra*** state is present on both the CC1 and CC2 pins.

The maximum times that a Port ***shall*** take to transition to ***AttachWait.SRC*** are the following:

- ***tNoToggleConnect*** when neither Port Partner is toggling
- ***tOnePortToggleConnect*** when one Port Partner only is toggling

When both Port Partners are toggling, a Port ***should*** transition to ***AttachWait.SRC*** within ***tTwoPortToggleConnect***. Note that when both Port Partners are DRPs it is indeterminate whether the local port will transition to ***AttachWait.SRC*** or ***AttachWait.SNK***.

Note: The times ***tOnePortToggleConnect*** and ***tTwoPortToggleConnect*** relate to how long toggling ports ***may*** take to sync and detect a connection.

Note: A cable without an attached device can be detected, when the ***SRC.Ra*** state is detected on one of the CC1 or CC2 pins and the other CC pin is ***SRC.Open***. However, in this case, the port ***shall not*** transition to ***AttachWait.SRC***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***AttachWait.SRC*** when host-side VBUS is ***vSafe0V*** and ***SRC.Rd*** state is detected on the Host-side port's CC pin.

A DRP ***shall*** transition to ***Unattached.SNK*** within ***tDRPTransition*** after ***dcSRC.DRP*** · ***tDRP***, or if directed.

A Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***Unattached.SNK*** within ***tDRPTransition*** after ***dcSRC.DRP*** · ***tDRP***, or if Charge-Through VBUS is removed.

4.5.2.2.8 AttachWait.SRC State

This state appears in Figure 4-12, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

The ***AttachWait.SRC*** state is used to ensure that the state of both CC1 and CC2 pins are stable after a Sink is connected.

When in the ***AttachWait.SRC*** state, the Charge-Through ***VCONN-Powered USB Device*** ensures that the state of Host-side port's CC pin is stable after a Sink is connected.

4.5.2.2.8.1 AttachWait.SRC State Requirements

The port ***shall not*** drive VBUS or VCONN.

The port ***shall*** apply a load to VBUS to ensure it reaches ***vSafe0V*** within ***tVsafe0V***. (Note: The connected Sink port might have charge left in its capacitors at up to ***vSafe5V*** that will prevent the Source port from transitioning to ***Attached.SRC***.)

The port ***shall*** source current on both the CC1 and CC2 pins independently.

The port ***shall*** provide a separate ***Rp*** termination on the CC1 and CC2 pins as specified in Table 4-27. Note: A Source with a captive cable or just a plug presents a single ***Rp*** termination on its CC pin (A5).

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through ***VCONN-Powered USB Device*** ***shall*** ensure that it is powered by VBUS from the Charge-Through port.

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Upon entry into this state, the Charge-Through ***VCONN-Powered USB Device*** ***shall*** remove its ***Rd*** termination to ground on the Host-side port CC and provide an ***Rp*** termination instead advertising Default USB Power, as specified in Table 4-27, and continue to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through ***Rd***.

4.5.2.2.8.2 Exiting from AttachWait.SRC State

The port ***shall*** transition to ***Attached.SRC*** when VBUS is at ***vSafe0V*** and the ***SRC.Rd*** state is detected on exactly one of the CC1 or CC2 pins for at least ***tCCDebounce***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***Try.SNK*** when the host-side VBUS is at ***vSafe0V*** and the ***SRC.Rd*** state is on the Host-side port's CC pin for at least ***tCCDebounce***.

If the port supports ***Debug Accessory Mode***, it ***shall*** transition to ***UnorientedDebugAccessory.SRC*** when VBUS is at ***vSafe0V*** and the ***SRC.Rd*** state is detected on both the CC1 and CC2 pins for at least ***tCCDebounce***.

A Source ***shall*** transition to ***Unattached.SRC*** and a DRP to ***Unattached.SNK*** when the ***SRC.Open*** state is detected on both the CC1 and CC2 pins. The Source ***shall*** detect the ***SRC.Open*** state within ***tSRCDisconnect*** but ***should*** detect it as quickly as possible.

A Source ***shall*** transition to ***Unattached.SRC*** and a DRP to ***Unattached.SNK*** when the ***SRC.Open*** state is detected on either the CC1 or CC2 pin and the other CC pin is ***SRC.Ra***. The Source ***shall*** detect the ***SRC.Open*** state within ***tSRCDisconnect*** but ***should*** detect it as quickly as possible.

The port ***may*** exit to ***ErrorRecovery*** or ***Disabled*** if the VBUS voltage has not reached ***vSafe0V*** within ***tVBUSOFF*** (Maximum) after entering the ***AttachWait.SRC*** state.

A Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***Unattached.SNK*** when the ***SRC.Open*** state is detected on the Host-side port's CC or if Charge-Through VBUS falls below ***vSinkDisconnect***. The Charge-Through ***VCONN-Powered USB Device*** ***shall*** detect the ***SRC.Open*** state within ***tSRCDisconnect*** but ***should*** detect it as quickly as possible.

A DRP that strongly prefers the Sink role ***may optionally*** transition to ***Try.SNK*** instead of ***Attached.SRC*** when VBUS is at ***vSafe0V*** and the ***SRC.Rd*** state is detected on exactly one of the CC1 or CC2 pins for at least ***tCCDebounce***.

4.5.2.2.9 Attached.SRC State

This state appears in Figure 4-12, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the ***Attached.SRC*** state, the port is attached and operating as a Source. When the port initially enters this state, it is also operating as a DFP. Subsequently, the initial power and data roles can be changed using ***USB PD*** commands.

When in the ***Attached.SRC*** state, the Charge-Through ***VCONN-Powered USB Device*** has detected a Sink on its Host-side port and has connected the Charge-Through port VBUS to the Host-side port VBUS.

4.5.2.2.9.1 Attached.SRC State Requirements

If the port needs to determine the orientation of the connector, it ***shall*** do so only upon entry to the ***Attached.SRC*** state by detecting which of the CC1 or CC2 pins is connected through the cable, i.e., which CC pin is in the ***SRC.Rd*** state.

If the port has entered this state from the ***AttachWait.SRC*** state or the ***Try.SRC*** state, the ***SRC.Rd*** state will be on only one of the CC1 or CC2 pins. The port ***shall*** source current on this CC pin and monitor its state.

If the port has entered this state from the ***Attached.SNK*** state as the result of a ***USB PD PR_Swap***, the port ***shall*** source current on the connected CC pin and monitor its state.

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The port ***shall*** provide an ***Rp*** as specified in Table 4-27.

The port ***shall*** supply VBUS current at the level it advertises on ***Rp***.

The port ***shall*** supply VBUS within ***tVBUSON*** of entering this state, and for as long as it is operating as a power source.

The port ***shall not*** initiate any ***USB PD*** communications until VBUS reaches ***vSafe5V***.

If the port supports signaling on USB TX/RX pairs, it ***shall***:

- Functionally connect the USB TX/RX pairs
- For VCONN, do one of two things:
    - Supply VCONN unconditionally to the CC pin not in the ***SRC.Rd*** state, or
    - Supply VCONN to the CC pin in the ***SRC.Ra*** state.

A port that does not support signaling on USB TX/RX pairs ***may*** supply VCONN in the same manner described above.

The port ***may*** negotiate a ***USB PD PR_Swap***, ***DR_Swap*** or ***VCONN_Swap***.

If the port supplies VCONN, it ***shall*** do so within ***tVCONNON***.

The port ***may*** query the identity of the cable via ***USB PD*** on SOP'. If it detects that it is connected to a ***VCONN-Powered USB Device***, the port ***may*** remove VBUS and discharge it to ***vSafe0V***, while continuing to remain in this state with VCONN applied. The port ***may*** also initiate other SOP' communication.

The port ***shall not*** supply VCONN if it has entered this state as a result of a ***USB PD PR_Swap*** and was not previously supplying VCONN. A ***USB PD DR_Swap*** has no effect on which port sources VCONN.

The port ***may*** negotiate a ***USB PD VCONN_Swap***. When the port successfully executes ***USB PD VCONN_Swap*** operation and was sourcing VCONN, it ***shall*** stop sourcing VCONN within ***tVCONNOFF***. The port ***shall*** execute the ***VCONN_Swap*** in a make-before-break sequence in order to keep active USB Type-C to USB Type-C cables powered. When the port successfully executes ***USB PD VCONN_Swap*** operation and was not sourcing VCONN, it ***shall*** start sourcing VCONN within ***tVCONNON***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** continue to isolate its Host-side port's CC pin from its Charge-Through CC pins.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** maintain its ***Rp*** termination advertising Default USB Power on the Host-side port's CC pin, and continue to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through ***Rd***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** immediately connect the Charge-Through port's VBUS through to the Host-side port's VBUS.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** ensure that it is powered entirely by VBUS.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** only respond to ***USB PD Discover Identity*** queries on SOP' on its Host-side port and complete any active queries prior to exiting this state. It ***shall*** ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in ***USB PD***.

4.5.2.2.9.2 Exiting from Attached.SRC State

A Source that is supplying VCONN or has yielded VCONN source responsibility to the Sink through ***USB PD VCONN_Swap*** messaging ***shall*** transition to ***UnattachedWait.SRC*** when the ***SRC.Open*** state is detected on the

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monitored CC pin. The Source ***shall*** detect the ***SRC.Open*** state within ***tSRCDisconnect*** but ***should*** detect it as quickly as possible.

A Source that is not supplying VCONN and has not yielded VCONN responsibility to the Sink through ***USB PD VCONN_Swap*** messaging ***shall*** transition to ***Unattached.SRC*** when the ***SRC.Open*** state is detected on the monitored CC pin. The Source ***shall*** detect the ***SRC.Open*** state within ***tSRCDisconnect*** but ***should*** detect it as quickly as possible.

When the ***SRC.Open*** state is detected on the monitored CC pin, a DRP ***shall*** transition to ***Unattached.SNK*** unless it strongly prefers the Source role. In that case, it ***shall*** transition to ***TryWait.SNK***. This transition to ***TryWait.SNK*** is needed so that two devices that both prefer the Source role do not loop endlessly between Source and Sink. In other words, a DRP that would enter ***Try.SRC*** from ***AttachWait.SNK*** ***shall*** enter ***TryWait.SNK*** for a Sink detach from ***Attached.SRC***.

A DRP that supports Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTUnattached.SNK*** if the connected device identifies itself as a Charge-Through ***VCONN-Powered USB Device*** in its ***Discover Identity*** Command response. The DRP ***may*** delay this transition to perform further SOP' communication.

A port ***shall*** cease to supply VBUS within ***tVBUSOFF*** of exiting ***Attached.SRC***.

A port that is supplying VCONN ***shall*** cease to supply it within ***tVCONNOFF*** of exiting ***Attached.SRC***, unless it is exiting as a result of a ***USB PD PR_Swap*** or is transitioning into the ***CTUnattached.SNK*** state.

After a ***USB PD PR_Swap*** is accepted (i.e., either an ***Accept*** message is received or acknowledged), a DRP ***shall*** transition directly to the ***Attached.SNK*** state (i.e., remove ***Rp*** from CC, assert ***Rd*** on CC and stop supplying VBUS) and maintain its current data role, connection and VCONN supply state.

A Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***Unattached.SNK*** when VBUS falls below ***vSinkDisconnect*** or the Host-side port's CC pin is ***SRC.Open***. The Charge-Through ***VCONN-Powered USB Device*** ***shall*** detect the ***SRC.Open*** state within ***tSRCDisconnect*** but ***should*** detect it as quickly as possible.

4.5.2.2.10 Try.SRC State

This state appears in Figure 4-16.

When in the ***Try.SRC*** state, the port is querying to determine if the port partner supports the Sink role.

Note: if both ***Try.SRC*** and ***Try.SNK*** mechanisms are implemented, only one ***shall*** be enabled by the port at any given time. Deciding which of these two mechanisms is enabled is product design-specific.

4.5.2.2.10.1 Try.SRC State Requirements

The port ***shall not*** drive VBUS or VCONN.

The port ***shall*** source current on both the CC1 and CC2 pins independently.

The port ***shall*** provide an ***Rp*** as specified in Table 4-27.

4.5.2.2.10.2 Exiting from Try.SRC State

The port ***shall*** transition to ***Attached.SRC*** when the ***SRC.Rd*** state is detected on exactly one of the CC1 or CC2 pins for at least ***tTryCCDebounce***.

The port ***shall*** transition to ***TryWait.SNK*** after ***tDRPTry*** and the ***SRC.Rd*** state has not been detected and VBUS is within ***vSafe0V***, or after ***tTryTimeout*** and the ***SRC.Rd*** state has not been detected.

4.5.2.2.11 TryWait.SNK State

This state appears in Figure 4-16.

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When in the ***TryWait.SNK*** state, the port has failed to become a Source and is waiting to attach as a Sink. Alternatively, the port is responding to the Sink being removed while in the ***Attached.SRC*** state.

4.5.2.2.11.1 TryWait.SNK State Requirements

The port ***shall not*** drive VBUS or VCONN.

Both the CC1 and CC2 pins ***shall*** be independently terminated to ground through ***Rd***.

4.5.2.2.11.2 Exiting from TryWait.SNK State

The port ***shall*** transition to ***Attached.SNK*** after ***tCCDebounce*** if or when VBUS is detected. Note the Source ***may*** initiate ***USB PD*** communications which will cause brief periods of the ***SNK.Open*** state on both the CC1 and CC2 pins, but this event will not exceed ***tPDDebounce***.

The port ***shall*** transition to ***Unattached.SNK*** when the state of both CC1 and CC2 pins is ***SNK.Open*** for at least ***tPDDebounce***.

4.5.2.2.12 Try.SNK State

This state appears in Figure 4-14, Figure 4-17 and Figure 4-18.

When in the ***Try.SNK*** state, the port is querying to determine if the port partner supports the Source role.

When in the ***Try.SNK*** state, the Charge-Through ***VCONN-Powered USB Device*** is querying to determine if the port partner on the Host-side port supports the Source role.

Note: if both ***Try.SRC*** and ***Try.SNK*** mechanisms are implemented, only one ***shall*** be enabled by the port at any given time. Deciding which of these two mechanisms is enabled is product design-specific.

4.5.2.2.12.1 Try.SNK State Requirements

The port ***shall not*** drive VBUS or VCONN.

Both the CC1 and CC2 pins ***shall*** be independently terminated to ground through ***Rd***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through ***VCONN-Powered USB Device*** ***shall*** ensure that it is powered by VBUS from the Charge-Through port.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** remove its ***Rp*** termination (Default USB Power advertisement) on the Host-side port CC and provide an ***Rd*** termination to ground instead, as specified in Table 4-27 and remain to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through ***Rd***.

4.5.2.2.12.2 Exiting from Try.SNK State

The port ***shall*** wait for ***tDRPTry*** and only then begin monitoring the CC1 and CC2 pins for the ***SNK.Rp*** state.

The port ***shall*** then transition to ***Attached.SNK*** when the ***SNK.Rp*** state is detected on exactly one of the CC1 or CC2 pins for at least ***tTryCCDebounce*** and VBUS is detected.

Alternatively, the port ***shall*** transition to ***TryWait.SRC*** if ***SNK.Rp*** state is not detected for ***tTryCCDebounce***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** wait for ***tDRPTry*** and only then begin monitoring the Host-side port's CC pin for the ***SNK.Rp*** state.

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The Charge-Through ***VCONN-Powered USB Device*** ***shall*** then transition to ***Attached.SNK*** when the ***SNK.Rp*** state is detected on the Host-side port's CC pin for at least ***tTryCCDebounce*** and VBUS or VCONN is detected on Host-side port.

Alternatively, the Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***TryWait.SRC*** if Host-side ***SNK.Rp*** state is not detected for ***tTryCCDebounce***.

A Sink with Accessory Support ***shall*** transition to ***Unsupported.Accessory*** if ***SNK.Rp*** state is not detected for ***tDRPTryWait***.

Note: The Source ***may*** initiate ***USB PD*** communications which will cause brief periods of the ***SNK.Open*** state on both the CC1 and CC2 pins, but this event will not exceed ***tTryCCDebounce***.

4.5.2.2.13 TryWait.SRC State

This state appears in Figure 4-17 and Figure 4-18.

When in the ***TryWait.SRC*** state, the port has failed to become a Sink and is waiting to attach as a Source.

When in the ***TryWait.SRC*** state, the Charge-Through ***VCONN-Powered USB Device*** has failed to become a Sink on its Host-side port and is waiting to attach as a Source on its Host-side port.

4.5.2.2.13.1 TryWait.SRC State Requirements

The requirements for this state are identical to ***Unattached.SRC***.

4.5.2.2.13.2 Exiting from TryWait.SRC State

The port ***shall*** transition to ***Attached.SRC*** when VBUS is at ***vSafe0V*** and the ***SRC.Rd*** state is detected on exactly one of the CC pins for at least ***tTryCCDebounce***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***Attached.SRC*** when host-side VBUS is at ***vSafe0V*** and the ***SRC.Rd*** state is detected on the Host-side port's CC pin for at least ***tTryCCDebounce***.

The port ***shall*** transition to ***Unattached.SNK*** after ***tDRPTry*** if neither of the CC1 or CC2 pins are in the ***SRC.Rd*** state.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***Unattached.SNK*** after ***tDRPTry*** if the Host-side port's CC pin is not in the ***SRC.Rd*** state.

4.5.2.2.14 Unattached.Accessory State

This state appears in Figure 4-14.

The ***Unattached.Accessory*** state allows accessory-supporting Sinks to connect to ***VCONN-Powered Accessories***.

This state is functionally equivalent to the ***Unattached.SRC*** state in a DRP, except that ***Attached.SRC*** is not supported.

4.5.2.2.14.1 Unattached.Accessory State Requirements

The port ***shall not*** drive VBUS or VCONN.

The port ***shall*** source current on both the CC1 and CC2 pins independently.

The port ***shall*** provide an ***Rp*** as specified in Table 4-27.

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4.5.2.2.14.2 Exiting from Unattached.Accessory State

A port that supports ***VCONN-Powered Accessories*** also ***shall*** transition to ***AttachWait.Accessory*** when the state of either CC1 or CC2 pin is ***SRC.Ra*** and the other CC pin is ***SRC.Rd***.

The maximum time the local port ***shall*** take to transition from ***Unattached.Accessory*** to the ***AttachWait.Accessory*** state when a ***VCONN-Powered Accessory*** is present is ***tOnePortToggleConnect***.

Otherwise, the port ***shall*** transition to ***Unattached.SNK*** within ***tDRPTransition*** after ***dcSRC.DRP*** · ***tDRP***, or if directed.

4.5.2.2.15 AttachWait.Accessory State

This state appears in Figure 4-14.

The ***AttachWait.Accessory*** state is used to ensure that the state of both CC1 and CC2 pins is stable after a cable is plugged in.

4.5.2.2.15.1 AttachWait.Accessory State Requirements

The requirements for this state are identical to ***Unattached.Accessory***.

4.5.2.2.15.2 Exiting from AttachWait.Accessory State

The port ***shall*** transition to ***Unattached.SNK*** when the state of either the CC1 or CC2 pin is ***SRC.Open*** for at least ***tCCDebounce***.

If the port supports ***VCONN-Powered Accessories***, it ***shall*** transition to ***PoweredAccessory*** state if the state of either the CC1 or CC2 pin is ***SRC.Rd*** and the other CC pin is ***SRC.Ra*** concurrently for at least ***tCCDebounce***.

4.5.2.2.16 CorrosionMitigation State

This state appears in Figure 4-12, Figure 4-14, Figure 4-16, Figure 4-17 and Figure 4-18.

The ***CorrosionMitigation*** state is used for the ***Liquid Corrosion Mitigation Mode*** specified in Appendix A.

4.5.2.2.16.1 CorrosionMitigation State Requirements

The port ***shall*** reconfigure its pins as detailed in Appendix A.

The port ***shall not*** drive VBUS or VCONN.

The port ***shall*** do one of the following implementations:

1. The port ***shall*** pull low with a resistance on both CC1 and CC2 less than or equal to the Maximum Impedance of ***Ra*** as specified in Table 4-29. The port should pull low with a resistance stronger than ***Ra***.
2. The port ***shall*** pull low with a resistance on only one of the CC1 or CC2 pins and have the other pin open (present an impedance to ground above ***zOPEN***). When using this single pull low implementation, the Sink ***shall*** monitor the voltage on the open CC pin and ***shall*** swap the resistance and open from one CC pin to the other when ***SNK.Rp*** is detected.

4.5.2.2.16.2 Exiting from CorrosionMitigation State

The port shall transition to ***ErrorRecovery*** when directed.

4.5.2.2.17 UnorientedDebugAccessory.SRC State

This state appears in Figure 4-12, Figure 4-16 and Figure 4-17.

The ***UnorientedDebugAccessory.SRC*** state is used for the ***Debug Accessory Mode*** specified in Appendix B.

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4.5.2.2.17.1 UnorientedDebugAccessory.SRC State Requirements

This mode is for debug only and ***shall not*** be used for communicating with commercial products.

The port ***shall*** provide an ***Rp*** as specified in Table 4-27 on both the CC1 and CC2 pins and monitor to detect when the state of either is ***SRC.Open***.

The port ***shall*** supply VBUS current at the level it advertises on ***Rp***. The port ***shall not*** drive VCONN.

The port ***may*** connect any non-orientation specific debug signals for ***Debug Accessory Mode*** operation only after entry to this state.

4.5.2.2.17.2 Exiting from UnorientedDebugAccessory.SRC State

If the port is a Source, the port ***shall*** transition to ***Unattached.SRC*** when the ***SRC.Open*** state is detected on either the CC1 or CC2 pin.

If the port is a DRP, the port ***shall*** transition to ***Unattached.SNK*** when the ***SRC.Open*** state is detected on either the CC1 or CC2 pin.

The port ***shall*** transition to ***OrientedDebugAccessory.SRC*** state if orientation is required and detected as described in Section B.2.6.1.2.

4.5.2.2.18 OrientedDebugAccessory.SRC State

This state appears in Figure 4-12, Figure 4-16 and Figure 4-17.

The ***OrientedDebugAccessory.SRC*** state is used for the ***Debug Accessory Mode*** specified in Appendix B.

4.5.2.2.18.1 OrientedDebugAccessory.SRC State Requirements

This mode is for debug only and ***shall not*** be used for communicating with commercial products.

The port ***shall*** provide an ***Rp*** as specified in Table 4-27 on both the CC1 and CC2 pins and monitor to detect when the state of either is ***SRC.Open***.

The port ***shall*** supply VBUS current at the level it advertises on ***Rp***. The port ***shall not*** drive VCONN.

The port ***shall*** connect any orientation specific debug signals for ***Debug Accessory Mode*** operation only after entry to this state. Any non-orientation specific debug signals for ***Debug Accessory Mode*** operation ***shall*** be connected or remain connected in this state.

If the port needs to establish ***USB PD*** communications, it ***shall*** do so only after entry to this state. The port ***shall not*** initiate any ***USB PD*** communications until VBUS reaches ***vSafe5V***. In this state, the port takes on the initial ***USB PD*** role of DFP/Source.

4.5.2.2.18.2 Exiting from OrientedDebugAccessory.SRC State

If the port is a Source, the port ***shall*** transition to ***Unattached.SRC*** when the ***SRC.Open*** state is detected on either the CC1 or CC2 pin.

If the port is a DRP, the port ***shall*** transition to ***Unattached.SNK*** when the ***SRC.Open*** state is detected on either the CC1 or CC2 pin.

4.5.2.2.19 DebugAccessory.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-16 and Figure 4-17.

The ***DebugAccessory.SNK*** state is used for the ***Debug Accessory Mode*** specified in Appendix B.

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4.5.2.2.19.1 DebugAccessory.SNK State Requirements

This mode is for debug only and ***shall not*** be used for communicating with commercial products.

The port ***shall not*** drive VBUS or VCONN.

The port ***shall*** provide an ***Rd*** as specified in Table 4-28 on both the CC1 and CC2 pins.

If supported, orientation is determined as outlined in Section B.2.6.1.1. The port ***shall*** connect any debug signals for ***Debug Accessory Mode*** operation only after entry to this state.

4.5.2.2.19.2 Exiting from DebugAccessory.SNK State

The port ***shall*** transition to ***Unattached.SNK*** when VBUS is no longer present.

4.5.2.2.20 PoweredAccessory State

This state appears in Figure 4-14.

When in the ***PoweredAccessory*** state, the port is powering a ***VCONN-Powered Accessory*** or ***VCONN-Powered USB Device***.

4.5.2.2.20.1 PoweredAccessory State Requirements

If the port needs to determine the orientation of the connector, it ***shall*** do so only upon entry to the ***PoweredAccessory*** state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., which CC pin is in the ***SRC.Rd*** state).

The ***SRC.Rd*** state is detected on only one of the CC1 or CC2 pins. The port ***shall*** advertise either 1.5 A or 3.0 A (see Table 4-27) on this CC pin and monitor its state.

The port ***shall*** supply VCONN on the unused CC pin within ***tVCONNON-PA*** of entering the ***PoweredAccessory*** state.

The port ***shall not*** drive VBUS.

When the port initially enters the ***PoweredAccessory*** state it ***shall*** operate as a ***USB Power Delivery*** Source with a DFP data role. In addition, the port ***shall*** support at least one of the following:

- Use ***USB PD*** to establish an explicit contract and then use Structured Vendor Defined Messages (Structured VDMs) to identify a ***VCONN-Powered Accessory*** and enter an ***Alternate Mode***.
- Use ***USB PD*** to query the identity of a ***VCONN-Powered USB Device*** (that operates as a cable plug responding to SOP').

4.5.2.2.20.2 Exiting from PoweredAccessory State

The port ***shall*** transition to ***Unattached.SNK*** when the ***SRC.Open*** state is detected on the monitored CC pin.

The port ***shall*** transition to ***Try.SNK*** if the attached device is not a ***VCONN-Powered Accessory*** or ***VCONN-Powered USB Device***. For example, the attached device does not support ***USB PD*** or does not respond to ***USB PD*** commands required for a ***VCONN-Powered Accessory*** (e.g., Discover SVIDs, Discover Modes, etc.) or is a Sink or DRP attached through a Powered Cable.

The port ***shall*** transition to ***Unsupported.Accessory*** if the attached device is a ***VCONN-Powered Accessory*** but the port has not successfully entered an ***Alternate Mode*** within ***tAMETimeout*** (see Appendix E).

A port that supports Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTUnattached.SNK*** if the connected device identifies itself as a Charge-Through ***VCONN-Powered USB Device*** in its ***Discover***

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Identity Command response. The port ***may*** delay this transition in order to perform further SOP' communication.

The port ***shall*** cease to supply VCONN within ***tVCONNOFF*** of exiting the ***PoweredAccessory*** state unless it is transitioning into the ***CTUnattached.SNK*** state.

4.5.2.2.21 Unsupported.Accessory State

This state appears in Figure 4-14.

If a ***VCONN-Powered Accessory*** does not enter an ***Alternate Mode***, the ***Unsupported.Accessory*** state is used to wait until the accessory is unplugged before continuing.

4.5.2.2.21.1 Unsupported.Accessory State Requirements

Only one of the CC1 or CC2 pins ***shall*** be in the ***SRC.Rd*** state. The port ***shall*** advertise Default USB Power (see Table 4-27) on this CC pin and monitor its voltage.

The port ***shall not*** drive VBUS or VCONN.

A Sink with either ***VCONN-Powered Accessory*** or ***VCONN-Powered USB Device*** support ***shall*** provide user notification that it does not recognize or support the attached accessory or device.

4.5.2.2.21.2 Exiting from Unsupported.Accessory State

The port ***shall*** transition to ***Unattached.SNK*** when the ***SRC.Open*** state is detected on the monitored CC pin.

4.5.2.2.22 CTUnattached.VPD State

This state appears in Figure 4-18.

When in the ***CTUnattached.VPD*** state, the Charge-Through ***VCONN-Powered USB Device*** has detected ***SNK.Open*** on its host port for ***tVPDCTDD***, indicating that it is connected to a Charge-Through capable Source, and is independently monitoring its Charge-Through port for the presence of a pass-through Power Source.

This state ***may*** also have been entered through detach of a Power Source on the Charge-Through port or detach of a sink from the ***CTVPD***'s Charge-through port.

4.5.2.2.22.1 CTUnattached.VPD State Requirements

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through ***VCONN-Powered USB Device*** ***shall*** ensure that it is powered by VCONN, does not consume more than ICCS (***USB 3.2***) / ICCSH (***USB 2.0***) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

Upon entry into this state, the device ***shall*** remove its ***Rd*** termination to ground (if present) on the Host-side port CC and provide an ***Rp*** termination advertising 3.0 A instead, as specified in Table 4-27. Note that because VBUS is not provided, the ***Rp*** termination signals continued connection to the port partner but does not carry with it any current advertisement.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** only respond to ***USB PD Discover Identity*** queries on SOP' on its Host-side port. It ***shall*** ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in ***USB PD***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** independently terminate both the Charge-Through port's CC1 and CC2 pins to ground through ***Rd***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** provide a bypass capacitance of CCTB on the Charge-Through Port's VBUS pins.

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4.5.2.2.22.2 Exiting from CTUnattached.VPD State

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTAttachWait.VPD*** when a Source connection is detected on the Charge-Through port, as indicated by the ***SNK.Rp*** state on exactly one of the Charge-Through port's CC pins.

Debug accessories are not supported on the Charge-Through port.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***Unattached.SNK*** if VCONN falls below ***vVCONNDisconnect***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTUnattached.Unsupported*** within ***tDRPTransition*** after the state of both the Charge-Through port's CC1 and CC2 pins is ***SNK.Open*** for ***tDRP*** – ***dcSRC.DRP*** · ***tDRP***, or if directed.

4.5.2.2.23 CTAttachWait.VPD State

This state appears in Figure 4-18.

When in the ***CTAttachWait.VPD*** state, the device has detected the ***SNK.Rp*** state on exactly one of its Charge-Through port's CC pins and is waiting for VBUS on the Charge-Through port.

4.5.2.2.23.1 CTAttachWait.VPD State Requirements

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through ***VCONN-Powered USB Device*** ***shall*** ensure that it is powered by VCONN, does not consume more than ICCS (***USB 3.2***) / ICCSH (***USB 2.0***) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** maintain its ***Rp*** termination advertising 3.0 A on the Host-side port's CC pin, as well as the independent terminations to ground through ***Rd*** on the Charge-Through port's CC1 and CC2 pins.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** only respond to ***USB PD Discover Identity*** queries on SOP' on its Host-side port and complete any active queries prior to exiting this state. It ***shall*** ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in ***USB PD***.

4.5.2.2.23.2 Exiting from CTAttachWait.VPD State

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTUnattached.VPD*** when the state of both the Charge-Through port's CC1 and CC2 pins are ***SNK.Open*** for at least ***tPDDebounce***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTAttached.VPD*** after the state of only one of the Charge-Through port's CC1 or CC2 pins is ***SNK.Rp*** for at least ***tCCDebounce*** and VBUS on the Charge-Through port is detected.

Note the Charge-Through Source ***may*** initiate ***USB PD*** communications which will cause brief periods of the ***SNK.Open*** state on one of the Charge-Through port's CC pins with the state of the Charge-Through port's other CC pin remaining ***SNK.Open***, but this event will not exceed ***tPDDebounce***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTDisabled.VPD*** if VCONN falls below ***vVCONNDisconnect***.

4.5.2.2.24 CTAttached.VPD State

This state appears in Figure 4-18.

When in the ***CTAttached.VPD*** state, the Charge-Through ***VCONN-Powered USB Device*** has detected a Power Source on its Charge-Through port and has connected the Charge-Through port's CC and VBUS pins directly to

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the Host-side port's CC and VBUS pins. Hence all power delivery, negotiation and ***USB PD*** communication are performed directly between the unit on Host-side port and the Power Source connected to the Charge-Through port.

4.5.2.2.24.1 CTAttached.VPD State Requirements

Upon entry to this state, the Charge-Through ***VCONN-Powered USB Device*** ***shall*** detect which of the Charge-Through port's CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the ***SNK.Rp*** state). The device ***shall*** then immediately, in the following order:

1. Remove or reduce any additional capacitance on the Host-side CC port that was introduced in order to meet cReceiver as defined in ***USB PD*** to present on CC a value equal to or less than two times the maximum value for cCablePlug_CC.
2. Disable the ***Rp*** termination advertising 3.0 A on the host port's CC pin.
3. Passively multiplex the detected Charge-Through port's CC pin through to the host port's CC pin with an impedance of less than RccCON.
4. Disable the ***Rd*** on the Charge-Through port's CC1 and CC2 pins.
5. Connect the Charge-Through port's VBUS through to the host port's VBUS.

These steps ***shall*** be completed within ***tVPDDetach*** minimum of entering this state.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** ensure that it is powered by VCONN, does not consume more than ICCS (***USB 3.2***) / ICCSH (***USB 2.0***) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

The Charge-Through ***VCONN-Powered USB Device*** ***shall not*** respond to any ***USB PD*** communication on any CC pin in this state. Any active queries on SOP' ***shall*** have been completed prior to entering this state.

4.5.2.2.24.2 Exiting from CTAttached.VPD State

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTUnattached.VPD*** when VBUS falls below ***vSinkDisconnect*** and the state of the passed-through CC pin is ***SNK.Open*** for ***tVPDCTDD***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTDisabled.VPD*** if VCONN falls below ***vVCONNDisconnect***.

4.5.2.2.25 CTDisabled.VPD State

This state appears in Figure 4-18.

When in the ***CTDisabled.VPD*** state, the Charge-Through ***VCONN-Powered USB Device*** has detected the detach on its Host-side port but ***may*** still potentially be connected to a Power Source on the Charge-Through port, and is thus ensuring that the VBUS from the Power Source is removed.

4.5.2.2.25.1 CTDisabled.VPD State Requirements

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** isolate its Host-side port from its Charge-Through port, including CCs and VBUS.

The device ***shall*** present a high-impedance to ground (above ***zOPEN***) on the Host-side port's CC pin and on the Charge-Through port CC1 and CC2 pins.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** ensure that it is powered entirely by VBUS.

4.5.2.2.25.2 Exiting from CTDisabled.VPD State

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***Unattached.SNK*** after ***tVPDDisable***.

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4.5.2.2.26 CTUnattached.SNK State

This state appears in Figure 4-14, Figure 4-16 and Figure 4-17.

When in the ***CTUnattached.SNK*** state, the port has detected that it is attached to a Charge-Through ***VCONN-Powered USB Device*** and is ready if a Power Source is attached to the Charge-Through ***VCONN-Powered USB Device***.

This state ***may*** also have been entered through detach of a Charge-Through Power Source.

4.5.2.2.26.1 CTUnattached.SNK State Requirements

Upon entry to this state, the port ***shall*** remove its ***Rp*** termination (if present) and terminate CC to ground through ***Rd***.

The port ***shall*** continue to supply VCONN.

The port ***shall*** stop sourcing or sinking VBUS and discharge it.

In ***USB PD*** Version 2.0, the port ***shall*** initiate PD messages.

The port ***may*** query the state of the attached ***VCONN-Powered USB Device*** by sending SOP' messages on ***USB PD*** to read the ***VPD***'s eMarker.

4.5.2.2.26.2 Exiting from CTUnattached.SNK State

The port ***shall*** transition to ***CTAttached.SNK*** when VBUS is detected. Note that by this point, the ***VCONN-Powered USB Device*** has already de-bounced the passed-through CC pin.

The port ***shall*** transition to ***Unattached.SNK*** if the state of the CC pin is ***SNK.Open*** for ***tVPDDetach*** after VBUS is ***vSafe0V***.

4.5.2.2.27 CTAttached.SNK State

This state appears in Figure 4-14, Figure 4-16 and Figure 4-17.

When in the ***CTAttached.SNK*** state, the port is connected to a Charge-Through ***VCONN-Powered USB Device***, which in turn is passing through the connection to a Power Source.

4.5.2.2.27.1 CTAttached.SNK State Requirements

The port ***shall*** continue to terminate CC to ground through ***Rd***. Since there is now a Power Source connected through to VBUS and CC, the port ***shall*** operate in one of the ***Sink Power Sub-States*** shown in Figure 4-19, and remain within the ***Sink Power Sub-States***, until either VBUS is removed, or a ***USB PD*** contract is established with the source.

The port ***shall not*** negotiate a voltage on VBUS higher than the maximum voltage specified in the Charge-Through ***VCONN-Powered USB Device***'s ***Discover Identity*** Command response.

The port ***shall*** continue to supply VCONN.

The port ***shall*** reject a VCONN swap request.

The port ***shall not*** perform ***USB BC 1.2*** primary detection, as that will interfere with ***VPD*** functionality.

In ***USB PD*** Version 2.0, the port ***shall not*** initiate ***USB PD*** messages, although it remains a DFP for USB data.

The port ***shall*** neither initiate nor respond to any SOP' communication.

The port ***shall*** meet the ***Sink Power Sub-State*** requirements specified in Section 4.5.2.3.

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The port ***shall*** meet the additional maximum current constraints described in Section 4.6.2.5.

The port ***shall*** follow the restrictions on ***USB PD*** messages described in Section 4.10.2.

The port ***shall*** alter its advertised capabilities to UFP role/sink only role as described in Section 4.10.2.

4.5.2.2.27.2 Exiting from CTAttached.SNK State

A port that is not in the process of a ***USB PD*** Hard Reset ***shall*** transition to ***CTUnattached.SNK*** within ***tSinkDisconnect*** when VBUS falls below ***vSinkDisconnect*** for VBUS operating at or below 5 V or below ***vSinkDisconnectPD*** when negotiated by ***USB PD*** to operate above 5 V.

A port that has entered into ***USB PD*** communications with the Source and has seen the CC voltage exceed ***vRd-USB*** ***may*** monitor the CC pin to detect cable disconnect in addition to monitoring VBUS.

A port that is monitoring the CC voltage for disconnect ***shall*** transition to ***CTUnattached.SNK*** within ***tSinkDisconnect*** after the CC voltage remains below ***vRd-USB*** for ***tPDDebounce***.

4.5.2.2.28 CTUnattached.Unsupported State

This state appears in Figure 4-18.

When in the ***CTUnattached.Unsupported*** state, the Charge-Through ***VCONN-Powered USB Device*** has previously detected ***SNK.Open*** on its host port for ***tVPDCTDD***, indicating that it is connected to a Charge-Through Capable Source, and is now monitoring its Charge-Through port for the presence of an unsupported sink.

A Charge-Through ***VCONN-Powered USB Device*** does not support Sinks or ***Debug Accessory Mode***.

4.5.2.2.28.1 CTUnattached.Unsupported State Requirements

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through ***VCONN-Powered USB Device*** ***shall*** ensure that it is powered by VCONN, does not consume more than ICCS (***USB 3.2***) / ICCSH (***USB 2.0***) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

Upon entry into this state, the Charge-Through ***VCONN-Powered USB Device*** ***shall*** maintain its ***Rp*** termination advertising 3.0 A on the Host-side port's CC pin, remove its ***Rd*** terminations to ground on the Charge-Through port's CC1 and CC2 pins, and provide a ***Rp*** termination advertising Default USB Power instead.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** only respond to ***USB PD Discover Identity*** queries on SOP' on its Host-side port. It ***shall*** ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in ***USB PD***.

4.5.2.2.28.2 Exiting from CTUnattached.Unsupported State

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTAttachWait.Unsupported*** when a Sink connection is detected on the Charge-Through port, as indicated by the ***SRC.Rd*** state on at least one of the Charge-Through port's CC pins or ***SRC.Ra*** state on both the CC1 and CC2 pins.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***Unattached.SNK*** if VCONN falls below ***vVCONNDisconnect***.

Otherwise, a Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTUnattached.VPD*** within ***tDRPTransition*** after ***dcSRC.DRP*** · ***tDRP***, or if directed.

4.5.2.2.29 CTAttachWait.Unsupported State

This state appears in Figure 4-18.

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The ***CTAttachWait.Unsupported*** state is used to ensure that the state of both the Charge-Through Port's CC1 and CC2 pins are stable for at least ***tCCDebounce***.

4.5.2.2.29.1 CTAttachWait.Unsupported State Requirements

The requirements for this state are identical to ***CTUnattached.Unsupported*** state.

4.5.2.2.29.2 Exiting from CTAttachWait.Unsupported State

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTTry.SNK*** if the state of at least one of the Charge-Through port's CC pins is ***SRC.Rd***, or if the state of both the CC1 and CC2 pins is ***SRC.Ra*** for at least ***tCCDebounce***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTUnattached.VPD*** when the state of either the Charge-Through Port's CC1 or CC2 pin is ***SRC.Open*** for at least ***tCCDebounce***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***Unattached.SNK*** if VCONN falls below ***vVCONNDisconnect***.

4.5.2.2.30 CTTry.SNK State

This state appears in Figure 4-18.

When in the ***CTTry.SNK*** state, the Charge-Through ***VCONN-Powered USB Device*** is querying to determine if the port partner on the Charge-Through port supports the source role.

4.5.2.2.30.1 CTTry.SNK State Requirements

The requirements for this state are identical to ***CTUnattached.VPD*** state.

4.5.2.2.30.2 Exiting from CTTry.SNK State

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** wait for ***tDRPTry*** and only then begin monitoring the Charge-Through port's CC pins for the ***SNK.Rp*** state.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** then transition to ***CTAttached.VPD*** when the ***SNK.Rp*** state is detected on the Charge-Through port's CC pins for at least ***tTryCCDebounce*** and VBUS is detected on Charge-Through port.

A Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTAttached.Unsupported*** if ***SNK.Rp*** state is not detected for ***tDRPTryWait***.

Note: The Source ***may*** initiate ***USB PD*** communications which will cause brief periods of the ***SNK.Open*** state on both the CC1 and CC2 pins, but this event will not exceed ***tTryCCDebounce***.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***Unattached.SNK*** if VCONN falls below ***vVCONNDisconnect***.

4.5.2.2.31 CTAttached.Unsupported State

This state appears in Figure 4-18.

If the port partner to the Charge-Through ***VCONN-Powered USB Device***'s Charge-Through port either does not support the source power role, or failed to negotiate the source role, the ***CTAttached.Unsupported*** state is used to wait until that device is unplugged before continuing.

4.5.2.2.31.1 CTAttached.Unsupported State Requirements

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through ***VCONN-Powered USB Device*** ***shall*** ensure that it is

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powered by VCONN, does not consume more than ICCS (***USB 3.2***) / ICCSH (***USB 2.0***) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

Upon entry into this state, the Charge-Through ***VCONN-Powered USB Device*** ***shall*** maintain its ***Rp*** termination advertising 3.0 A on the Host-side port's CC pin, remove its ***Rd*** terminations to ground on the Charge-Through port's CC1 and CC2 pins, and provide a ***Rp*** termination advertising Default USB Power instead.

At least one of the CC1 or CC2 pins will be in the ***SRC.Rd*** state or both will be in the ***SRC.Ra*** state. The Charge-Through port ***shall*** advertise Default USB Power (see Table 4-27) on its CC pins and monitor their voltage.

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** present a ***USB Billboard Device Class*** interface indicating that it does not recognize or support the attached accessory or device.

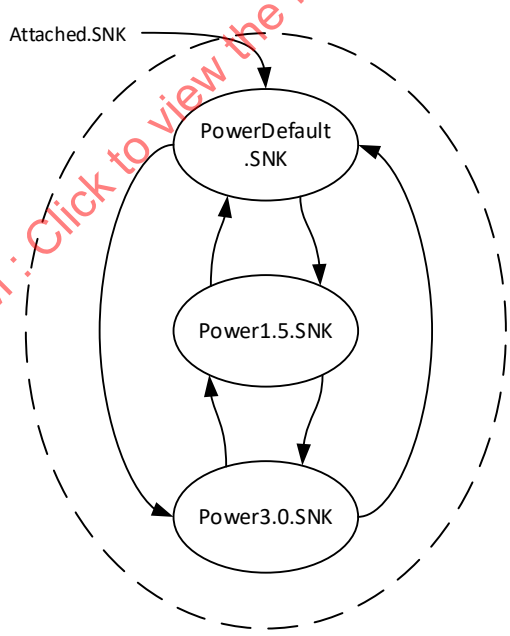
4.5.2.2.31.2 Exiting from CTAttached.Unsupported State

The Charge-Through ***VCONN-Powered USB Device*** ***shall*** transition to ***CTUnattached.VPD*** when ***SRC.Open*** state is detected on both the Charge-Through port's CC pins or the ***SRC.Open*** state is detected on one CC pin and ***SRC.Ra*** is detected on the other CC pin.

4.5.2.3 Sink Power Sub-State Requirements

When in the ***Attached.SNK*** or ***CTAttached.SNK*** states and the Source is supplying default VBUS, the port ***shall*** operate in one of the sub-states shown in Figure 4-19. The initial ***Sink Power Sub-State*** is ***PowerDefault.SNK***. Subsequently, the ***Sink Power Sub-State*** is determined by Source's USB Type-C current advertisement. The port in ***Attached.SNK*** ***shall*** remain within the ***Sink Power Sub-States*** until either VBUS is removed, or a ***USB PD*** contract is established with the Source.

Figure 4-19 Sink Power Sub-States



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The Sink is only required to implement ***Sink Power Sub-State*** transitions if the Sink wants to consume more than default USB current.

Note that for the ***CTAttached.SNK*** state, there are further limitations on maximum current (see Section 4.6.2.5).

4.5.2.3.1 PowerDefault.SNK Sub-State

This sub-state supports Sinks consuming current within the lowest range (default) of Source-supplied current.

4.5.2.3.1.1 PowerDefault.SNK Sub-State Requirements

The port ***shall*** draw no more than the default USB power from VBUS. See Section 4.6.2.1.

If the port wants to consume more than the default USB power, it ***shall*** monitor ***vRd*** to determine if more current is available from the Source.

4.5.2.3.1.2 Exiting from PowerDefault.SNK Sub-State

For any change in ***vRd*** indicating a change in allowable power, the port ***shall not*** transition until the new ***vRd*** has been stable for at least ***tRpValueChange***.

For a ***vRd*** in the ***vRd-1.5*** range, the port ***shall*** transition to the ***Power1.5.SNK*** Sub-State.

For a ***vRd*** in the ***vRd-3.0*** range, the port ***shall*** transition to the ***Power3.0.SNK*** Sub-State.

4.5.2.3.2 Power1.5.SNK Sub-State

This sub-state supports Sinks consuming current within the two lower ranges (default and 1.5 A) of Source-supplied current.

4.5.2.3.2.1 Power1.5.SNK Sub-State Requirements

The port ***shall*** draw no more than 1.5 A from VBUS.

The port ***shall*** monitor ***vRd*** while it is in this sub-state.

4.5.2.3.2.2 Exiting from Power1.5.SNK Sub-State

For any change in ***vRd*** indicating a change in allowable power, the port ***shall not*** transition until the new ***vRd*** has been stable for at least ***tRpValueChange***.

For a ***vRd*** in the ***vRd-USB*** range, the port ***shall*** transition to the ***PowerDefault.SNK*** Sub-State and reduce its power consumption to the new range within ***tSinkAdj***.

For a ***vRd*** in the ***vRd-3.0*** range, the port ***shall*** transition to the ***Power3.0.SNK*** Sub-State.

4.5.2.3.3 Power3.0.SNK Sub-State

This sub-state supports Sinks consuming current within all three ranges (default, 1.5 A and 3.0 A) of Source-supplied current.

4.5.2.3.3.1 Power3.0.SNK Sub-State Requirements

The port ***shall*** draw no more than 3.0 A from VBUS.

The port ***shall*** monitor ***vRd*** while it is in this sub-state.

4.5.2.3.3.2 Exiting from Power3.0.SNK Sub-State

For any change in ***vRd*** indicating a change in allowable power, the port ***shall not*** transition until the new ***vRd*** has been stable for at least ***tRpValueChange***.

For a ***vRd*** in the ***vRd-USB*** range, the port ***shall*** transition to the ***PowerDefault.SNK*** Sub-State and reduce its power consumption to the new range within ***tSinkAdj***.

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For a ***vRd*** in the ***vRd-1.5*** range, the port ***shall*** transition to the ***Power1.5.SNK*** Sub-State and reduce its power consumption to the new range within ***tSinkAdj***.

4.5.2.4 Cable eMarker State Machine Requirements

Figure 4-20 and Figure 4-21 illustrate the cable eMarker connection state diagrams for passive and active cables, respectively.

Figure 4-20 Passive Cable eMarker State Diagram

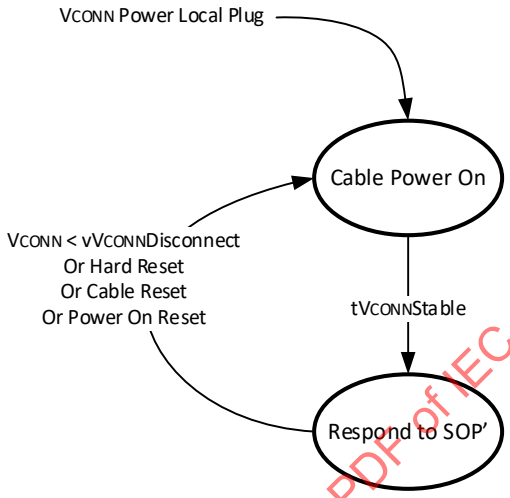
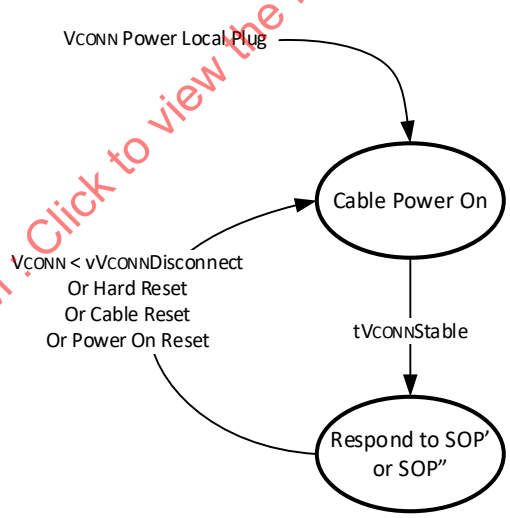


Figure 4-21 Active Cable eMarker State Diagram



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4.5.2.4.1 Cable Power On State

This state appears in Figure 4-20. This is the initial power on state for each eMarker in the cable when VCONN is applied.

4.5.2.4.1.1 Cable Power On State Requirements

Each eMarker in the cable ***shall*** power on.

The cable ***shall not*** respond to SOP' and SOP" commands in this state.

4.5.2.4.1.2 Exiting from Cable Power On State

Each eMarker in a passive or active cable ***shall*** transition to Assign Cable SOP* when it has completed its boot process. Each eMarker ***shall*** transition to Assign Cable SOP* within ***tVCONNStable***.

4.5.2.4.2 Respond to SOP'/SOP" State

This state appears in Figure 4-20 and Figure 4-21.

A passive cable has only one eMarker powered at a time. This cable eMarker in a passive cable ***shall*** respond to SOP' in this state.

Each cable eMarker in an active cable ***shall*** respond to a pre-set SOP' or SOP''. If only one eMarker exists in the cable, it ***shall*** only respond to SOP'.

Cable designers ***shall*** ensure that the eMarker works correctly in the presence of ground and VCONN maximum IR drop.

4.5.2.4.2.1 Respond to SOP'/SOP" State Requirements

Each eMarker in the passive or active cable ***shall*** be able to respond to any ***USB PD*** communication sent to its pre-set SOP' or SOP''. For a passive cable, only one eMarker ***should*** be powered at a time and ***shall*** respond to SOP' only. If two eMarkers exist in a passive or active cable and are powered at the same time, then only one ***shall*** respond to SOP' and the other ***shall*** respond to SOP''. The assignment of SOP' and SOP'' is fixed for each eMarker in a cable and ***shall not*** be dynamically set when power is applied to VCONN.

4.5.2.4.2.2 Exiting from Respond to SOP'/SOP" State

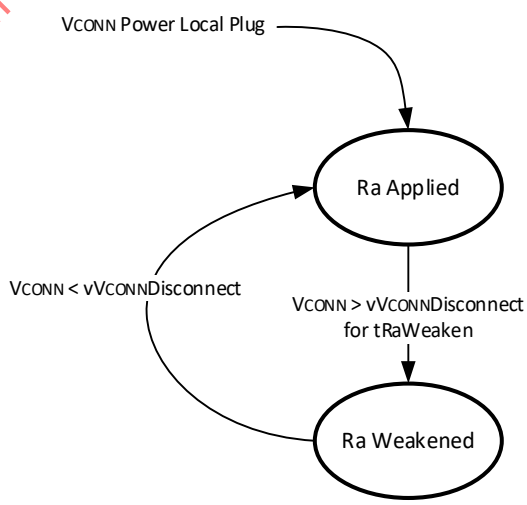
Each eMarker in the cable ***shall*** transition to Cable Power On upon sensing VCONN less than ***vVCONNDisconnect*** or upon a Power On Reset event.

Each eMarker in the cable ***shall*** transition to Cable Power On upon sensing a Hard Reset or Cable Reset.

4.5.2.5 Cable Ra Management State Machine Requirements

Figure 4-22 illustrates the cable eMarker state diagram for applying and weakening or removing ***Ra***. This state machine runs independently from the Cable eMarker state machine described in Section 4.5.2.4.

Figure 4-22 Cable Ra Management State Diagram



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4.5.2.5.1 Ra Applied State

This state appears in Figure 4-22. This is the initial state at power on for each eMarker in the cable.

4.5.2.5.1.1 Ra Applied State Requirements

Each eMarker in the cable ***shall*** apply ***Ra*** to VCONN within ***tRaReconnect***.

4.5.2.5.1.2 Exiting from Ra Applied State

Each eMarker in a passive or active cable ***shall*** transition to the ***Ra*** Weakened state when VCONN is greater than ***vVCONNDisconnect*** for ***tRaWeaken***.

4.5.2.5.2 Ra Weakened State

This state appears in Figure 4-22.

4.5.2.5.2.1 Ra Weakened State Requirements

The eMarker in the cable ***shall*** remove or weaken ***Ra***.

Passive cables ***shall*** meet the Power for electronically marked passive cables defined in Table 4-6. Active cables ***shall*** meet the Power for Active Cables in Table 4 6.

4.5.2.5.2.2 Exiting from Ra Weakened State

Each eMarker in a passive or active cable ***shall*** transition to the ***Ra*** Applied state when VCONN is below ***vVCONNDisconnect***.

4.5.2.6 Connection States Summary

Table 4-18 defines the mandatory and ***optional*** states for each type of port.

Table 4-18 Mandatory and Optional States

	SOURCE	SINK	DRP	*USB PD* Communications
Disabled	***Optional***	***Optional***	***Optional***	Not Permitted
ErrorRecovery	Mandatory[10]	Mandatory[10]	Mandatory[10]	Not Permitted
Unattached.SNK	***N/A***	Mandatory	Mandatory	Not Permitted
AttachWait.SNK	***N/A***	Mandatory[1]	Mandatory	Not Permitted
Attached.SNK	***N/A***	Mandatory	Mandatory	Permitted
UnattachedWait.SRC	Mandatory or ***N/A***[7]	***N/A***	***N/A***	Not Permitted
Unattached.SRC	Mandatory	***N/A***	Mandatory	Not Permitted
AttachWait.SRC	Mandatory	***N/A***	Mandatory	Not Permitted
Attached.SRC	Mandatory	***N/A***	Mandatory	Permitted
Try.SRC[4]	***N/A***	***N/A***	***Optional***	Not Permitted
TryWait.SNK[2]	***N/A***	***N/A***	***Optional***	Not Permitted
Try.SNK[4, 8]	***N/A***	***N/A***	***Optional***	Not Permitted
TryWait.SRC[5, 8]	***N/A***	***N/A***	***Optional***	Not Permitted

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	SOURCE	SINK	DRP	*USB PD* Communications
CorrosionMitigation	***Optional***	***Optional***	***Optional***	Not Permitted
UnorientedDebugAccessory.SRC	Optional[6]	***N/A***	Optional[6]	Not Permitted
OrientedDebugAccessory.SRC	Optional[6]	***N/A***	Optional[6]	Permitted
DebugAccessory.SNK	***N/A***	***Optional***	***Optional***	Permitted
Unattached.Accessory	***N/A***	***Optional***	***N/A***	Not Permitted
AttachWait.Accessory	***N/A***	***Optional***	***N/A***	Not Permitted
PoweredAccessory	***N/A***	***Optional***	***N/A***	Permitted
Unsupported.Accessory[3]	***N/A***	***Optional***	***N/A***	Not Permitted
CTUnattached.VPD	***N/A***	***N/A***	***Optional***	SOP' Permitted
CTAttachWait.VPD[8]	***N/A***	***N/A***	***Optional***	SOP' Permitted
CTAttached.VPD[8]	***N/A***	***N/A***	***Optional***	Not Permitted
CTDisabled.VPD[8]	***N/A***	***N/A***	***Optional***	Not Permitted
CTUnattached.SNK	***N/A***	***N/A***	***Optional***	SOP' Permitted
CTAttached.SNK[9]	***N/A***	***N/A***	***Optional***	Permitted
CTUnattached.Unsupported[8]	***N/A***	***N/A***	***Optional***	SOP' Permitted
CTAttachWait.Unsupported[8]	***N/A***	***N/A***	***Optional***	SOP' Permitted
CTTry.SNK[8]	***N/A***	***N/A***	***Optional***	SOP' Permitted
CTAttached.Unsupported[8]	***N/A***	***N/A***	***Optional***	SOP' Permitted
PowerDefault.SNK	***N/A***	Mandatory	Mandatory	Permitted
Power1.5.SNK	***N/A***	***Optional***	***Optional***	Permitted
Power3.0.SNK	***N/A***	***Optional***	***Optional***	Permitted

Notes:

1. ***Optional*** for UFP applications that are ***USB 2.0***-only, consume USB Default Power and do not support ***USB PD*** or accessories.
2. *TryWait.SNK* is mandatory when *Try.SRC* is supported.
3. *Unsupported.Accessory* is mandatory when *PoweredAccessory* is supported.
4. *Try.SRC* and *Try.SNK* ***shall not*** be supported at the same time, although an unattached device ***may*** dynamically choose between *Try.SRC* and *Try.SNK* state machines based on external factors.
5. *TryWait.SRC* is mandatory when *Try.SNK* is supported.
6. *UnorientedDebugAccessory.SRC* is required for any Source or DRP that supports *Debug Accessory Mode*. *OrientedDebugAccessory.SRC* is only required if orientation detection is necessary in *Debug Accessory Mode*.
7. Mandatory for a DFP that was providing VCONN in the previous *Attached.SRC* state. ***N/A*** for a DFP that was not providing VCONN in the previous *Attached.SRC* state.
8. *CTAttachWait.VPD*, *CTAttached.VPD*, *CTDisabled.VPD*, *Try.SNK*, *TryWait.SRC*, *CTUnattached.Unsupported*, *CTAttachWait.Unsupported*, *CTAttached.Unsupported*, and *CTTry.SNK* are mandatory when *CTUnattached.VPD* is supported.
9. *CTAttached.SNK* is mandatory when *CTUnattached.SNK* is supported.
10. ***Optional*** for non-***USB4*** and non-***USB PD*** implementations

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4.5.3 USB Port Interoperability Behavior

This section describes interoperability behavior between USB Type-C to USB Type-C ports and between USB Type-C to legacy USB ports.

4.5.3.1 USB Type-C Port to USB Type-C Port Interoperability Behaviors

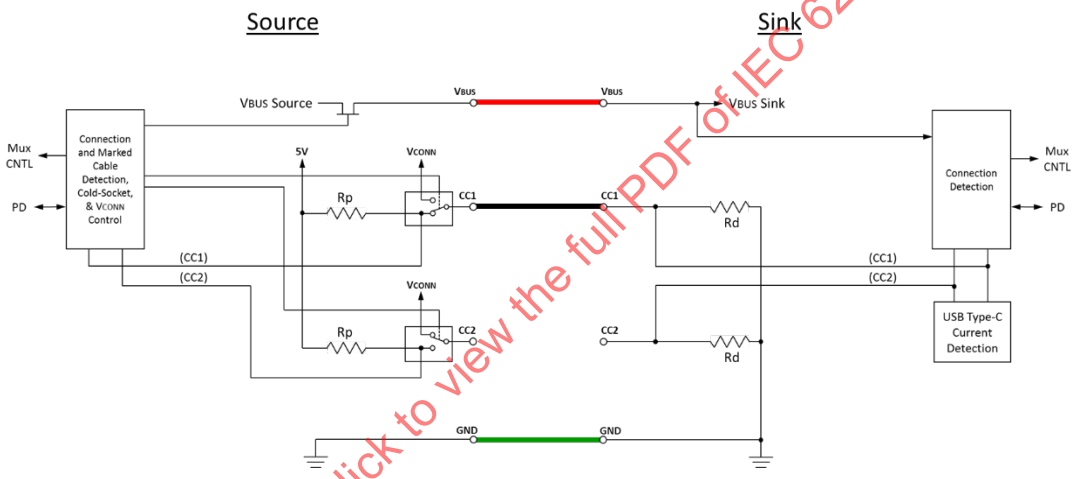
The following sub-sections describe typical port-to-port interoperability behaviors for the various combinations of USB Type-C Source, Sink and DRPs as presented in Table 4-9. In all the described behaviors, the impact of ***USB PD***-based swaps (***PR_Swap***, ***DR_Swap*** or ***VCONN_Swap***) are not considered.

The figures in the following sections illustrate the CC1 and CC2 routing after the CC detection process is complete.

4.5.3.1.1 Source to Sink Behavior

Figure 4-23 illustrates the functional model for a Source connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

Figure 4-23 Source to Sink Functional Model



The following describes the behavior when a Source is connected to a Sink.

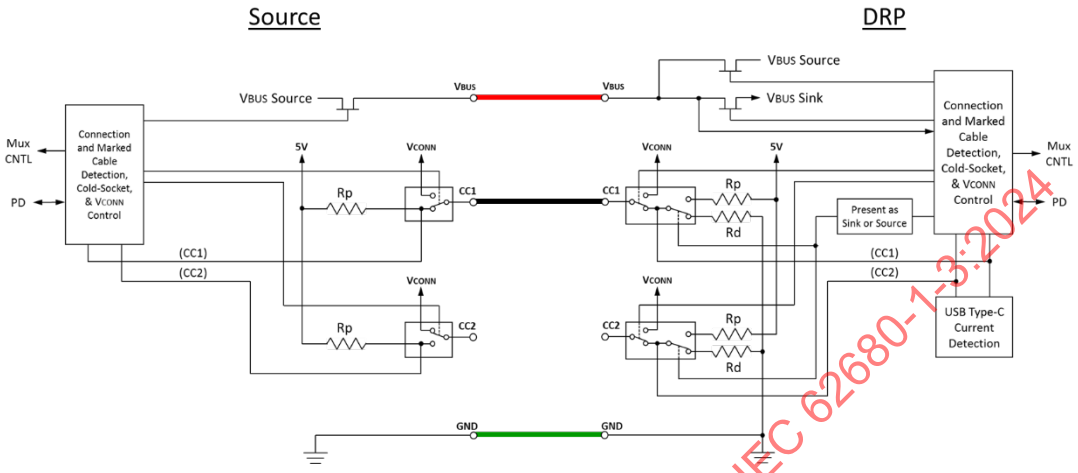
1. Source and Sink in the unattached state.
2. Source transitions from ***Unattached.SRC*** to ***Attached.SRC*** through ***AttachWait.SRC***.
   - Source detects the Sink's pull-down on CC and enters ***Attached.SRC*** through ***AttachWait.SRC***.
   - Source turns on VBUS and VCONN.
3. Sink transitions from ***Unattached.SNK*** to ***Attached.SNK*** through ***AttachWait.SNK***. Sink ***may*** skip ***AttachWait.SNK*** if it is ***USB 2.0*** only and does not support accessories.
   - Sink detects VBUS and enters ***Attached.SNK*** through ***AttachWait.SNK***.
4. While the Source and Sink are in the attached state:
   - Source adjusts ***Rp*** as needed to limit the current the Sink ***may*** draw.
   - Sink detects and monitors ***vRd*** for available current on VBUS.
   - Source monitors CC for detach and when detected, enters ***Unattached.SRC***.
   - Sink monitors VBUS for detach and when detected, enters ***Unattached.SNK***.

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4.5.3.1.2 Source to DRP Behavior

Figure 4-24 illustrates the functional model for a Source connected to a DRP. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

Figure 4-24 Source to DRP Functional Model



The following describes the behavior when a Source is connected to a DRP.

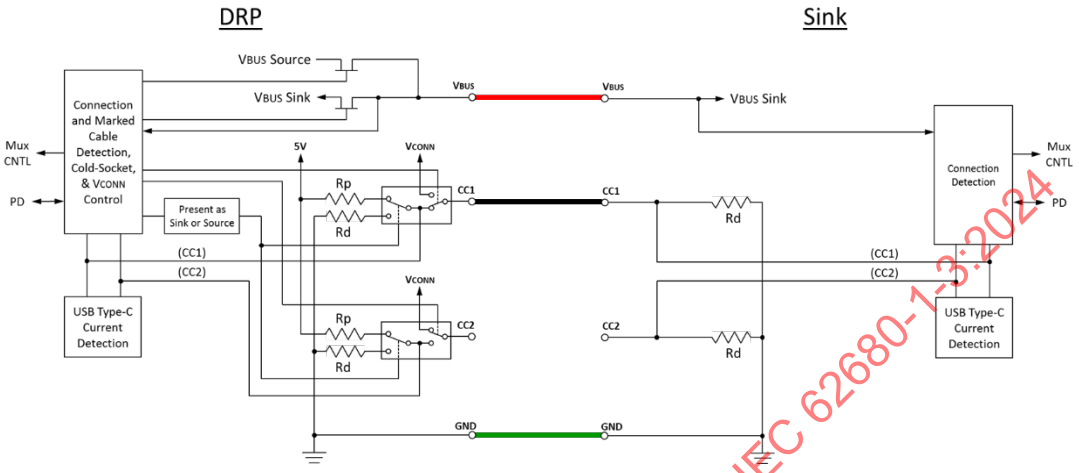
1. Source and DRP in the unattached state.
   - DRP alternates between ***Unattached.SRC*** and ***Unattached.SNK***.
2. Source transitions from ***Unattached.SRC*** to ***Attached.SRC*** through ***AttachWait.SRC***.
   - Source detects the DRP's pull-down on CC and enters ***AttachWait.SRC***. After ***tCCDebounce*** it then enters ***Attached.SRC***.
   - Source turns on VBUS and VCONN.
3. DRP transitions from ***Unattached.SNK*** to ***Attached.SNK*** through ***AttachWait.SNK***.
   - DRP in ***Unattached.SNK*** detects pull up on CC and enters ***AttachWait.SNK***. After that state persists for ***tCCDebounce*** and it detects VBUS, it enters ***Attached.SNK***.
4. While the Source and DRP are in their respective attached states:
   - Source adjusts ***Rp*** as needed to limit the current the DRP (as Sink) ***may*** draw.
   - DRP (as Sink) detects and monitors ***vRd*** for available current on VBUS.
   - Source monitors CC for detach and when detected, enters ***Unattached.SRC***.
   - DRP (as Sink) monitors VBUS for detach and when detected, enters ***Unattached.SNK*** (and resumes toggling between ***Unattached.SNK*** and ***Unattached.SRC***).

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4.5.3.1.3 DRP to Sink Behavior

Figure 4-25 illustrates the functional model for a DRP connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

Figure 4-25 DRP to Sink Functional Model



The following describes the behavior when a DRP is connected to a Sink.

1. DRP and Sink in the unattached state.
   - DRP alternates between ***Unattached.SRC*** and ***Unattached.SNK***.
2. DRP transitions from ***Unattached.SRC*** to ***AttachWait.SRC*** to ***Attached.SRC***.
   - DRP in ***Unattached.SRC*** detects one of the CC pull-downs of Sink which is in ***Unattached.SNK*** and DRP enters ***AttachWait.SRC***.
   - DRP in ***AttachWait.SRC*** detects that pull down on CC persists for ***tCCDebounce***. It then enters ***Attached.SRC*** and turns on VBUS and VCONN.
3. Sink transitions from ***Unattached.SNK*** to ***Attached.SNK*** through ***AttachWait.SNK*** if required.
   - Sink detects VBUS and enters ***Attached.SNK***.
4. While the DRP and Sink are in their respective attached states:
   - DRP (as Source) adjusts ***Rp*** as needed to limit the current the Sink ***may*** draw.
   - Sink detects and monitors ***vRd*** for available current on VBUS.
   - DRP (as Source) monitors CC for detach and when detected, enters ***Unattached.SNK*** (and resumes toggling between ***Unattached.SNK*** and ***Unattached.SRC***).
   - Sink monitors VBUS for detach and when detected, enters ***Unattached.SNK***.

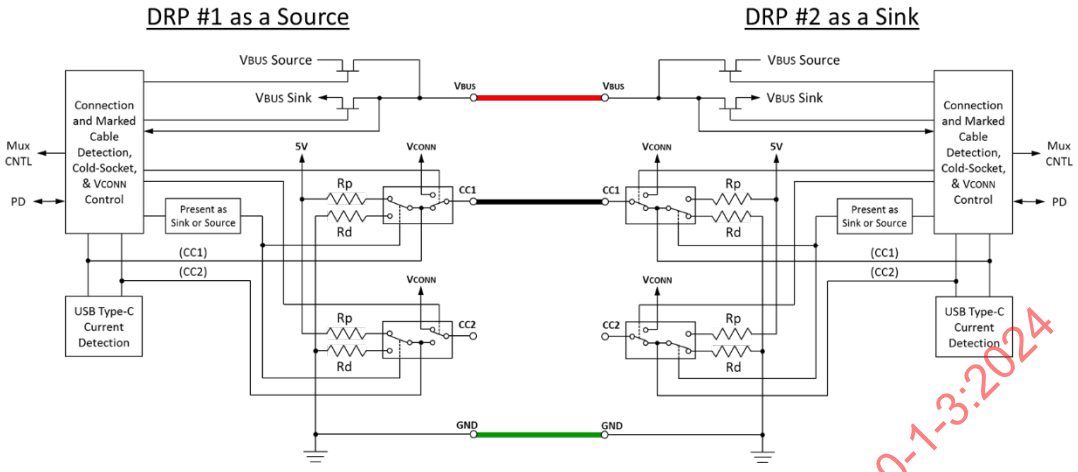
4.5.3.1.4 DRP to DRP Behavior

Two behavior descriptions based on the connection state diagrams are provided below. In the first case, the two DRPs accept the resulting Source-to-Sink relationship achieved randomly whereas in the second case the DRP #2 chooses to drive the random result to the opposite result using the ***Try.SRC*** mechanism.

Figure 4-26 illustrates the functional model for a DRP connected to a DRP in the first case described. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.

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Figure 4-26 DRP to DRP Functional Model – CASE 1



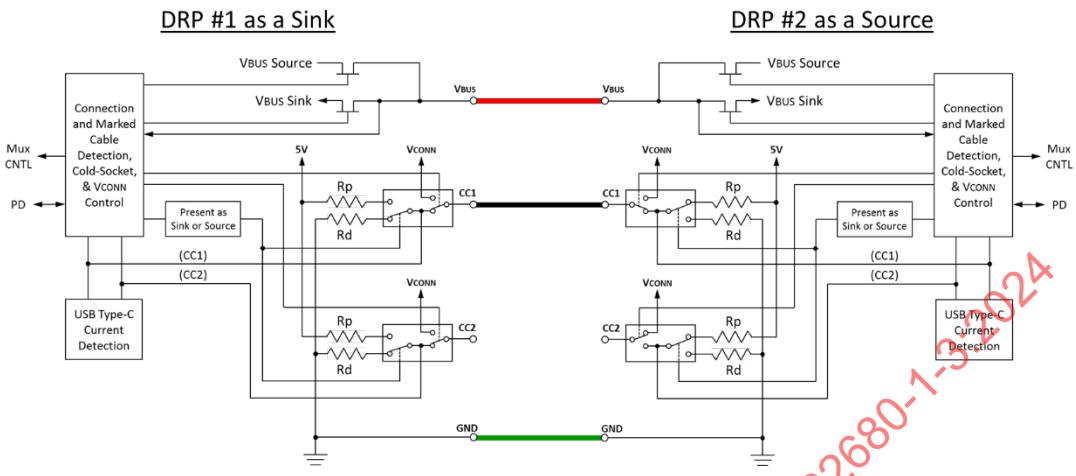
CASE 1: The following describes the behavior when a DRP is connected to another DRP. In this flow, the two DRPs accept the resulting Source-to-Sink relationship achieved randomly.

1. Both DRPs in the unattached state.
   - DRP #1 and DRP #2 alternate between ***Unattached.SRC*** and ***Unattached.SNK***.
2. DRP #1 transitions from ***Unattached.SRC*** to ***AttachWait.SRC***.
   - DRP #1 in ***Unattached.SRC*** detects a CC pull down of DRP #2 in ***Unattached.SNK*** and enters ***AttachWait.SRC***.
3. DRP #2 transitions from ***Unattached.SNK*** to ***AttachWait.SNK***.
   - DRP #2 in ***Unattached.SNK*** detects pull up on a CC and enters ***AttachWait.SNK***.
4. DRP #1 transitions from ***AttachWait.SRC*** to ***Attached.SRC***.
   - DRP #1 in ***AttachWait.SRC*** continues to see CC pull down of DRP #2 for ***tCCDebounce***, enters ***Attached.SRC*** and turns on VBUS and VCONN.
5. DRP #2 transitions from ***AttachWait.SNK*** to ***Attached.SNK***.
   - DRP #2 after having been in ***AttachWait.SNK*** for ***tCCDebounce*** and having detected VBUS, enters ***Attached.SNK***.
6. While the DRPs are in their respective attached states:
   - DRP #1 (as Source) adjusts ***Rp*** as needed to limit the current DRP #2 (as Sink) ***may*** draw.
   - DRP #2 (as Sink) detects and monitors ***vRd*** for available current on VBUS.
   - DRP #1 (as Source) monitors CC for detach and when detected, enters ***Unattached.SNK*** (and resumes toggling between ***Unattached.SNK*** and ***Unattached.SRC***).
   - DRP #2 (as Sink) monitors VBUS for detach and when detected, enters ***Unattached.SNK*** (and resumes toggling between ***Unattached.SNK*** and ***Unattached.SRC***).

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Figure 4-27 illustrates the functional model for a DRP connected to a DRP in the second case described.

Figure 4-27 DRP to DRP Functional Model – CASES 2 & 3



CASE 2: The following describes the behavior when a DRP is connected to another DRP. In this flow, the DRP #2 chooses to drive the random result to the opposite result using the ***Try.SRC*** mechanism.

1. Both DRPs in the unattached state.
   - DRP #1 and DRP #2 alternate between ***Unattached.SRC*** and ***Unattached.SNK***.
2. DRP #1 transitions from ***Unattached.SRC*** to ***AttachWait.SRC***.
   - DRP #1 in ***Unattached.SRC*** detects a CC pull down of DRP #2 in ***Unattached.SNK*** and enters ***AttachWait.SRC***.
3. DRP #2 transitions from ***Unattached.SNK*** to ***AttachWait.SNK***.
   - DRP #2 in ***Unattached.SNK*** detects pull up on a CC and enters ***AttachWait.SNK***.
4. DRP #1 transitions from ***AttachWait.SRC*** to ***Attached.SRC***.
   - DRP #1 in ***AttachWait.SRC*** continues to see CC pull down of DRP #2 for ***tCCDebounce***, enters ***Attached.SRC*** and turns on VBUS and VCONN.
5. DRP #2 transitions from ***AttachWait.SNK*** to ***Try.SRC***.
   - DRP #2 in ***AttachWait.SNK*** has been in this state for ***tCCDebounce*** and detects VBUS but strongly prefers the Source role, so transitions to ***Try.SRC***.
   - DRP #2 in ***Try.SRC*** asserts a pull-up on CC and waits.
6. DRP #1 transitions from ***Attached.SRC*** to ***Unattached.SNK*** to ***AttachWait.SNK***.
   - DRP #1 in ***Attached.SRC*** no longer detects DRP #2's pull-down on CC and transitions to ***Unattached.SNK***.
   - DRP #1 in ***Unattached.SNK*** turns off VBUS and VCONN and applies a pull-down on CC.
   - DRP #1 in ***Unattached.SNK*** detects pull up on a CC and enters ***AttachWait.SNK***.
7. DRP #2 transitions from ***Try.SRC*** to ***Attached.SRC***.
   - DRP #2 in ***Try.SRC*** detects the DRP #1 in ***Unattached.SNK***'s pull-down on CC and enters ***Attached.SRC***.
   - DRP #2 in ***Attached.SRC*** turns on VBUS and VCONN.

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8. DRP #1 transitions from ***AttachWait.SNK*** to ***Attached.SNK***.
    - DRP #1 in ***AttachWait.SNK*** after ***tCCDebounce*** and detecting VBUS, enters ***Attached.SNK***.
9. While the DRPs are in their respective attached states:
    - DRP #2 (as Source) adjusts ***Rp*** as needed to limit the current DRP #1 (as Sink) ***may*** draw.
    - DRP #1 (as Sink) detects and monitors ***vRd*** for available current on VBUS.
    - DRP #2 (as Source) monitors CC for detach and when detected, enters ***Unattached.SNK*** (and resumes toggling between ***Unattached.SNK*** and ***Unattached.SRC***).
    - DRP #1 (as Sink) monitors VBUS for detach and when detected, enters ***Unattached.SNK*** (and resumes toggling between ***Unattached.SNK*** and ***Unattached.SRC***).

CASE 3: The following describes the behavior when a DRP is connected to another DRP. In this flow, the DRP #1 chooses to drive the random result to the opposite result using the ***Try.SNK*** mechanism.

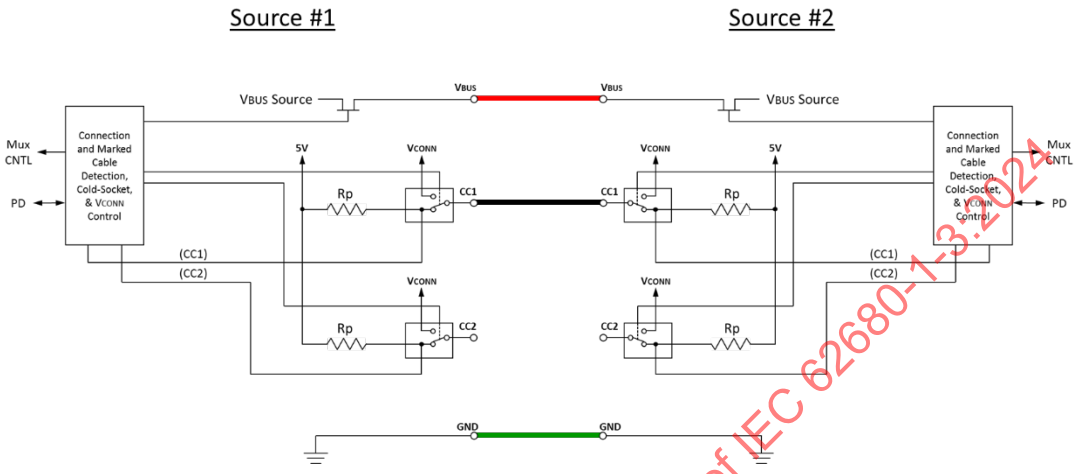
1. Both DRPs in the unattached state.
    - DRP #1 and DRP #2 alternate between ***Unattached.SRC*** and ***Unattached.SNK***.
2. DRP #1 transitions from ***Unattached.SRC*** to ***AttachWait.SRC***.
    - DRP #1 in ***Unattached.SRC*** detects a CC pull down of DRP #2 in ***Unattached.SNK*** and enters ***AttachWait.SRC***.
3. DRP #2 transitions from ***Unattached.SNK*** to ***AttachWait.SNK***.
    - DRP #2 in ***Unattached.SNK*** detects pull up on a CC and enters ***AttachWait.SNK***.
4. DRP #1 transitions from ***AttachWait.SRC*** to ***Try.SNK***.
    - DRP #1 in ***AttachWait.SRC*** has been in this state for ***tCCDebounce*** and detects DRP #2's pull-down on CC but strongly prefers the Sink role, so transitions to ***Try.SNK***.
    - DRP #1 in ***Try.SNK*** asserts a pull down on CC and waits.
5. DRP #2 transitions from ***AttachWait.SNK*** to ***Unattached.SRC*** to ***AttachWait.SRC***.
    - DRP #2 in ***AttachWait.SNK*** no longer detects DRP #1's pull up on CC and transitions to ***Unattached.SRC***.
    - DRP #2 in ***Unattached.SRC*** applies a pull up on CC.
    - DRP #2 in ***Unattached.SRC*** detects a pull down on a CC pin and enters ***AttachWait.SRC***.
    - DRP #1 detects DRP #2's pull up on CC and remains in ***Try.SNK***.
6. DRP #2 transitions from ***AttachWait.SRC*** to ***Attached.SRC***.
    - DRP #2 in ***AttachWait.SRC*** times out (***tCCDebounce***) and transitions to ***Attached.SRC***.
    - DRP #2 in ***Attached.SRC*** turns on VBUS and VCONN.
7. DRP #1 transitions from ***Try.SNK*** to ***Attached.SNK***.
    - DRP #1 in ***Try.SNK*** after detecting VBUS, enters ***Attached.SNK***.
8. While the DRPs are in their respective attached states:
    - DRP #2 (as Source) adjusts ***Rp*** as needed to limit the current DRP #1 (as Sink) ***may*** draw.
    - DRP #1 (as Sink) detects and monitors ***vRd*** for available current on VBUS.
    - DRP #2 (as Source) monitors CC for detach and when detected, enters ***Unattached.SNK*** (and resumes toggling between ***Unattached.SNK*** and ***Unattached.SRC***).
    - DRP #1 (as Sink) monitors VBUS for detach and when detected, enters ***Unattached.SNK*** (and resumes toggling between ***Unattached.SNK*** and ***Unattached.SRC***).

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4.5.3.1.5 Source to Source Behavior

Figure 4-28 illustrates the functional model for a Source connected to a Source. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.

Figure 4-28 Source to Source Functional Model



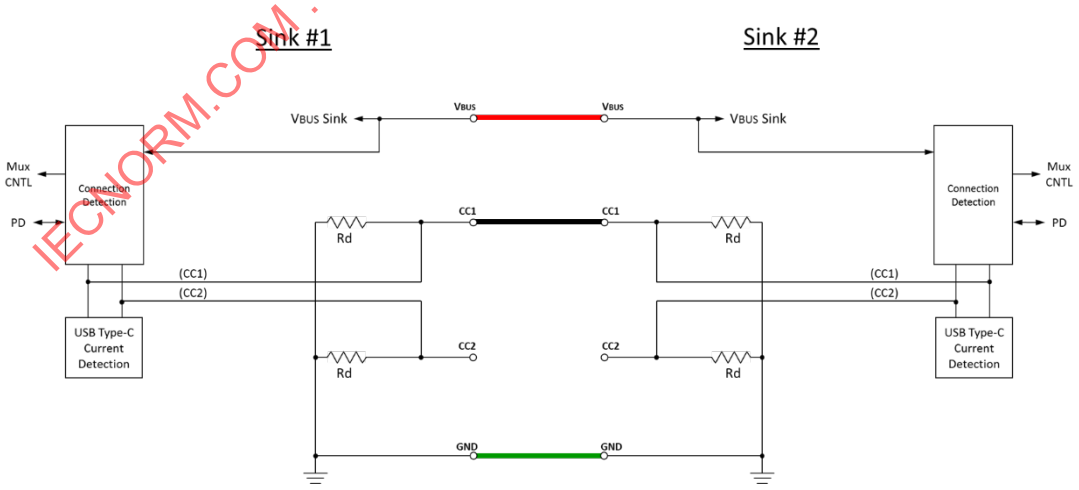
The following describes the behavior when a Source is connected to another Source.

1. Both Sources in the unattached state.
    - Source #1 fails to detect a Sink's pull-down on CC and remains in ***Unattached.SRC***.
    - Source #2 fails to detect a Sink's pull-down on CC and remains in ***Unattached.SRC***.

4.5.3.1.6 Sink to Sink Behavior

Figure 4-29 illustrates the functional model for a Sink connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.

Figure 4-29 Sink to Sink Functional Model



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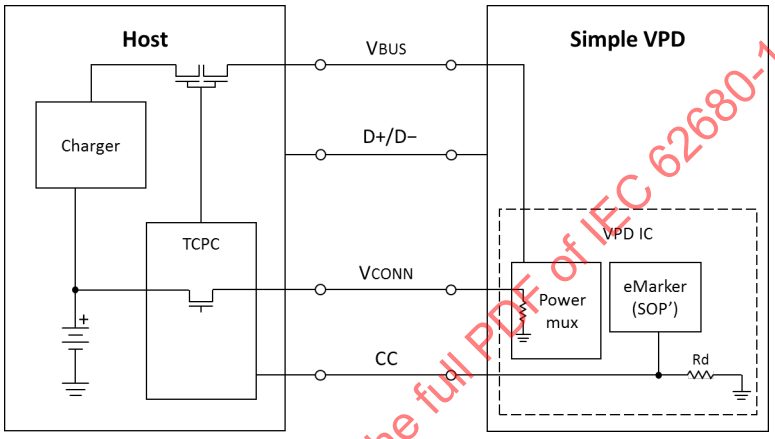
The following describes the behavior when a Sink is connected to another Sink.

1. Both Sinks in the unattached state.
    - Sink #1 fails to detect pull up on CC or VBUS supplied by a Source and remains in ***Unattached.SNK***.
    - Sink #2 fails to detect pull up on CC or VBUS supplied by a Source and remains in ***Unattached.SNK***.

4.5.3.1.7 DRP to VCONN-Powered USB Device (VPD) Behavior

Figure 4-30 illustrates the functional model for a DRP connected to a ***VCONN-Powered USB Device*** that does not feature charge-through functionality.

Figure 4-30 DRP to VPD Model



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The following describes the behavior when a DRP that supports ***VPD***s is connected to a ***VPD***.

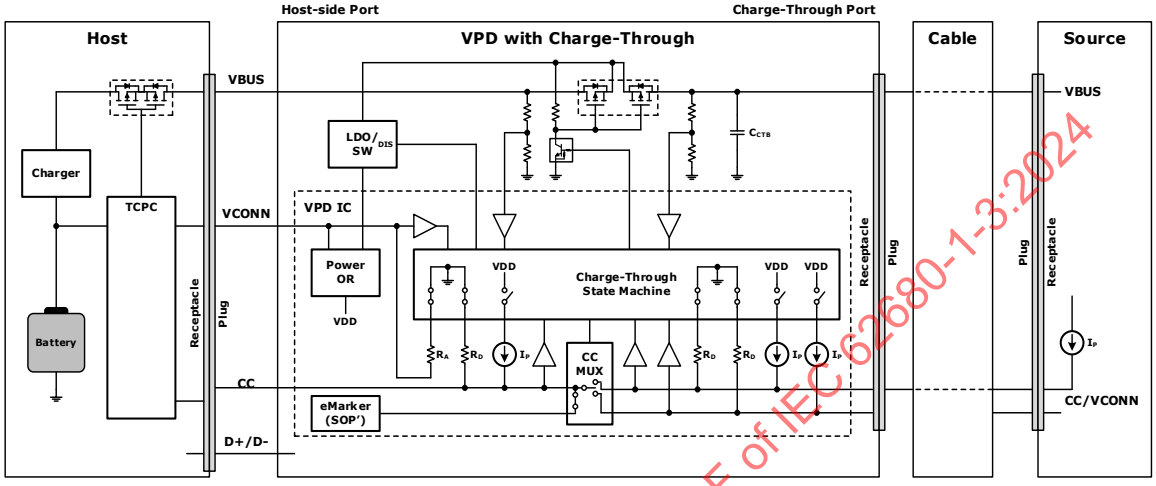
1. DRP and ***VPD*** in the unattached state.
    - DRP alternates between ***Unattached.SRC*** and ***Unattached.SNK***.
2. DRP transitions from ***Unattached.SRC*** to ***Attached.SRC*** through ***AttachWait.SRC***.
    - DRP in ***Unattached.SRC*** detects the CC pull-down of ***VPD*** which is in ***Unattached.SNK*** and DRP enters ***AttachWait.SRC***.
    - DRP in ***AttachWait.SRC*** detects that pull-down on CC persists for ***tCCDebounce***. It then enters ***Attached.SRC*** and turns on VBUS and VCONN.
3. ***VPD*** transitions from ***Unattached.SNK*** to ***Attached.SNK*** through ***AttachWait.SNK***.
    - ***VPD*** detects VCONN and enters ***Attached.SNK***.
4. While DRP and ***VPD*** are in their respective attached states, DRP discovers the ***VPD*** and removes VBUS.
    - DRP (as Source) queries the cable identity via ***USB PD*** on SOP'.
    - ***VPD*** responds on SOP', advertising that it is a ***VCONN-Powered USB Device*** that does not support charge-through.
    - DRP (as Source) removes VBUS.
    - DRP (as Source) maintains its ***Rp***.
5. DRP and ***VPD*** monitor for detach.
    - DRP (as Source) monitors CC for detach and when detected, enters ***Unattached.SNK*** (and resumes toggling between ***Unattached.SNK*** and ***Unattached.SRC***).

- ***VPD*** monitors VCONN for detach and when detected, enters ***Unattached.SNK***.

4.5.3.1.8 DRP to Charge-Through VCONN-Powered Device (CTVPD) Behavior

Figure 4-31 illustrates the functional model for a DRP connected to a Charge-Through ***VCONN-Powered USB Device***, with a Source attached to the Charge-Through port on the ***VCONN-Powered USB Device***.

Figure 4-31 Example DRP to Charge-Through VPD Model



CASE 1: The following describes the behavior when a DRP is connected to a Charge-Through ***VCONN-Powered USB Device*** (abbreviated ***CTVPD***), with no Power Source attached to the Charge-Through port on the ***CTVPD***.

1. DRP and ***CTVPD*** are both in the unattached state.
    a. DRP alternates between ***Unattached.SRC*** and ***Unattached.SNK***.
    b. ***CTVPD*** has applied ***Rd*** on its Charge-Through port's CC1 and CC2 pins and ***Rd*** on the Host-side port's CC pin.
2. DRP transitions from ***Unattached.SRC*** to ***Attached.SRC*** through ***AttachWait.SRC***.
    a. DRP in ***Unattached.SRC*** detects a CC pull down of ***CTVPD*** which is in ***Unattached.SNK*** and DRP enters ***AttachWait.SRC***.
    b. DRP in ***AttachWait.SRC*** detects that pull down on CC persists for ***tCCDebounce***, enters ***Attached.SRC*** and turns on VBUS and VCONN.
3. ***CTVPD*** transitions from ***Unattached.SNK*** to ***Attached.SNK*** through ***AttachWait.SNK***.
    a. ***CTVPD*** detects the host-side CC pull-up of the DRP and ***CTVPD*** enters ***AttachWait.SNK***.
    b. ***CTVPD*** in ***AttachWait.SNK*** detects that pull up on the Host-side port's CC persists for ***tCCDebounce***, VCONN present and enters ***Attached.SNK***.
    c. ***CTVPD*** presents a high-impedance to ground (above ***zOPEN***) on its Charge-Through port's CC1 and CC2 pins.
4. While DRP and ***CTVPD*** are in their respective attached states, DRP discovers the ***CTVPD*** and transitions to ***CTUnattached.SNK***.
    a. DRP (as Source) queries the device identity via ***USB PD*** (Device Identity Command) on SOP'.
    b. ***CTVPD*** responds on SOP', advertising that it is a Charge-Through ***VCONN-Powered USB Device***.
    c. DRP (as Source) removes VBUS.
    d. DRP (as Source) changes its ***Rp*** to a ***Rd***.

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e. DRP (as Sink) continues to provide VCONN and enters ***CTUnattached.SNK***.

5. ***CTVPD*** transitions to ***CTUnattached.VPD***.
   a. ***CTVPD*** detects VBUS removal, VCONN presence, the low Host-side CC pin and enters ***CTUnattached.VPD***.
   b. ***CTVPD*** changes its host-side ***Rd*** to a ***Rp*** advertising 3.0 A.
   c. ***CTVPD*** isolates itself from VBUS.
   d. ***CTVPD*** apply ***Rd*** on its Charge-Through port's CC1 and CC2 pins.
6. While the ***CTVPD*** in ***CTUnattached.VPD*** state and the DRP in ***CTUnattached.SNK*** state:
   a. ***CTVPD*** monitors Charge-Though CC pins for a source or sink; when a Power Source attach is detected, enters ***CTAttachWait.VPD***; when a sink is detected, enters ***CTAttachWait.Unsupported***.
   b. ***CTVPD*** monitors VCONN for Host detach and when detected, enters ***Unattached.SNK***.
   c. DRP monitors VBUS and CC for ***CTVPD*** detach for ***tVPDDetach*** and when detected, enters ***Unattached.SNK***.
   d. DRP monitors VBUS for Power Source attach and when detected, enters ***CTAttached.SNK***.

CASE 2: The following describes the behavior when a Power Source is connected to a Charge-Through ***VCONN-Powered USB Device*** (abbreviated ***CTVPD***), with a Host already attached to the Host-side port on the ***CTVPD***.

1. DRP is in ***CTUnattached.SNK*** state, ***CTVPD*** in ***CTUnattached.VPD***, and Power Source in the unattached state.
   a. ***CTVPD*** has applied ***Rd*** on the Charge-Through port's CC1 and CC2 pins and ***Rp*** termination advertising 3.0 A on the Host-side port's CC pin.
2. Power Source transitions from ***Unattached.SRC*** to ***Attached.SRC*** through ***AttachWait.SRC***.
   a. Power Source detects the CC pull-down of the ***CTVPD*** and enters ***AttachWait.SRC***.
   b. Power Source in ***AttachWait.SRC*** detects that pull down on CC persists for ***tCCDebounce***, enters ***Attached.SRC*** and turns on VBUS.
3. ***CTVPD*** transitions from ***CTUnattached.VPD*** through ***CTAttachWait.VPD*** to ***CTAttached.VPD***.
   a. ***CTVPD*** detects the Source's ***Rp*** on one of its Charge-Through CC pins, and transitions to ***CTAttachWait.VPD***.
   b. ***CTVPD*** finishes any active ***USB PD*** communication on SOP' and ceases to respond to SOP' queries.
   c. ***CTVPD*** in ***CTAttachWait.VPD*** detects that the pull up on Charge-Through CC pin persists for ***tCCDebounce***, detects VBUS and enters ***CTAttached.VPD***.
   d. ***CTVPD*** connects the active Charge-Through CC pin to the Host-side port's CC pin.
   e. ***CTVPD*** disables its ***Rp*** termination advertising 3.0 A on the Host-side port's CC pin.
   f. ***CTVPD*** disables its ***Rd*** on the Charge-Through CC pins.
   g. ***CTVPD*** connects VBUS from the Charge-Through side to the Host side.
4. DRP (as Sink) transitions to ***CTAttached.SNK***.
   a. DRP (as Sink) detects VBUS, monitors ***vRd*** for available current and enter ***CTAttached.SNK***.
5. While the devices are all in their respective attached states:
   a. ***CTVPD*** monitors VCONN for DRP detach and when detected, enters ***CTDisabled.VPD***.
   b. ***CTVPD*** monitors VBUS and CC for Power Source detach and when detected, enters ***CTUnattached.VPD*** within ***tVPDCTDD***.

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c. DRP (as Sink) monitors VBUS for Charge-Through Power Source detach and when detected, enters ***CTUnattached.SNK***.

d. DRP (as Sink) monitors VBUS and CC for ***CTVPD*** detach and when detected, enters ***Unattached.SNK*** (and resumes toggling between ***Unattached.SNK*** and ***Unattached.SRC***).

e. Power Source monitors CC for ***CTVPD*** detach and when detected, enters ***Unattached.SRC***.

CASE 3: The following describes the behavior when a Power Source is connected to a Charge-Through ***VCONN-Powered USB Device*** (abbreviated ***CTVPD***), with no Host attached to the Host-side port on the ***CTVPD***.

1. ***CTVPD*** and Power Source are both in the unattached state.
    a. ***CTVPD*** has applied ***Rd*** on the Charge-Through port's CC1 and CC2 pins and ***Rd*** on the Host-side port's CC pin.
2. Power Source transitions from ***Unattached.SRC*** to ***Attached.SRC*** through ***AttachWait.SRC***.
    a. Power Source detects the CC pull-down of the ***CTVPD*** and enters ***AttachWait.SRC***.
    b. Power Source in ***AttachWait.SRC*** detects that pull down on CC persists for ***tCCDebounce***, enters ***Attached.SRC*** and turns on VBUS.
3. ***CTVPD*** alternates between ***Unattached.SNK*** and ***Unattached.SRC***.
    a. ***CTVPD*** detects the Source's ***Rp*** on one of its Charge-Through CC pins, detects VBUS for ***tCCDebounce*** and starts alternating between ***Unattached.SRC*** and ***Unattached.SNK***.
4. While the ***CTVPD*** alternates between ***Unattached.SRC*** and ***Unattached.SNK*** state and the Power Source in ***Attached.SRC*** state:
    a. ***CTVPD*** monitors the Host-side port's CC pin for device attach and when detected, enters ***AttachWait.SRC***.
    b. ***CTVPD*** monitors VBUS for Power Source detach and when detected, enters ***Unattached.SNK***.
    c. Power Source monitors CC for ***CTVPD*** detach and when detected, enters ***Unattached.SRC***.

CASE 4: The following describes the behavior when a DRP is connected to a Charge-Through ***VCONN-Powered USB Device*** (abbreviated ***CTVPD***), with a Power Source already attached to the Charge-Through side on the ***CTVPD***.

1. DRP and ***CTVPD*** are in unattached state and Power Source in ***Attached.SRC*** state.
    a. DRP alternates between ***Unattached.SRC*** and ***Unattached.SNK***.
    b. ***CTVPD*** alternates between ***Unattached.SRC*** and ***Unattached.SNK***.
    c. ***CTVPD*** has applied ***Rd*** on its Charge-Through port's CC1 and CC2 pins.
    d. Power Source has applied VBUS.
2. DRP transitions from ***Unattached.SNK*** to ***AttachWait.SNK***.
    a. DRP in ***Unattached.SNK*** detects the CC pull-up of ***CTVPD*** which is in ***Unattached.SRC*** and DRP enters ***AttachWait.SNK***.
3. ***CTVPD*** transitions from ***Unattached.SRC*** to ***Try.SNK*** through ***AttachWait.SRC***.
    a. ***CTVPD*** in ***Unattached.SRC*** detects the CC pull-down of DRP which is in ***Unattached.SNK*** and ***CTVPD*** enters ***AttachWait.SRC***.
    b. ***CTVPD*** in ***AttachWait.SRC*** detects that pull down on CC persists for ***tCCDebounce*** and enters ***Try.SNK***.
    c. ***CTVPD*** disables ***Rp*** termination advertising Default USB Power on the Host-side port's CC pin.
    d. ***CTVPD*** enables ***Rd*** on the Host-side port's CC pin.

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4. DRP transitions from ***AttachWait.SNK*** to ***Attached.SRC*** through ***Unattached.SRC*** and ***AttachWait.SRC***.
    a. DRP in ***AttachWait.SNK*** detects the CC pull-up removal of ***CTVPD*** which is in ***Try.SNK*** and DRP enters ***Unattached.SRC***.
    b. DRP in ***Unattached.SRC*** detects the CC pull-down of ***CTVPD*** which is in ***Try.SNK*** and DRP enters ***AttachWait.SRC***.
    c. DRP in ***AttachWait.SRC*** detects that pull down on CC persists for ***tCCDebounce***. It then enters ***Attached.SRC*** and enables VBUS and VCONN.
5. ***CTVPD*** transitions from ***Try.SNK*** to ***Attached.SNK***.
    a. ***CTVPD*** detects the CC pull-up of the DRP persists for ***tTryCCDebounce***.
    b. ***CTVPD*** detects VBUS on the Host-side port and enters ***Attached.SNK***.
6. While DRP and ***CTVPD*** are in their respective attached states, DRP discovers the Charge-Through ***CTVPD*** and transitions to ***CTUnattached.SNK***.
    a. DRP (as Source) queries the device identity via ***USB PD*** (***Discover Identity*** Command) on SOP'.
    b. ***CTVPD*** responds on SOP', advertising that it is a Charge-Through ***VCONN-Powered USB Device***.
    c. DRP (as Source) removes VBUS.
    d. DRP (as Source) changes its ***Rp*** into an ***Rd***.
    e. DRP (as Sink) continues to provide VCONN and enters ***CTUnattached.SNK***.
7. ***CTVPD*** transitions to ***CTUnattached.VPD***.
    a. ***CTVPD*** detects VBUS removal, VCONN presence, and the low CC pin on its host port and enters ***CTUnattached.VPD***.
    b. ***CTVPD*** changes its host-side ***Rd*** into an ***Rp*** termination advertising 3.0 A.
    c. ***CTVPD*** isolates itself from VBUS.
8. ***CTVPD*** transitions from ***CTUnattached.VPD*** through ***CTAttachWait.VPD*** to ***CTAttached.VPD***.
    a. ***CTVPD*** detects the Source's ***Rp*** on one of its Charge-Through CC pins, and transitions to ***CTAttachWait.VPD***.
    b. ***CTVPD*** in ***CTAttachWait.VPD*** detects that the pull up on Charge-Through CC pin persists for ***tCCDebounce***, detects VBUS and enters ***CTAttached.VPD***.
    c. ***CTVPD*** finishes any active ***USB PD*** communication on SOP' and ceases to respond to SOP' queries.
    d. ***CTVPD*** connects the active Charge-Through CC pin to the Host-side port's CC pin.
    e. ***CTVPD*** disables its ***Rp*** termination advertising 3.0 A on the Host-side port's CC pin.
    f. ***CTVPD*** disables its ***Rd*** on the Charge-Through CC pins.
    g. ***CTVPD*** connects VBUS from the Charge-Through side to the Host side.
9. DRP (as Sink) transitions to ***CTAttached.SNK***.
    a. DRP (as Sink) detects VBUS and monitors ***vRd*** for available current and enter ***CTAttached.SNK***.
10. While the devices are all in their respective attached states:
    a. ***CTVPD*** monitors VCONN for DRP detach and when detected, enters ***CTDisabled.VPD***.

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b. ***CTVPD*** monitors VBUS and CC for Power Source detach and when detected, enters ***CTUnattached.VPD*** within ***tVPDCTDD***.

c. DRP (as Sink) monitors VBUS for Charge-Through Power Source detach and when detected, enters ***CTUnattached.SNK***.

d. DRP (as Sink) monitors VBUS and CC for ***CTVPD*** detach and when detected, enters ***Unattached.SNK*** (and resumes toggling between ***Unattached.SNK*** and ***Unattached.SRC***).

e. Power Source monitors CC for ***CTVPD*** detach and when detected, enters ***Unattached.SRC***.

CASE 5: The following describes the behavior when a Power Source is connected to a Charge-Through ***VCONN-Powered USB Device*** (abbreviated ***CTVPD***), with a DRP (with dead battery) attached to the Host-side port on the ***CTVPD***.

1. DRP, ***CTVPD*** and Power Source are all in the unattached state.
   a. DRP apply dead battery ***Rd***.
   b. ***CTVPD*** apply ***Rd*** on the Charge-Through port's CC1 and CC2 pins and ***Rd*** on the Host-side port's CC pin.
2. Power Source transitions from ***Unattached.SRC*** to ***Attached.SRC*** through ***AttachWait.SRC***.
   a. Power Source detects the CC pull-down of the ***CTVPD*** and enters ***AttachWait.SRC***.
   b. Power Source in ***AttachWait.SRC*** detects that pull down on CC persists for ***tCCDebounce***, enters ***Attached.SRC*** and turns on VBUS.
3. ***CTVPD*** alternates between ***Unattached.SNK*** and ***Unattached.SRC***.
   a. ***CTVPD*** detects the Source's ***Rp*** on one of its Charge-Through CC pins, detects VBUS for ***tCCDebounce*** and starts alternating between ***Unattached.SRC*** and ***Unattached.SNK***.
4. ***CTVPD*** transitions from ***Unattached.SRC*** to ***Try.SNK*** through ***AttachWait.SRC***.
   a. ***CTVPD*** in ***Unattached.SRC*** detects the CC pull-down of DRP which is in ***Unattached.SNK*** and ***CTVPD*** enters ***AttachWait.SRC***.
   b. ***CTVPD*** in ***AttachWait.SRC*** detects that pull down on CC persists for ***tCCDebounce*** and enters ***Try.SNK***.
   c. ***CTVPD*** disables ***Rp*** termination advertising Default USB Power on the Host-side port's CC pin.
   d. ***CTVPD*** enables ***Rd*** on the Host-side port's CC pin.
5. DRP in dead battery condition remains in ***Unattached.SNK***.
6. ***CTVPD*** transitions from ***Try.SNK*** to ***Attached.SRC*** through ***TryWait.SRC***.
   a. ***CTVPD*** didn't detect the CC pull-up of the DRP for ***tTryCCDebounce*** after ***tDRPTry*** and enters ***TryWait.SRC***.
   b. ***CTVPD*** disables ***Rp*** on the Host-side port's CC pin.
   c. ***CTVPD*** enables ***Rp*** termination advertising Default USB Power on the Host-side port's CC pin.
   d. ***CTVPD*** detects the CC pull-down of the DRP for ***tTryCCDebounce*** and enters ***Attached.SRC***.
   e. ***CTVPD*** connects VBUS from the Charge-Through side to the Host side.
7. DRP transitions from ***Unattached.SNK*** to ***Attached.SNK*** through ***AttachWait.SNK***.
   a. DRP in ***Unattached.SNK*** detects the CC pull-up of ***CTVPD*** which is in ***Attached.SRC*** and DRP enters ***AttachWait.SNK***.
   b. DRP in ***AttachWait.SNK*** detects that pull up on CC persists for ***tCCDebounce***, VBUS present and enters ***Attached.SNK***.

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8. While the devices are all in their respective attached states:
    a. ***CTVPD*** monitors the Host-side port's CC pin for device attach and when detected, enters ***Unattached.SNK***.
    b. ***CTVPD*** monitors VBUS for Power Source detach and when detected, enters ***Unattached.SNK***.
    c. Power Source monitors CC for ***CTVPD*** detach and when detected, enters ***Unattached.SRC***.
    d. DRP monitors VBUS for ***CTVPD*** detach and when detected, enters ***Unattached.SNK***.
    e. Additionally, the DRP ***may*** query the identity of the cable via ***USB PD*** on SOP' when it has sufficient battery power and when a Charge-Through VPD is identified enters ***TryWait.SRC*** if implemented or enters ***Unattached.SRC*** if ***TryWait.SRC*** is not supported.

CASE 6: The following describes the behavior when a DRP is connected to a Charge-Through ***VCONN-Powered USB Device*** (abbreviated ***CTVPD***) and a Sink is attached to the Charge-Through port on the ***CTVPD***.

1. DRP, ***CTVPD*** and Sink are all in the unattached state.
    a. DRP alternates between ***Unattached.SRC*** and ***Unattached.SNK***.
    b. ***CTVPD*** has applied ***Rd*** on its Charge-Through port's CC1 and CC2 pins and ***Rd*** on the Host-side port's CC pin.
2. DRP transitions from ***Unattached.SRC*** to ***Attached.SRC*** through ***AttachWait.SRC***.
    a. DRP in ***Unattached.SRC*** detects the CC pull-down of ***CTVPD*** which is in ***Unattached.SNK*** and DRP enters ***AttachWait.SRC***.
    b. DRP in ***AttachWait.SRC*** detects that pull down on CC persists for ***tCCDebounce***. It then enters ***Attached.SRC*** and enables VBUS and VCONN.
3. ***CTVPD*** transitions from ***Unattached.SNK*** to ***Attached.SNK*** through ***AttachWait.SNK***.
    a. ***CTVPD*** detects the host-side CC pull-up of the DRP and ***CTVPD*** enters ***AttachWait.SNK***.
    b. ***CTVPD*** in ***AttachWait.SNK*** detects that pull up on the Host-side port's CC persists for ***tCCDebounce***, VCONN present and enters ***Attached.SNK***.
    c. ***CTVPD*** presents a high-impedance to ground (above ***zOPEN***) on its Charge-Through port's CC1 and CC2 pins.
4. While DRP and ***CTVPD*** are in their respective attached states, DRP discovers the Charge-Through ***CTVPD*** and transitions to ***CTUnattached.SNK***.
    a. DRP (as Source) queries the device identity via ***USB PD*** (***Discover Identity*** Command) on SOP'.
    b. ***CTVPD*** responds on SOP', advertising that it is a Charge-Through ***VCONN-Powered USB Device***.
    c. DRP (as Source) removes VBUS.
    d. DRP (as Source) changes its ***Rp*** into an ***Rd***.
    e. DRP (as Sink) continues to provide VCONN and enters ***CTUnattached.SNK***.
5. ***CTVPD*** transitions to ***CTUnattached.VPD***.
    a. ***CTVPD*** detects VBUS removal, VCONN presence, and the low CC pin on its host port and enters ***CTUnattached.VPD***.
    b. ***CTVPD*** changes its host-side ***Rd*** into an ***Rp*** termination advertising 3.0 A.
    c. ***CTVPD*** isolates itself from VBUS.
    d. ***CTVPD*** apply ***Rd*** on its Charge-Through port's CC1 and CC2 pins.
6. ***CTVPD*** alternates between ***CTUnattached.VPD*** and ***CTUnattached.Unsupported***.

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a. ***CTVPD*** detects ***SRC.Open*** on its Charge-Through CC pins and starts alternating between ***CTUnattached.VPD*** and ***CTUnattached.Unsupported***.

7. ***CTVPD*** transitions from ***CTUnattached.Unsupported*** to ***CTTry.SNK*** through ***CTAttachWait.Unsupported***.
   a. ***CTVPD*** in ***CTUnattached.Unsupported*** detects the CC pull-down of the Sink which is in ***Unattached.SNK*** and ***CTVPD*** enters ***CTAttachWait.Unsupported***.
   b. ***CTVPD*** in ***CTAttachWait.Unsupported*** detects that pull down on CC persists for ***tCCDebounce*** and enters ***CTTry.SNK***.
   c. ***CTVPD*** disables ***Rp*** termination advertising Default USB Power on the Charge-Through port's CC pins.
   d. ***CTVPD*** enables ***Rd*** on the Charge-Through port's CC pins.
8. ***CTVPD*** transitions from ***CTTry.SNK*** to ***CTAttached.Unsupported***.
   a. ***CTVPD*** didn't detect the CC pull-up of the potential Source for ***tDRPTryWait*** after ***tDRPTry*** and enters ***CTAttached.Unsupported***.
9. While the ***CTVPD*** in ***CTAttached.Unsupported*** state, the DRP in ***CTUnattached.SNK*** state and the Sink in ***Unattached.SNK*** state:
   a. ***CTVPD*** disables the ***Rd*** termination on the Charge-Through port's CC pins and applies ***Rp*** termination advertising Default USB Power.
   b. ***CTVPD*** exposes a ***USB Billboard Device Class*** to the DRP indicating that it is connected to an unsupported device on its Charge Through port.
   c. ***CTVPD*** monitors Charge-Though CC pins for Sink detach and when detected, enters ***CTUnattached.VPD***.
   d. ***CTVPD*** monitors VCONN for Host detach and when detected, enters ***Unattached.SNK***
   e. DRP monitors CC for ***CTVPD*** detach for ***tVPDDetach*** and when detected, enters ***Unattached.SNK***.
   f. DRP monitors VBUS for ***CTVPD*** Charge-Through source attach and, when detected, enters ***CTAttached.SNK***.

4.5.3.2 USB Type-C Port to USB Legacy Port Interoperability Behaviors

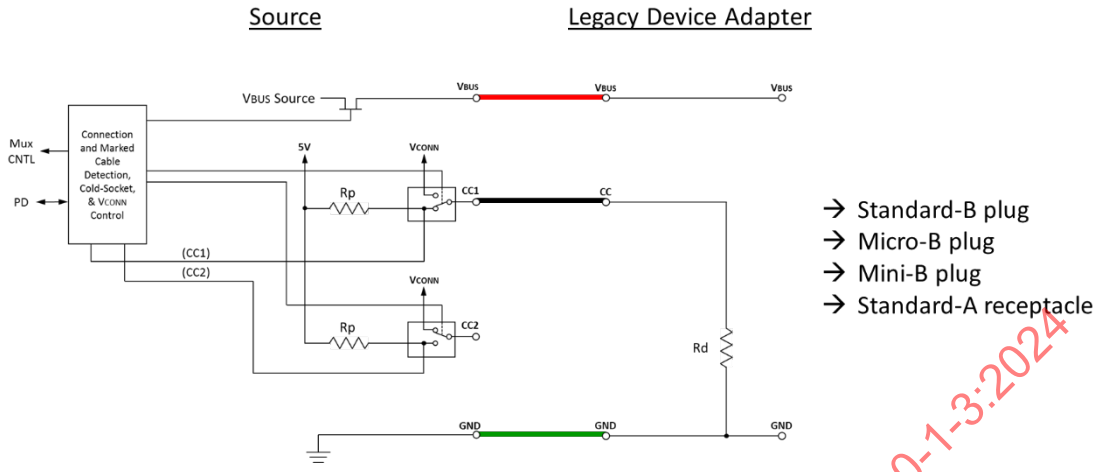
The following sub-sections describe port-to-port interoperability behaviors for the various combinations of USB Type-C Source, Sink and DRPs and legacy USB ports.

4.5.3.2.1 Source to Legacy Device Port Behavior

Figure 4-32 illustrates the functional model for a Source connected to a legacy device port. This model is based on having an adapter present as a Sink to the Source. This adapter has a USB Type-C plug on one end plugged into the Source and either a USB Standard-B plug, USB Micro-B plug, USB Mini-B plug, or a USB Standard-A receptacle on the other end.

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Figure 4-32 Source to Legacy Device Port Functional Model



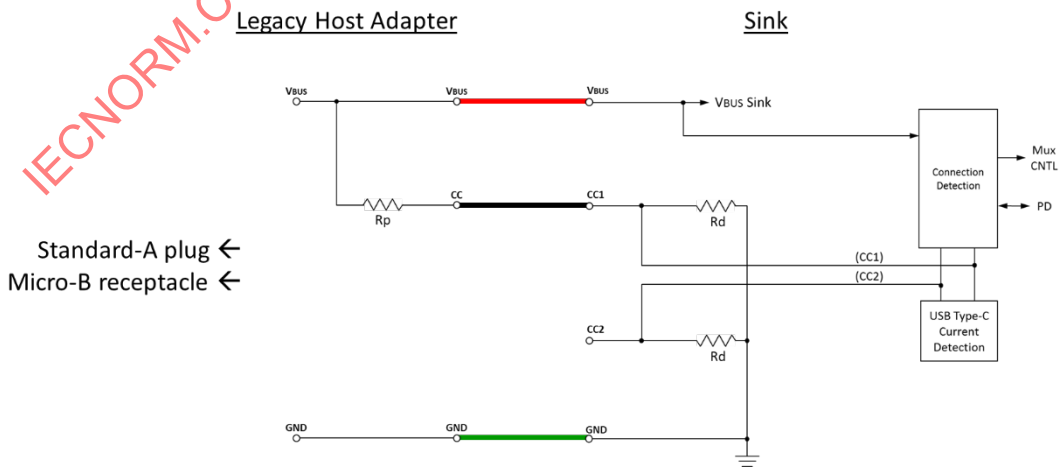
The following describes the behavior when a Source is connected to a legacy device adapter that has an ***Rd*** to ground to mimic the behavior of a Sink.

1. Source in the unattached state.
2. Source transitions from ***Unattached.SRC*** to ***Attached.SRC*** through ***AttachWait.SRC***.
   - Source detects the Sink's pull-down on CC and enters ***AttachWait.SRC***. After ***tCCDebounce***, it enters ***Attached.SRC***.
   - Source turns on VBUS and VCONN.
3. While the Source is in the attached state:
   - Source monitors CC for detach and when detected, enters ***Unattached.SRC***.

4.5.3.2.2 Legacy Host Port to Sink Behavior

Figure 4-33 illustrates the functional model for a legacy host port connected to a Sink. This model is based on having an adapter that presents itself as a Source to the Sink. This adapter is either a USB Standard-A legacy plug or a USB Micro-B legacy receptacle on one end and the USB Type-C plug on the other end plugged into a Sink.

Figure 4-33 Legacy Host Port to Sink Functional Model



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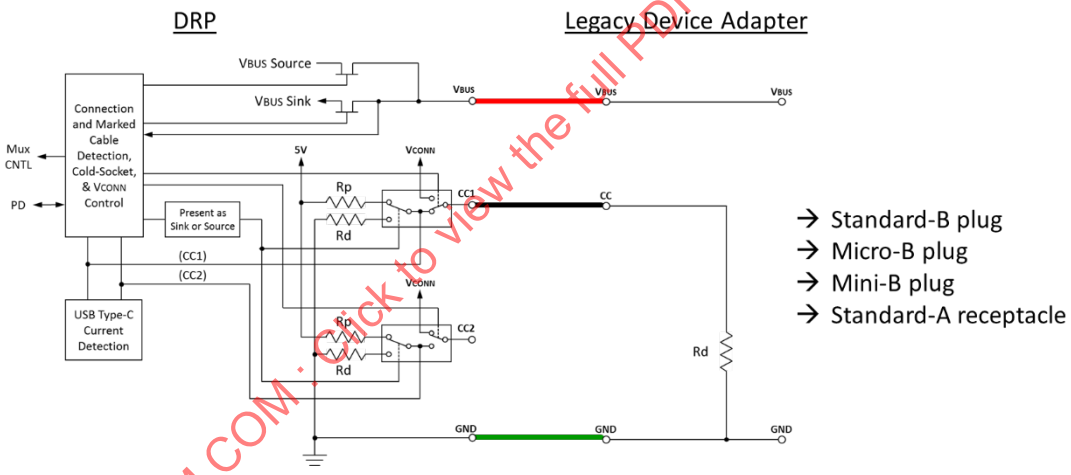
The following describes the behavior when a legacy host adapter that has an ***Rp*** to VBUS to mimic the behavior of a Source that is connected to a Sink. The value of ***Rp*** ***shall*** indicate an advertisement of Default USB Power (See Table 4-27), even though the cable itself can carry 3 A. This is because the cable has no knowledge of the capabilities of the power source, and any higher current is negotiated via ***USB BC 1.2***.

1. Sink in the unattached state.
2. Sink transitions from ***Unattached.SNK*** to ***Attached.SNK*** through ***AttachWait.SNK*** if needed.
   - While in ***Unattached.SNK***, if device is not ***USB 2.0*** only, supports accessories or requires more than default power, it enters ***AttachWait.SNK*** when it detects a pull up on CC and ignores VBUS. Otherwise, it ***may*** enter ***Attached.SNK*** directly when VBUS is detected.
   - Sink detects VBUS and enters ***Attached.SNK***.
3. While the Sink is in the attached state:
   - Sink monitors VBUS for detach and when detected, enters ***Unattached.SNK***.

4.5.3.2.3 DRP to Legacy Device Port Behavior

Figure 4-34 illustrates the functional model for a DRP connected to a legacy device port. This model is based on having an adapter present as a Sink (Device) to the DRP. This adapter has a USB Type-C plug on one end plugged into a DRP and either a USB Standard-B plug, USB Micro-B plug, USB Mini-B plug, or a USB Standard-A receptacle on the other end.

Figure 4-34 DRP to Legacy Device Port Functional Model



The following describes the behavior when a DRP is connected to a legacy device adapter that has an ***Rd*** to ground to mimic the behavior of a Sink.

1. DRP in the unattached state.
   - DRP alternates between ***Unattached.SRC*** and ***Unattached.SNK***.
2. DRP transitions from ***Unattached.SRC*** to ***Attached.SRC***.
   - DRP in ***Unattached.SRC*** detects the adapter's pull-down on CC and enters ***AttachWait.SRC***.
   - DRP in ***AttachWait.SRC*** times out (***tCCDebounce***) and transitions to ***Attached.SRC***.
   - DRP in ***Attached.SRC*** turns on VBUS and VCONN.
   - DRP in ***AttachWait.SRC*** ***may*** support ***Try.SNK*** and if so, ***may*** transition through ***Try.SNK*** and ***TryWait.SRC*** prior to entering ***Attached.SRC***.
3. While the DRP is in the attached state:

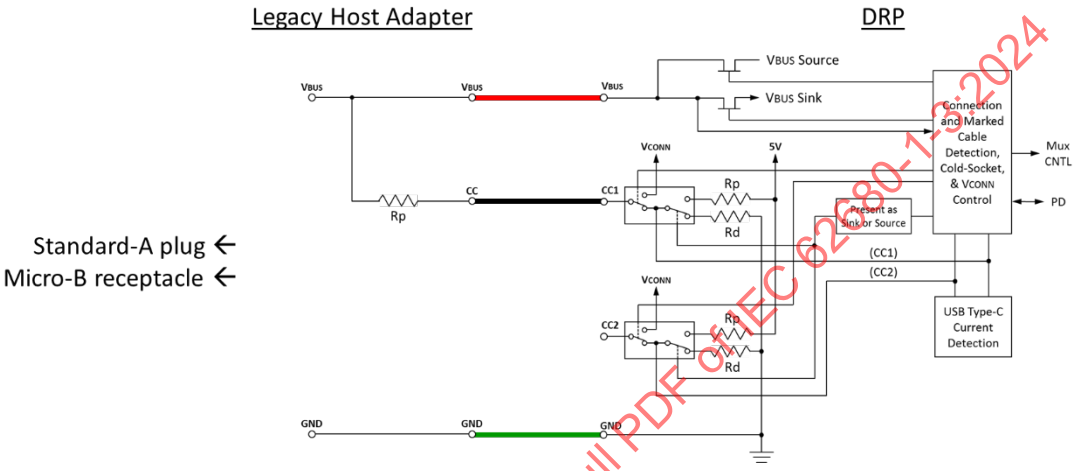
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- DRP monitors CC for detach and when detected, enters ***Unattached.SNK*** (and resumes toggling between ***Unattached.SNK*** and ***Unattached.SRC***).

4.5.3.2.4 Legacy Host Port to DRP Behavior

Figure 4-35 illustrates the functional model for a legacy host port connected to a DRP operating as a Sink. This model is based on having an adapter that presents itself as a Source (Host) to the DRP operating as a Sink, this adapter is either a USB Standard-A legacy plug or a USB Micro-B legacy receptacle on one end and the USB Type-C plug on the other end plugged into a DRP.

Figure 4-35 Legacy Host Port to DRP Functional Model



The following describes the behavior when a legacy host adapter that has an ***Rp*** to VBUS to mimic the behavior of a Source is connected to a DRP. The value of ***Rp*** ***shall*** indicate an advertisement of Default USB Power (See Table 4-27), even though the cable itself can carry 3 A. This is because the cable has no knowledge of the capabilities of the power source, and any higher current is negotiated via ***USB BC 1.2***.

1. DRP in the unattached state.
   - DRP alternates between ***Unattached.SRC*** and ***Unattached.SNK***.
2. DRP transitions from ***Unattached.SNK*** to ***AttachWait.SNK*** to ***Attached.SNK***.
   - DRP in ***Unattached.SNK*** detects pull up on CC and enters ***AttachWait.SNK***.
   - DRP in ***AttachWait.SNK*** detects VBUS and enters ***Attached.SNK***.
   - DRP in ***AttachWait.SNK*** ***may*** support ***Try.SRC*** and if so, ***may*** transition through ***Try.SRC*** and ***TryWait.SNK*** prior to entering ***Attached.SNK***.
3. While the DRP is in the attached state:
   - DRP monitors VBUS for detach and when detected, enters ***Unattached.SNK*** (and resumes toggling between ***Unattached.SNK*** and ***Unattached.SRC***).

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4.6 Power

Power delivery over the USB Type-C connector takes advantage of the existing USB methods as defined by the ***USB 2.0*** and ***USB 3.2*** specifications, the ***USB BC 1.2*** specification, and the ***USB Power Delivery*** specification. Power for ***USB4*** operation requires a ***USB PD*** explicit contract as defined in Section 5.3 and the ***USB Power Delivery*** specification. Prior to entering a ***USB PD*** explicit contract, a ***USB4*** port operates as a ***USB 3.2*** port regarding power.

The ***USB Type-C Current*** mechanism allows the Source to offer more current than defined by the ***USB BC 1.2*** specification. A USB power source ***shall not*** provide more than 48 V nominal on VBUS. ***USB PD*** power sources

that deliver power over a USB Type-C connector ***shall*** follow the power rules as defined in Section 10 of the ***USB Power Delivery*** specification.

All USB Type-C-based devices ***shall*** support ***USB Type-C Current*** and ***may*** support other USB-defined methods for power. The following order of precedence of power negotiation ***shall*** be followed: ***USB BC 1.2*** supersedes the ***USB 2.0*** and ***USB 3.2*** specifications, ***USB Type-C Current*** at 1.5 A and 3.0 A supersedes ***USB BC 1.2***, and ***USB Power Delivery*** supersedes ***USB Type-C Current***. Table 4-19 summarizes this order of precedence of power source usage.

Table 4-19 Precedence of Power Source Usage

Precedence	Mode of Operation		Nominal Voltage	Maximum Current
Highest	***USB PD***		Configurable up to 48 V	5 A
	USB Type-C Current @ 3.0 A		5 V	3.0 A
↓	***USB Type-C Current*** @ 1.5 A		5 V	1.5 A
	USB BC 1.2		5 V	Up to 1.5 A[1]
	Default USB Power	***USB 3.2***	5 V	See ***USB 3.2***
Lowest		***USB 2.0***	5 V	See ***USB 2.0***

Note 1: ***USB BC 1.2*** permits a power provider to be designed to support a level of power between 0.5 A and 1.5 A. If the ***USB BC 1.2*** power provider does not support 1.5 A, then it is required to follow power droop requirements. A ***USB BC 1.2*** power consumer ***may*** consume up to 1.5 A provided that the voltage does not drop below 2 V, which ***may*** occur at any level of power above 0.5 A.

For example, once the ***USB PD*** mode (e.g., a power contract has been negotiated) has been entered, the device ***shall*** abide by that power contract ignoring any other previously made or offered by the ***USB Type-C Current***, ***USB BC 1.2*** or ***USB 2.0*** and ***USB 3.2*** specifications. When the ***USB PD*** mode is exited, the device ***shall*** fallback, in precedence order, to the ***USB Type-C Current***, ***USB BC 1.2***, or ***USB 2.0*** and ***USB 3.2*** specification power levels.

All USB Type-C ports ***shall*** tolerate being connected to USB power source supplying default USB power, e.g., a host being connected to a legacy USB charger that always supplies VBUS.

4.6.1 Power Requirements during USB Suspend

USB Type-C implementations with ***USB Type-C Current***, ***USB PD*** and VCONN, along with active cables, require the need to expand the traditional USB suspend definition.

4.6.1.1 VBUS Requirements during USB Suspend

The ***USB 2.0*** and ***USB 3.2*** specifications define the amount of current a Sink is allowed to consume during suspend.

USB suspend power rules ***shall*** apply when the ***USB Type-C Current*** is at the Default USB Power level or when ***USB PD*** is being used and the Suspend bit is set appropriately.

When ***USB Type-C Current*** is set at 1.5 A or 3.0 A, the Sink is allowed to continue to draw current from VBUS during USB suspend. During USB suspend, the Sink's requirement to track and meet the ***USB Type-C Current*** advertisement remains in force (See Section 4.5.2.3).

USB PD provides a method for the Source to communicate to the Sink whether the Sink must follow the USB power rules for suspend.

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4.6.1.2 VCONN Requirements during USB Suspend

If the Source supplies VBUS power during USB suspend, it ***shall*** also supply VCONN and meet the requirements defined in Table 4-5.

Electronically Marked Cables ***shall*** meet the requirements in Table 4-6 during USB suspend.

VCONN powered accessories ***shall*** meet the requirements defined in Table 4-7 during USB suspend.

4.6.2 VBUS Power Provided Over a USB Type-C Cable

The minimum requirement for VBUS power supplied over the USB Type-C cable assembly matches the existing requirement for VBUS supplied over existing legacy USB cable assemblies.

USB Power Delivery in Standard Power Range (SPR) operation is intended to work over un-modified USB Type-C to USB Type-C cables, therefore any USB Type-C cable assembly that incorporates electrical components or electronics ***shall*** ensure that it tolerate, or be protected from, a VBUS voltage of 21 V.

USB Power Delivery in Extended Power Range (EPR) operation requires EPR-compatible USB Type-C to USB Type-C cables. Any USB Type-C cable assembly that incorporates electrical components or electronics that ***may*** be powered by VBUS ***shall*** ensure that it can functionally tolerate, or be protected from, a VBUS voltage of up to 50.9 V (48 V + 5% + 500 mV).

4.6.2.1 USB Type-C Current

Default USB voltage and current are defined by the ***USB 2.0*** and ***USB 3.2*** specifications. All ***USB Type-C Current*** advertisements are at the USB VBUS voltage defined by these specifications.

The ***USB Type-C Current*** feature provides the following extensions:

- Higher current than defined by the ***USB 2.0***, the ***USB 3.2***, or the BC 1.2 specifications.
- Allows the power source to manage the current it provides.

The USB Type-C connector uses CC pins for configuration including an ability for a Source to advertise to its port partner (Sink) the amount of current it ***shall*** supply:

- Default is the as-configured for high-power operation current value as defined by the USB Specification (500 mA for ***USB 2.0*** ports; 900 mA or 1,500 mA for ***USB 3.2*** ports in single-lane or dual-lane operation, respectively).
- 1.5 A.
- 3.0 A.

When a Source is advertising USB Type-C Default current, the Sink behavior is defined as follows:

- It connects as a ***USB 2.0*** or ***USB 3.2*** device, after which the Sink ***shall*** follow the appropriate USB specification.
- It enters a ***USB PD*** contract, after which the Sink ***shall*** follow the ***USB PD*** specification to determine the current (e.g., ***Rp*** will no longer be Default as it is superseded by the ***USB PD*** contract).
- It detects a ***USB BC 1.2*** charging port, after which the Sink ***shall*** follow the ***USB BC 1.2*** specification.
- It attaches as a USB Type-C Power Sinking Device (PSD), after which the Sink ***may*** draw up to 500 mA and ***shall*** meet the inrush requirement for ***USB 2.0***.

A PSD ***shall*** fully support ***USB Type-C Current*** operation, ***should*** support ***USB PD***, and ***may*** support ***USB BC 1.2***. A PSD ***may*** be a Sink or a DRP operating in Sink mode. A PSD ***shall not*** have a USB or USB Type-C ***Alternate Mode*** communications function.

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The relationship of ***USB Type-C Current*** and the equivalent ***USB PD*** Power (PDP) value is shown in Table 4-20.

Table 4-20 USB Type-C Current Advertisement and PDP Equivalent

USB Type-C Current		PDP Equivalent
Default	500 mA (***USB 2.0***)	2.5 W
	900 mA (***USB 3.2*** single-lane)	4.5 W
	1,500 mA (***USB 3.2*** dual-lane)	7.5 W
1.5 A		7.5 W
3.0 A		15 W

A Sink that takes advantage of the additional current offered (e.g., 1.5 A or 3.0 A) ***shall*** monitor the CC pins and ***shall*** adjust its current consumption within ***tSinkAdj*** to remain within the value advertised by the Source. While a ***USB PD*** contract is in place, a Sink is not required to monitor USB Type-C current advertisements and ***shall not*** respond to USB Type-C current advertisements.

The Source ***shall*** supply VBUS to the Sink within ***tVBUSON***. VBUS ***shall*** be in the specified voltage range at the advertised current.

A Source (port supplying VBUS) ***shall*** protect itself from a Sink that draws current more than the port's ***USB Type-C Current*** advertisement.

The Source adjusts ***Rp*** (or current source) to advertise which of the three current levels it supports. See Table 4-27 for the termination requirements for the Source to advertise currents.

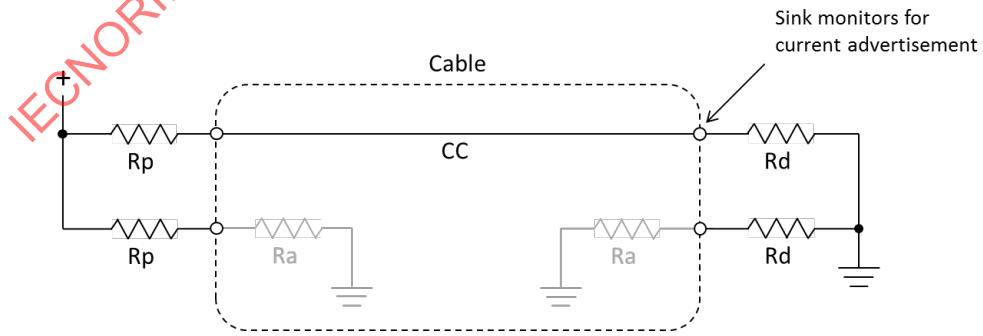
The value of ***Rp*** establishes a voltage (***vRd***) on CC that is used by the Sink to determine the maximum current it ***may*** draw.

Table 4-38 defines the CC voltage range observed by the Sink that only support default USB current.

If the Sink wants to consume more than the default USB current, it ***shall*** track ***vRd*** to determine the maximum current it ***may*** draw. See Table 4-39.

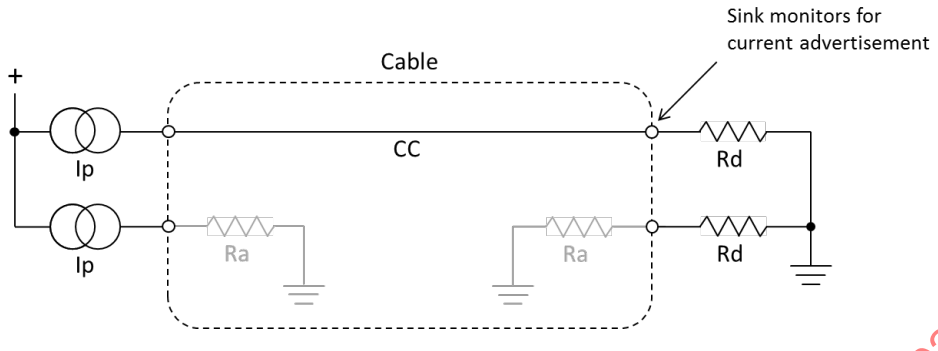
Figure 4-36 and Figure 4-37 illustrate where the Sink monitors CC for ***vRd*** to detect if the host advertises more than the default USB current.

Figure 4-36 Sink Monitoring for Current in Pull-Up/Pull-Down CC Model



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Figure 4-37 Sink Monitoring for Current in Current Source/Pull-Down CC Model



4.6.2.2 USB Battery Charging 1.2

USB Battery Charging Specification, Revision 1.2 defines a method that uses the ***USB 2.0*** D+ and D− pins to advertise VBUS can supply up to 1.5 A. Support for ***USB BC 1.2*** charging is ***optional***.

A USB Type-C port that implements ***USB BC 1.2*** that is capable of supplying at least 1.5 A ***shall*** advertise ***USB Type-C Current*** at the 1.5 A level within ***tVBUSON*** of entering the ***Attached.SRC*** state, otherwise the port ***shall*** advertise ***USB Type-C Current*** at the Default USB Power level. A USB Type-C port that implements ***USB BC 1.2*** that also supports ***USB Type-C Current*** at 3.0 A ***may*** advertise ***USB Type-C Current*** at 3.0 A.

If a Sink that supports ***USB BC 1.2*** detection, detects ***Rp*** at the Default USB Power level and does not discover a ***USB BC 1.2***-compliant Source, then it ***shall*** limit its maximum current consumption to the standard USB levels based on Table 4-19. This will ensure maximum current limits are not exceeded when connected to a Source which does not support ***USB BC 1.2***.

A Sink that supports ***USB BC 1.2*** detection and has a maximum current draw greater than Default ***USB Type-C Current*** ***shall*** monitor ***vRd*** on the CC pins to detect the Source's ***Rp*** and ***shall*** implement ***Sink Power Sub-State*** transitions (Figure 4-19). If a Sink that supports ***USB BC 1.2*** detection and has a maximum current draw greater than Default ***USB Type-C Current*** detects ***Rp*** at ***USB Type-C Current*** of 1.5 A or 3.0 A levels but does not detect a ***USB BC 1.2*** source, it ***shall*** limit its maximum current consumption to the appropriate ***USB Type-C Current*** level advertised, and ***shall*** adjust its current consumption to remain within the value advertised by the Source on Sub-State transitions. For Sub-State transitions starting from a higher power level and ending at a lower power level, the Sink ***shall*** reduce power consumption within ***tSinkAdj***. See Sections 4.5.2.3.2.2 and 4.5.2.3.3.2.

While in a ***USB Power Delivery*** Mode, a device acting as a Sink ***shall not*** initiate a ***USB BC 1.2*** detection until the port pair is detached or there is an Error Recovery or Hard Reset.

4.6.2.3 Proprietary Power Source

This section has been deprecated. Devices with USB Type-C connectors ***shall*** only employ signaling methods defined in USB specifications to negotiate power.

4.6.2.4 USB Power Delivery

USB Power Delivery is a feature on the USB Type-C connector. When ***USB PD*** is implemented, ***USB PD*** Bi-phase Mark Coded (BMC) carried on the CC wire ***shall*** be used for ***USB PD*** communications between USB Type-C ports.

At attach, VBUS ***shall*** be operationally stable prior to initiating ***USB PD*** communications.

Figure 4-38 illustrates how the ***USB PD*** BMC signaling is carried over the USB Type-C cable's CC wire.

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Figure 4-38 *USB PD* over CC Pins

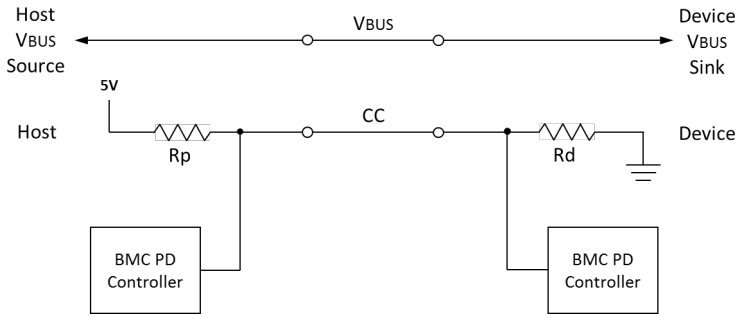
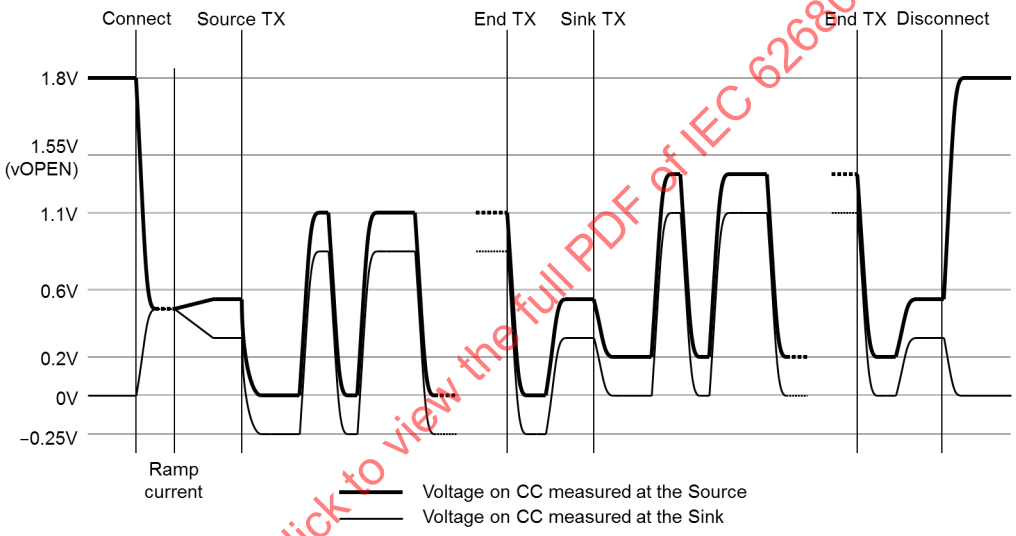


Figure 4-39 illustrates ***USB PD*** BMC signaling as seen on CC from both the perspective of the Source and Sink. The breaks in the signaling are intended to represent the passage of time.

Figure 4-39 *USB PD* BMC Signaling over CC



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When not in an Explicit Contract, ***USB PD*** Sources that are, based on their PDP, capable of supplying:

- 5 V at 3 A or greater ***shall*** advertise ***USB Type-C Current*** at the 3 A level,
- 5 V at 1.5A or greater but less than 3 A ***shall*** advertise ***USB Type-C Current*** at the 1.5 A level, or
- 5 V at less than 1.5A ***shall*** advertise ***USB Type-C Current*** at the Default USB Power level

within ***tVBUSON*** of entering the ***Attached.SRC*** state. For Multi-Port Shared Capacity Chargers, a ***USB PD*** Source capable of supplying 5 V at 3 A or greater ***may*** initially offer ***USB Type-C Current*** at the 1.5 A level and subsequently increase the offer after attach (see Section 4.8.6.2). During USB Suspend a ***USB PD*** Source ***may*** set its ***Rp*** value to default to indicate that the Sink ***shall*** only draw USB suspend current as defined in Section 4.6.1.1.

While a ***USB PD*** Explicit Contract is in place, a Source compliant with ***USB PD*** Revision 2 ***shall*** advertise a ***USB Type-C Current*** of either 1.5 A or 3.0 A. The ***USB PD*** Revision 2 Source upon entry into an Explicit Contract ***shall*** advertise an ***Rp*** value of 1.5 A or 3.0 A after it receives the GoodCRC in response to the first PS_RDY Message.

While a ***USB PD*** Explicit Contract is in place, a Source compliant with ***USB PD*** Revision 3 ***shall*** set the ***Rp*** value according to the collision avoidance scheme defined in Section 5.7 of the ***USB PD*** Revision 3 specification. The

USB PD Revision 3 Source upon entry into an Explicit Contract ***shall*** advertise an ***Rp*** value consistent with the ***USB PD*** Revision 3 collision avoidance scheme.

Refer to Section 1.6 of the ***USB Power Delivery*** specification for a definition of an Explicit Contract.

4.6.2.5 Charge-Through VCONN-Powered USB Device (CTVPD) Current Limitations

Since Charge-Through ***VCONN-Powered USB Devices*** implement charging by passively connecting the Source's CC and VBUS to the Host, the ***VCONN-Powered USB Device*** is effectively increasing the impedance on VBUS, GND, and CC between the Power Source and the Host, resulting in impedances that can exceed the maximum allowed for cables. To avoid communication issues and false disconnects from the increased GND and VBUS drops, the following ***shall*** occur:

1. The Charge-Through ***VCONN-Powered USB Device*** ***shall*** report its worst-case GND and VBUS impedance (including the extra mated connector pair and FETs) in its ***USB PD Discover Identity*** Command response on SOP'.
2. The Host that supports Charge-Through ***VCONN-Powered USB Device*** ***shall*** use this information, along with inferred information about the cable, to limit its maximum current in the case where the Power Source advertises a current greater than what the Charge-Through ***VCONN-Powered USB Device*** would allow.

The Host has no way to query the cable, as its VCONN source is consumed by the ***VCONN-Powered USB Device***. Instead, the Host ***may*** assume the cable is 5 A for the purposes of calculating the Charge-Through current limit only if it receives a ***USB PD*** Source Capability PDO of greater than 3 A (even if the Host ultimately does not ***Request*** that PDO, or if the host requests a current of 3 A or less).

The Host ***shall*** further limit its maximum current beyond that advertised by the Power Source, based on the reported GND impedance and the inferred cable capability. GND impedance is reported in the ***VPD Discover Identity*** Command Response in 1-milliohm steps and is used in the following formulas:

- GND-limited current with a 3A cable inferred = 0.25 V / (0.25 V / 3 A + VPD_GND_DCR), and
- GND-limited current with a 5A cable inferred = 0.25 V / (0.25 V / 5 A + VPD_GND_DCR).

Some examples are in Table 4-21.

Table 4-21 Sink Maximum Current Limit When Attached to CTVPD

Reported GND Impedance	3A Cable Inferred[1]	5A Cable Inferred[2]
0.010 Ω	2.679 A	4.167 A
0.015 Ω	2.542 A	3.846 A
0.020 Ω	2.419 A	3.571 A
0.025 Ω	2.308 A	3.333 A
0.030 Ω	2.206 A	3.125 A
0.035 Ω	2.113 A	2.941 A
0.040 Ω	2.027 A	2.778 A

Notes:
1. As calculated by 0.25 V / (0.25 V / 3 A + VPD_GND_DCR).
2. As calculated by 0.25 V / (0.25 V / 5 A + VPD_GND_DCR).

In addition, the increased VBUS impedance could result in a greater than 1 V VBUS drop as measured at the input to the Host. Based on the VBUS impedance reported in the ***VPD Discover Identity*** Command Response

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in 2-milliohm steps and the inferred cable capability, the Host ***shall*** either lower its VBUS detach threshold or further limit its maximum current based on the following formulas:

- VBUS and GND-limited current with a 3A cable inferred = 0.75 V / (0.75 V / 3 A + VPD_VBUS_DCR + VPD_GND_DCR), and
- VBUS and GND-limited current with a 5A cable inferred = 0.75 V / (0.75 V / 5 A + VPD_VBUS_DCR + VPD_GND_DCR).

Table 4-22 Example Charge-Through VPD Sink Maximum Currents based on VBUS Impedance and GND Impedance

Reported VBUS Impedance[4]	Reported GND Impedance[4]	3A Cable Inferred[1]	5A Cable Inferred[2]
0.020 Ω	0.010 Ω	2.679 A	4.167 A
0.030 Ω	0.015 Ω	2.542 A	3.846 A
0.040 Ω	0.020 Ω	2.419 A	3.571 A
0.050 Ω	0.025 Ω	2.308 A	3.333 A
0.060 Ω	0.030 Ω	2.206 A	3.125 A
0.070 Ω	0.035 Ω	2.113 A	2.941 A
0.080 Ω	0.040 Ω	2.027 A	2.778 A

Notes:

1. As calculated by 0.75 V / (0.75 V / 3 A + VPD_VBUS_DCR + VPD_GND_DCR).
2. As calculated by 0.75 V / (0.75 V / 5 A + VPD_VBUS_DCR + VPD_GND_DCR).
3. The table does not show all allowable combinations, only a subset provided for illustration.
4. The ratio of the reported VBUS impedance to the reported GND impedance is 2:1.

4.6.2.6 USB Type-C Sink Requirements for High Voltage Operation

This section sets electrical requirements for USB Type-C Sinks that support high-voltage operation. See Section 3.11 for EPR requirements for USB Type-C cables that support EPR.

The Sink ***shall*** keep the voltage on its VBUS contact to within 12 volts of the voltage on the Source VBUS contact at the time of the cable plug withdrawal for a minimum of 250 µs from the time the VBUS contacts separate (see Figure 3-1). Refer to Appendix H for more information related to high-voltage contact arcing and mitigation guidelines.

4.7 USB Hubs

USB 2.0, ***USB 3.2***, and ***USB4*** hubs are defined by the ***USB 2.0***, ***USB 3.2***, and ***USB4*** specifications, respectively. USB hubs implemented with one or more USB Type-C connectors ***shall*** comply with these specifications as relevant to a USB Type-C implementation. All the downstream facing USB Type-C ports on a USB hub ***should*** support the same functionality or ***shall*** be clearly marked as to the functionality supported.

USB hubs ***shall*** have an upstream facing port (to connect to a host or hub higher in the USB tree) that ***may*** be a Sourcing Device (See Section 4.8.4). The hub ***shall*** clearly identify to the user its upstream facing port. This ***may*** be accomplished by physical isolation, labeling or a combination of both.

USB hub's downstream facing ports ***shall not*** have Dual-Role-Data (DRD) capabilities. However, these ports ***may*** have Dual-Role-Power (DRP) capabilities.

CC pins are used for port-to-port connections and ***shall*** be supported on all USB Type-C connections on the hub.

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For ***USB 2.0*** and ***USB 3.2*** hubs, downstream-facing ports ***shall not*** implement or pass-through Alternate or Accessory Modes and SBU pins ***shall not*** be connected (***zSBUTermination***) on any USB hub port. For ***USB4*** hubs, see Section 5.2.3 regarding support for ***Alternate Modes***.

The USB hub's DFPs ***shall*** support power source requirements for a Source. See Section 4.8.1.

Additional requirements for ***USB4*** hubs are in Chapter 5.

4.8 Power Sourcing and Charging

This section defines requirements and recommendations related to using USB Type-C ports for delivering power. Any USB Type-C port that offers more than Default Current and/or supports ***USB Power Delivery*** ***shall*** meet the requirements as if it is a charger.

The following lists the most applicable subsections by USB Type-C ports on:

- Host systems: 4.8.1 and 4.8.5. Note: 4.8.6 is not intended for host systems.
- Devices that can supply power: 4.8.4.
- Hubs:
  - Traditional hubs – Refer to ***USB 2.0***/***USB 3.2*** base specifications and 4.8.1 as applicable if ***USB BC 1.2*** is supported.
  - Hubs that can supply power beyond the base specs – 4.8.1, 4.8.4, 4.8.5 and 4.8.6.
- Dedicated chargers:
  - Single-port chargers – 4.8.1.
  - Multi-port chargers – 4.8.1 and 4.8.6.

4.8.1 DFP as a Power Source

Sources (e.g., battery chargers, hub downstream ports and hosts) ***may*** all be used for battery charging. When a charger is implemented with a USB Type-C receptacle or a USB Type-C captive cable, it ***shall*** follow all the applicable requirements.

- A Source ***shall*** expose its power capabilities using the ***USB Type-C Current*** method and it ***may*** additionally support other USB-standard methods (***USB BC 1.2*** or ***USB PD***).
- A Source advertising its current capability using ***USB BC 1.2 shall*** meet the requirements in Section 4.6.2.2 regarding ***USB Type-C Current*** advertisement.
- A Source that has negotiated a ***USB PD*** contract ***shall*** meet the requirements in Section 4.6.2.4 regarding ***USB Type-C Current*** advertisement.
- If a Source is capable of supplying a voltage greater than default VBUS, it ***shall*** fully conform to the ***USB PD*** specification and ***shall*** negotiate its power contracts using only ***USB PD***.
- If a Source is capable of reversing source and sink power roles, it ***shall*** fully conform to the ***USB PD*** specification and ***shall*** negotiate its power contracts using only ***USB PD***.
- If a Source is capable of supplying a current greater than 3.0 A, it ***shall*** use the ***USB PD Discover Identity*** to determine the current carrying capacity of the cable.

4.8.1.1 USB-based Chargers with USB Type-C Receptacles

- A USB-based charger with a USB Type-C receptacle (Source) ***shall*** only apply power to VBUS when it detects a Sink is attached and ***shall*** remove power from VBUS when it detects the Sink is detached (***vOPEN***).

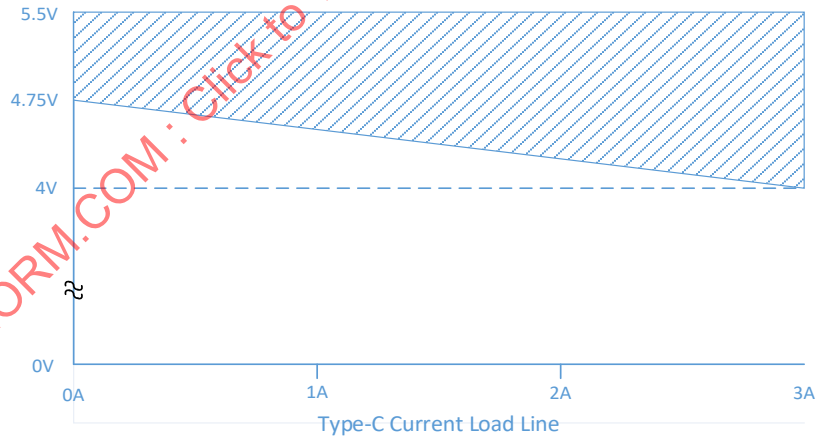
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- A USB-based charger with a USB Type-C receptacle ***shall not*** advertise current exceeding 3.0 A except when it uses the ***USB PD Discover Identity*** mechanism to determine the cable's actual current carrying capability and then it ***shall*** limit the advertised current accordingly.
- A USB-based charger with a USB Type-C receptacle (Source) which is not capable of data communication ***shall*** advertise ***USB Type-C Current*** of at least 1.5 A within ***tVBUSON*** of entering the ***Attached.SRC*** state and ***shall*** short D+ and D– together with a resistance less than 200 ohms. This will ensure backwards compatibility with legacy sinks which ***may*** use ***USB BC 1.2*** for charger detection.

4.8.1.2 USB-based Chargers with USB Type-C Captive Cable

- A USB-based charger with a USB Type-C captive cable ***shall*** only apply power to VBUS when it detects a Sink is attached and ***shall*** remove power from VBUS when it detects the Sink is detached (***vOPEN***).
- A USB-based charger with a USB Type-C captive cable ***shall*** limit its current advertisement so as not to exceed the current capability of the cable (up to 5 A).
- A USB-based charger with a USB Type-C captive cable which is not capable of data communication ***shall*** advertise ***USB Type-C Current*** of at least 1.5 A. It ***shall*** short D+ and D– together with a resistance less than 200 ohms. This will ensure backwards compatibility with legacy sinks which ***may*** use ***USB BC 1.2*** for charging detection.
- The voltage as measured at the plug of a USB-based charger with a USB Type-C captive cable ***may*** be up to 0.75 × I / 3 V (0 < I ≤ 3 A), or 0.75 × I / 5 V (0 < I ≤ 5 A) lower than the standard tolerance range for the chosen voltage, where I is the actual current being drawn.
    - A USB-based charger that advertises ***USB Type-C Current*** ***shall*** output a voltage in the range of 4.75 V – 5.5 V when no current is being drawn and between 4.0 V – 5.5 V at 3 A. The output voltage as a function of load up to the advertised ***USB Type-C Current*** (default, 1.5 A and 3 A) ***shall*** remain within the cross-hatched area shown in Figure 4-40.

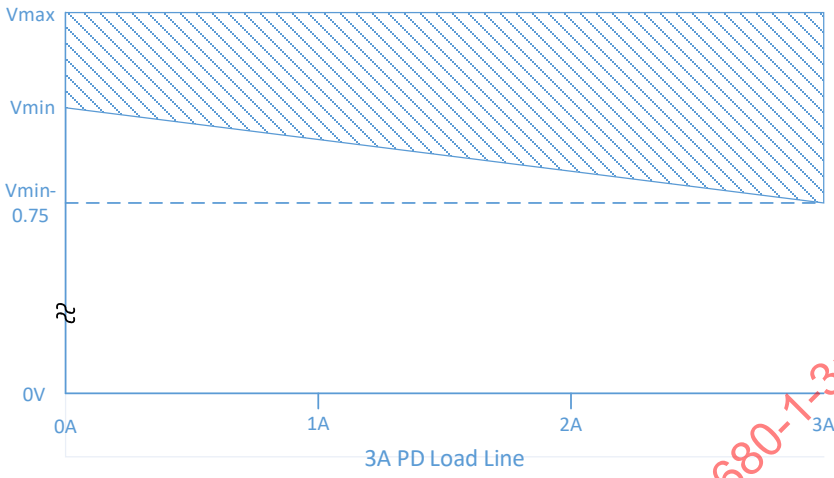
Figure 4-40 USB Type-C Cable's Output as a Function of Load for Non-PD-based USB Type-C Charging



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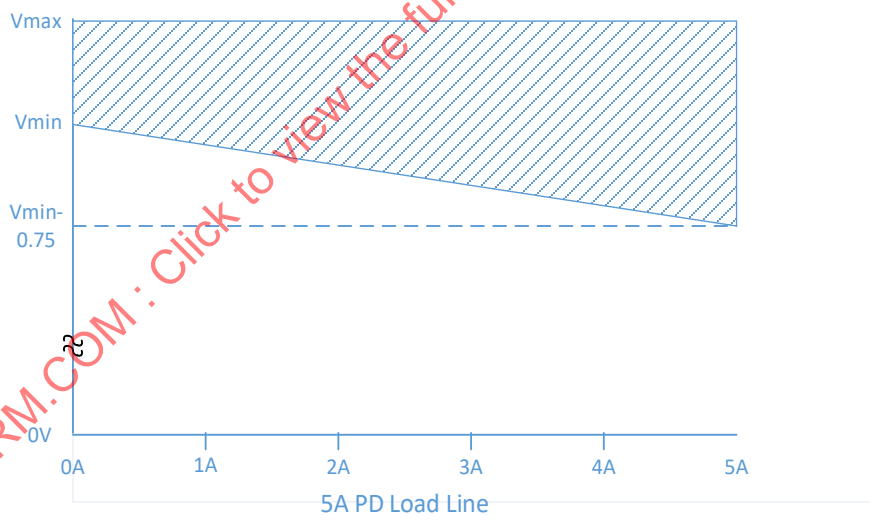
    - A ***USB PD***-based charger that has negotiated a voltage V at ≤ 3 A ***shall*** output a voltage in the range of Vmax (V + 5%) and Vmin (V – 5%) when no current is being drawn and Vmax and Vmin – 0.75 V at 3 A. Under all loads, the output voltage ***shall*** remain within the cross-hatched area shown in Figure 4-41.

Figure 4-41 0 – 3 A *USB PD*-based Charger USB Type-C Cable's Output as a Function of Load



- A ***USB PD***-based charger that has negotiated a voltage V at between 3 A and 5 A ***shall*** output a voltage in the range of Vmax (V + 5%) and Vmin (V – 5%) when no current is being drawn and Vmax and Vmin – 0.75 V at 5 A. Under all loads, the output voltage ***shall*** remain within the cross hatched area shown in Figure 4-42.

Figure 4-42 3 – 5 A *USB PD*-based Charger USB Type-C Cable's Output as a Function of Load



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- Note: The maximum allowable cable IR drop for ground is 250 mV (see Section 4.4.1). This is to ensure the signal integrity of the CC wire when used for connection detection and ***USB PD*** BMC signaling.

4.8.2 Non-USB Charging Methods

A product (Source and/or Sink) with a USB Type-C connector ***shall*** only employ signaling methods defined in USB specifications to negotiate power over its USB Type-C connector(s).

4.8.3 Sinking Host

A Sinking Host is a special sub-class of a DRP that is capable of consuming power but is not capable of acting as a USB device. For example, a hub's DFP or a notebook's DFP that operates as a host but not as a device.

The Sinking Host ***shall*** follow the rules for a DRP (See Section 4.5.1.4 and Figure 4-15). The Sinking DFP ***shall*** support ***USB PD*** and ***shall*** support the ***DR_Swap*** command. If the Sinking Host ends up in the UFP data role after entering ***Attached.SNK*** and establishing an Explicit ***USB PD*** contract, it ***shall*** accept or send a ***DR_Swap*** command in order to get itself into the DFP data role.

4.8.4 Sourcing Device

A Sourcing Device is a special sub-class of a DRP that is capable of supplying power but is not capable of acting as a USB host. For example, a hub's UFP or a monitor's UFP that operates as a device but not as a host.

The Sourcing Device ***shall*** follow the rules for a DRP (See Section 4.5.1.4 and Figure 4-15). It ***shall*** also follow the requirements for the Source as Power Source (See Section 4.8.1). The Sourcing Device ***shall*** support ***USB PD*** and ***shall*** support the ***DR_Swap*** command. If the Sourcing Device ends up in the DFP data role after entering ***Attached.SRC*** and establishing an Explicit ***USB PD*** contract, it ***shall*** accept or send a ***DR_Swap*** command in order to get itself into the UFP data role.

4.8.5 Charging a System with a Dead Battery

A system that supports being charged by USB whose battery is dead ***shall*** apply ***Rd*** to both CC1 and CC2 and follow all Sink rules. When it is connected to a Source, DRP or Sourcing Device, the system will receive the default V_{BUS}. It ***may*** use any allowed method to increase the amount of power it can use to charge its battery.

Circuitry to present ***Rd*** in a dead battery case only needs to guarantee the voltage on CC is pulled within the same range as the voltage clamp implementation of ***Rd*** in order for a Source to recognize the Sink and provide V_{BUS}. For example, a 20% resistor of value ***Rd*** in series with a FET with $V_{GTH}(max) < V_{CLAMP}(max)$ with the gate weakly pulled to CC would guarantee detection and be removable upon power up.

When the system with a dead battery has sufficient charge, it ***may*** use the ***USB PD DR_Swap*** message to become the DFP.

4.8.6 USB Type-C Multi-Port Chargers

A USB Type-C Multi-Port Charger is a product that exposes multiple USB Type-C Source ports for the purpose of charging multiple connected devices. A compliant USB Type-C charger ***may*** offer on each of its ports a mix of power options as defined in Section 4.6.

Multi-Port Chargers will generally fall into two categories as defined by the following.

1. Assured Capacity Chargers: a multi-port charger where the sum of the maximum capabilities of all of the exposed ports, as indicated to the user, is equal to the total power delivery capacity of the charger. A port in an Assured Capacity group has a fixed allocated amount of power and is either a Guaranteed Capability port or Managed Capability port as defined in the ***USB PD*** specification.
2. Shared Capacity Chargers: a multi-port charger where the sum of the maximum capabilities of all of the exposed ports, as indicated to the user, is less than the total power delivery capacity of the charger. A port in a Shared Capacity group does not have a fixed allocated amount of power and is a Managed Capability port as defined in the ***USB PD*** specification.

A Multi-Port Charger ***may*** offer in a single product separate visually identifiable groupings of charging ports. In this case, each group can independently offer either one of the two charging categories, either an Assured Capacity Charger or a Shared Capacity Charger.

This section defines the requirements and provides guidelines for the operation and behavior of a USB Type-C Multi-Port Charger.

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4.8.6.1 General Requirements

Individual source ports ***shall*** always comply with power negotiation and rules set forth by the USB Type-C and ***USB Power Delivery*** specifications, adjusted as needed when available resources change as other ports take more or less power.

The minimum capability of all individual USB Type-C ports of a USB Type-C Multi-Port Charger ***shall*** be 5 V @ 1.5 A independent of how many of the other ports are in use.

For Shared Capacity Chargers, the following are defined:

- **Total Shared Capacity** is the total power available for a Shared Capacity group of ports. This is the overall power available when none of the ports in the group are connected to Sinks
- **Remaining Power Available** = Total Shared Capacity minus the sum of the power allocated to the attached ports. When doing this calculation, for ports in a ***USB PD*** power contract, the maximum power offered in the ***USB PD*** source capabilities is used, not the power requested in the RDO.
- **Shared Port Power Available** is either:
    a) the port's PDP when it is less than or equal to the Remaining Power Available,
    b) the Remaining Power Available when it is greater than 7.5 W and less than the port's PDP, or
    c) 7.5 W.

When a Shared Capacity Charger reclaims power from one or more already connected ports to meet the 7.5 W minimum requirement for a newly attached device, the charger ***shall*** use standard ***USB Type-C Current*** and/or ***USB PD*** renegotiation methods and ***shall not*** use Hard Resets, ***Error Recovery***, or the ***Disabled*** state.

When a USB Type-C Charger includes charging ports that are based on USB Standard-A receptacles, the following requirements ***shall*** be met.

- The USB Standard-A ports ***shall*** be implemented as an independent group, i.e., USB Standard-A ports ***shall not*** be included in a group of USB Type-C ports behaving as a Shared Capacity Charger. Any load change on a USB Type-A port ***shall not*** result in a voltage change on any of the USB Type-C ports and vice-versa.
- The minimum capability of each USB Standard-A port ***shall*** be 5 V @ 500 mA independent of how many of the other ports are in use.

Implementation Note: When designing a Shared Capacity Charger, user experience should be an important factor in deciding the Total Shared Capacity to support. There are tradeoffs to be made regarding port PDP, the number of ports, and the total power available to be shared that will notably impact what a user can expect when charging multiple devices.

Table 4-23 gives some comparative examples of a 4-port Shared Capacity Charger to illustrate how the PDP and Total Shared Capacity impacts user experience as more devices are connected to the charger. Two simplistic power sharing policies are illustrated: a Highest-to-Lowest policy that emphasizes supplying the highest power to ports based on a first-come/first-serve priority, and a Balanced policy that always equally balances power across all connected ports. These example policies assume that the charger has no knowledge of the device's specific needs other than what the device requests when selecting from the charger's advertised capabilities, and that the order of connecting devices is from highest to lowest power consumer.

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Table 4-23 Examples of 4-port Shared Capacity Chargers and Power Sharing Policies

	Port PDP Rating	Total Shared Capacity	Highest-to-Lowest				Balanced				Notes
			1	2	3	4	1	2	3	4	
1	**7.5 W**	30 W	**7.5**	-	-	-	**7.5**	-	-	-	The minimal implementation is the functional equivalent to a group of Assured Ports where the Total Shared Capacity = PDP · *n* with *n* being the number of ports in the group.
			7.5	**7.5**	-	-	**7.5**	**7.5**	-	-	
			7.5	**7.5**	**7.5**	-	**7.5**	**7.5**	**7.5**	-	
			7.5	**7.5**	**7.5**	**7.5**	**7.5**	**7.5**	**7.5**	**7.5**	
2	**30 W**	30 W	**30**	-	-	-	**30**	-	-	-	These implementation examples illustrate that as Total Shared Capacity increases while port count and PDP remain constant, the user experience when charging multiple devices improves. Also, as the ratio of Total Shared Capacity to Port PDP Rating increases, the sharing policy of the charger relies less on reclaiming power from already connected ports.
			22.5	7.5	-	-	15	15	-	-	
			15	7.5	7.5	-	10	10	10	-	
			7.5	7.5	7.5	7.5	7.5	7.5	7.5	7.5	
3	**30 W**	60 W	**30**	-	-	-	**30**	-	-	-	
			30	**30**	-	-	**30**	**30**	-	-	
			30	22.5	7.5	-	20	20	20	-	
			30	15	7.5	7.5	15	15	15	15	
4	**30 W**	100 W	**30**	-	-	-	**30**	-	-	-	
			30	**30**	-	-	**30**	**30**	-	-	
			30	**30**	**30**	-	**30**	**30**	**30**	-	
			30	**30**	**30**	10	25	25	25	25	

More sophisticated policies could be implemented for an even better user experience, these likely considering capabilities information retrieved from the device. For example, when multiple devices are attached, the needs of each device can be determined, and power allocated to give preference to devices that require higher power. As each new device is attached, power can be rebalanced after considering the additional needs of the new device.

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4.8.6.2 Multi-Port Charger Behaviors

Each Source port of Assured Capacity Chargers ***shall***, by design, behave independently and be unaffected by the status and loading of the other ports. An exception to this behavior is allowed if the charger has to take any action necessary to meet an overall product operational safety requirement due to unexpected behavior on any port.

For Shared Capacity Chargers, the following behavioral rules ***shall*** apply:

- Each of the exposed Source Ports ***shall*** have the same power capabilities. Each port of the charger ***shall*** be capable of the same maximum capability, minimum capability, and be able to draw from the shared power equally.
    - Ports ***shall*** have the ability to supply the available shared capacity power up to the port's maximum power (PDP).
        - Ports ***may*** offer less than this value but ***shall*** increase the offer up to the required value when the Sink sets the Capabilities Mismatch bit in its response. This ***may*** be done in multiple steps, but all ports in the Shared Capacity Group ***shall*** reach the maximum power within three seconds.

  - Whenever a power contract is made or changed on any port, the Remaining Power Available and the Shared Port Power Available ***shall*** be re-computed, and the Source ***shall*** send updated Source Capability messages as needed.
  - Ports when not in a ***USB PD*** contract ***shall*** follow the rules for a shared ***USB Type-C Current*** source.
- All exposed ***USB Type-C Current*** ports ***shall*** have the ability to offer the same power capabilities.
  - All ports ***shall*** initially offer at least 1.5 A, e.g., ***shall not*** offer Default.
  - The total of offers across all the ports ***shall*** never exceed the capacity of the shared supply.
  - Ports that initially offer 1.5 A ***shall*** increase to 3 A after attach if they have sufficient available shared capacity within one second.

As Source ports are connected and begin providing power, the remaining Source ports will each have the same power capabilities. The maximum capability ***may*** be less than the previously connected ports due to less unused capacity of the total power delivery capacity of the charger. For example, if the total power delivery capacity of a USB Type-C two-port charger is 60 W with a port PDP of 35 W and the first connected Source port has established a 35 W power contract with its connected Sink, then the second Source port will only be able to offer a PDP of 25 W.

Each port ***should*** start by offering the minimum capability for the port and increase the offering to the Sink upon a connection. For example, if the maximum capability of a USB Type-C only Source port is 3 A, then all the exposed Source ports will be able to offer 3 A. Each port ***should*** start by offering less than the max (such as 1.5 A) and then increase the offering to 3 A after an attach. This would happen for each port as it is connected until the unused shared capacity is exhausted, at which point no other ports would increase to 3 A offering. A sink, in this example, would see a starting advertisement of ***USB Type-C Current*** @ 1.5 A at attach and would then see the ***USB Type-C Current*** advertisement increase to 3 A. As another example, if the maximum capability of a USB Type-C Source port is to offer ***USB PD*** with a PDP of 35 W, then all the exposed Source ports would also support ***USB PD*** 35 W. Each port would start by offering something less on initial connection, like 15 W, and then increase the offering with new Source Capabilities when it determines the Sink would like more power. If the Sink is not offered the power it requires, it will send a request with the Capability Mismatch bit set to indicate to the source it wants more power. This will happen for each port as it is connected until the unused shared capacity is exhausted, at which point no other ports would increase the power offering.

When establishing the remaining available capacity, a charger that supports policy-based power rebalancing ***may*** include the power that can be reclaimed from ports already in use:

1. by adjusting advertised source capabilities equivalent with a reduced PDP to one or more ports that are already in use; or
2. by issuing a ***USB PD*** GotoMin command to one or more ports already in use.

Policy-based power rebalancing ***should*** consider providing good user experience and preserving nominal USB functionality of impacted devices. Fixed rebalancing algorithms that do not factor in overall USB system policy ***may not*** be appropriate for power rebalancing implementations.

4.8.6.3 Multi-Port Charger Port Labeling

Multi-port chargers ***shall*** have OEM-designed port labeling consistent with the following rules.

- For Assured Capacity Chargers, each exposed Source port ***shall*** be labeled to indicate the PDP of the port. In this case, the user will be able to expect that each of the labeled ports will be able to meet power contracts consistent with the labeling independent of how many of the Source ports are in use.
- For Shared Capacity Chargers, each Source port ***shall*** be labeled to indicate the same PDP. Additionally, the charger ***shall*** have a label that, with a minimum of equal visual prominence,

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indicates the Total Shared Capacity (see Section 4.8.6.1) shared across all the ports identified as a group.

A Multi-Port Charger that offers in a single product separate groupings of charging ports, each grouping ***shall*** be clearly identified as a separate grouping and each grouping ***shall*** be individually labeled consistent with that group's behavior model, either as an Assured Capacity Charger or a Shared Capacity Charger.

Refer to the USB Implementers Forum (***USB-IF***) for USB Type-C Chargers certification along with further labeling guidelines.

4.8.6.4 Multi-Port Charger that includes USB Data Hub Functionality

Multi-Port chargers that also incorporate USB data hub capabilities ***shall*** meet the same requirements as standalone chargers. These charging-capable hubs ***shall*** be self-powered and ***shall*** fully operate as a charger independent of the state of the USB data bus connections.

For hub-based Multi-Port Chargers that offer power to the upstream-facing port (to the host), this port ***may*** either behave as an Assured Capacity Charging port (e.g., be a dedicated charging port) or as a Shared Capacity Charging port (e.g., sharing capacity with downstream-facing ports). In either case, it ***should*** be clearly labeled consistent with its designed behavior, including identifying it as part of a group if it is sharing capacity with other ports.

When the upstream-facing port is sharing capacity with the downstream-facing ports, the PDP of the upstream-facing port can differ from the downstream-facing ports.

4.9 Electronically Marked Cables

All USB Full-Featured Type-C cables ***shall*** be electronically marked. ***USB 2.0*** Type-C cables ***may*** be electronically marked. An eMarker is an element in an Electronically Marked Cable that returns information about the cable in response to a ***USB PD Discover Identity*** command.

Electronically marked cables ***shall*** support ***USB Power Delivery*** Structured VDM ***Discover Identity*** command directed to SOP' (the eMarker). This provides a method to determine the characteristics of the cable, e.g., its current carrying capability, its performance, vendor identification, etc. This ***may*** be referred to as the USB Type-C Cable ID function.

Prior to an explicit ***USB PD*** contract, a Sourcing Device is allowed to use SOP' to discover the cable's identity. After an explicit ***USB PD*** contract has been negotiated, only the VCONN Source ***shall*** communicate with SOP' and SOP" (see also Section 6.1.1).

Passive cables that include an eMarker ***shall*** follow the Cable State Machine defined in Section 4.5.2.4 and Figure 4-20.

Once VCONN is available, all electronically marked cables ***shall*** use it as the only power source. If VCONN is applied after VBUS then until VCONN is available, the cable ***may*** remain unpowered or ***may*** draw power from VBUS. Within ***tVCONNSwitch***, the cable ***shall*** switch from VBUS to VCONN. Cables that include an eMarker ***shall*** meet the maximum power defined in Table 4-6. The only exception is an Optically Isolated Active Cable (OIAC Section 6), which can draw from both VCONN and VBUS.

Refer to Table 4-5 for the requirements of a Source to supply VCONN. When VCONN is not present, a powered cable ***shall not*** interfere with normal CC operation including Sink detection, current advertisement, and ***USB PD*** operation.

Figure 4-43 illustrates a typical electronically marked cable. The isolation elements (Iso) ***shall*** prevent VCONN from traversing end-to-end through the cable. ***Ra*** is required in the cable to allow the Source to determine that VCONN is needed.

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Figure 4-43 Electronically Marked Cable with VCONN connected through the cable

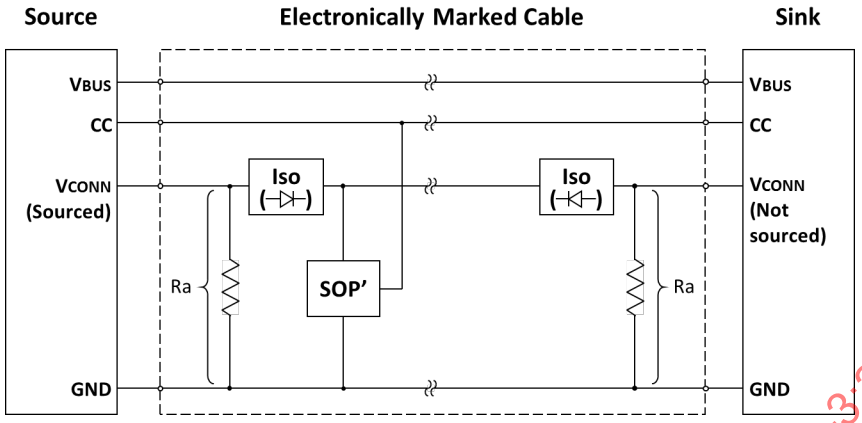
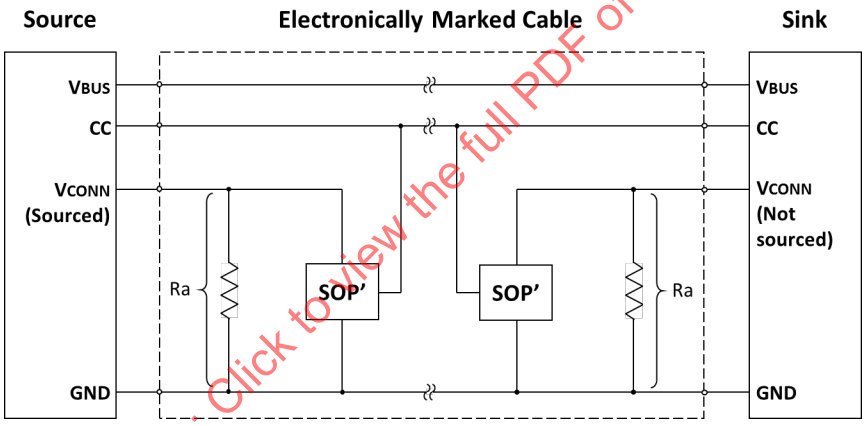


Figure 4-44 illustrates an electronically marked cable where the VCONN wire does not extend through the cable, therefore an SOP' (eMarker) element is required at each end of the cable. In this case, no isolation elements are needed.

Figure 4-44 Electronically Marked Cable with SOP' at both ends



For cables that only respond to SOP', the location of the responder is not relevant.

4.9.1 Parameter Values

Table 4-24 provides the power on timing requirements for the eMarker SOP' and SOP" to be ready to communicate.

Table 4-24 SOP' and SOP" Timing

	Maximum	Description
tVCONNStable	50 ms	The time between the application of VCONN until SOP' and SOP" ***shall*** be ready for communication.

4.9.2 Active Cables

An active cable is an electronically marked cable that incorporates data bus signal conditioning circuits, for example to allow for implementing longer cables. Active cables with data bus signal conditioning in both

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plugs ***shall*** implement SOP' and ***may*** implement SOP". Active cables ***shall*** meet the power requirements defined in Table 4-6.

Active cables ***may*** support either one TX/RX pair or two TX/RX pairs. The eMarker in the cable ***shall*** identify the number of TX/RX lanes supported. Active cables ***may*** or ***may not*** require configuration management. Active cable configuration management is defined in Section 6.

4.10 VCONN-Powered Accessories (VPAs) and VCONN-Powered USB Devices (VPDs)

VCONN-Powered Accessories and ***VCONN-Powered USB Devices*** are both direct-attach Sinks that can operate with just VCONN.

Both expose a maximum impedance to ground of ***Ra*** on the VCONN pin and ***Rd*** on the CC pin.

The removal of VCONN when VBUS is not present ***shall*** be treated as a detach event.

4.10.1 VCONN-Powered Accessories (VPAs)

A ***VCONN-Powered Accessory*** implements an ***Alternate Mode*** (See Appendix E).

VCONN-Powered Accessories ***shall*** comply with Table 4-7.

When operating in the Sink role and when VBUS is not present, ***VCONN-Powered Accessories*** ***shall*** treat the application of VCONN as an attach signal and ***shall*** respond to ***USB Power Delivery*** messages.

When powered by only VCONN, a ***VCONN-Powered Accessory*** ***shall*** negotiate an ***Alternate Mode***. If it fails to negotiate an ***Alternate Mode*** within ***tAMETimeout***, its port partner removes VCONN.

When VBUS is supplied, a ***VCONN-Powered Accessory*** is subject to all the requirements for ***Alternate Modes***, including presenting a ***USB Billboard Device Class*** interface if negotiation for an ***Alternate Mode*** fails.

Should a ***VCONN-Powered Accessory*** wish to provide charge-through functionality, it must do so by negotiating voltage and current independently on both the Host and charge-through ports, and possibly re-regulating the voltage from the Source before passing it through to the Sink. The Sink can take the full current that is advertised to it by the ***VCONN-Powered Accessory***.

4.10.2 VCONN-Powered Devices (VPDs)

A ***VCONN-Powered USB Device*** ***shall*** implement a USB UFP endpoint.

VCONN-Powered USB Devices ***shall*** comply with Table 4-8.

When VBUS is not present, ***VCONN-Powered USB Devices*** ***shall*** treat the application of VCONN as an attach signal.

A ***VCONN-Powered USB Device*** ***shall*** respond to ***USB PD*** messaging on SOP' and ***shall not*** respond to other ***USB PD*** messaging. A ***VCONN-Powered USB Device*** ***shall*** respond to ***USB PD*** Hard Reset and Cable Reset signaling.

A Charge-Through ***VCONN-Powered USB Device*** ***shall*** discard all ***USB PD*** messages while a connection is enabled between the host port CC and Charge-Through port CC.

When VBUS is supplied by the Host, the ***VCONN-Powered USB Device*** ***shall*** behave like a normal UFP Sink, but still only respond to ***USB PD*** messaging on SOP'. If VBUS is subsequently removed while VCONN remains applied, the ***VCONN-Powered USB Device*** ***shall*** remain connected, and use VCONN as the sole detach signal.

Since ***VCONN-Powered USB Devices*** do not respond to ***USB PD*** on SOP, they cannot enter ***Alternate Modes***.

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A ***VCONN-Powered USB Device*** ***may*** provide Charge-Through functionality via ***VPD*** Charge-Through. ***VCONN-Powered USB Devices*** ***shall not*** provide any data pass-through to the Charge-Through port other than the CC wire.

Since the power and CC negotiation is passed through directly, the Sink ***shall*** limit its maximum current based on the additional impedance introduced by the ***VCONN-Powered USB Device***.

Additionally, since power can only flow from the Charge-Through port to the Host, VCONN must be provided by the host, and there is no data connection beyond the CC wire passed through to the connected source, there are limitations on what the Host can advertise and support via ***USB PD***:

- The Host ***shall not*** negotiate or accept a ***PR_Swap*** or ***VCONN_Swap***.
- The Host ***shall not*** enable ***FR_Swap***.
- The Host ***may*** only negotiate a ***DR_Swap*** when using ***USB PD*** Revision 2.0, and only for the purpose of switching which side initiates PD communications. The Host will always remain a DFP for USB data.
- The Host ***shall not*** advertise dual-role data or dual-role power in its Source Capability or Sink Capability messages – Host changes its advertised capabilities to UFP role/sink only role.
- The Host ***shall not*** negotiate any ***Alternate Modes*** that change the function of pins on the connector.
- The Host ***shall*** represent itself to the Charge-Through Source using ***USB PD*** as if it were a Sink-only, data-less device.

Table 4-25 Charge-Through VPD CC Impedance (RccCON) Requirements

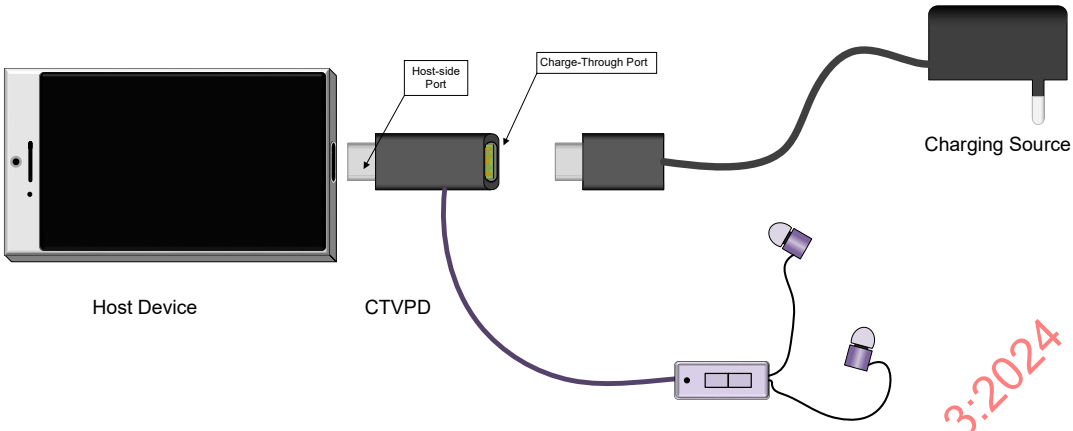
	Minimum	Maximum	Description
RccCON		15 Ω	Impedance in the Charge-Though ***VPD*** while a connection is enabled between the host port CC and Charge-Through port CC.
	zOPEN		Impedance between the host port CC and Charge-Through CC when a connection is disabled.

Table 4-26 CTVPD Charge-Through Port VBUS Bypass Requirements

	Minimum	Maximum	Description
CCTB	1 µF	10 µF	Bypass capacitance on Charge-Through port VBUS connection to support ADP max CADP_THR.

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Figure 4-45 Example Charge-Through VCONN-Power USB Device Use Case



4.11 Parameter Values

4.11.1 Termination Parameters

Table 4-27 provides the values that ***shall*** be used for the Source's ***Rp*** or current source. Other pull-up voltages ***shall*** be allowed if they remain less than 5.5 V and fall within the correct voltage ranges on the Sink side – see Table 4-35, Table 4-36 and Table 4-37. Note: when two Sources are connected together, they ***may*** use different termination methods which could result in unexpected current flow.

Table 4-27 Source CC Termination (Rp) Requirements

Source Advertisement	Current Source to 1.7 – 5.5 V	Resistor pull-up to 4.75 – 5.5 V	Resistor pull-up to 3.3 V ± 5%
Default USB Power	80 µA ± 20%	56 kΩ ± 20% (Note 1)	36 kΩ ± 20%
1.5 A @ 5 V	180 µA ± 8%	22 kΩ ± 5%	12 kΩ ± 5%
3.0 A @ 5 V	330 µA ± 8%	10 kΩ ± 5%	4.7 kΩ ± 5%

Note 1: For ***Rp*** when implemented in the USB Type-C plug on a USB Type-C to ***USB 3.1*** Standard-A Cable Assembly, a USB Type-C to ***USB 2.0*** Standard-A Cable Assembly, a USB Type-C to ***USB 2.0*** Micro-B Receptacle Adapter Assembly or a USB Type-C captive cable connected to a USB host, a value of 56 kΩ ± 5% ***shall*** be used, in order to provide tolerance to IR drop on VBUS and GND in the cable assembly.

The Sink ***may*** find it convenient to implement ***Rd*** in multiple ways simultaneously (a wide range ***Rd*** when unpowered and a trimmed ***Rd*** when powered). Transitions between ***Rd*** implementations that do not exceed ***tCCDebounce*** ***shall not*** be interpreted as exceeding the wider ***Rd*** range. Transitions between ***Rd*** implementations ***shall not*** allow the voltage on CC to go outside the voltage band that defines a connection. Table 4-28 provides the methods and values that ***shall*** be used for the Sink's ***Rd*** implementation.

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Table 4-28 Sink CC Termination (Rd) Requirements

Rp Implementation	Nominal Value	Can detect power capability?	Max voltage on pin
± 20% voltage clamp[1]	1.1 V	No	1.32 V
± 20% resistor to GND	5.1 kΩ	No	2.18 V
± 10% resistor to GND	5.1 kΩ	Yes	2.04 V

Note 1: The clamp implementation inhibits ***USB PD*** communication although the system can start with the clamp and transition to the resistor once it is able to do ***USB PD***.

Table 4-29 provides the impedance value to ground on VCONN in powered cables.

Table 4-29 Powered Cable Termination Requirements

	Minimum Impedance	Maximum Impedance
Ra	800 Ω[1]	1.2 kΩ

Note:
1. The minimum impedance ***may*** be less after VCONN is applied. The current consumed from VCONN ***shall*** be as specified in Table 4-6, Table 4-7, and Table 4-8 when the voltage is less than vVCONNValid. The voltage across ***Ra*** when connected to any valid ***Rp*** ***shall*** be below the Max voltage in Table 4-39 Voltage on Sink CC pins (Multiple Source Current Advertisements) for ***vRa***.

Table 4-30 provides the minimum impedance value to ground on CC for a device (Sink or Source) to be undetected by a Source. This ***shall*** apply for ports in the ***Disabled*** state or ***ErrorRecovery*** state. This ***shall*** also apply for Sources when unpowered (for example a power brick unplugged from AC mains).

Table 4-30 CC Termination Requirements for Disabled state, ErrorRecovery state, and Unpowered Source

	Minimum Impedance to GND	Notes
zOPEN	126 kΩ	***zOPEN shall*** only be evaluated below ***vCC-Clamp***.

Table 4-31 provides the impedance value for an SBU to appear open.

Table 4-31 SBU Termination Requirements

	Termination	Notes
zSBUTermination	≥ 950 kΩ	Functional equivalent to an open circuit.

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4.11.2 Timing Parameters

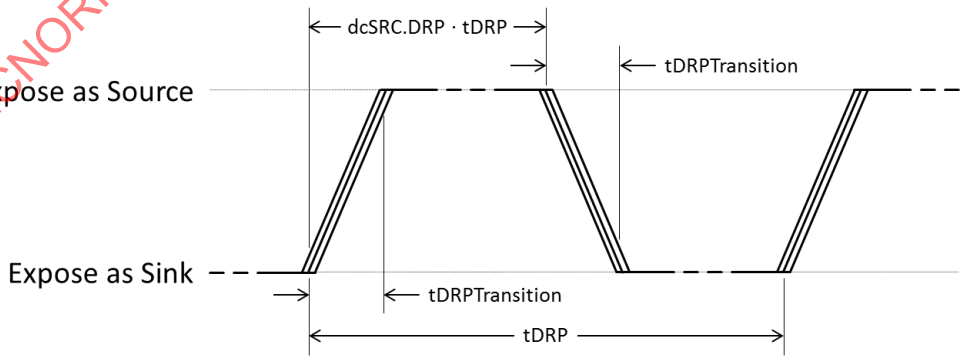
Table 4-32 provides the timing values that ***shall*** be met for delivering power over VBUS and VCONN.

Table 4-32 VBUS and VCONN Timing Parameters

	Minimum	Maximum	Description
tVBUSON	0 ms	275 ms	From entry to ***Attached.SRC*** until VBUS reaches the minimum ***vSafe5V*** threshold as measured at the source's receptacle.
tVBUSOFF	0 ms	650 ms	From the time the Sink is detached until the Source removes VBUS and reaches ***vSafe0V*** (See ***USB PD***).
tVsafe0V	0 ms	650 ms	The time the Source is allowed to use for discharging the Sink capacitors to reach ***vSafe0V*** in ***AttachWait.SRC*** state in order to progress to ***Attached.SRC***.
tVCONNON	Note 1	2 ms	From the time the Source supplied VBUS in the ***Attached.SRC*** state. Measured from ***vSafe5V*** to the minimum VCONN voltage (see Table 4-5)
tVCONNON-PA	0 ms	100 ms	From the time a Sink with accessory support enters the ***PoweredAccessory*** state until the Sink sources minimum VCONN voltage (see Table 4-5)
tVCONNOFF	0 ms	35 ms	From the time that a Sink is detached or as directed until the VCONN supply is disconnected.
tSinkAdj	***tRpValueChange*** (Min)	60 ms	Response time for a Sink to adjust its current consumption to be in the specified range due to a change in ***USB Type-C Current*** advertisement.
Note 1: VCONN ***may*** be applied prior to the application of VBUS.			

Figure 4-46 illustrates the timing parameters associated with the DRP toggling process. The ***tDRP*** parameter represents the overall period for a single cycle during which the port is exposed as both a Source and a Sink. The portion of the period where the DRP is exposed as a Source is established by ***dcSRC.DRP*** and the maximum transition time between the exposed states is dictated by ***tDRPTransition***.

Figure 4-46 DRP Timing



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Table 4-33 provides the timing values that ***shall*** be met for DRPs. The clock used to control DRP swap ***should not*** be derived from a precision timing source such as a crystal, ceramic resonator, etc. to help minimize the probability of two DRP devices indefinitely failing to resolve into a Source-to-Sink relationship. Similarly, the percentage of time that a DRP spends advertising Source ***should not*** be derived from a precision timing source.

Table 4-33 DRP Timing Parameters

	Minimum	Maximum	Description
tDRP	50 ms	100 ms	The period a DRP ***shall*** complete a Source to Sink and back advertisement.
dcSRC.DRP	30%	70%	The percent of time that a DRP ***shall*** advertise Source during ***tDRP***.
tDRPTransition	0 ms	1 ms	The time a DRP ***shall*** complete transitions between Source and Sink roles during role resolution.
tDRPTry	75 ms	150 ms	Wait time associated with the ***Try.SRC*** state.
tDRPTryWait	400 ms	800 ms	Wait time associated with the ***Try.SNK*** state.
tTryTimeout	550 ms	1100 ms	Timeout for transition from ***Try.SRC*** to ***TryWait.SNK***.
tVPDDetach	10 ms	20 ms	Time for a DRP to detect that the connected Charge-Through VCONN -Powered USB Device has been detached, after VBUS has been removed.

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Table 4-34 provides the timing requirement for CC connection behaviors.

Table 4-34 CC Timing Parameters

	Minimum	Maximum	Description
tCCDebounce	100 ms	200 ms	Time a port ***shall*** wait before it can determine it is attached.
tPDDebounce	10 ms	20 ms	Time a Sink port ***shall*** wait before it can determine it is detached due to the potential for ***USB PD*** signaling on CC as described in the state definitions.
tTryCCDebounce	10 ms	20 ms	Time a port ***shall*** wait before it can determine it is re-attached during the try-wait process.
tErrorRecovery	25 ms		Time a self-powered port ***shall*** remain in the ***ErrorRecovery*** state.
	240 ms		Time a source ***shall*** remain in the ***ErrorRecovery*** state if it was sourcing VCONN in the previous state.
tRpValueChange	10 ms	20 ms	Time a Sink port ***shall*** wait before it can determine there has been a change in ***Rp*** where CC is not BMC Idle, or the port is unable to detect BMC Idle.
	0 ms	5 ms	Time a Sink port ***shall*** wait before it can determine that there has been a change in ***Rp*** when ***USB PD*** signaling can be detected by the port and CC line is BMC Idle.
tSRCDisconnect	0 ms	20 ms	Time a Source ***shall*** detect the ***SRC.Open*** state. The Source ***should*** detect the ***SRC.Open*** state as quickly as practical.
tNoToggleConnect	0 ms	5 ms	Time to detect connection when neither Port Partner is toggling.
tOnePortToggleConnect	0 ms	80 ms	Time to detect connection when one Port Partner is toggling (0ms … ***dcSRC.DRP*** max * ***tDRP*** max + 2 * ***tNoToggleConnect***).
tTwoPortToggleConnect	0 ms	510 ms	Time to detect connection when both Port Partners are toggling (0ms … 5 * ***tDRP*** max + 2 * ***tNoToggleConnect***).
tVPDCTDD	30 µs	5 ms	Time for a Charge-Through VCONN -Powered USB Device to detect that the Charge-Through source has disconnected from CC after VBUS has been removed, transition to ***CTUnattached.VPD***, and re-apply its ***Rp*** termination advertising 3.0 A on the host port CC.
tVPDDisable	25 ms		Time for a Charge-Through VCONN -Powered USB Device ***shall*** remain in ***CTDisabled.VPD*** state.

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4.11.3 Voltage Parameters

Table 4-35, Table 4-36 and Table 4-37 provide the CC voltage values that a Source ***shall*** use to detect what is attached based on the ***USB Type-C Current*** advertisement (Default USB, 1.5 A @ 5 V, or 3.0 A @ 5 V) that the Source is offering.

Table 4-35 CC Voltages on Source Side – Default USB

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (*vRa*)	0.00 V	0.15 V	0.20 V
Sink (*vRd*)	0.25 V	1.50 V	1.60 V
No connect (*vOPEN*)	1.65 V		

Table 4-36 CC Voltages on Source Side – 1.5 A @ 5 V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (*vRa*)	0.00 V	0.35 V	0.40 V
Sink (*vRd*)	0.45 V	1.50 V	1.60 V
No connect (*vOPEN*)	1.65 V		

Table 4-37 CC Voltages on Source Side – 3.0 A @ 5 V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (*vRa*)	0.00 V	0.75 V	0.80 V
Sink (*vRd*)	0.85 V	2.45 V	2.60 V
No connect (*vOPEN*)	2.75 V		

Table 4-38 provides the CC voltage values that ***shall*** be detected across a Sink's ***Rd*** for a Sink that does not support higher than default ***USB Type-C Current*** Source advertisements.

Table 4-38 Voltages on Sink CC Pins – Default USB Type-C Current Only

Detection	Minimum Voltage	Maximum Voltage	Threshold
vRa	–0.25 V	0.15 V	0.2 V
vRd-Connect	0.25 V	2.18 V	

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Table 4-39 provides the CC voltage values that ***shall*** be detected across a Sink's ***Rd*** for a Sink that implements detection of higher than default ***USB Type-C Current*** Source advertisements. This table includes consideration for the effect that the IR drop across the cable GND has on the voltage across the Sink's ***Rd***.

Table 4-39 Voltages on Sink CC Pins – Multiple Source Current Advertisements

Detection	Minimum Voltage	Maximum Voltage	Threshold
vRa	−0.25 V	0.15 V	0.2 V
vRd-Connect	0.25 V	2.04 V	
vRd-USB	0.25 V	0.61 V	0.66 V
vRd-1.5	0.70 V	1.16 V	1.23 V
vRd-3.0	1.31 V	2.04 V	

Table 4-40 provides the clamping voltage that any port (Source, Sink or DRP) ***may*** clamp its CC pin to protect from damage. The inclusion of clamping ***shall not*** impact the functionality when the CC pin is functioning as VCONN Source or Sink.

Table 4-40 CC Pin Clamping Voltage

	Minimum Voltage
vCC-Clamp	2.9 V

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5 *USB4* Discovery and Entry

USB4 discovery and operational entry differs significantly from ***USB 2.0*** and ***USB 3.2***. This chapter defines the process of discovering across a USB Type-C connection that both port partners are ***USB4***-capable (or not), having the DFP-side of the link decide regarding to enter ***USB4*** operation (or not), and how operational entry is accomplished.

5.1 Overview of the Discovery and Entry Process

The following provides an overview of the general process for discovery and entry into ***USB4*** operation.

1. USB Type-C CC Connection State Machines resolve Source/Sink and the initial data roles (DFP/UFP).
2. Initial VBUS and VCONN power is supplied.
3. ***USB Power Delivery*** protocol is used to establish a power contract between the port partners.
4. ***USB PD Discover Identity*** process is used by the DFP to identify port partner (SOP) capabilities.
5. ***USB PD Discover Identity*** process is used by the DFP to identify cable (SOP') capabilities.
6. If the cable and port partner both support ***USB4*** operation, the DFP issues ***USB PD Enter_USB*** Messages to both the cable (if it is an active cable) and port partner to enter ***USB4*** operation.
7. If both port partners are Dual-Role-Data (DRD) capable, either the DFP or UFP can ***optionally*** initiate a data-role swap to exchange host and device roles.

The first three steps above are the same as used for all USB connections for establishing port relationships and power between the port partners. Step 5 where the cable is queried for its capabilities ***may optionally*** occur during Step 3, this would most likely be done before if the Source needs to know if the cable supports supplying current beyond 3 A.

Depending on the resulting power source relationship after the first few steps, the use of ***USB PD DR_Swap may*** be necessary to establish the port partner that is closest to the host as the data role DFP. For example, a hub supplying power to a host and ***DR_Swap*** is used to correct the data roles between the hub and host.

After the port partner's capabilities are identified by the DFP, it ***may*** be appropriate based on what is discovered about the port partner to also query the port partner using the ***USB PD Alternate Mode*** SVID discovery process as an extension to Step 4. There are situations where a port partner supports ***Alternate Modes*** that ***may*** also be useable during ***USB4*** operation and this would be discovered during this additional query.

After the cable capabilities are identified by the DFP, it ***may*** be appropriate based on what is discovered about the cable to also query the cable using the ***USB PD Alternate Mode*** SVID discovery process as an extension to Step 5. There are situations where a cable that supports ***Thunderbolt 3 Alternate Mode may*** also be useable for ***USB4*** operation, and this would be discovered during this additional query.

USB4 operation is entered using a ***USB PD Enter_USB*** Message. This message will be sent to both the cable (SOP', and SOP'' if present) and the port partner (SOP), each of which will respond with an ***Accept*** message to confirm and establish when the cable or port partner is functionally ready for ***USB4*** operation. If the cable to be used will be operating in ***Thunderbolt 3 Alternate Mode***, then the cable will be enabled using the ***USB PD*** Enter Mode Command instead of the ***USB PD Enter_USB*** Message (See Appendix F).

USB4 functionally enables an ability for connecting two host platforms and establishing a data channel between the hosts, this is dependent on at least one of these host platforms being capable of Dual-Role-Data operation so that a proper USB Type-C DFP-to-UFP data relationship can be established between them. In most cases, both host platforms will be DRD-capable and once ***USB4*** operation is established, either of these host platforms can choose to initiate a change of its role in the DFP-to-UFP relationship. To accomplish this, the ***USB PD DR_Swap*** process is used during Step 7 listed above.

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5.2 *USB4* Functional Requirements

The following functional requirements are for ***USB4*** hosts and devices.

5.2.1 *USB4* Host Functional Requirements

USB4 hosts ***shall*** meet the following functional requirements:

- ***USB4*** hosts with dual-role-data (DRD) support ***shall*** respond to ***USB PD Discover Identity*** command with both DFP and UFP VDOs.

5.2.2 USB Device Functional Requirements

USB4 devices ***shall*** meet the following functional requirements:

- ***USB4*** devices ***shall*** respond to ***USB PD Discover Identity*** command with UFP VDOs.
- The ***USB4*** device ***shall*** provide a USB interface exposing a ***USB Billboard Device Class*** when it cannot connect as a ***USB4*** device and doesn't support and expose equivalent functionality over an ***Alternate Mode***, ***USB 3.2*** and/or ***USB 2.0*** within ***tUSB4Timeout***.
- If the ***USB4*** device supports ***Alternate Modes***, the device ***shall*** complete the ***USB4*** discovery and entry process (successful or not) before falling back to ***USB 3.2*** or ***USB 2.0*** and, when required, exposing an appropriate ***USB Billboard Device Class***.

5.2.3 *USB4* Alternate Mode Support

The ***USB4*** specification enables products to be designed to support ***Alternate Modes***, specifically ***DisplayPort Alt Mode*** and ***Thunderbolt 3 Alt Mode***. Unlike ***USB 3.2*** and ***USB 2.0*** hubs, this also includes supporting specific ***Alternate Modes*** on ***USB4*** hubs.

5.2.3.1 *USB4* Alternate Mode Support on Hosts

For ***USB4*** hosts that implement ***DisplayPort*** Tunneling, ***DP Alt Mode*** with Multi-function support (DP_BR 1 channel signaling combined with ***USB 3.2*** support) as defined by the ***DP Alt Mode*** specification ***shall*** be implemented on all its USB Type-C DFPs.

The ***USB4*** host ***shall*** support the first connected ***DisplayPort*** display on any of its USB Type-C ports. Support for subsequently connected ***DisplayPort*** displays is ***optional***.

USB4 hosts ***may optionally*** implement ***TBT3*** compatibility support as defined by the ***USB4*** specification on its USB Type-C DFPs.

5.2.3.2 *USB4* Alternate Mode Support on Hubs and *USB4*-based Docks

USB4 hubs and ***USB4***–based docks ***shall*** implement ***DP Alt Mode*** with Multi-function support (DP_BR 1 channel signaling combined with ***USB 3.2*** support) as defined by the ***DP Alt Mode*** specification on all exposed USB Type-C DFPs.

USB4 hubs ***shall*** support the first connected ***DisplayPort*** display on any of its USB Type-C DFPs. Support for subsequently connected ***DisplayPort*** displays is ***optional***.

USB4-based docks ***shall*** support the first connected display on any of its USB Type-C DFPs or non-USB display connectors (if present, collectively). Support for subsequent connected displays is ***optional***.

USB4 hubs ***shall*** implement ***TBT3*** compatibility support as defined by the ***USB4*** specification on its USB Type-C DFPs. ***USB4***–based docks ***shall*** implement ***TBT3*** compatibility support as defined by the ***USB4*** specification on its USB Type-C UFP and USB Type-C DFPs.

For ***USB4*** hubs, downstream-facing ports ***shall not*** implement ***Alternate Modes*** that do not have a ***USB-IF*** Standard ID (SID) or Accessory Modes.

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5.3 *USB4* Power Requirements

USB4 requires that the power connection between the port partners be established and maintained using ***USB PD*** prior to and through-out ***USB4*** operation. A ***USB4*** port, prior to entering ***USB4*** operation, ***shall*** operate as a ***USB 3.2*** port with regarding power (See Section 4.6). ***USB4*** does not use the USB device protocols defined in ***USB 2.0*** and ***USB 3.2*** for managing device power.

5.3.1 Source Power Requirements

For USB Type-C ports that support ***USB4*** data bus operation, the following requirements ***shall*** be met.

- ***USB4*** ports ***shall*** be minimally capable of supplying at least 7.5 W (i.e., 5 V @ 1.5 A) on VBUS to bus-powered ***USB4*** devices.
- The minimum capability for powering bus powered devices on data-capable ports ***shall*** be independently met on each USB Type-C port of a multi-port host or hub.

5.3.2 Sink Power Requirements

For ***USB4*** devices that rely on bus power to operate (independent of any charging needs), the following requirements ***shall*** be met.

- ***USB4*** devices ***shall*** draw only up to 250 mA on VBUS when the Source advertises Default USB power (see Section 4.11.1) prior to a ***USB PD*** power contract being made between the device and its port partner.
    - ***USB4*** devices ***may*** draw higher levels of power prior to a ***USB PD*** power contract being made if the Source advertises ***USB Type-C Current*** at either 1.5 A or 3.0 A.
- ***USB4*** devices ***shall*** be minimally capable of operating with a Source that only delivers up to 7.5 W (i.e., 5 V @ 1.5 A).
- ***USB4*** devices ***shall not*** enter ***USB4*** data bus operation until after a ***USB PD*** power contract has been established, and while in ***USB4*** operation, the device ***shall*** adhere to ***USB PD*** power behavioral requirements at all times including appropriately responding to changes in Source capabilities.

In cases where the full functional capabilities or the highest performance of the ***USB4*** device requires more than the power being offered by the host, the device ***shall*** be minimally capable of providing the user with basic functionality as expected for the type and listed functions of the device. This allows for making available a higher level of operation or performance when a higher level of power is supplied, e.g., 15 W for full functionality versus 7.5 W for basic functionality. In this case, the device ***shall*** expose a ***USB Billboard Device Class*** if the device is unable to provide equivalent functionality limited by the available power.

5.3.3 Device Power Management Requirements

For ***USB4***, device power management is enabled using a combination of ***USB PD*** capabilities that operate in conjunction with the ***USB4*** link states of the device's UFP connection.

The connection between the device's UFP and its DFP port partner can be put into a suspend state based on the value of the USB Suspend Supported Flag in the Source-Capabilities Message used in the ***USB PD*** explicit power contract.

When the USB Suspend Supported Flag is set by the Source, the Sink ***shall*** meet the Suspend power requirement when the ***USB4*** link is in the CLd state. Prior to the entry of the link into CLd state, it is expected that the host will have placed all of the device's functions into an appropriate suspend state.

Suspend power is defined based on the capabilities of the ***USB4*** device:

- ***USB4*** Device that is not capable of remote wake or has remote wake disabled: 25 mW.
- ***USB4*** Device that supports remote wake and has remote wake enabled: 50 mW.

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If the Source clears the USB Suspend Supported Flag, the Sink ***shall*** follow Explicit Contract power requirements regardless of the ***USB4*** link state. For ***USB4***, the use of ***USB PD*** zero negotiated current is not a valid Suspend entry method since it is not coordinated with the host operating system and the function device drivers.

5.4 *USB4* Discovery and Entry Flow Requirements

This section provides the detailed requirements for ***USB4*** discovery and entry. Additional requirements related to ***USB4*** operation are in the ***USB4*** specification.

Prior to entering and during ***USB4*** operation, the functional requirements of Chapter 4 ***shall*** be met including all functional interface and configuration channel (CC) requirements.

5.4.1 USB Type-C Initial Connection

For a ***USB4***-capable port, prior to initiating ***USB4*** cable and device discovery, a valid Source-to-Sink connection ***shall*** exist and the USB Type-C connection state machine of the port ***shall*** either be in the ***Attached.SRC*** or ***Attached.SNK*** state.

When two ***USB4*** dual-role-data (DRD) ports are connected together, e.g., two ***USB4*** hosts, USB Type-C connection process will establish the initial data roles between the port partners.

Once the initial data roles are established, the ***USB4*** DFP ***may*** immediately proceed to train the link for ***USB 3.2***. If a UFP is ***USB4*** capable, it ***shall*** hold off exposing ***USB 2.0*** speed identification (Section 7.1.5. of the ***USB 2.0*** specification) and ***USB 3.2*** receiver terminations until receipt of an ***USB PD Enter_USB*** message, completing entry (including any pin reassignment) into an ***Alternate Mode***, or the ***tUSB4Timeout*** has expired.

5.4.2 USB Power Delivery Contract

Prior to initiating ***USB4*** device discovery, the port partners ***shall*** negotiate a ***USB PD*** Explicit Contract.

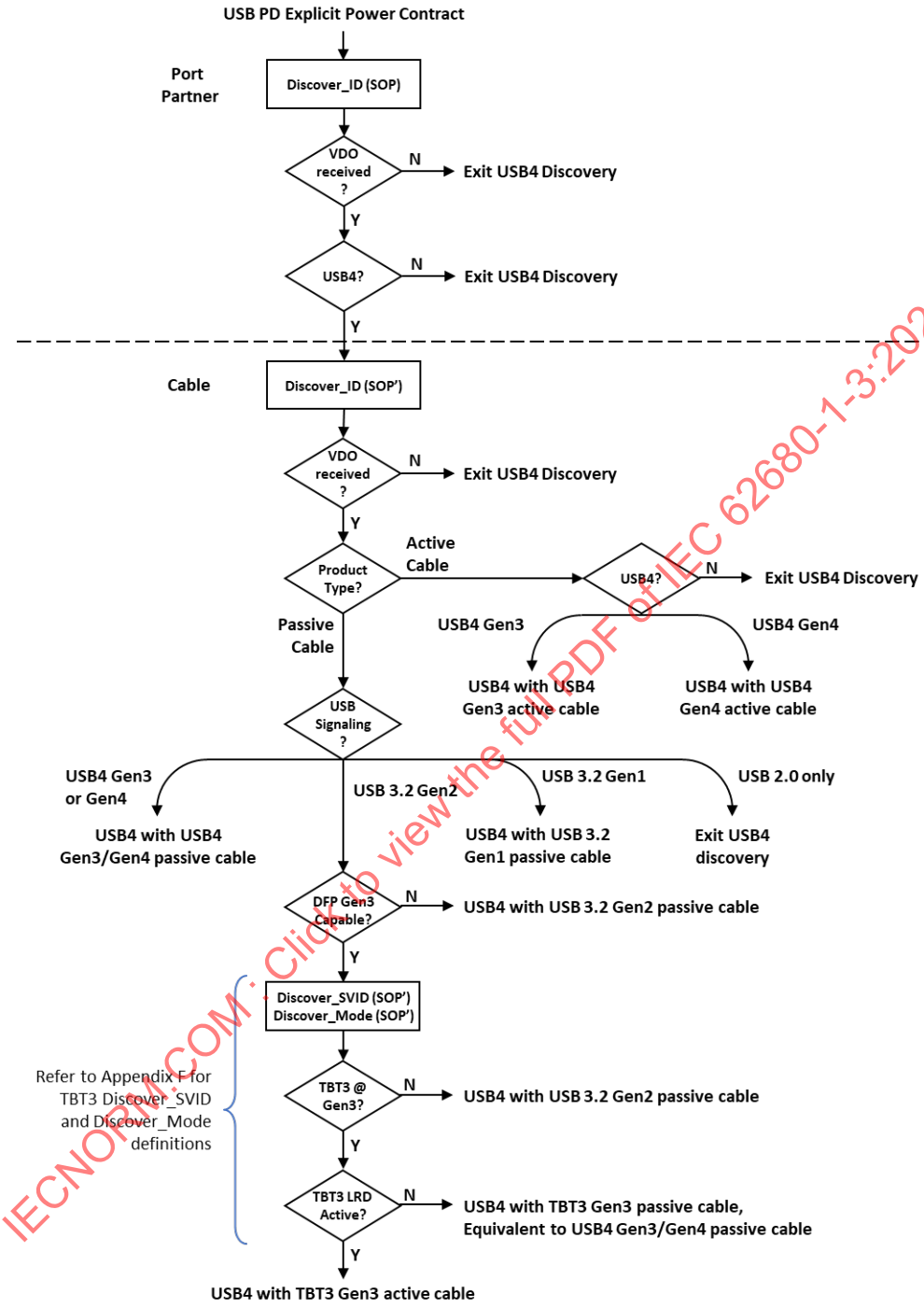
During the process of establishing a stable ***USB PD*** Explicit Contract, the Source or Sink ***may*** have initiated power-role and VCONN swaps. Prior to moving on to ***USB4*** discovery, the functional data role ***shall*** be properly established (e.g., a self-powered hub upstream facing port is a DRP and comes up as a Source where ***DR_Swap*** is then required to the correct data role to the hub) and the DFP ***shall*** be the source of VCONN.

5.4.3 *USB4* Discovery and Entry Flow

Figure 5-1 illustrates the basic flow model for ***USB4*** discovery and entry.

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Figure 5-1 *USB4* Discovery and Entry Flow Model



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5.4.3.1 *USB4* Port Partner Discovery (SOP)

USB4 port partner discovery ***shall*** occur only after having a negotiated ***USB PD*** Explicit Contract.

USB4 port partner discovery involves the use of the ***USB PD*** Discover ID process between the DFP and its port partner (SOP).

The ***USB4*** port partner to be discovered can be any data-capable product presenting itself as the UFP port partner during the discovery process. Depending on the type and capabilities of the port partner, either or both UFP and DFP VDOs ***may*** be returned in response to the DFP's ***USB PD*** Discover_ID(SOP) command. As long as at least one of those VDOs are received, then the DFP ***should*** proceed to assess its port partner's ability to support ***USB4*** operation based on the content of the VDOs received. For a received UFP VDO, this is based on the Device Capability Field (B27…24) and for a received DFP VDO, this is based on the Host Capability Field (B26…24).

Refer to Appendix I for more information and guidance on the use of UFP and DFP Product Types and VDOs.

5.4.3.2 *USB4* Cable Discovery (SOP')

The DFP ***shall*** determine that the attached cable is ***USB4***-compatible prior to entering into ***USB4*** operation. In cases where the ***USB4*** device is directly connected or has a captive cable, the ***USB4*** device ***shall*** respond to ***USB4*** cable discovery on SOP' as a captive passive cable and indicating the appropriate USB Signaling support.

Table 5-1 summarizes the list of cables that are intended to support ***USB4***-compatible operation. Regarding Active Cables, this list does not include Optically-Isolated Active Cables (OIACs) which are to be handled as a special case given that these cables do not support ***USB 2.0*** and power delivery over the cable (See Chapter 6).

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Table 5-1 Certified Cables Where *USB4*-compatible Operation is Expected

	Cable Signaling	*USB4* Operation	Notes
USB Type-C Full-Featured Cables (Passive)	***USB 3.2*** Gen 1	20 Gbps	This cable will indicate support for ***USB 3.2*** Gen1 (001b) in the USB Signaling field of its Passive Cable VDO response. Note: even though this cable isn't explicitly tested, certified or logo'ed for ***USB 3.2*** Gen2 operation, ***USB4*** Gen2 operation will generally work.
	USB 3.2 Gen 2 (***USB4*** Gen2)	20 Gbps	This cable will indicate support for ***USB 3.2*** Gen2 (010b) in the USB Signaling field of its Passive Cable VDO response.
	USB4 Gen4 (***USB4*** Gen3)	80 Gbps	This cable will indicate support for ***USB4*** Gen3 (011b) or ***USB4*** Gen4 (100b) in the USB Signaling field of its Passive Cable VDO response.
Thunderbolt™ 3 Cables (Passive)	***TBT3*** Gen2 (***USB 3.2*** Gen 1 or ***USB4*** Gen2)	20 Gbps	This cable will indicate support for ***USB 3.2*** Gen1 (001b) or ***USB 3.2*** Gen2 (010b) in the USB Signaling field of its Passive Cable VDO response.
	TBT3 Gen3 (***USB4*** Gen4)	80 Gbps	In addition to indicating support for ***USB 3.2*** Gen2 (010b) in the USB Signaling field of its Passive Cable VDO response, this cable will indicate that it supports ***TBT3*** Gen3 in the Cable Speed parameter and Passive Cable in the Active_Passive parameter of the Discover Mode VDO response.[2]
Thunderbolt™ 3 Cables (Active Linear Re-driver)	***TBT3*** Gen3 (***USB4*** Gen3)	40 Gbps	In addition to indicating support for ***USB 3.2*** Gen2 (010b) in the USB Signaling field of its Passive Cable VDO response, this cable will indicate that it supports ***TBT3*** Gen3 in the Cable Speed parameter and Active Cable in the Active_Passive parameter of the Discover Mode VDO response.[2]
USB Type-C Full-Featured Cables (Active)[1]	***USB4*** Gen2	20 Gbps	This cable will indicate support for ***USB4*** Gen2 (010b) in the USB Signaling field of its Active Cable VDO response.
	USB4 Gen3	40 Gbps	This cable will indicate support for ***USB4*** Gen3 (011b) in the USB Signaling field of its Active Cable VDO response.
	USB4 Gen4	80 Gbps	This cable will indicate support for ***USB4*** Gen4 (100b) in the USB Signaling field of its Active Cable VDO response.

Note 1: SuperSpeed USB active cables do not support ***USB4***-compatible operation.
Note 2: See Appendix F.2.6 and Table F-11.

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Determining if the cable is ***USB4***-compatible starts the use of the ***USB PD*** Discover ID process between the DFP and the attached cable (SOP'). If no response is received when the DFP issues a ***USB PD*** Discover ID command to the cable, then the ***USB4*** discovery process ***shall*** be exited and the DFP ***shall*** proceed to establish a functional connection to its UFP port partner following traditional ***USB 2.0*** process.

USB4-compatible support is generally determined based on the USB Signaling Support indicated in the cable VDO responses appropriate for the type of cable it is, passive or active, with compatible passive cables being those that indicate USB signaling support for Gen1 or higher and with compatible active cables being those that indicate USB signaling support for Gen2 or higher.

When a passive cable is identified as a ***USB 3.2*** Gen2 cable and the DFP is Gen3 capable, the DFP needs to check further using ***USB PD Alternate Mode*** process to determine if the cable is a ***Thunderbolt 3*** passive cable supporting Gen3.

Some existing ***Thunderbolt 3*** active cables ***may not*** support ***USB4*** operation, discovery and use of this cable is ***optional***. Please refer to Appendix F regarding how to discover and support these cables.

5.4.3.2.1 Discovering Passive Cables

The ***USB PD*** specification defines the Passive Cable VDO responses to the ***Discover Identity*** Command sent by the DFP to a ***USB4***-compatible passive cable.

If the USB Signaling field [B2…0] in the Passive Cable VDO response is 011b (***USB4*** Gen3) or 100b (***USB4*** Gen4), the ***USB4*** discovery process is complete and ***USB4*** operation up to as high as 80 Gbps is supported. In Chapter 3 of this specification, these cable assemblies are those with the following cable references: CC4G3-3, CC4G3-5 and CC4G3-5E indicated in Table 3-1.

If the USB Signaling field [B2…0] in the Passive Cable VDO response is 000b (***USB 2.0*** only), the ***USB4*** discovery process will be exited and the DFP ***shall*** proceed to establish a functional connection to its UFP port partner following traditional ***USB 2.0*** process.

If the USB Signaling field [B2…0] in the Passive Cable VDO response is either 010b (***USB 3.2*** Gen2) or 001b (***USB 3.2*** Gen1), the ***USB4*** discovery process is complete if the DFP is limited to ***USB4*** Gen2. In Chapter 3 of this specification, these cable assemblies are those with the following cable references: CC3G2-3, CC3G2-5, CC3G1-3, and CC3G1-3 indicated in Table 3-1. Note that ***USB 3.2*** Gen1 cables, while not tested and certified to be used for ***USB 3.2*** Gen2 operation, are expected to work for ***USB4*** Gen2 operation.

If the USB Signaling field [B2…0] in the Passive Cable VDO response is 010b (***USB 3.2*** Gen2) but the DFP is capable of ***USB4*** Gen3 operation, then the DFP ***shall*** use the ***USB PD Alternate Mode*** process to determine if the cable also can be identified as a ***TBT3*** Gen3 cable. Refer to Section 5.4.3.2.3 for ***TBT3*** cable discovery process. If the Cable Speed field of the Discover Modes VDO response is set to 011b, then the ***USB4*** discovery process is complete and ***USB4*** operation up to as high as Gen3 is supported using the ***TBT3*** passive cable (see Table F-11).

5.4.3.2.2 Discovering Active Cables

The ***USB PD*** specification defines the Active Cable VDO responses to the ***Discover Identity*** Command sent by the DFP to a ***USB4***-compatible active cable.

If the USB Signaling Support field [B2…0] in the Active Cable VDO 1 response is 011b (***USB4*** Gen3), the ***USB4*** discovery process is complete and ***USB4*** operation up to as high as Gen3 is supported. If the USB Signaling Support field [B2…0] in the Active Cable VDO 1 response is 100b (***USB4*** Gen4), the ***USB4*** discovery process is complete and ***USB4*** operation up to as high as Gen4 is supported.

Optionally, discovery and use of existing ***TBT3*** active cables that indicate support for rounded data rate operation is allowed if the active cable isn't explicitly identified as ***USB4***-compatible.

Failure to identify that the attached active cable is ***USB4***-compatible will result in exiting the ***USB4*** discovery process and reverting to following traditional ***USB 3.2*** and ***USB 2.0*** process.

5.4.3.2.3 Process for Discovering Thunderbolt 3 Cables

The ***USB PD*** specification defines the process for discovering ***Alternate Mode***-enabled cables. The following summarizes this process specific to discovering ***Thunderbolt 3*** cables for purposes of determining ***USB4***-compatibility. Prior to performing these steps, the ***USB PD Discover Identity*** process will have already been used to establish if the cable is passive or active.

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The following steps are used for discovering ***Thunderbolt 3*** cables and the cable's capabilities using the ***USB PD Alternate Mode*** process.

1. DFP issues the Discover SVIDs command to the cable SOP'.
2. If the cable's Discover SVID response indicates 0x8087 (Intel/***TBT3***) as one of its SVIDs, then proceed to next step, otherwise the cable is not a ***Thunderbolt 3*** cable (see Section F.2.4).
3. DFP issues the Discover Modes command with its SVID set to 0x8087 to the cable's SOP'.
4. If this discovery is part of the ***USB4***-compatible passive cable discovery process, from the cable's Discover Modes VDO responses (see Section F.2.6), extract the value in the Cable Speed field to complete the process. Additionally, if this cable is a ***TBT3*** LRD cable as indicated by the cable's Discover Modes VDO response (Bit 22 = 0 and Bit 25 = 1), then the DFP ***may optionally*** send a ***USB PD Enter_USB*** Message or ***USB PD*** Enter Mode Command to the cable.
5. If this discovery is part of the ***USB4***-compatible active cable discovery process, from the cable's Discover Modes VDO responses (see Section F.2.6), extract the value in the TBT_Rounded_Support field to complete the process. [Note: discovery and use of ***USB4***-compatible ***TBT3*** active cables is an ***optional*** feature that also would require use of ***USB PD*** Enter Mode command to enable the cable for ***USB4*** operation.].

5.4.3.3 *USB4* Operational Entry

USB4 operational entry ***shall*** occur only after having established that the attached cable, if present, and the port partner are ***USB4***-capable.

USB4 operational entry involves the use of the ***USB PD Enter_USB*** Message process between the DFP and both the attached ***USB4***-compatible cable and the ***USB4***-capable port partner – sending this message is order specific: SOP' first, SOP" second if present, and SOP third. Sending the ***USB PD Enter_USB*** Message to SOP' and SOP" is not needed for passive cables.

When using the ***USB PD Enter_USB*** Message for enabling ***USB4*** operation, the DFP ***shall*** indicate 010b (***USB4***) in the USB Mode field of the ***USB PD Enter_USB*** Data Object. The remaining fields ***shall*** be set appropriately by the DFP based on the capabilities of the DFP and attached cable.

5.4.4 *USB4* Post-Entry Operation

5.4.4.1 During *USB4* Operation

While in ***USB4*** operation, the following are allowed:

- The ***USB PD*** explicit power contract ***may*** be re-negotiated.
- Issue a ***USB PD*** Data_Reset command to change the mode of operation, e.g., from ***USB4*** to ***USB 3.2*** or an ***Alternate Mode***.
- Enable ***Alternate Modes*** that do not reconfigure the port interface and operate in parallel with ***USB4***.

5.4.4.2 Exiting *USB4* Operation

The ***USB PD*** Data_Reset process causes USB data connections to be reset and ***Alternate Modes*** to be exited. This process does not change the existing power contract and data roles between the port partners. The Data_Reset process ***shall*** include the following steps:

- Issue a ***USB PD*** Data_Reset command to the SOP port partner to reset the data bus, reset the cable, and exit any ***Alternate Modes*** while preserving the power on VBUS.
- The ***tUSB4Timeout*** and ***tAMETimeout*** timers within the UFP ***shall*** be reset upon sending or receiving a ***USB PD*** Data_Reset command.
- Re-enter the ***USB4*** Discovery and Entry process (Section 5.4.3).

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5.5 *USB4* Hub Connection Requirements

USB4 hub behavior in managing its DFP connections has ***USB4***-specific dependencies on the connection status and capabilities of its single UFP. Additionally, hubs have ***USB4***-specific responsibilities for communicating the capabilities of the ***USB4*** host to downstream-connected ***USB4*** hubs. This section provides both requirements and guidance for ***USB4*** hub port connection behavior.

5.5.1 *USB4* Hub Port Initial Connection Requirements

The following requirements apply to all hub ports.

1. Run the USB Type-C Connection process,
2. Establish an initial ***USB PD*** explicit contract,
3. If desired, use ***USB PD PR_Swap*** to establish the preferred power role, and
4. Use ***USB PD DR_Swap*** to establish data role to be consistent with the port's position in the USB tree if needed.

5.5.2 *USB4* Hub UFP and Host Capabilities Discovery

The ***USB4*** hub DFPs capabilities are ultimately based on the capabilities seen at its UFP (once it has established a connection to the host). If the ***USB4*** hub's UFP is connected to an upstream ***USB4*** hub, then the capabilities over the connection between the two hubs ***may not*** initially represent the capabilities all the way back to the host.

The following summarizes the general principles regarding how UFP and host capabilities impact DFP connections.

- The downstream connection to a device or hub that is attached to the ***USB4*** hub's DFP is based on the capabilities of the hub.
- Once the ***USB4*** hub's UFP has established a connection, the hub's capabilities are limited to the capabilities of that UFP connection.
- When the ***USB4*** hub's UFP connection indicates that a host is not present, once the hub is notified that a host becomes present, the hub will limit its capabilities as needed to match those of the host.
    - Any connections on the ***USB4*** hub's DFPs that existed prior to the host being present are adjusted to align with changes in capabilities if needed.
- Once a host becomes present in a ***USB4*** tree, all intermediary hubs will update their connections to align with the host capabilities as the host present status is propagated to the downstream connected ***USB4*** hubs.

The capabilities seen by the hub's UFP are based on one of the following:

- A ***USB PD Enter_USB*** message is received which indicates the USB operation (***USB4***, ***USB 3.2*** or ***USB 2.0***) and associated characteristics supported (***USB4*** PCIe-supported, ***USB4 DP*** supported, etc.) by the upstream port partner.
- A ***USB PD*** Enter Mode command is received to start a supported ***Alternate Mode*** (***Thunderbolt 3***, ***DisplayPort***).
- No ***USB PD Enter_USB*** message is received within the ***tUSB4Timeout***, or ***USB PD*** Enter Mode message is received within the ***tAMETimeout*** indicating only ***USB 3.2*** and ***USB 2.0*** are available.

If the ***USB4*** hub's UFP is connected to an upstream ***USB4*** hub, then the capabilities reported in the received ***USB PD Enter_USB*** message ***shall*** only be considered the host's capabilities if the Host Present bit is set. If the Host Present bit is reset, then the hub ***shall*** wait for a subsequent ***USB PD Enter_USB*** message to be received with the Host Present bit set. Once the Host Present bit is set, the capabilities as represented in the

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USB PD USB PD Enter_USB message can be used as the host's capabilities for the purpose of establishing final DFP connections.

If the ***USB4*** hub's UFP receives an ***USB PD Enter_USB*** message which indicates the USB operation as either ***USB 3.2*** or ***USB 2.0***, the ***USB4*** hub ***shall not*** wait for the completion of the ***tUSB4Timeout*** before proceeding to establish its UFP and DFP connections following ***USB 3.2*** or ***USB 2.0*** hub requirements, respectively.

5.5.3 Hub DFP Connection Requirements

5.5.3.1 Speculative Connections

When a device is attached to the DFP of a ***USB4*** hub prior to the hub's UFP being connected and the host capabilities are known, the hub will speculatively connect to the attached device based on the following requirements.

- Use ***USB PD*** Discover ID and the ***USB PD Alternate Mode*** process to determine the full capabilities of the attached cable and device.
- Based on the discovered capabilities, establish the most capable connection based on the capabilities of the ***USB4*** hub's DFP in the following priority order:
    1. ***USB4***
    2. ***Thunderbolt 3 Alt Mode***
    3. ***DP Alt Mode***
    4. ***USB 3.2***
    5. ***USB 2.0***
- Inhibit port status notifications and data paths upstream from the ***USB4*** hub's DFPs while waiting for the ***USB4*** hub's UFP connection to be established.

5.5.3.2 Operational Connections

Once the ***USB4*** hub's UFP connection is established and the host capabilities are determined (see Section 5.5.2), the hub ***shall*** evaluate each existing DFP connection based on the capabilities associated with the hub's UFP connection and perform one of the following actions.

- If the DFP connection properly aligns with the capabilities of the UFP connection, enable the status notifications and data path for that port.
- If the DFP connection does not properly align with the capabilities of the UFP connection, the DFP connection ***shall*** do one of the following:
    - If the UFP remains in ***USB4*** and the DFP connection is with a downstream ***USB4*** hub, send a revised ***USB PD Enter_USB*** message with the Host Present bit set.
    - If the UFP changed to ***USB 3.2*** or ***USB 2.0*** and the DFP connection is with a downstream ***USB4*** hub, the DFP ***shall*** be reset the connection using ***USB PD*** Data_Reset followed by sending a revised ***USB PD Enter_USB*** message indicating ***USB 3.2*** or ***USB 2.0*** and the Host Present bit set.
    - Otherwise, the DFP ***shall*** enter the ***ErrorRecovery*** state to reset the connection and establish a new connection that aligns with the hub's UFP capabilities.

5.5.4 Hub Ports Connection Behavior Flow Examples

This section illustrates several example connection flows that assume that the hub's DFP connection is established prior to the hub's UFP connection. In these cases, the host capabilities are unknown at the time that the hub's DFP is connecting with the attached device. Given this, the initial connection established by the hub's DFP is speculatively based only on the hub and device's capabilities and ***may*** have to be revised once the host capabilities are known if there is a functional mismatch. When the hub's UFP connection is fully

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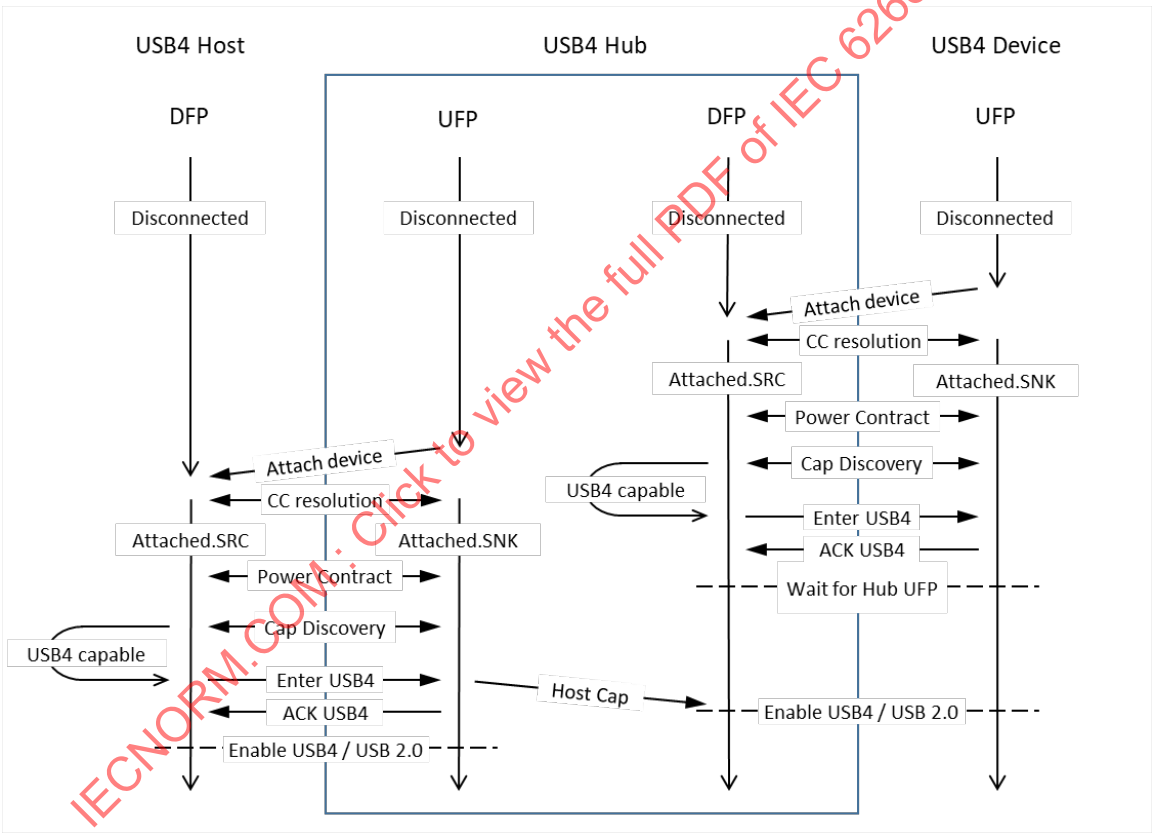
established prior to devices appearing on the hub's DFP, the connection can be established with full knowledge of the host's capabilities – flows associated with this relationship are not illustrated.

For the example flows in this section, the Source/Sink power roles remain as initially resolved by the CC connection state machine with no ***PR_Swap*** or ***DR_Swap*** activity.

All these example flows intend to minimize the total connection time for enabling the functionality of the device connected to the hub's DFP. This is accomplished by establishing the highest functional connection based on mutual capabilities between the hub and the device even as the hub's UFP capabilities are unknown or not ready for operation. If the speculatively established connection turns out to be valid once the hub's UFP capabilities are established, then the DFP's connection will be enabled as is. If the speculatively established connection turns out to be invalid, the DFP connection will be reset and a connection that aligns with the hub's UFP capabilities ***shall*** be established.

Figure 5-2 Illustrates a connection flow aligned across the combination of a ***USB4*** host, hub, and device. The expected result is the successful enabling of end-to-end ***USB4*** operation.

Figure 5-2 *USB4* Hub with *USB4* Host and Device Connection Flow Alignment



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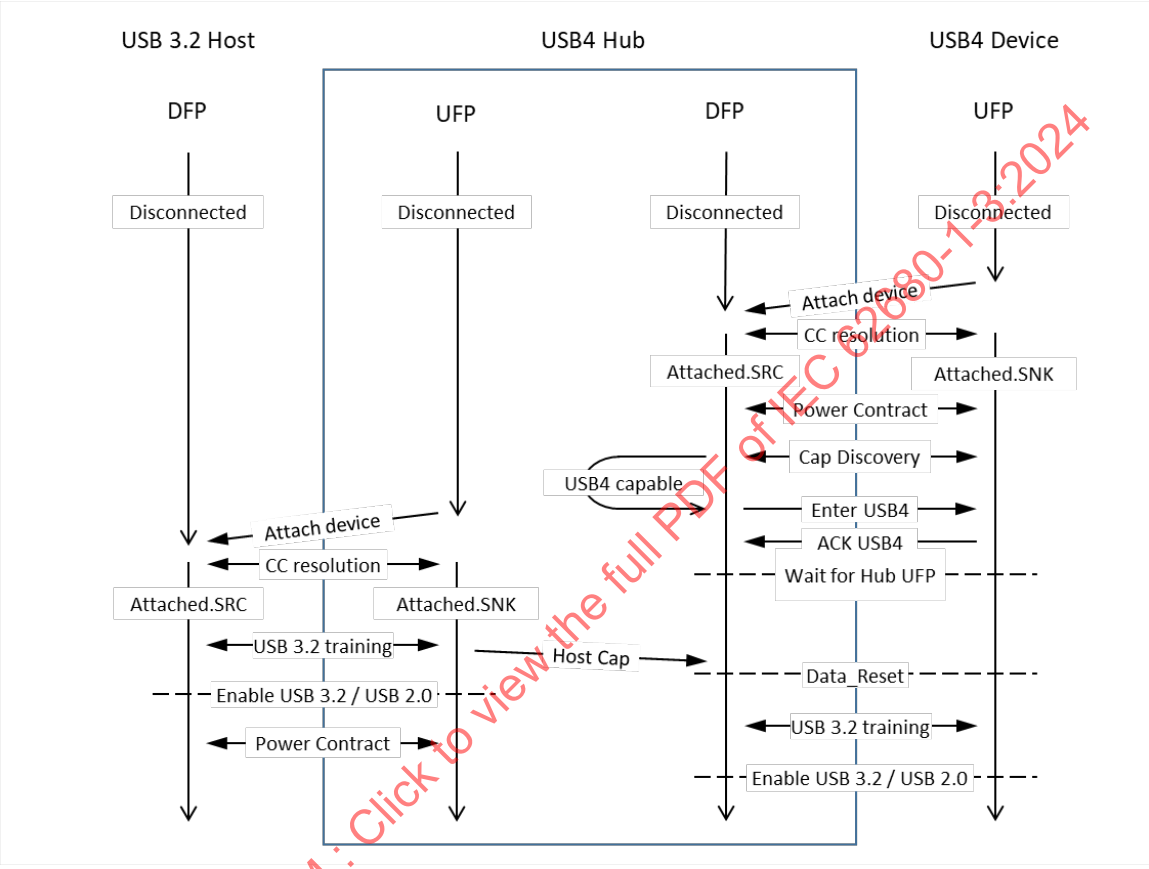
In the illustrated flow, Cap Discovery includes all ***USB PD*** message exchanges needed between the DFP and its UFP port partner to discover the UFP's USB capabilities along with ***TBT3***-compatibility and ***DP Alt Mode*** capabilities. For the ***USB4*** hub's DFP, Cap Discovery is done on a speculative basis whenever it does not already know of the capabilities of the host that will eventually be connected via the hub's UFP.

Upon completion of Cap Discovery between the hub's DFP and its UFP port partner, the hub DFP will establish the highest functional connection and then wait for the hub UFP to complete its connection. Once the hub's UFP connection is established, the host capabilities available are used to determine what ***should*** be done to complete the hub DFP connection to the UFP port partner.

Host Cap is based on the resulting configuration (e.g., data bus protocol and speed) of the ***USB4*** Hub's UFP and the Host capabilities information received in the ***USB PD Enter_USB*** Message from its DFP port partner (see Section 5.5.2). The ***USB4*** hub uses Host Cap to set the available capabilities of the hub's DFPs.

Figure 5-3 illustrates a connection flow aligned across the combination of a ***USB 3.2*** host, a ***USB4*** hub and a ***USB4*** device.

Figure 5-3 *USB4* Hub with *USB 3.2* Host and *USB4* Device Connection Flow Alignment

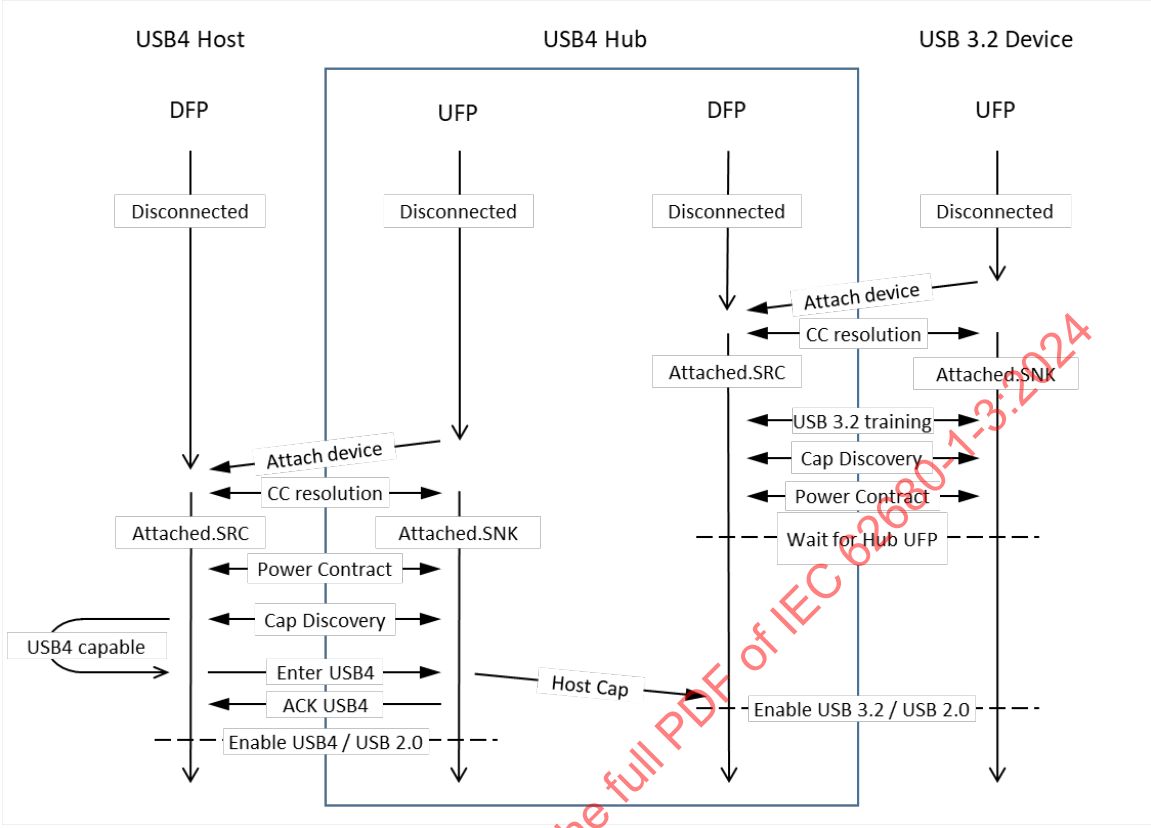


In the flow above, once connected to a ***USB 3.2*** host, the Host Cap reflects that the hub can only support ***USB 3.2*** on its DFPs and the speculatively established ***USB4*** connection on the DFP is exited with the ***USB4*** hub now operating as a traditional ***USB 3.2*** hub.

Figure 5-4 illustrates a connection flow aligned across the combination of a ***USB4*** hub with a ***USB4*** host and ***USB 3.2*** device.

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Figure 5-4 *USB4* Hub with *USB4* Host and *USB 3.2* Device Connection Flow Alignment



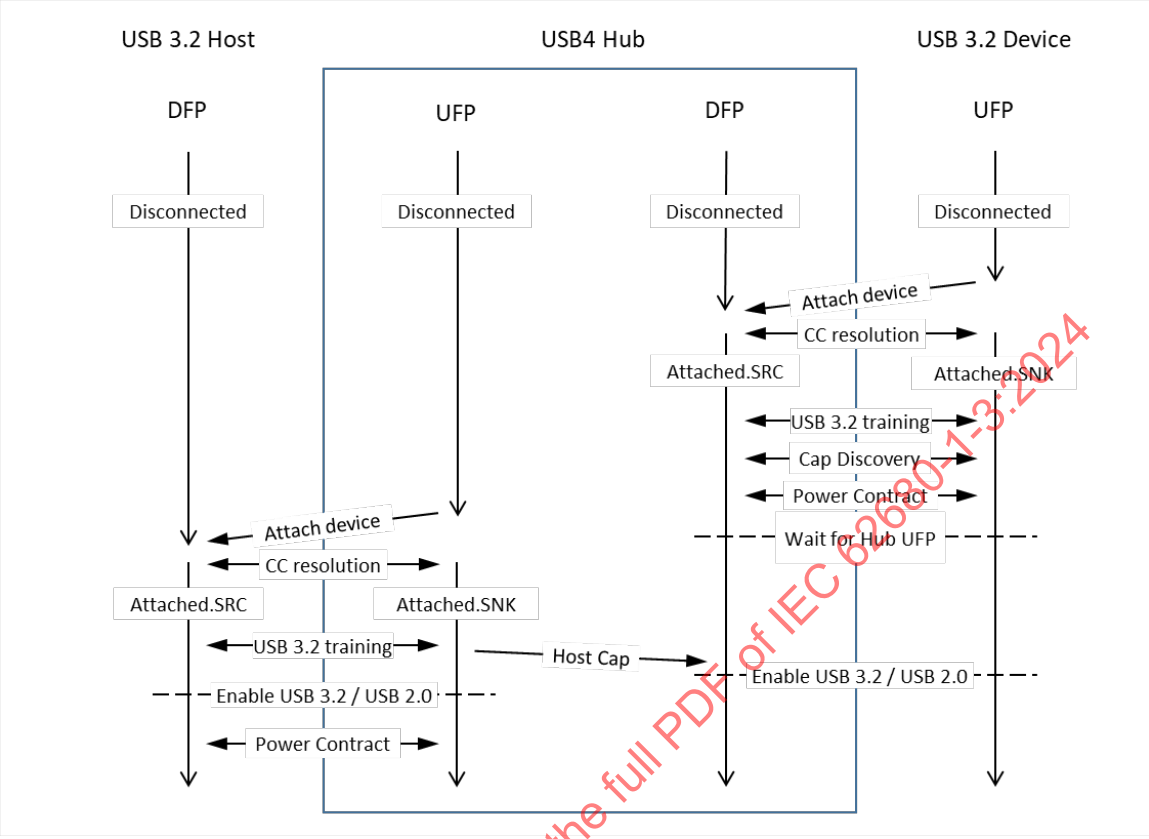
While ***USB 3.2*** devices won't necessarily respond to the Discover ID (SOP), the ***USB4*** hub's DFP will attempt to discover the capabilities of the attached device.

In the flow above, after the ***USB4*** connection of the hub's UFP is established, the DFP connection remains valid with the ***USB 3.2*** data path of the DFP being serviced by the ***USB4*** Enhanced SuperSpeed tunnel.

Figure 5-5 illustrates a connection flow aligned across the combination of a ***USB4*** hub with a ***USB 3.2*** host and device.

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Figure 5-5 *USB4* Hub with *USB 3.2* Host and Device Connection Flow Alignment



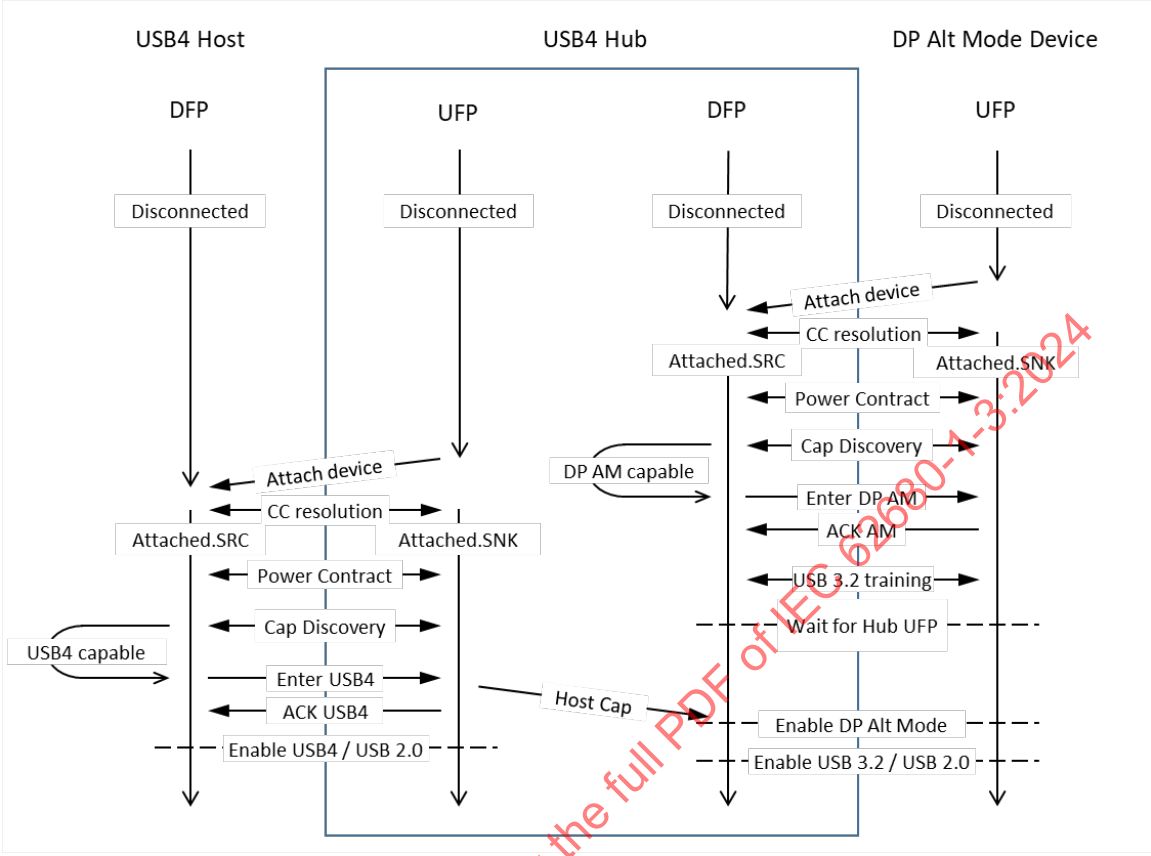
While ***USB 3.2*** devices won't necessarily respond to the Discover ID (SOP), the ***USB4*** hub's DFP will attempt to discover the capabilities of the attached device.

In the flow above, after the ***USB 3.2*** connection of the hub's UFP is established, the DFP connection remains valid with the ***USB4*** hub now operating as a traditional ***USB 3.2*** hub.

Figure 5-6 illustrates a connection flow aligned across the combination of a ***USB4*** host, ***USB4*** hub and a ***DP Alt Mode*** device (operating in Multi-function mode). In this case, the expected result is the enabling of the ***DP Alt Mode*** as bridged from ***USB4 DisplayPort*** tunneling.

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Figure 5-6 *USB4* Hub with *USB4* Host and DP Alt Mode Device Connection Flow Alignment

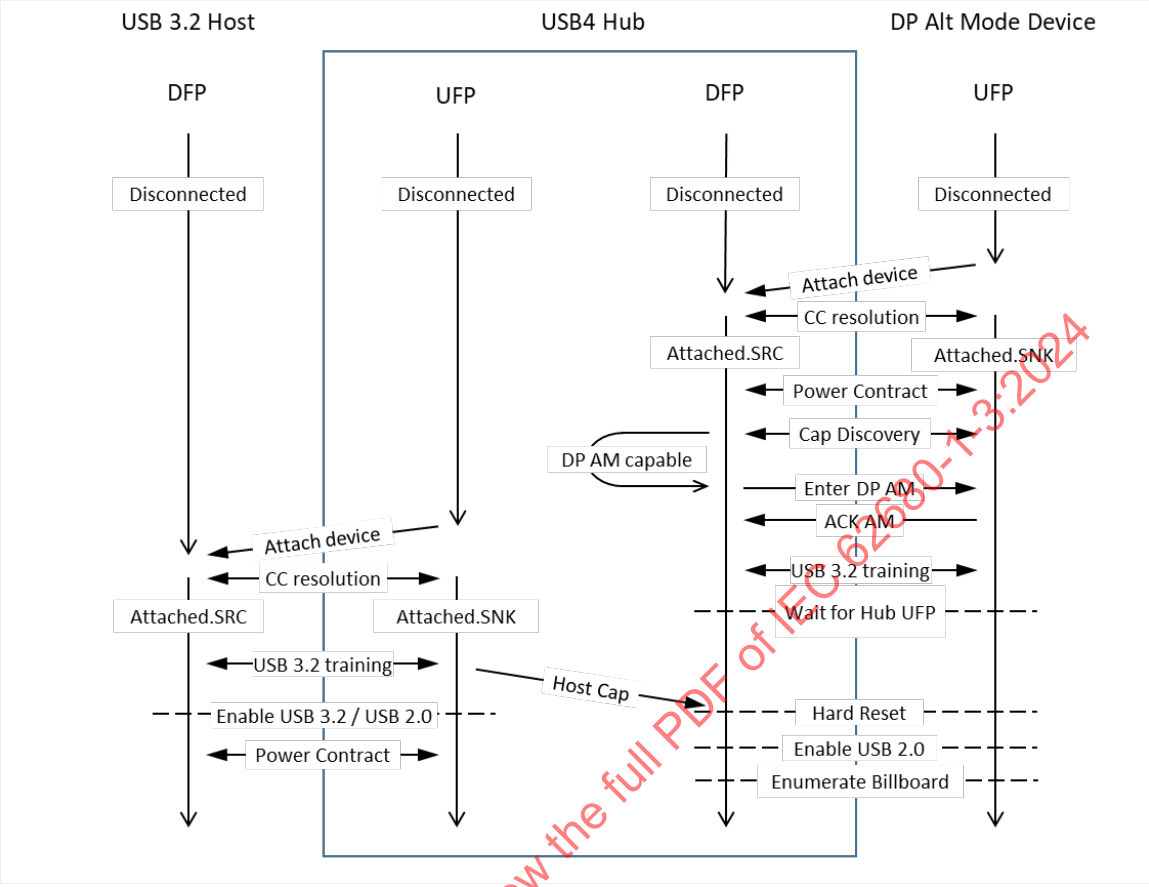


In the flow above, after the ***USB4*** connection of the hub's UFP is established, the DFP connection remains valid with the ***DisplayPort*** and ***USB 3.2*** data paths of the DFP being serviced by the ***USB4 DisplayPort*** and Enhanced SuperSpeed tunnels.

Figure 5-7 illustrates a connection flow aligned across the combination of a ***USB 3.2*** host, a ***USB4*** hub and a ***DP Alt Mode*** device (operating in Multi-function mode). The expected result in this case is that the ***DP Alt Mode*** will not be enabled, and a ***USB Billboard Device Class*** exposed by the device since the host doesn't support ***USB4***.

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Figure 5-7 *USB4* Hub with *USB 3.2* Host and DP Alt Mode Device Connection Flow Alignment



In the flow above, after the ***USB 3.2*** connection of the hub's UFP is established, the DFP connection is no longer valid with the ***USB4*** hub now operating as a traditional ***USB 3.2*** hub. The hub's DFP would then reset the port which will lead to a ***USB 2.0*** connection and the exposure of the ***USB Billboard Device Class***.

5.5.5 Connecting to Downstream *USB4* Hubs

When a ***USB4*** hub is attached on its DFP to the UFP of another ***USB4*** hub, the ***USB4*** hub ***shall*** use the Host Present bit of the ***USB PD Enter_USB*** message to inform the downstream hub if the ***USB4*** capabilities listed in the message reflects the host's capabilities or not. If an initial connection is made with the downstream hub with the Host Present bit reset in the ***USB PD Enter_USB*** message, the ***USB4*** hub ***shall*** subsequently send a revised ***USB PD Enter_USB*** message with the Host Present bit set after its UFP has been fully established (see Section 5.5.2).

5.5.6 Fallback Functional Requirements for *USB4* Hubs

When a ***USB4*** hub is attached on its UFP to a non-***USB4*** DFP, the ***USB4*** hub ***shall*** seamlessly fall back to functioning as and meeting the requirements for a ***USB 3.2*** hub.

5.6 *USB4* Device Connection Requirements

5.6.1 Fallback Mapping of *USB4* Peripheral Functions of USB Device Class Types

USB4 peripheral devices provide functions based on data transferred over one or more of the protocol tunnels of ***USB4***: ***Enhanced SuperSpeed USB***, ***DisplayPort*** and ***PCI Express***. For all peripheral functions that use the Enhanced SuperSpeed USB protocol tunnel, the mapping of those functions to USB device class specifications

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is clear but for those based on the other tunneled protocols, this mapping doesn't apply since those functions don't rely on USB device class drivers to operate.

Each function of a ***USB4*** device ***shall*** be mapped to an equivalent USB device class when possible. ***USB4*** devices that contain mapped USB device class functions ***shall*** support operation at ***USB 3.2*** or ***USB 2.0*** when connected to non-***USB4*** hosts. This requirement is exempt for those functions that rely on ***DisplayPort*** or ***PCIe*** tunnels for ***USB4*** data transfer that don't reasonably map to an existing USB device class, e.g., a PCIe graphics adapter.

The performance of the function when mapped to a lower speed connection is expected to scale appropriately while still providing the functional equivalent of the primary capabilities of the peripheral function.

Table 5-2 lists USB Device Class types and the mapping requirements for ***USB4*** device peripheral functions as it relates to fallback when operating over ***USB 3.2*** or ***USB 2.0***.

Table 5-2 Fallback Mapping *USB4* Functions to USB Device Class Types

Device Class Category	*USB4* Peripheral Function Mapping	Notes
Audio	***Required***	
Video	***Required***	
Mass Storage	***Required***	
Comms/Networking	***Required***	
Printer	***Required***	
HID	***Required***	Only required when an equivalent HID subclass or report usage is defined.
Media Transfer Protocol	***Required***	
Smart Card	***Required***	
Still Image Capture	***Required***	
Monitor Device	***Required***	Only required in conjunction with providing associated display applications.

For all ***USB4*** peripheral functions based on ***DisplayPort*** and ***PCIe*** protocol tunneling that do not map to USB device class equivalents when operating over ***USB 3.2*** or ***USB 2.0***, an appropriate ***USB Billboard Device Class shall*** be exposed to enable user notifications by the operating system of the host platform.

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5.7 Parameter Values

5.7.1 Timing Parameters

Table 5-3 provides the timeout requirement for a device that supports ***USB4*** to enable a ***USB Billboard Device Class*** interface when the device cannot connect as a ***USB4*** device during the discovery and entry process (Section 5.4).

Table 5-3 USB Billboard Device Class Availability Following *USB4* Device Entry Failure

	Maximum	Description
tUSB4Timeout	1000 ms	The time between (1) a Sink attach or (2) the data connection is reestablished in the ***USB PD*** Data Reset process until the ***USB Billboard Device Class*** interface is exposed when ***USB4*** device entry is not successful.

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6 Active Cables

Active cables ***shall*** minimally support ***USB 3.2*** Gen 2x2. ***USB4*** active cables ***shall*** support ***USB4*** in addition to all ***USB 3.2*** rates. Active cables ***shall*** support ***USB PD*** eMarkers and ***may*** support ***Alternate Modes*** and advertise them as defined in Section 6.1.1.

All ***USB4*** active cables ***shall*** be interoperable with ***Thunderbolt 3*** as defined in the ***USB4*** Specification (Chapter 13) and this specification (Section 6.1.1 and Appendices E and F).

Active cables supporting lengths up to 5 meters ***shall*** work in both directions and plug orientations and ***should*** function like passive cables from the user's perspective.

Hybrid Optical active cables use copper for power and ***USB 2.0*** data and optical for high-speed data signaling (TX/RX) and are functionally the same as copper-based active cables and ***shall*** function like passive cables from the user's perspective.

Optically Isolated Active Cables (OIACs) are a special case of active cables with unique requirements and limitations that are specific to OIACs. OIACs can support longer lengths up to 50 meters and provide electrical isolation between the two ends of the cable. OIACs are targeted for Industrial, Machine Vision, Remote Sensor, Pro Video, and Medical applications. OIACs do not 'just work' like normal cables. Further details on the requirements and limitations for the OIAC are in Section 6.3.

6.1 General Specifications for All Active Cables

6.1.1 Discovering Active Cable Characteristics

The ***USB PD*** Discover_Identity Command is used to discover the characteristics of the active cable. This command ***shall*** only be sent to SOP'. All active cables ***shall*** respond to the Discover_Identity Command with Active Cable VDOs that returns information about the cable. Note the active cable ***should*** respond with ***USB PD*** Revision 3 but ***may*** respond with ***USB PD*** Revision 2 following the ***USB PD*** Interoperability rules.

Table 6-1 summarizes the ***USB4*** cables regarding key identity values that will be returned to ***USB PD*** Revision 3 Discover_Identity commands.

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Table 6-1 *USB4* Cable Identity Summary

***USB4* Cable**	**Function**				**SOP' Configuration (*USB PD* Revision 3)**					
					ID Header VDO	**Passive Cable VDO**	**Active Cable VDO 1**	**Active Cable VDO 2**		
	USB2	**USB3**	***TBT3***	**DP**	**Cable Plug Passive/ Active B29…27**	**Cable Termination Type B12…11**	**Cable Termination Type B12…11**	**Physical connection B10**	**Active element B9**	**Optical Isolated Active Cable B2**
Passive[1]	Yes	Yes	Yes	Yes	011b	00b/01b	n/a	n/a	n/a	n/a
***TBT3* Linear Re-driver**[1]	Yes	Yes	Yes	Opt.	011b	01b[2]	n/a	n/a	n/a	n/a
Linear Re-driver (Gen4)[1]	Yes	Yes	Yes	Opt.	100b[4]	n/a	10b/11b	0b	0b	0b
					011b[4]	01b[2]	n/a	n/a	n/a	n/a
Re-timer[1]	Yes	Yes	Yes	Opt.	100b	n/a	10b/11b	0b	1b	0b
Hybrid Optical [1, 3]	Yes	Yes	Yes	Opt.	100b	n/a	11b	1b	0b/1b	0b
Optically Isolated	No	Yes	Opt.	No	100b	n/a	11b	1b	0b/1b	1b

Notes:
1. ***USB4*** cables, except for Optically-Isolated cables, are required to support ***Thunderbolt 3*** compatibility. The ***TBT3***-specific identity requirements are defined in Appendix F.
2. The ***TBT3*** Linear Re-driver active cable represents as only a Passive Cable that is discovered per Figure 5-1.
3. A Hybrid Optical active cable is defined as using an intermediate optical transmission line for the high-speed signaling path (TX/RX) while retaining a copper-based solution for the rest of the defined interfaces.
4. The ***USB4*** Gen4 Linear Re-driver active cable identifies as either an Active Cable or Passive Cable (for backward compatibility) depending on the version number (B14…11) given in the ***USB PD*** Structured VDM ***Discover Identity*** message as follows: for B14…11 = 0101b, the cable identifies as Active, and for B14…11 = 0100b, the cable identifies as Passive.

Note: As indicated in Table 6-1, ***USB4*** passive cables are required to support ***Thunderbolt 3*** compatibility. The implication of this requirement is that ***USB4*** Gen3 passive cables will properly respond to ***TBT3*** Passive Cable Discover Identity commands with the VDOs as defined in Table F-1 and Table F-3 of Section F.2.1 in order that they will be used in a ***TBT3*** connection at Gen3 speeds. ***USB4*** Gen2 cables ***should not*** implement ***TBT3*** Passive Cable Identity VDOs.

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Table 6-2 Active Cable Features

Cable Type	Length	*USB PD*	VBUS	VCONN Wiring	CC	*USB 2.0*	*USB 3.2* (All required)	*USB4*	Alternate Modes	SBU
USB 3.2 Active	< 5 m	SOP' ***Required*** (SOP" ***Optional***)	3 A or 5 A	Same as passive cable	Same as passive cable	Same as passive cable	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	***N/A***	***Optional***	Note 2 Note 3
USB4 Active	< 5 m	SOP' ***Required*** (SOP" ***Optional***)	3 A or 5 A	Same as passive cable	Same as passive cable	Same as passive cable	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	Gen2 Gen3 Gen4	***TBT3*** Note 1	Note 2 Note 4
USB4 Hybrid Active	< 5 m	SOP' ***Required*** (SOP" ***Optional***)	3 A or 5 A	Same as passive cable	Same as passive cable	Same as passive cable	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	Gen2 Gen3 Gen4	***TBT3*** Note 1	Note 2 Note 4

Notes:
1. ***Thunderbolt 3 Alternate Mode*** support required as defined in Appendix F.
2. A passive connection in ***USB 3.2*** mode is required.
3. Support for SBU is ***optional normative*** in ***Alternate Modes***.
4. SBU support for ***USB4*** can be either passive or active in the case of a linear re-driver-based active cable or active in the case of a re-timer-based active cable.

All active cables, regardless of length, ***shall*** be compliant with this specification, the ***USB 3.2*** including Appendix E, and the ***USB 3.2*** Active Cable CTS.

6.1.2 Electrical Requirements

6.1.2.1 Shielding Effectiveness Requirement

All active cables ***shall*** meet the shielding effectiveness requirement defined in Section 3.7.7 and Figure 3-65.

6.1.2.2 Low Speed Signal Requirements

6.1.2.2.1 CC Channel Requirements

Active cables ***shall*** meet the Low-Speed Signal Requirements in Section 3.7.2.6.

6.1.2.2.2 SBU Requirements

The SBUs are a pair of end-to-end electrical connections in the cable. While ***USB 3.2*** does not use these connections, they are used by ***Alternate Modes*** such as ***DisplayPort***. ***USB4*** also uses these connections but has renamed them as SBTX and SBRX. The electrical requirements are the same for both.

Active cable SBU wires ***shall*** meet the requirements defined in Table 6-3 and ***shall*** meet the crosstalk requirements both near-end and far-end between the low speed signals as defined in Section 3.7.2.6.

SBUs have no guaranteed performance when VCONN is not provided to the cable. The Host or Device ***shall not*** provide any signal beyond what is defined in Table 6-3 when VCONN has not been provided.

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Table 6-3 Active Cable SBU Requirements

Name	Description	Min	Max	Units
zCable_SBU	Cable characteristic impedance on the SBU wires	32	53	Ω
tCableDelay_SBU	Cable propagation delay on the SBU wire		26	ns
rCable_SBU	DC resistance of SBU wires in the cable in USB		40	Ω
vCable_SBU	Cable voltage swing on SBU wires	−0.3	4.0	V
Insertion Loss[1]	Cable insertion Loss		5 @ 0.5 MHz 7 @ 1 MHz 12 @ 10 MHz 13 @ 25 MHz 15 @ 50 MHz 16 @ 100 MHz	dB
iCableSBU	Maximum end-to-end current	−25	25	mA
Note 1: Measurement referenced to 50 Ohms.				

6.1.2.3 *USB 2.0*

Active cables ***shall*** meet the ***USB 2.0*** requirements defined in Section 3.7.2.6 and 3.7.2.7.

Note: Active Cables greater than 5 m report the number of hub hops consumed in the Active Cable VDOs.

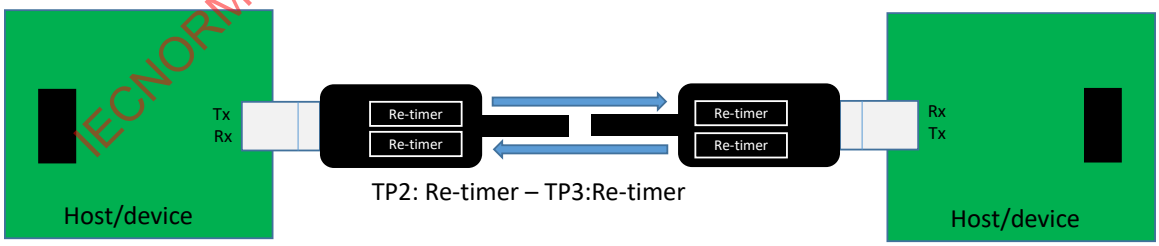
6.1.2.4 *USB 3.2*

Active cables ***shall*** incorporate AC-coupling from the plug to repeater on both the ***USB 3.2*** TX and RX signals. Active cables ***shall*** provide a discharge path for discharging the AC-coupling capacitors in the cable on unplug per ***USB 3.2***.

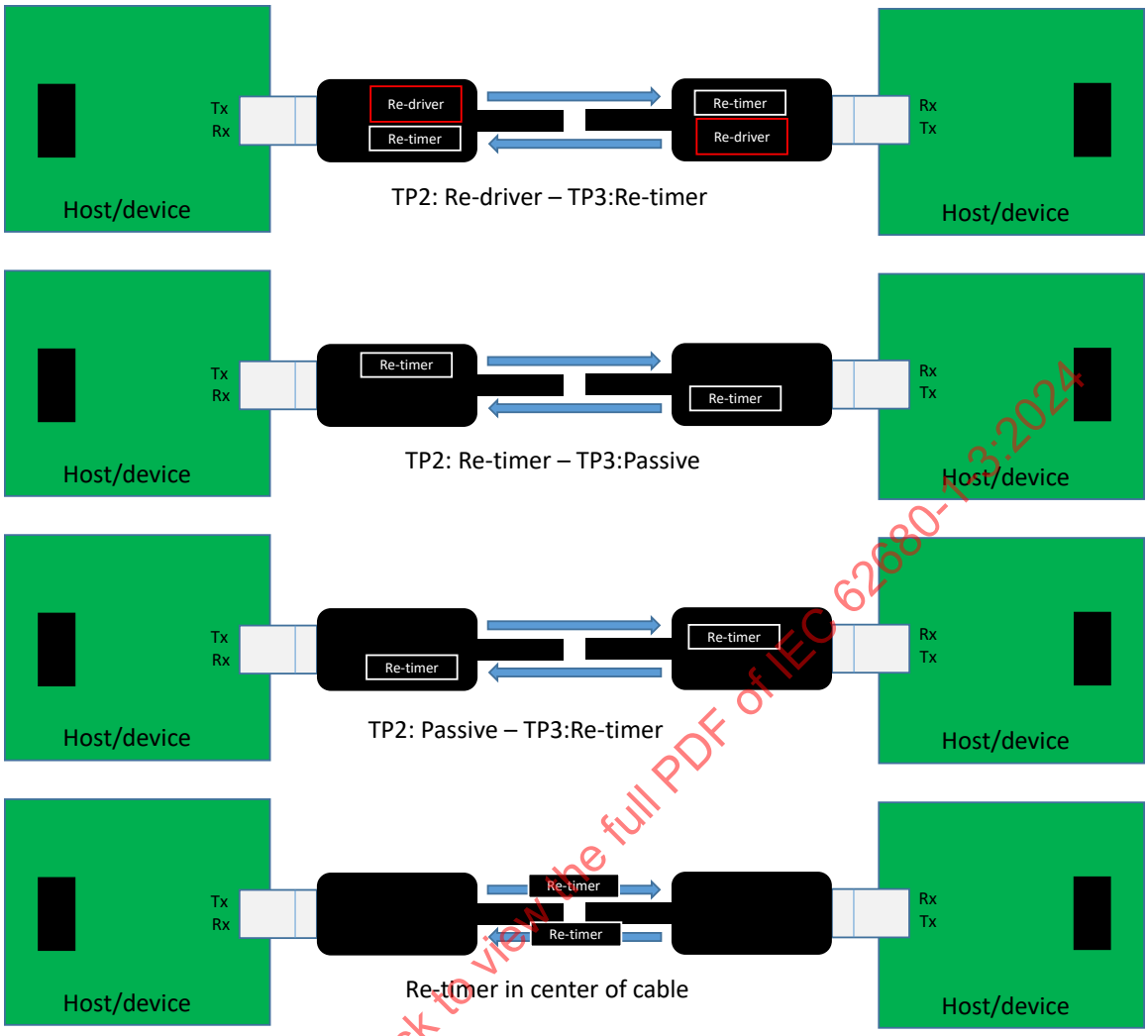
6.1.2.4.1 *USB 3.2* Active Cable Architectures

Active cables ***may*** have the combinations of re-timers and re-drivers as illustrated in Figure 6-1. Active cables without at least one re-timer are out of scope. Active cables without re-timers connected to TP3 are out of scope. Active cables ***shall*** support the features defined in Table 6-2.

Figure 6-1 Active Cable Topologies



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6.1.2.4.2 *USB 3.2* Power-On and Rx.Detect

Active cables ***shall*** present a high impedance to ground of $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ when not powered. Active cables ***shall*** present a high impedance to ground of $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ at initial power-on. The active cable ***shall*** perform far-end receiver termination detection on both cable ends upon receiving V_{CONN}. Upon detecting a far-end low-impedance receiver termination ($R_{RX\text{-}DC}$), the active cable ***shall*** enable its low-impedance receiver termination ($R_{RX\text{-}DC}$) to mirror the presence of the Host/Device. The active cable ***shall*** perform far-end receiver termination detection for Repeaters per ***USB 3.2*** including in low power states U2/U3.

An active cable ***shall*** complete power-on and far-end receiver termination detection through the cable within $t_{FWD_RX.DETECT}$.

Table 6-4 Active Cable Power-on Requirements

Name	Minimum	Maximum	Units
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$	Per ***USB 3.2***	Per ***USB 3.2***	
$R_{RX\text{-}DC}$	Per ***USB 3.2***	Per ***USB 3.2***	
$t_{FWD_RX.DETECT}$		42[1]	ms
Note 1: 84 ms – (2 · 12 ms + 18 ms) worst case.			

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Active cables including OIACs ***shall*** reflect the receiver terminations across the cable to replicate the behavior of a passive cable.

6.1.2.4.3 *USB 3.2* U0 Delay

All active cables ***shall*** meet the ***USB 3.2*** delay defined in Table 6-5.

Table 6-5 Maximum *USB 3.2* U0 Delay

USB 3.2 Gen	Cable Maximum U0 Delay	Notes
Gen1	3000 ns	Active cables with ***USB 3.2*** Gen1 latency larger than 125 ns ***may not*** function correctly when used in conjunction with host, devices, and hubs that do not support ***USB 3.2***.
Gen2	3000 ns	Active cables with ***USB 3.2*** Gen2 latency larger than 305 ns ***may not*** function correctly when used in conjunction with host, devices, and hubs that do not support ***USB 3.2***.

6.1.2.4.4 *USB 3.2* U-State Power Requirements

Active cables ***shall*** meet the VCONN power requirements for ***USB 3.2*** operation in Table 6-6. These requirements are for the entire cable, not just a cable plug.

Table 6-6 *USB 3.2* U-State Requirements

State	Maximum VCONN Power Consumption	Power Consumption Notes
U0	1.0 W single-lane 1.5 W dual-lane	Applies to POLLING.LFPS, TRAINING, and RECOVERY states.
U1	≤ U0 power	Forwarding LFPS is required
U2	≤ U1 power	Forwarding LFPS is required
U3	20 mW	Steady state power. eMarker in sleep.
Rx.Detect	20 mW	Rx.Detect period ***may*** be lengthened when no ***USB 3.2*** terminations have been detected. eMarker in sleep.
eSS.Disabled	20 mW	***USB 3.2*** is disabled. eMarker in sleep.

6.1.2.4.5 *USB 3.2* U-State Exit Latency

Active cables ***shall*** meet the U-state exit latency defined in ***USB 3.2*** Appendix E.

6.1.2.4.6 *USB 3.2* Signal Swing

An active cable transmitter only must drive 8.5 dB insertion loss at 5 GHz to the Host/Device controller receiver for ***USB 3.2*** Gen2, if the transmitter is located in the cable plug next to the receiving port.

A Host/Device controller transmitter must drive a total loss of 23 dB at 5 GHz to the far side for ***USB 3.2*** Gen2. The difference in loss budget allows the active cable transmitter swing to be reduced. An active cable receiver can assume a larger receiver swing than in the Host/Device for the same reason.

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Figure 6-2 defines the SuperSpeed electrical test points and is copied from the ***USB 3.2*** specification. Figure 6-3 indicates the test points and test equipment connections.

Figure 6-2 SuperSpeed USB Electrical Test Points

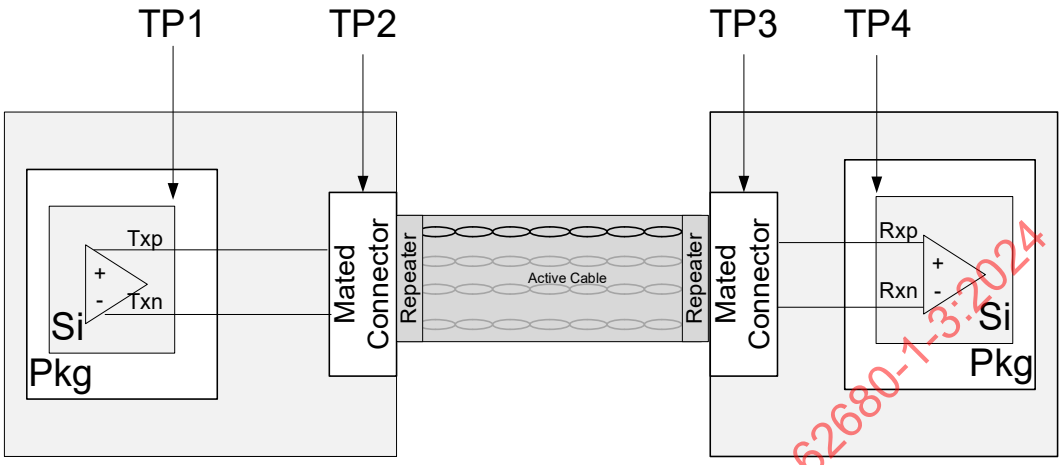
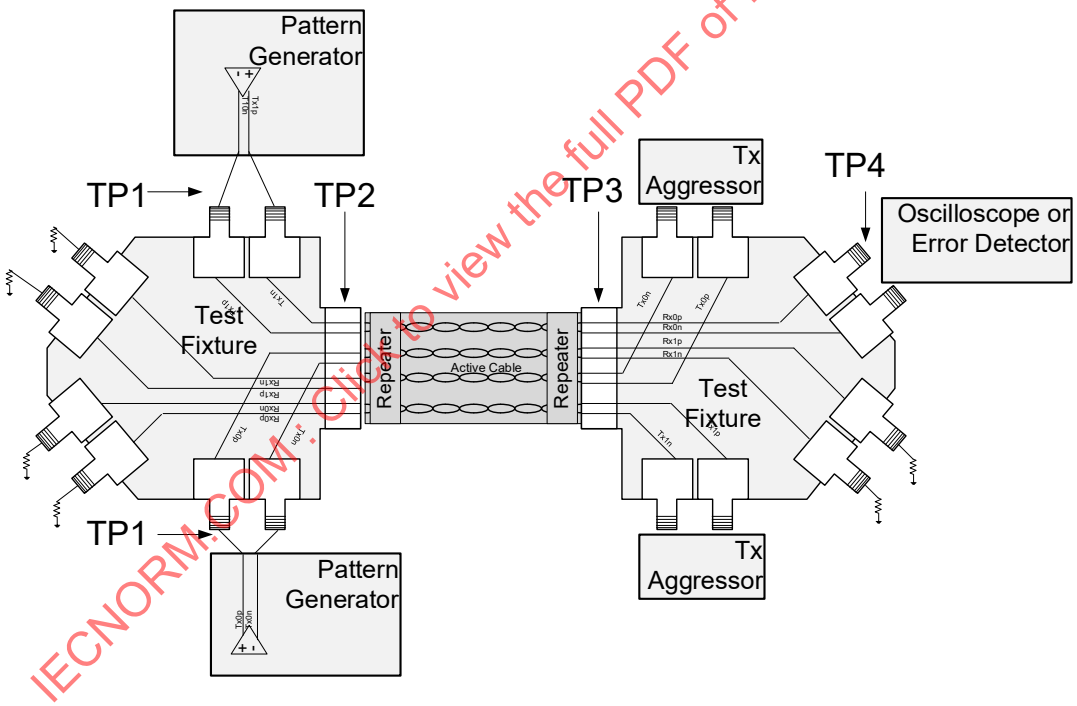


Figure 6-3 SuperSpeed USB Compliance Test Setup



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6.1.2.4.6.1 TP1 – Active Cable Input Stressed Source

The active cable input stressed source is generated at TP1 per Table 6-7 for amplitude and per Table 6-8 for jitter. SSC ***shall*** be present in the stressed signal at TP1. Table 6-7 is a subset of the ***USB 3.2*** Table 6-18. Table 6-8 is a subset of ***USB 3.2*** Table 6-28. If any discrepancy exists between this specification and the ***USB 3.2*** specification, the ***USB 3.2*** specification ***shall*** take precedence.

The maximum swing with the maximum de-emphasis and pre-shoot ***shall*** be tested with the minimum loss compliance test board. The minimum swing with the minimum de-emphasis and pre-shoot ***shall*** be tested with the maximum loss compliance test board. The input jitter composition is the same for both the minimum and maximum swing stressed sources.

The active cable ***shall*** function over the range of parameter in Table 6-7 and ***USB 3.2*** Table 6-17.

Table 6-7 Active Cable *USB 3.2* Stressed Source Swing, TP1

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX-DIFF-PP}$	Differential p-p TX voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p.
$V_{TX-DE-RATIO}$	TX de-emphasis	***USB 3.2*** Table 6-17	−3.1 ± 1.0	dB	Nominal is 3.5 dB for Gen1 operation. Gen2 transmitter equalization requirements are described in ***USB 3.2*** Section 6.7.5.2.
$V_{PRESHOOT}$	TX Preshoot	***USB 3.2*** Table 6-17	2.2 ± 1.0	dB	Gen2 transmitter equalization requirements are described in ***USB 3.2*** Section 6.7.5.2.

Table 6-8 Active Cable *USB 3.2* Stressed Source Jitter, TP1

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Notes
f1	Tolerance corner	4.9	7.5	MHz	
J_{Rj}	Random Jitter	0.0121	0.0100	UI rms	1
J_{Rj_p-p}	Random Jitter peak-peak at 10^{-12}	0.17	0.14	UI p-p	1,4
J_{Pj_500kHZ}	Sinusoidal Jitter	2	4.76	UI p-p	1,2,3
J_{Pj_1Mhz}	Sinusoidal Jitter	1	2.03	UI p-p	1,2,3
J_{Pj_2MHz}	Sinusoidal Jitter	0.5	0.87	UI p-p	1,2,3
J_{Pj_4MHz}	Sinusoidal Jitter	***N/A***	0.37	UI p-p	1,2,3
J_{Pj_f1}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_50MHz}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_100MHz}	Sinusoidal Jitter	***N/A***	0.17	UI p-p	1,2,3

Notes:

1. All parameters measured at TP1. The test point is shown in Figure 6-2 and Figure 6-3.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the RX is required to tolerate Pj at all frequencies between the compliance test points.
3. During the RX tolerance test, SSC is generated by test equipment and is always present. Each JPj source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the RX tolerance test.
5. The JTOL specs for Gen2 comprehend jitter peaking with re-timers in the system and has a 25 dB/decade slope.

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6.1.2.4.6.2 TP2 – Active Cable Input (*Informative*)

The values in Table 6-9 indicate the ***informative*** input signal swings at TP2 for an active cable. Table 6-9 is included to provide guidance beyond the ***normative*** requirements of Table 6-7 and Table 6-8. An active cable can be fully compliant with the ***normative*** requirements of this specification and not meet all the values in Table 6-9. Similarly, an active cable that meets all the values in Table 6-9, is not guaranteed to be in fully compliance with the ***normative*** part of this specification.

Table 6-9 Active Cable *USB 3.2* Input Swing at TP2 (*Informative*)

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX-DIFF-PP}$	Differential p-p TX voltage swing	250 (min) 1000 (max)	250 (min) 850 (max)	mV	Nominal is 550 mV p-p.
$V_{TX-DE-RATIO}$	TX de-emphasis	0 (min) 4.0 (max)	2.1 (min) 4.1 (max)	dB	There is no de-emphasis requirement for Gen1.
$V_{PRESHOOT}$	TX Preshoot	NA	1.2 (min) 3.2 (max)	dB	Applicable to ***USB 3.2*** Gen2 operation only.

6.1.2.4.6.3 TP3 – Active Cable Output (*Informative*)

The values in Table 6-10 indicate the ***informative*** output signal swings at TP3 for an active cable. Table 6-10 is included to provide guidance beyond the ***normative*** requirements of Table 6-7 and Table 6-8. An active cable can be fully compliant with the ***normative*** requirements of this specification and not meet all the values in Table 6-10. Similarly, an active cable that meets all the values in Table 6-10, is not guaranteed to be in full compliance with the ***normative*** part of this specification.

Table 6-10 Active Cable *USB 3.2* Output Swing at TP3 (*Informative*)

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX-DIFF-PP}$	Differential RX peak-to-peak voltage	300 (min) 850 (max)	300 (min) 850 (max)	mV	Measured after the RX EQ function. Nominal is 0.5 V p-p.
$V_{TX-DE-RATIO-GEN1}$	TX de-emphasis	0 (min) 4.0 (max)	NA	dB	No pre-shoot allowed.
$V_{TX-DE-RATIO}$ + $V_{PRESHOOT-GEN2}$	TX de-emphasis + TX Preshoot	NA	0 (min) 3.0 (max)	dB	Sum of the de-emphasis and pre-shoot. There is no de-emphasis and pre-shoot requirement.

6.1.2.4.6.4 TP4 – Active Cable Output

The active cable transmitter output is defined at TP4 for both high and low loss channels. The requirements for TP4 are defined in the ***USB 3.2*** specification Table 6-20. The input signal for the test ***shall*** be applied at TP1 as defined in the ***USB 3.2*** specification.

The low loss test board ***shall*** be used to test the maximum output swing. The maximum loss test board ***shall*** be used to test the minimum output swing. Jitter must be met with both test boards.

The active cable bit-error-rate ***shall*** be tested at TP4 and meet or exceed a BER of 10^{-12}. The error detector used ***shall*** have the ability to remove SKP ordered sets.

6.1.2.5 *USB4*

This section describes the electrical requirements and compliance testing for ***USB4*** active cables. Compliance testing is defined to ensure interoperability in terms of data integrity and electrical specifications enabling the active cable to reliably receive an input signal and output a valid signal at its other end.

The ***USB4*** active cable types are:

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1. Re-timer-based active cable (this section covers re-timer based cable for ***USB4*** only, ***USB 3.2*** re-timer cable is defined in Section 6.1.2.4),

2. Linear re-driver-based (LRD-based) active cable (***USB 3.2*** and ***USB4***), or

3. Linear optical active cable (the electrical LRD requirements in Section 6.1.2.5.4 will generally apply to a ***USB4*** OIAC).

6.1.2.5.1 Electrical Requirements Applying to All Active Cables

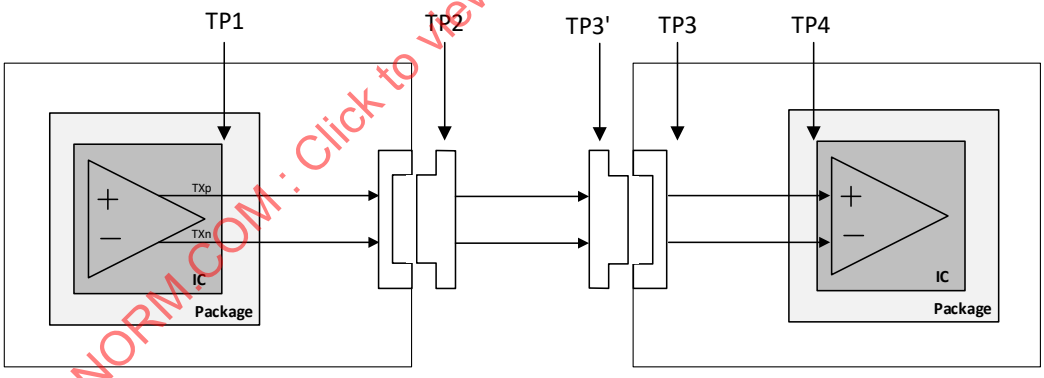
6.1.2.5.1.1 System Compliance Test Point Definition

All measurements ***shall*** be referenced to the following compliance points. Calibration ***shall*** be applied in cases where direct measurement is not feasible.

Table 6-11 Compliance Points Definition

Test Point	Description	Comments
TP1	Transmitter IC output	Not used for electrical testing
TP2	Transmitter port connector output	Measured at the plug side of the connector
TP3	Receiver port connector output	Measured at the receptacle side of the connector. All the measurements at this point ***shall*** be done while applying reference equalization function
TP3’	Receiver port connector input	Measured at the plug side of the connector
TP4	Receiver IC input	Not used for electrical testing

Figure 6-4 Compliance Points Definition



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6.1.2.5.1.2 Compliance Receptacle Test Boards

The USB Type-C high speed test fixture ***shall*** be used to enable cable compliance testing. The fixture ***shall*** be comprised of a high-quality USB Type-C receptacle and a short PCB trace that ***may*** be connected to coaxial cable with SMA/SMP connector at its end. Because TP2 and TP3’ reference points are located on the USB Type-C plug side of the connector, the loss and distortion of the receptacle fixture ***shall*** be calibrated such that all the measured values correspond to the standard reference points. The reference point TP3 is defined such that the insertion-loss from the connector pads to the compliance point is 0.5 dB ± 0.25 dB at 5 GHz and 1 dB ± 0.25 dB at 10 GHz. Extra loss and distortion elements ***shall*** be compensated by physical and/or mathematical means.

The target impedance of the fixture ***shall*** be 85 Ω. AC coupling capacitors ***shall*** be placed on the receptacle test fixture following the Router Assembly requirements as specified in ***USB4*** specification and CTS.

6.1.2.5.1.3 AC Coupling Capacitor

Active cables ***shall*** include AC-coupling capacitance between 135 nF and 265 nF inside their plugs placed at the output transmit path and between 300 nF and 363 nF at the input receive path. Discharge resistors between 200 KΩ and 242 KΩ ***shall*** be placed at the input receive path. See Figure 3-3 in the ***USB4*** specification for a diagram of the AC-coupling capacitors and discharge resistors.

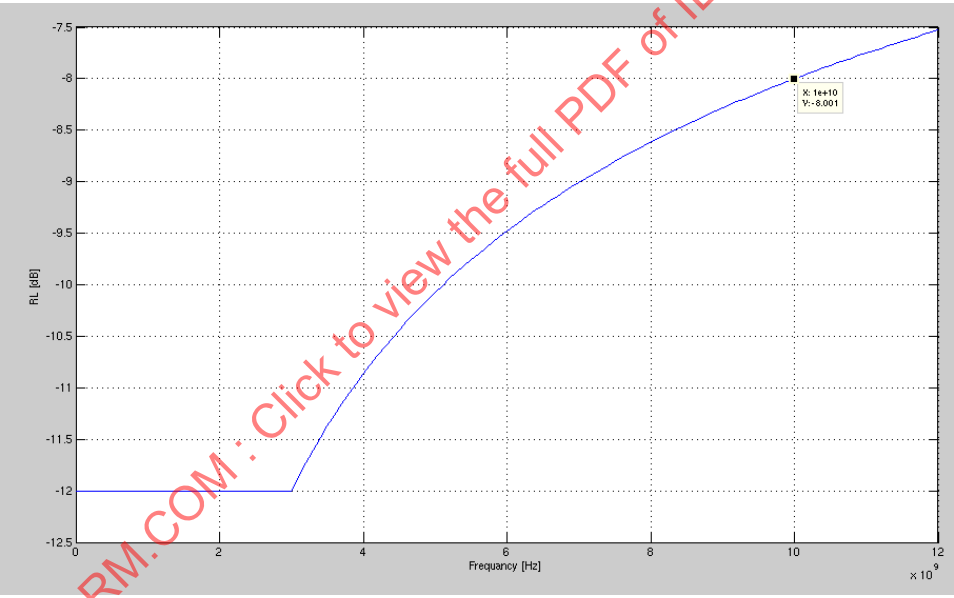
Active cable designs need to consider that a change of current consumption from VBUS as allowed by ***USB Power Delivery*** can add a considerable amount of common mode offset that ***may not*** be handled by the AC-coupling in this spec.

6.1.2.5.1.4 Differential Return-Loss Mask (*Informative*)

Re-timer and re-driver cable input and output return-loss measurements ***shall*** be referenced to a differential impedance of 85 Ω. When measured at TP3' and TP1 (respectively), the differential mode return loss recommended to not exceed the limits given in the following equation:

$$SDD22(f), SDD11(f) = \begin{cases} -12 & 0.05 < f_{GHz} \leq 3 \\ -7.5 + 7.5 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$

Figure 6-5 RX Differential Return-Loss Mask



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6.1.2.5.2 *USB4* CL-State Power Requirements for Active Cables

Active cables ***shall*** support all the CL-States and meet the VCONN power requirements for ***USB4*** operation in Table 6-12. These requirements are for the entire cable, not just a cable plug.

Table 6-12 *USB4* CL-State Requirements for Active Cables

State	Maximum VCONN Power Consumption	Power Consumption Notes
CL0	1.5 W	Applies to training states and CL0.
CL0s	≤ CL0 power	

State	Maximum VCONN Power Consumption	Power Consumption Notes
CL1	≤ CL0 power	
CL2	≤ CL1 power	
CLd	20 mW	Steady state power.
Note: OIAC CL-State Power requirements are in Section 6.3.6.5.2.		

6.1.2.5.3 Re-timer-based Active Cable Electrical Requirements

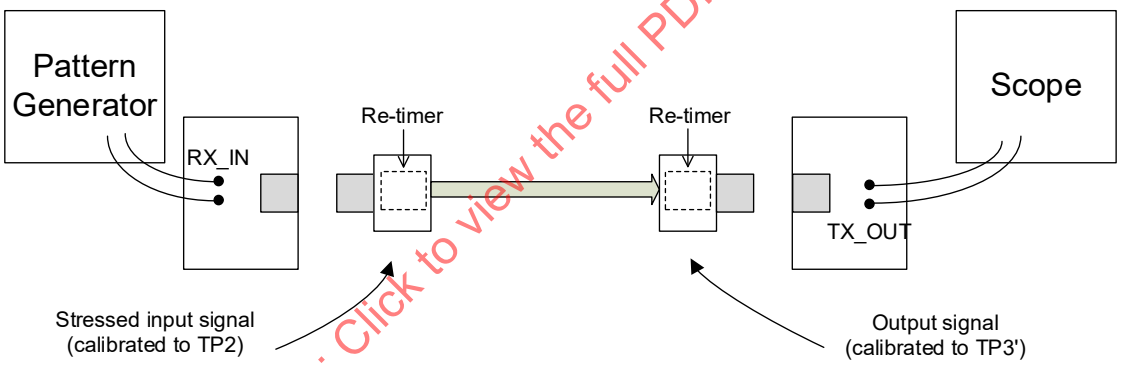
This section describes the electrical requirements and compliance testing for ***USB4*** re-timer-based active cables.

6.1.2.5.3.1 Output Equalization

A ***USB4*** active cable ***shall*** implement tunable 3-tap finite-impulse-response (FIR) equalization at its output. The transmit equalization ***shall*** support 16 preset configurations with different de-emphasis and pre-shoot settings as specified in the ***USB4*** specification, and ***shall*** be measured at TP3'.

6.1.2.5.3.2 Re-timer-based Active Cable Compliance Test Setup

Figure 6-6 Re-timer-based Active Cable Compliance Test Setup



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6.1.2.5.3.3 Cable Compliance Testing

Table 6-13 defines the ***USB4*** Active Cable specifications for Gen2 and Gen3 systems at TP3'. These parameters ***shall*** be measured at the Active Cable's output while applying a stressed signal at the input as specified in Table 6-14.

A ***USB4*** active cable ***shall*** be tested by injecting several different periodic jitter components, one at a time. The test ***shall*** include sinusoidal jitter frequencies of 1 MHz, 2 MHz, 10 MHz, 50 MHz, and 100 MHz. In all cases, the incoming signal ***shall*** include SSC modulation on top of the sinusoidal jitter component at the range of 300ppm to −5300ppm. PRBS31 pattern ***shall*** be used for ***USB4*** active cable compliance testing. However, calibration of the stressed signal source ***may*** be performed with a periodic pattern shorter than PRBS31. AC common-mode noise ***shall*** be added at the pattern generator output to ensure worst-case transmitter characteristics. The total common-mode noise ***shall*** be 100 mV peak-to-peak at TP2, where the added noise profile ***shall*** be sinewave at frequency not smaller than 400 MHz. All the specified jitter values ***shall*** be calibrated while applying the reference CDR defined in the ***USB4*** specification.

A ***USB4*** active cable receiver ***may*** configure its Link Partner's TX equalizer during the Link establishment. The pattern generator ***shall*** support tunable 3-tap FIR at its output, which ***may*** be adjusted during the test by the receiver under test through out-of-band software channel.

Table 6-13 Re-timer-based *USB4* Active Cable Output Specifications Applied for All Speeds (at TP3')

Name	Description	Min	Max	Units	Comments
CABLE_BER	End to End bit error rate		1E−12		See Note 1
AC_CM	Output AC Common Mode Voltage		100	mV pp	
LANE_TO_LANE_SKEW	Cable's Input-to-Output Skew between lanes		18	ns	
NRL	Noise Contributed by Integrated Return Loss				See 6.1.2.5.3.5
JTF_BW	Jitter tracking (forwarding) 3dB bandwidth from cable input to output		0.5	MHz	See Note 2
JTF_PEAKING	Jitter amplification from cable input to output		0.3	dB	Measured from 0 to 0.5 MHz. See Note 2
SSC_VARIATION	SSC output to input down-spread variation	−0.3	+0.3	dB	See Note 2
SSC_SLEW_RATE	SSC frequency slew rate (df/dt) during steady-state		1250	ppm/µs	See Note 3
INIT_FREQ_VARIATION	Non-modulated transmit frequency accuracy during the initial stages of the training period	−300	+300	ppm	See Notes 4 and 5
DELTA_FREQ_200ns	Transmit frequency variation over 200 ns measurement windows following the switching from local to recovered clock		1400	ppm	See Notes 4 and 5
DELTA_FREQ_1000ns	Transmit frequency variation over 1 µs measurement windows following the switching from local to recovered clock		2200	ppm	See Notes 4 and 5
V_OUTPUT_DC_AC_CONN	Instantaneous DC+AC voltages at the cable output side of the AC coupling capacitors	−0.5 (min1) −0.3 (min2)	+1.0	V	See Note 6
TJ	Total Jitter		0.32	UI pp	See Notes 7 and 9
UDJ	Deterministic jitter that is uncorrelated to the transmitted data		0.13	UI pp	
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter		0.06	UI pp	See Note 10
DCD	Deterministic Jitter Associated by Duty-Cycle-Distortion		0.03	UI pp	

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Name	Description	Min	Max	Units	Comments
Y1	Eye inner height at TP3' (one-sided voltage opening of the differential signal)	200		mV	Measured for 1E6 UI. See Notes 8 and 9, and ***USB4*** specification.
Y2	Eye outer height at TP3' (one-sided voltage opening of the differential signal)		650	mV	Measured for 1E6 UI. See Notes 8 and 9, and ***USB4*** specification.

Notes:

1. The cable BER requirement refers to the raw data, without applying forward error correction nor pre -coding.
2. JTF_BW and JTF_PEAKING characterizes the corresponding input-to-output low-pass Jitter Transfer Function bandwidth and peaking. In addition, it is required that the cable will not change the SSC modulation depth by more than specified. For verifying that, the SSC down-spreading depth of the cable input and output ***shall*** be compared.
3. The SSC slew rate ***shall*** be extracted from the transmitted signal over measurement intervals of 0.5 µs. The SSC slew-rate ***shall*** be extracted from the transmitter phase after applying a 2nd order low-pass filter with 3 dB point at 5 MHz. Steady-state clocking ***shall*** be applied from the point that SLOS training pattern is forwarded by the transmitter.
4. As shown in Figure 6-7, the initial transmit frequency is not modulated. The transmit frequency variation following the switching from local to recovered clock ***shall*** be measured over time intervals of 200 ns and 1 µs.
5. Measurement ***shall*** be performed over the transmitted signal. The signal phase ***shall*** be extracted while applying 2nd order low-pass filter with 3 dB point at 5 MHz.
6. The absolute single-ended voltage seen by the receiver. This requirement applies to all link states and during power-on, and power-off. (min1, max) is measured with a 200 KΩ receiver load, and (min2, max) is measured with a 50 Ω receiver load. The ground offset between the cable output and UFP is not included in V_OUTPUT_DC_AC_CONN.
7. TJ is defined as the sum of all "deterministic" components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top).
8. The output voltage is differential.
9. Transmit jitter ***shall*** be measured while applying the reference CDR described in the ***USB4*** Specification. Note that the measured jitter includes residual SSC jitter passing the reference CDR.
10. UDJ_LF is the uncorrelated deterministic jitter measured after applying 2nd order Low-Pass-Filter with 3 dB cut-off at 0.5 MHz on the measured jitter. This filter needs to be applied on top of the reference CDR rejection function. The measurement ***shall*** be performed while applying input stress signal with periodic jitter component of 100 MHz.

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Figure 6-7 Example of Transmitter Frequency Variation During Clock Switching

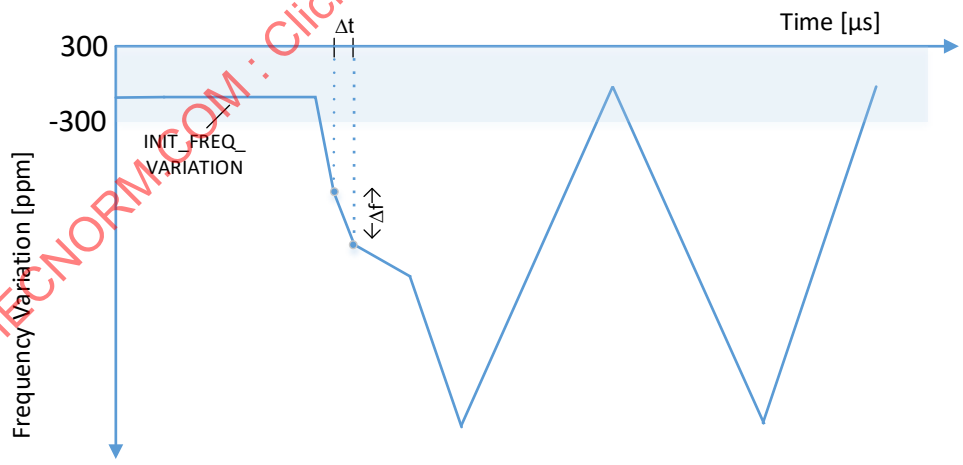
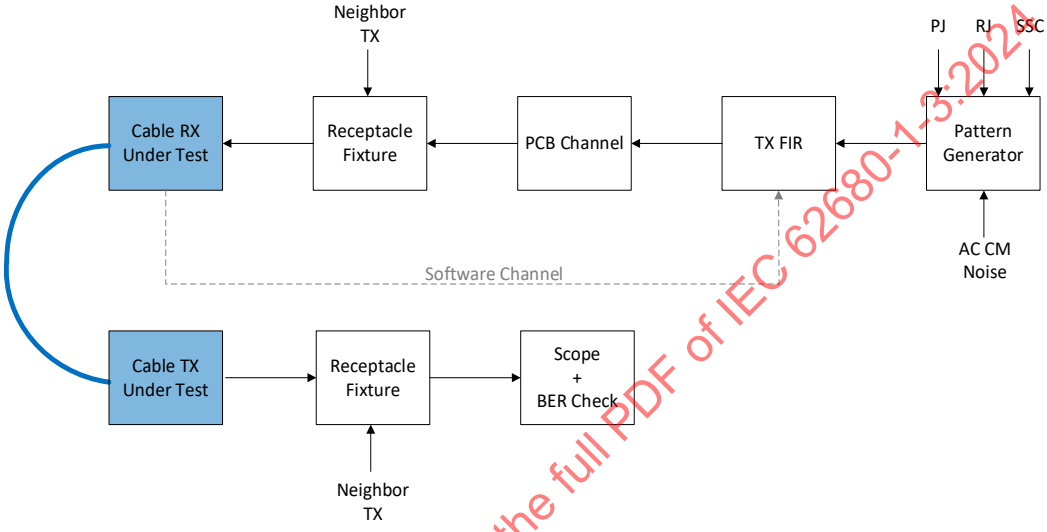


Table 6-14 Stressed Receiver Conditions for *USB4* Gen2 and Gen3 Cable Compliance Testing (at TP2)

USB4 Gen	Inner eye Voltage [mV peak]	Data Dependent Jitter (DDJ) [UI peak-to-peak]	Random Jitter [UI peak-to-peak]	Periodic Jitter [UI peak-to-peak]	Total Jitter [UI peak-to-peak]
Gen2	140	0.12	0.14	0.17	0.43
Gen3	120	0.15	0.14	0.17	0.46

Figure 6-8 Active Cable Functional Test Setup



6.1.2.5.3.4 Cable Error-Bursts Testing

To facilitate proper FEC operation, an active cable receiver ***shall*** take steps to limit the probability that a burst of errors is restarted immediately after receiving one or more correct bits (see ***USB4*** specification). The cable receiver under test ***shall*** trigger on bit-errors and ***shall*** capture error events that follow.

The test setup ***shall*** be initialized with the same configuration used for testing the uncoded BER with periodic jitter component of 100 MHz. As part of this setup, PRBS31 pattern is assumed and neither forward-error-correction nor pre-coding are applied. After initialization, the periodic jitter magnitude ***shall*** be increased to the point where uncoded BER of 1E−8 is observed. The receiver under test ***shall*** trigger on bit-error and ***shall*** capture error events that follow. An error event is defined as a mismatch between the received data and the reference PRBS31 pattern. At least 32 consecutive bits ***shall*** be examined for errors starting from the initial trigger. The probability for burst renewal ***shall*** be 5E−7 or less (i.e., one error burst restart per 2 million error captures).

The following is an example analysis:

No burst restart: captured_data[31:0]=00000000000000000000001111111111

Burst restart: captured_data[31:0]=00000000000000000000111001111111

where '1' represents a bit error and '0' represents a correct bit, as expected from "exclusive or" (XOR) operation between the received bits and the synchronized reference PRBS31 pattern. Captured_data[0] corresponds to the error event trigger.

Note: A burst of errors contains 1 or more consecutive bit errors.

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6.1.2.5.3.5 Noise Contributed by Integrated Return-Loss (NRL)

This section will be added in a future ECN.

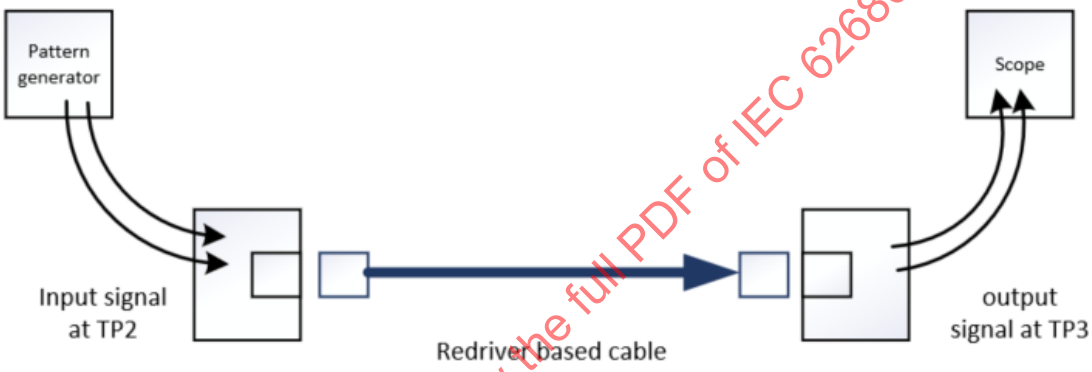
6.1.2.5.4 LRD-based Active Cable Electrical Requirements

Linear re-driver-based (LRD-based) active cables ***shall*** be tested as a complete component for compliance.

An LRD-based active cable is expected to receive a reference signal (referenced to TP2) defined in this specification and output a signal at the other end with electrical characterization that meets the requirements (referenced to TP3).

As shown in Figure 6-9, a compliant USB Type-C receptacle ***shall*** be connected to both ends of the active cable for injecting and measuring the signal to the corresponding TP2 and TP3 reference points. Details of the Compliance Receptacle and boards can be found in Section 3.3.6 of ***USB4*** Specification.

Figure 6-9 Linear Re-driver-based Active Cable Compliance Setup



Note: The internal placement of the re-driver ICs is purposely not specified to allow full flexibility to the manufacture to develop various re-driver-based solutions.

6.1.2.5.4.1 General Implementation Notes

This specification was developed considering electrical interoperability with legacy systems, as the LRD-based Active Cables were added to the USB ecosystem in a late phase when a lot of devices were already in the field.

The USB Type-C interconnect ecosystem assumes the worst case 1 m/2 m/0.8 m passive cable is the worst-case connection (for ***USB 3.2***, ***USB4*** Gen2 and ***USB4*** Gen3 respectively).

The intent is to align the LRD-based Active-Cable specifications to the existing passive cable specifications defined in Chapter 3 of this specification, such that the LRD-based active cable characteristics will be equal or better than those of the worst-case passive cable. The worst-case passive cable is defined in the ***USB 3.2*** and ***USB4*** Compliance Test Specification (CTS). This specification will define the electrical characteristics of the LRD-based cable that ***shall*** meet this requirement.

The LRD-based active cable specification assumes no change is needed to the existing TX/RX specification of the endpoint PHYs so that compatibility to existing certified ***USB 3.2*** and ***USB4*** devices is maintained.

For the Gen4 update to the ***USB4*** specification, LRD-based cable technology was considered, and all TX/RX implications are implicitly comprehended in the base specification.

Given this background, the following are assumptions regarding the LRD-based active cable implementation:

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1. LRD-based active cable is assumed to have no clock mechanism in its datapath (such as CDR).
2. For ***USB 3.2*** Gen2 and ***USB4*** Gen2/3, LRD-based active cable is assumed to not have a dynamic amplitude control (such as AGC) to avoid masking the TxFFE training from the receiver.
3. For ***USB4*** Gen4, it is a valid implementation choice to include AGC in the cable, however the time which this AGC can be enabled is limited to tLRDSelfTune which defined in this specification in Section 6.1.2.5.4.13.
4. LRD-based active cable is assumed to not use the training patterns to train itself, especially it is assumed to not block the output data during any phase of the training period.
5. Receiver systems rely on the low-pass-filter nature of the cable and having an over-equalized cable (i.e., weak LPF characteristic) can lead to interoperability issues. Therefore, it is recommended that when developing an LRD-based active cable, the cable ***should*** be built and tuned in a way that will make it the most passive-cable-like as opposed to most equalized cable.
6. During the development of the ***USB4*** Gen4 LRD cable we used a set of design assumptions that can be found in Appendix J.

6.1.2.5.4.2 *USB4* LRD-based Active Cable Compliance Testing

Table 6-15 defines the ***USB4*** linear re-driver-based active cable specifications for ***USB 3.2*** and for ***USB4*** Gen2, Gen3 and Gen4 systems at TP3.

These parameters ***shall*** be measured at the LRD-based active cable's output while applying a reference signal at the input as specified in Table 6-16.

An LRD-based active cable ***shall*** be tested by injecting several patterns, calibrated to TP2.

Table 6-15 Linear Re-driver-based Active Cable Output Parameters

Symbol	Description	Min	Max	Units	Conditions
$ILfitatDC$	Defining the ILfit mask for the cable response. Note: The main intention is to keep the cable with LPF characteristic similar to the passive cable. Note: Not applicable to ***USB4*** Gen4, see 6.1.2.5.4.11.	*ILfitatNq* + 1.5 ***USB4*** Gen2: −5	0	dB	See 6.1.2.5.4.4
$ILfitatf1$		$ILfitatNq$	$ILfitatDC$	dB	See 6.1.2.5.4.4
$ILfitatNq$		***USB 3.2***: −6 ***USB4*** Gen2: −12 ***USB4*** Gen3: −7.5	$ILfitatDC$ − 1.5	dB	See 6.1.2.5.4.4
$ILfitatf2$		$ILfitatNq - 3$	$ILfitatNq$	dB	See 6.1.2.5.4.4
$ILfitatf3$		$ILfitatf2 - 4$	$ILfitatf2$	dB	See 6.1.2.5.4.4
$ILfitatWB$	Max gain of the cable in the range of DC to f_N		0	dB	See 6.1.2.5.4.4
OUTPUT_NOISE	Standard deviation of the cable output noise. Combination of all noises beside the non-linearity noise.	See 6.1.2.5.4.5		mV	See 6.1.2.5.4.5

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Symbol	Description	Min	Max	Units	Conditions
SIGMA_E	Standard deviation of the Non-linearity noise measured in the cable output		***USB 3.2***, ***USB4*** Gen2/3: 15	mV	See 6.1.2.5.4.6
CABLE_SNDR	Signal to non-linearity noise ratio in the cable output	***USB4*** Gen4: TBD		dB	See 6.1.2.5.4.6
Operating margin	Receiver margin evaluation	***USB4*** Gen3: 3 ***USB4*** Gen4: 0		dB	See 6.1.2.5.4.9 ***normative*** only for ***USB4*** Gen3 and Gen4
Eye mask	Eye mask in the cable output				See 6.1.2.5.4.10
CM_NOISE	Common mode noise		100	mV pp	See 6.1.2.5.4.12
IRL	Integrated Return Loss				See 6.1.2.5.4.7
IMR	Integrated multi-reflection (integration of ILD (Insertion loss deviation))				See 6.1.2.5.4.8

Table 6-16 Input Signal at TP2 for Compliance Testing

Pattern (defined in ***USB4*** Specification 8.3.2.1.1)	Swing (reference to TP2)	Added Jitter	TX Equalization	SSC	Minimum Measurement Time	Usage
PRBS15	800 mV p-p	No	No EQ	No	20 µs	Cable gain, non-linearity noise
PRBS15	***USB4***: 1300 mV p-p ***USB 3.2***: 1200 mV p-p	No	No EQ	No	20 µs	Non-linearity noise
PRTS7	800 mV p-p	No	No EQ	No	20 µs	Cable gain, non-linearity noise (Gen4)
PRTS7	1000 mV p-p	No	No EQ	No	20 µs	Non-linearity noise (Gen4)
SQ512	300 mV p-p	No	No EQ	No	20 µs	Output noise
PRBS31	As defined in ***USB4*** Specification and CTS					Eye mask at TP3

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6.1.2.5.4.3 Measurement Methods

The compliance testing of an LRD-based active cable to this specification will be done based on measurements from both time and frequency domains.

For all time domain specification items, the measured LRD-based active cable parameters will be compared to the worst-case passive cable supported in each technology (with nominal cable length of 1 m for ***USB 3.2***, 2 m for ***USB4*** Gen2 and 0.8 m for ***USB4*** Gen3) measured in the exact same setup to reduce testing complexity. The worst-case passive cable is defined in the active cable CTS.

For ***USB4*** Gen4, the measurements will be against absolute values and not referenced to the worst-case passive cable.

More details on the measurement methods can be found in the active cable CTS.

6.1.2.5.4.4 Cable ILfit Mask (DC/f1/Nq/f2/f3/WB) for *USB 3.2* and *USB4* Gen2/Gen3

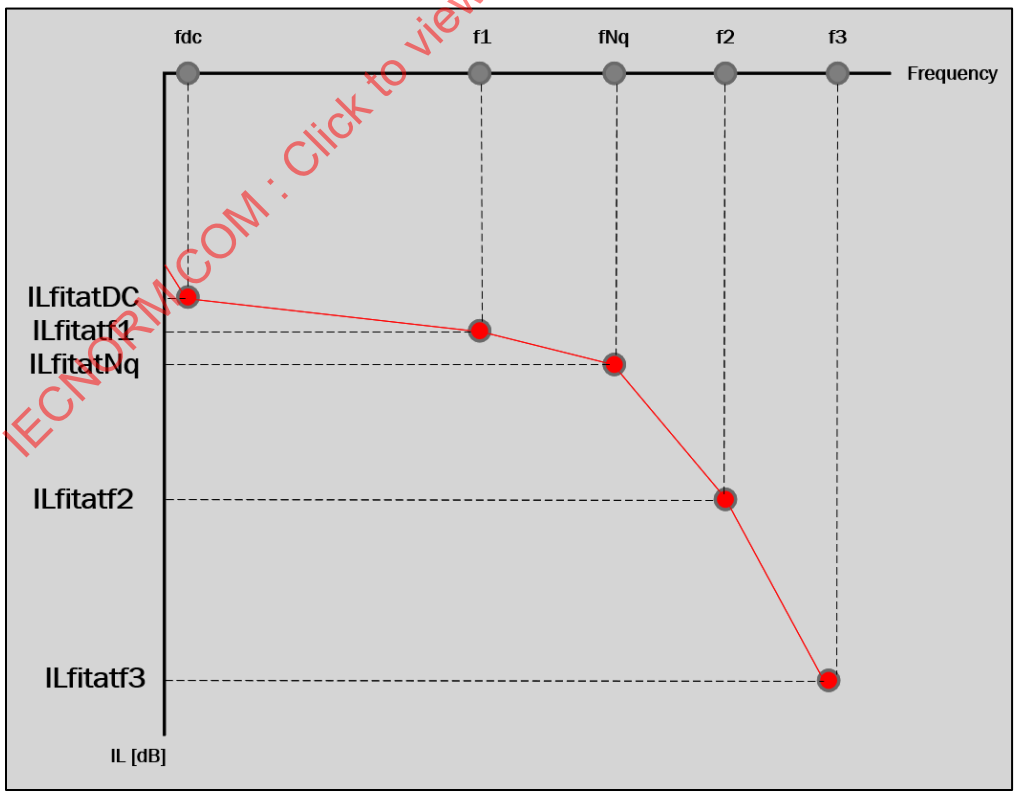
Based on the pulse response extraction from the time domain measurements, ($h(n)$) Fourier Transform is used to extract the impulse frequency response $H_{impulse}(f)$. For the specification parameters calculation, a fitted version of $H_{impulse}(f)$ ***shall*** be used. The pulse extraction and fitting methods are detailed in the active cable CTS and in Appendix G of this document.

$$ILfitatDC = 20 \cdot \log_{10}(ILfit(DC))$$
$$ILfitatf_1 = 20 \cdot \log_{10}(ILfit(f_1))$$
$$ILfitatf_N = 20 \cdot \log_{10}(ILfit(f_N))$$
$$ILfitatf_2 = 20 \cdot \log_{10}(ILfit(f_2))$$
$$ILfitatf_3 = 20 \cdot \log_{10}(ILfit(f_3))$$
$$ILfitatWB = \max\left(20 \cdot \log_{10}(ILfit(f_0)), where\ f_0\ is\ in\ the\ range\ of\ DC\ to\ f_N\right)$$

$$DC = 100\ MHz$$
$$f_1 = f_N \cdot 0.7$$
$$f_2 = f_N \cdot 1.25$$
$$f_3 = f_N \cdot 1.5$$
$$f_N\ for\ USB3.2: 5\ GHz$$
$$f_N\ for\ USB4\ Gen2: 5\ GHz$$
$$f_N\ for\ USB4\ Gen3: 10\ GHz$$

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Figure 6-10 Gain Parameters Specified for the Linear Re-driver Active Cable



6.1.2.5.4.5 OUTPUT_NOISE (σ_n)

σ_n is the standard deviation of the uncorrelated additive noise added to the output signal of the LRD-based active cable.

To achieve an accurate measurement, the calculation will be done based on a low frequency signal (SQ512 pattern) applied to the cable input, with 0.3 Vpp amplitude.

Since the noise calculation is referred to the receiver input, a 2nd order Butterworth LPF filter with −2 dB @ Nq ***shall*** be applied on the captured wave to account for the receiver BW and device side platform.

The limit of OUTPUT_NOISE is defined as function of the IL at Nyquist frequency. This allows a degree of freedom to the cable developer to trade between the cable's gain and noise.

The limit is defined as:

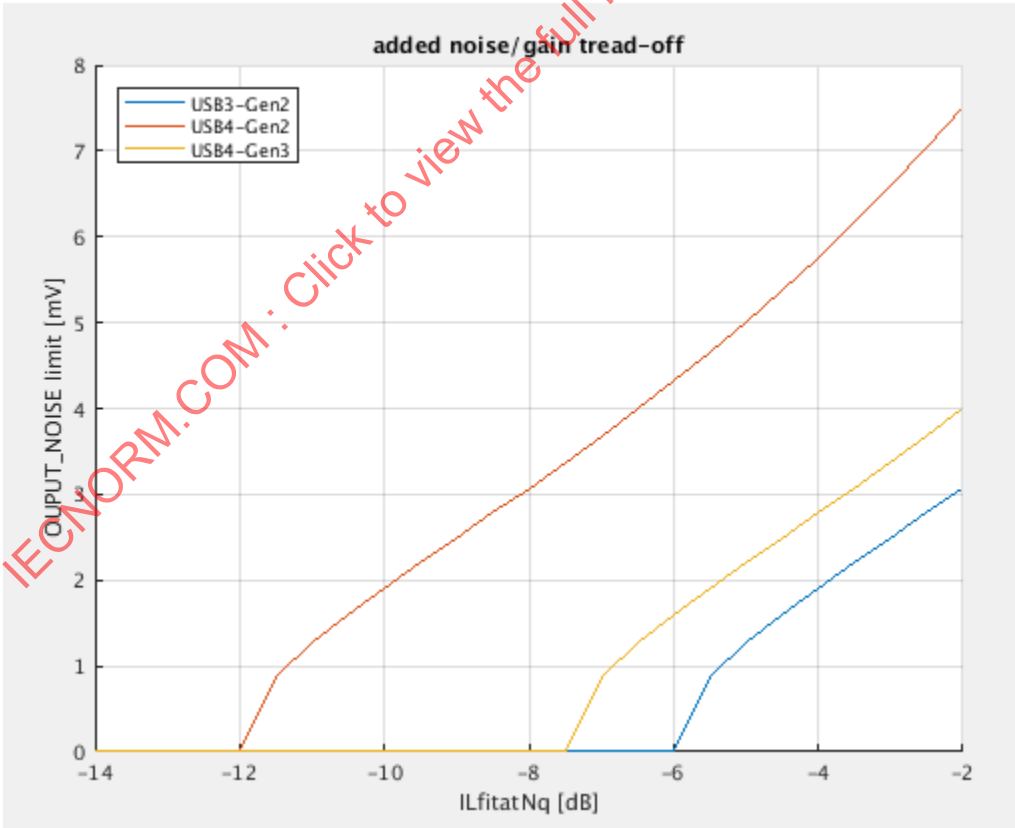
$$\sigma_{cable} \leq \sqrt{\frac{\sigma_1^2}{10^{\frac{H(f_N)_{PC}-H(f_N)_{RC}}{10}}} - \sigma_1^2} \cdot \frac{1}{\alpha}$$

Using the following parameters:

σ_1	2 mV
α	0.9
$H_{PC}(f_N)$	***USB 3.2***: −6 dB ***USB4*** Gen2: −12 dB ***USB4*** Gen3: −7.5 dB

Figure 6-11 shows a graph of this function for the given parameters.

Figure 6-11 OUTPUT_NOISE Limit Versus *ILfitatNq*



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6.1.2.5.4.6 SIGMA_E (σ_e)

σ_e is the standard deviation of the non-linearity related noise added by the LRD-based active cable.

This measurement ***shall*** be performed twice: once with minimum input swing and once with maximum input swing.

Then, $\sigma_e = \max(\sigma_{e\,\max\,swing}, \sigma_{e\,\min\,swing})$.

where:

maximum input $swing$
$= 1300mVpp\ (USB4\ Gen2/3), or\ 1200mVpp\ (USB\ 3.2)$ or $1000mVpp\ (USB4\ Gen4)$
Minimum $input\ swing = 800mVpp$
$(compatible\ with\ USB\ 3.2/USB4\ specification\ \max\ swing\ definition)$

For ***USB4*** Gen4, CABLE_SNDR results ***should*** be further calculated as:

$$CableSNDR = db\left(\frac{PulseResponsePeak}{sqrt(C_e \cdot \sigma_e^2 + C_n \cdot \sigma_N^2)}\right)$$

The value of $C_e and\ C_n$ is still TBD and will be added by an ECN when determined.

More details on the calculation of the non-linearity noise can be found in the Active Cable CTS and in Appendix G of this document.

6.1.2.5.4.7 Integrated Return-Loss (IRL)

The IRL term for an LRD-based active cable is calculated similarly to the passive cable, see 3.7.2.3.5.

The IRL limit is different for LRD-based active cables and is given by the following functions:

Mode:	IRL Limit:
USB 3.2 Gen2	$IRL \le 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 8.784$
USB4 Gen2	$IRL \le 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 8.784$
USB4 Gen3	$if(-4dB \le ILfit@Nq)$: $IRL \le -13dB$ $if(ILfit@Nq < -4dB)$: $IRL \le ILfit@Nq - 9$
USB4 Gen4	TBD (Will be added by an ECN when determined)

6.1.2.5.4.8 Integrated Multi-Reflection (IMR)

The IMR term for an LRD-based active cable is calculated similarly to the passive cable, see 3.7.2.3.2.

The IMR limit is different for LRD-based active cables and is given by the following functions:

Mode:	IRL Limit:
USB 3.2 Gen2	$IMR \le 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 20.392$
USB4 Gen2	$IMR \le 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 20.392$
USB4 Gen3	$if(-4dB \le ILfit@Nq)$: $IMR \le -29dB$ $if(ILfit@Nq < -4dB)$: $IMR \le 1.741 \cdot ILfit@Nq - 22.143$
USB4 Gen4	TBD (Will be added by an ECN when determined)

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6.1.2.5.4.9 Evaluating Channel Operating Margin (COM)

For ***USB4*** Gen3, Channel operating margin (COM) ***shall*** be calculated for LRD-based active cables supporting ***USB4*** Gen3, for evaluating a reference receiver margin based on the cable's measured S parameters.

The measurements of the cable and the setting of the associated COM tool is defined in the Active Cable CTS.

For ***USB4*** Gen4, Channel operating margin ***shall*** be calculated with the eCOM tool instead of the standard COM tool.

6.1.2.5.4.10 Cable Output Eye Mask

An LRD-based active cable ***shall*** meet eye mask limits at its output.

The test setup ***shall*** be identical to the ***USB 3.2*** and ***USB4*** calibrated receiver test which includes worst case passive cable.

During the test, a reference CTLE, DFE and TXFFE settings ***shall*** be tuned according to the ***USB 3.2*** /***USB4*** spec for obtaining the optimal eye.

1. ***USB 3.2*** has fixed TXFFE settings according to the ***USB 3.2*** Gen2 TX specification.
2. ***USB4*** can tune the TXFFE according to the TXFFE preset table in ***USB4*** Specification Table 3-5.

After obtaining the optimal eye with the passive cable, repeat the same measurement with the LRD cable under test, and compare the extracted eyes.

The optimal LRD cable eye ***shall*** meet these criteria:

$$LRD\ cable\ eye\ area \geq Passive\ cable\ eye\ area$$
AND
$$LRD\ cable\ eye\ width > 0.9 \cdot Passive\ cable\ eye\ width$$

For ***USB4*** Gen4, the optimal LRD cable eye ***shall*** meet the limits as defined in the CTS.

Note that the maximum eye height is constrained by the spec item *ILfitatWB* that prevents active amplification over the entire frequency range.

6.1.2.5.4.11 *USB4* Gen4 ILfitMask Limits

The ILfitMask for an LRD-based active cable supporting ***USB4*** Gen4 is defined in Table 6-17.

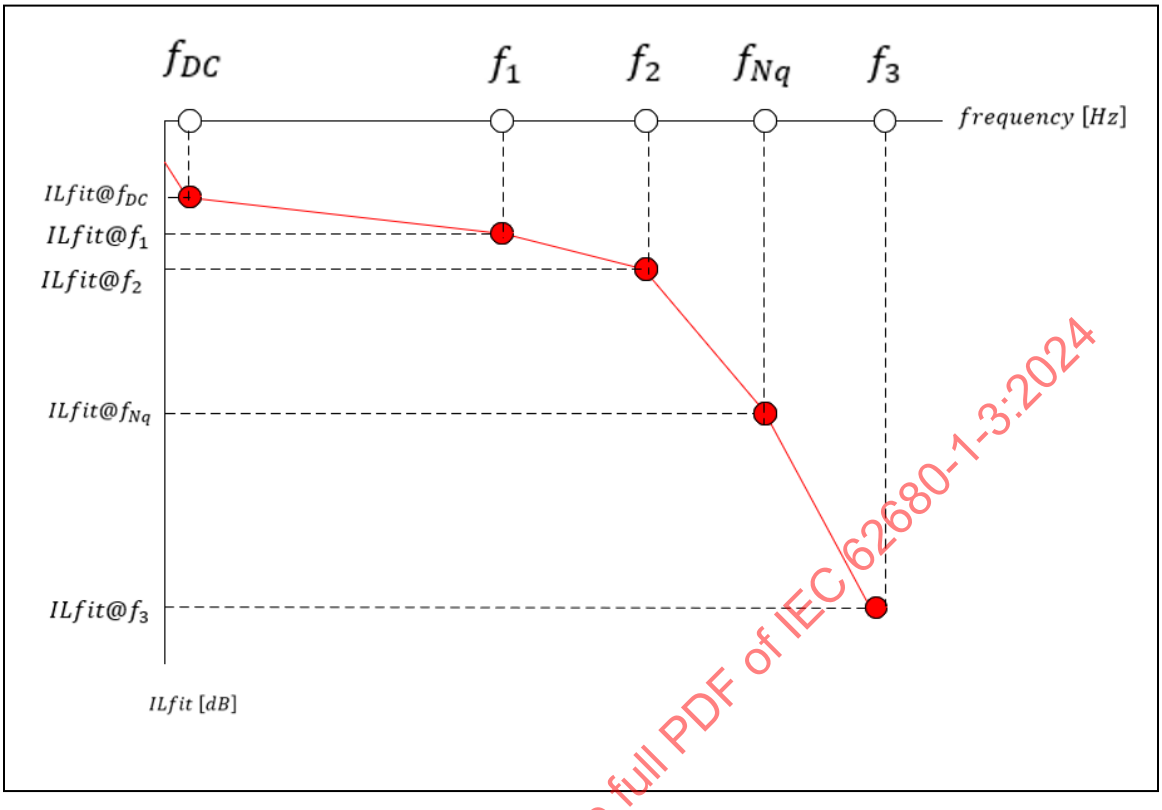
Table 6-17 *USB4* Gen4 LRD-based Active Cable ILfitMask Limits

Symbol	Frequency	Min	Max	Units
$ILfitatDC$	100 MHz	-3 $[TBD]$	0	dB
$ILfitatf1$	$0.7 \cdot fNq$	$ILfitatf2$	$ILfitatDC$	dB
$ILfitatf2$	$0.85 \cdot fNq$	$ILfitatNq$	$ILfitatf1$	dB
$ILfitatNq$	12.8 GHz	$ILfitatDC - 7.5$	$ILfitatDC - 3$	dB
$ILfitatf3$	$1.2 \cdot fNq$	$ILfitatNq - 4$ $[TBD]$	$ILfitatNq$	dB

This mask ***shall*** be met for any TXFFE setting in the cable input, and for minimum and maximum swing level in the TX.

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Figure 6-12 Gain Parameters for *USB4* Gen4 LRD Active Cables



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6.1.2.5.4.12 Cable CM_NOISE

CM_NOISE is defined as the maximum peak value of the signal captured in the cable output with common mode setting on the scope (p+n) and prbs15 data pattern.

The CM_NOISE ***shall not*** exceed 100mV.

6.1.2.5.4.13 Self-Gain Tuning Capabilities in *USB4* Gen4 LRD Cables

For the ***USB4*** Gen4 rate, the cable can tune its own gain to the optimal settings depending on the incoming signal. Refer to 6.1.2.5.4.16.3 Phase 4 and Phase 5 for details on when the cable ***may*** tune its gain.

tLRDSelfTune is defined to be 250 µs.

After that period the LRD response ***shall*** be fixed.

Note: this self-tune ability is for gain only, the EQ response ***shall*** be fixed for all input (see more on the ILfitMask for ***USB4*** Gen4 in 6.1.2.5.4.4).

Section 6.1.2.5.4.17 defines how the cable snoops and adjusts its gain.

6.1.2.5.4.14 *USB4* Gen4 Lane Direction Change

LRD-based active cables that support ***USB4*** Gen4 ***shall*** support the asymmetric mode as defined in the ***USB4*** specification (Section 4.2.2.5) and the LRD_Tuning.Force_Lane_Reversal for cable compliance. That means that each high-speed pair of the cable (TX0/TX1/RX0/RX1) ***shall*** be able to operate in both directions.

The cable ***shall*** follow 6.1.2.5.4.16.5 and 6.1.2.5.4.16.6 when switching into and out of asymmetric mode.

6.1.2.5.4.15 LRD Active Cable Logical Layer Wiring Diagram

The LRD active cable ***shall*** follow the wiring diagram as indicated in Table 6-18. The assumption in this table is that there is an LRD in each cable plug.

Table 6-18 *USB4* Gen4 LRD-based Active Cable Wiring Diagram for Compliance

USB Type-C Plug #1		Cable Connection			USB Type-C Plug #2	
Pin	Signal Name				Pin	Signal Name
A1, B1, A12, B12	GND	Fixed Connection			A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	Fixed Connection			A4, B4, A9, B9	VBUS
A5	CC	Fixed Connection			A5	CC
B5	VCONN	***Ra*** to GND, diode connection			B5	VCONN
A6	Dp1	⟷			A6	Dp1
A7	Dn1	⟷			A7	Dn1
A8	SBU1	Fixed Connection			B8	SBU2
B8	SBU2	Fixed Connection			A8	SBU1
Shell	Shield	Fixed Connection, outer shield			Shell	Shield
Normal Operation or Compliance Force Lane Reversal = 0b						
		Symmetric Connection	**Enable3TX Plug #1 Enable3RX Plug #2**	**Enable3RX Plug #1 Enable3TX Plug #2**		
A2	TXp1	—— LRD ⟶	—— LRD ⟶	—— LRD ⟶	B11	RXp1
A3	TXn1	—— LRD ⟶	—— LRD ⟶	—— LRD ⟶	B10	RXn1
B11	RXp1	⟵ LRD ——	⟵ LRD ——	⟵ LRD ——	A2	TXp1
B10	RXn1	⟵ LRD ——	⟵ LRD ——	⟵ LRD ——	A3	TXn1
B2	TXp2	—— LRD ⟶	—— LRD ⟶	⟵ LRD ——	A11	RXp2
B3	TXn2	—— LRD ⟶	—— LRD ⟶	⟵ LRD ——	A10	RXn2
A11	RXp2	⟵ LRD ——	—— LRD ⟶	⟵ LRD ——	B2	TXp2
A10	RXn2	⟵ LRD ——	—— LRD ⟶	⟵ LRD ——	B3	TXn2
Compliance Force Lane Reversal = 1b						
		Symmetric Connection	**Enable3TX Plug #1 Enable3RX Plug #2**	**Enable3RX Plug #1 Enable3TX Plug #2**		
A2	TXp1	—— LRD ⟶	⟵ LRD ——	⟵ LRD ——	B11	RXp1
A3	TXn1	—— LRD ⟶	⟵ LRD ——	⟵ LRD ——	B10	RXn1
B11	RXp1	⟵ LRD ——	⟵ LRD ——	⟵ LRD ——	A2	TXp1
B10	RXn1	⟵ LRD ——	⟵ LRD ——	⟵ LRD ——	A3	TXn1
B2	TXp2	—— LRD ⟶	⟵ LRD ——	—— LRD ⟶	A11	RXp2
B3	TXn2	—— LRD ⟶	⟵ LRD ——	—— LRD ⟶	A10	RXn2
A11	RXp2	⟵ LRD ——	—— LRD ⟶	⟵ LRD ——	B2	TXp2
A10	RXn2	⟵ LRD ——	—— LRD ⟶	⟵ LRD ——	B3	TXn2

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Table 6-19 defines the SBx transactions the LRD active cable is required to snoop and common ***optional*** SBx transactions which ***may*** be snooped. The LRD active cable ***may*** snoop more SBx transactions if desired. SBx transactions snooped on SBU1 have been transmitted from SBTX of the attached Router or Re-timer and ***may*** have an assumption of direction depending on the transaction.

Table 6-19 *USB4* Gen4 Active Cable SBx Transaction Snooping

Transaction Type	Symbol or Transaction Contents	Optional or Required?	Action
LT	LT_Fall	Required	Transition to CLd.
	LT_Resume	***Optional*** if LOS (loss of signal) is used	Transition to Forwarding.
	LT_LROff	Required	Transition to CLd. Issued on Lane 0 but affects all both lanes.
	LT_SwitchRx2Tx	Required	Transition to/from Asymmetrical when snooped on SBU1.
	LT_SwitchAck	Required	Transition to/from Asymmetrical when snooped on SBU1.
	LT_Gen2	***Optional*** if LOS is used	Transition to Forwarding. ***Optional*** to use specific Gen2 fixed gain and equalization.
	LT_Gen3	***Optional*** if LOS is used	Transition to Forwarding. ***Optional*** to use specific Gen3 fixed gain and equalization.
	LT_Fall	Required	Transition to CLd.
RT Broadcast	***TBT3***-CompatibleSpeed	***Optional***	Modify gain and equalization for TBT rates.
	USB4	Required	0b – Use LT transactions for link training. 1b – Use RT transactions for link training.
	SelectedGen	***Optional***	Modify gain and equalization per data rate Gen2, Gen3, Gen4.
	Enable3Tx	Required	Asymmetrical Initial link training.
	Enable3Rx	Required	Asymmetrical Initial link training.
	Lane1Enabled	***Optional*** if LOS is used	0b – CLd lane1. 1b – Enable forwarding lane1.
	Lane0Enabled	***Optional*** if LOS is used	0b – CLd lane0. 1b – Enable forwarding lane0.
RT Addressed Index 0 to Gen4TxFFE	Partner_Tx_Status_Byte.TxFFE_Start	***Optional***	Adjustment of AGC is allowed.
	Partner_Tx_Status_Byte.Request_Done	***Optional***	0b – Do not start AGC. 1b – start AGC for tLRDSelfTune.
RT Addressed Index 0 to LRD Tuning	Force Lane Reversal (bit 1)	Required	Required for Compliance Force Lane Reversal. ***Optional*** to adjust gain and equalization in a TBD way.
ELT	ELT_OpDone	***Optional***	No action.
	ELT_Recovery	Required	Transition to Forwarding.

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6.1.2.5.4.16 *USB4* and *TBT3* Logical Layer

The LRD active cable ***shall*** determine its ***USB4*** behavior based on snooping the RT broadcast (RTb) and RT addressed (RTa) transactions, the LT, and the ELT transactions.

6.1.2.5.4.16.1 *USB4* and *TBT3* Timing Parameters

The LRD active cable ***shall*** meet the timing requirements in Table 6-20.

Table 6-20 *USB4* LRD Active Cable Logical Timing Parameters

Parameter	Description	Min	Max	Units
tLRDForward	The amount of time the LRD takes to transition to Forwarding upon snooping Lane Enable.		1	ms
tLRDSwitch	The amount of time the LRD takes to switch direction after snooping LT_SwitchRX2TX or LT_SwitchAck and receiving no high speed data.		1	ms

6.1.2.5.4.16.2 *USB4* and *TBT3 USB PD* Mode Entry

This section defines the behavior of the LRD cable during the phases of link training.

The ***USB PD*** controller ***shall*** use the information from the SOP' and SOP'' (if present) in the ***USB PD*** Enter Mode command to configure to the LRD to ***USB4/TBT3***.

6.1.2.5.4.16.3 *USB4* and *TBT3* Lane Initialization

The following describes initializing the lanes, including training, across an LRD active cable. See the ***USB4*** specification for more details regarding the five phases of lane initialization.

Phase 1: Initial Conditions

Receiver and Transmitter terminations are enabled. The common-mode voltage is unchanged. The LRD ***shall*** assume the Router far side termination is not present in this state. The Router ***may*** change its common-mode voltage with or without terminations present when transitioning to this state.

The ***USB PD*** Controller informs the LRD in the active cable of the connection and mode.

Phase 2: Router Detection

No action.

Phase 3: Port Characteristics

No action.

Phase 4: Transmission Start

General Requirements:

Snooping of any SBU transaction other than LT_Fall or LT_LRoff starts this phase. The LRD ***may*** change its common-mode voltage after snooping a LT or RT transaction. The LRD ***shall*** meet Vdc+ac-conn if changing its common-mode voltage when measured into a 50 Ohm load. The common-mode voltage ramp ***shall*** complete in tLaneParams minimum defined in ***USB4*** V2 specification.

Note: Routers and Re-timers present terminations before transmitting LT or RT transactions.

TBT3 Legacy Requirements:

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1. Snooped LT transactions on SBU1:
    a. LT_Gen2 and LT_Gen3: Set fixed gain and equalization. It is ***optional*** for the gain and equalization to change based on the speed indication. Enable forwarding if not already enabled.
    b. LT_Resume: Enable forwarding if not already enabled.
2. Snooped Broadcast RT transactions on SBU1:
    a. ***USB4***: If the ***USB4*** bit is set to 1b, addressed RT transactions are used for link training.
    b. SelectGen: Set fixed gain and equalization. It is ***optional*** for the gain and equalization to change based on the speed indication.
    c. Lane0Enabled, Lane1Enabled: Enable forwarding if not already enabled. ***Optional*** to use LOS to enable forwarding.

USB4 Requirements:

1. Snooped Broadcast RT transactions on SBU1:
    a. ***USB4***: If the ***USB4*** bit is set to 1b, addressed RT transactions are used for link training.
    b. SelectGen: Set fixed gain and equalization. It is ***optional*** for the gain and equalization to change based on the speed indication.
    c. Lane0Enabled, Lane1Enabled: Enable forwarding if Enable3Tx or Enable3Rx are not enabled. The LRD ***shall*** enable forwarding in tLRDForward after snooping the Lane Enable. ***Optional*** to use LOS to enable forwarding.
    d. Enable3Tx: Enable three transmitters and one receiver as defined in Table 6-18. Enable forwarding after the LRD has switched direction within tLRDSwitch.
    e. Enable3Rx: Enable three receivers and one transmitter as defined in Table 6-18. Enable forwarding after the LRD has switched direction within tLRDSwitch.
2. Snooped Addressed RT transaction to SB Register Gen_4_TxFFE with Gen4TxFFE.Tx_Status_Byte.Start_TXFFE:
    a. If Gen4TxFFE.Tx_Status_Byte. Start_TXFFE (bit 7) =1b, the LRD ***may*** adjust its AGC in Phase 5.
    b. If Gen4TxFFE.Tx_Status_Byte.Start_TXFFE (bit 7) =0b, the LRD ***may not*** adjust its AGC in Phase 5.
    c. Note that the bytes in Gen4TxFFE.Tx_Status_Byte change if the link is initialized as an asymmetrical link. Refer to the ***USB4*** V2 specification for details.
3. Snooped addressed RT transaction to SB Register LRD_Tuning on SBU1:
    a. If LRD_Tuning.Force_Lane_Reversal=0b, use normal Lane1 and Lane2 operation relative to CC without changing the SBU1/2.
    b. If LRD_Tuning.Force_Lane_Reversal=1b, swap Lane1 and Lane2 without changing the SBU1/2. The lane reversal ***shall*** complete within tLRDSelfTune.

Phase 5: Link Equalization

Requirements (only applies to ***USB4*** Gen4):

1. Snooped addressed RT transaction to SB Register Gen_4_TxFFE:
    a. Partner_Tx_Status_Byte.Request_Done (bit 6)=1b is the indication to the LRD to start the AGC training in the SBU1 to SBU2 direction.

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b. The LRD active cable AGC ***shall*** complete it adjustments within tLRDSelfTune. If there are two LRDs in the cable, each ***may*** be adjusted independently but tLRDSelfTune ***shall*** be met for the cable assembly.

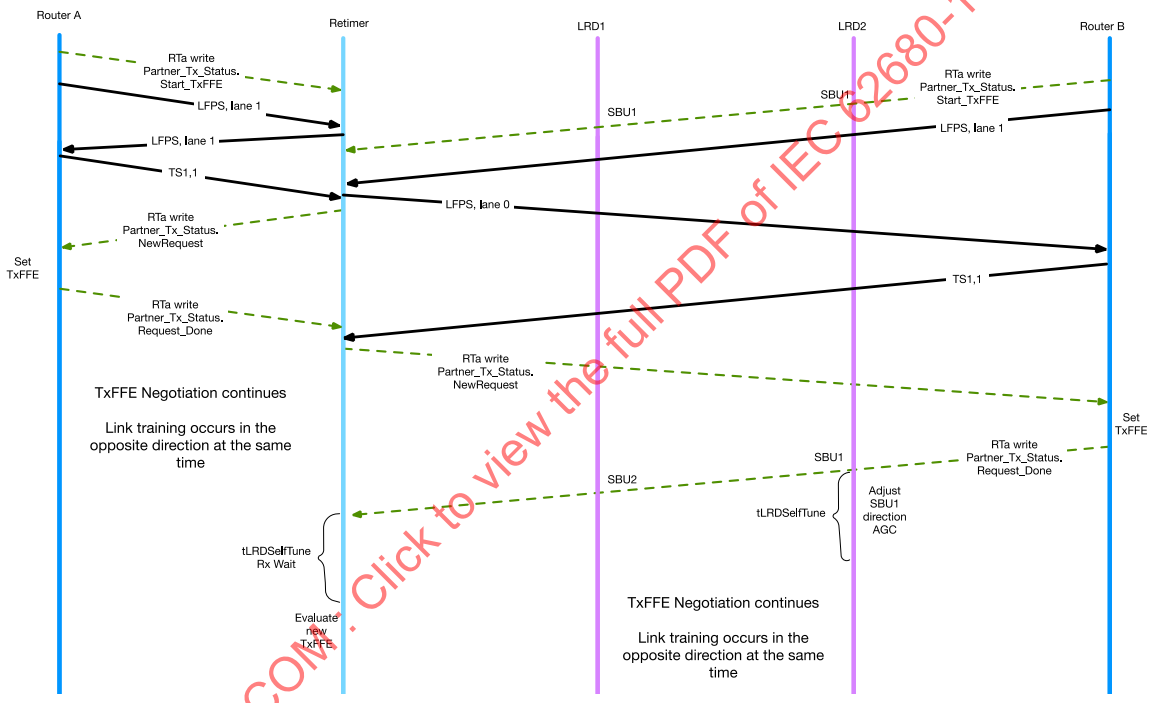
2. Snooped addressed RT transaction to SB Register LRD_Tuning on SBU1:

a. ***Optionally*** save the entire LRD_Tuning register. The LRD ***may optionally*** adjust its gain and equalization in a TBD way based on the contents of the register. The LRD ***shall*** complete its gain and equalization adjustment in tLRDSelfTune minimum time (***USB4*** V2 specification) when it snoops a write to LRD_Tuning.

An example of link training with LRD AGC adjustment is indicated in Figure 6-13.

Note: The LRD has no sideband indication of the switch from PAM2 to PAM3 and AGC and equalization training must function on both PAM2 and PAM3 incoming data.

Figure 6-13 *USB4* LRD Active Cable Snooping of TxFFE Negotiation



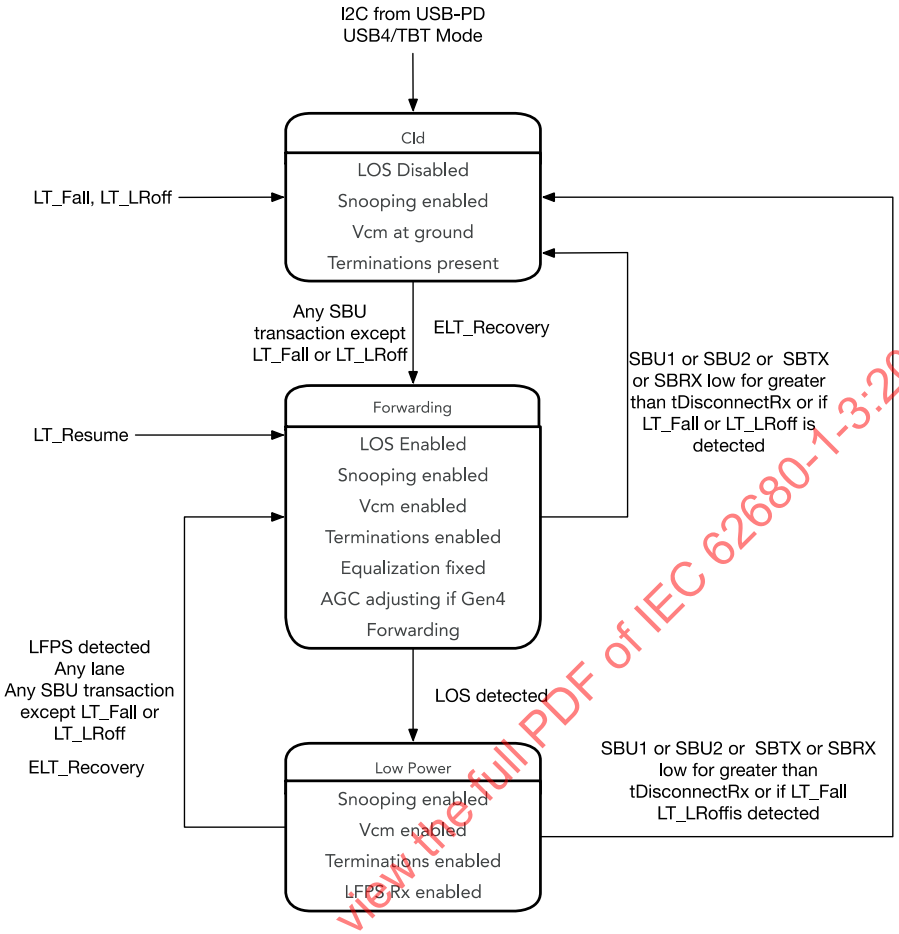
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6.1.2.5.4.16.4 *USB4* and *TBT3* Logical Layer State Machine (*Informative*)

The state machine in Figure 6-14 describes the behavior of the Logical Layer of the LRD(s) in the active cable. The state machine is per channel (i.e., per direction per lane).

- CLd State – the LRD is disabled but snooping for any traffic on SBU1 (and ***optionally*** SBU2)
- Forwarding State – the LRD is forwarding. The LRD snoops the link characteristics on the RT broadcast transactions and adjusts its AGC if Gen4 and enabled.
- Low Power State – reduced power state.

Figure 6-14 *USB4* State Machine per Channel (*Informative*)



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6.1.2.5.4.16.4.1 CLd State

Entry to State

The LRD ***shall*** enter this state on the following events:

- Entry to ***USB4/TBT3*** Alt mode being set from the ***USB PD*** Controller
- Snooping of LT_Fall or LT_LRoff transaction
- SBU1 or SBU2 low for greater than tDisconnectRx

Behavior in State

- LOS detector disabled.
- SBU1 (and ***optionally*** SBU2) ***shall*** be snooped for activity.
- The common mode voltage remains constant.
- The 50 Ohm terminations are present on all TX and RX.

Exit from State

- Transition to Forwarding State upon detection of SBU1 (and ***optionally*** SBU2) transaction which is not LT_Fall (per lane) or LT_LRoff (lane independent).

- Transition to Forwarding State upon detection of SBU1 (and ***optionally*** SBU2) ELT_Recovery.

6.1.2.5.4.16.4.2 Forwarding

Entry to State

The LRD ***shall*** enter this state on the following events:

- Any SBU1 (or ***optionally*** SBU2) transaction which is not LT_Fall or LT_LRoff
- After exiting Low Power state
- Snooping ELT_Recovery

Behavior in State

- Enable the LOS receiver.
- Snoop SBU1 (and ***optionally*** SBU2).
- Determine the direction of the lanes if ***USB4*** Gen4.
- Ramp the common mode voltage if needed as defined in the link training.
- Forward the high-speed data. Use the last known AGC setting if the transition was from Low Power or ELT_Recovery.
- Forward the high-speed data and adjust the AGC per Phase 4 and 5 Link training if Gen4.
- Forward the high-speed data and use the fixed stored AGC and EQ if Gen2 or Gen3.

Exit from State

- Transition to CLd on detection of low on SBU1 (or ***optionally*** SBU2) for greater than tDisconnectRx or upon snooping LT_Fall or LT_LRoff.
- Transition to Low Power if LOS is detected.

6.1.2.5.4.16.4.3 Low Power State

The low power state is used to conserve power in electrical idle.

Entry to State

- Transition to Low Power when detecting no high-speed signal on the Rx input.

Behavior in State

- Snoop SBU1 (and ***optionally*** SBU2).
- Common mode voltage ***shall*** be maintained.
- Terminations ***shall*** be maintained.
- Consume less power than in Forwarding.

Exit from State

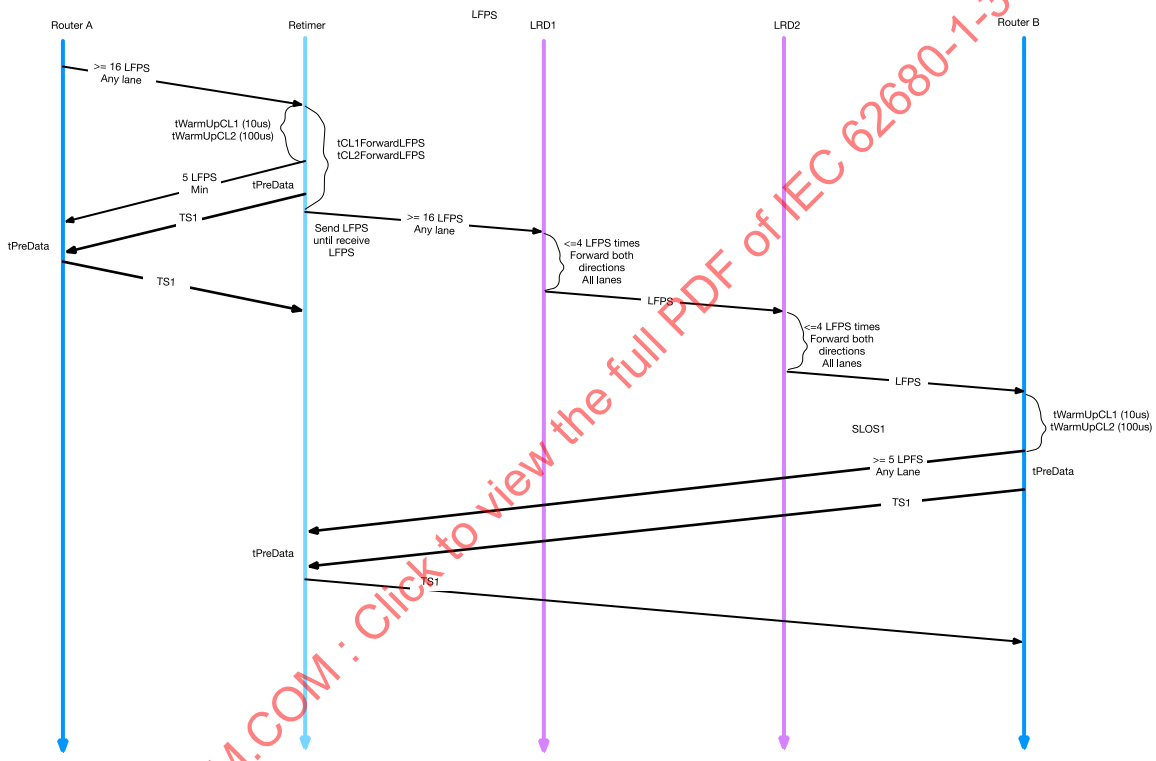
- Transition to Forwarding:
    - Detection of LFPS on any channel ***shall*** transition the LRD to Forwarding on the channel receiving the LFPS and the channel in the same lane in the opposite direction. Note that LFPS ***may*** be on only one channel (one lane in one direction) if the link is in CL0s.

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- The LRD active cable ***shall*** consume a maximum of eight LFPS when transitioning to Forwarding.
- The LRD ***shall not*** forward LFPS until it has enabled forwarding in both directions. Refer to Figure 6-15.
- Meet the electrical requirements when forwarding LFPS
- Snoop of ELT_Recovery

- Transition to CLd:
  - If SBU1 (or ***optionally*** SBU2) is low for greater than tDisconnectRx or if LT_Fall, or LT_LR_Off is detected.
  - The transmitter and receiver ***shall*** maintain the common-mode voltage and terminations.

Figure 6-15 *USB4* Gen4 CL1/CL2 Exit Flow with LRD Active Cable



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6.1.2.5.4.16.5 *USB4* Gen4 Symmetric to Asymmetric Transitions

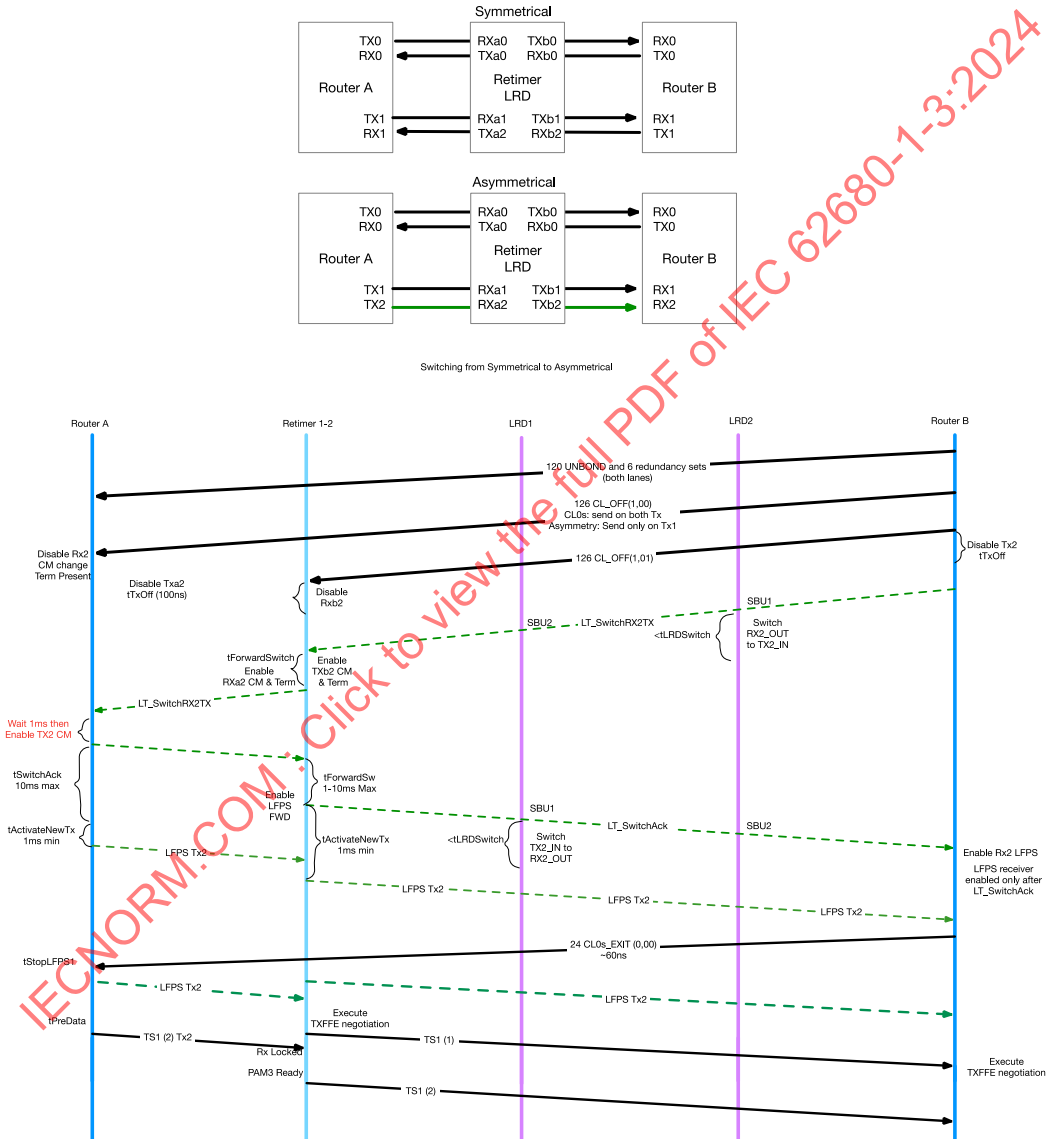
- Figure 6-16 provides an example of the Symmetric to Asymmetric flow for an LRD active cable.
- The LRD transitions from symmetrical to asymmetrical when it snoops the LT_SwitchRX2TX or LT_SwitchACK on SBU1.
- The LRD switches its RX2_OUT to a TX2_IN on receipt of the LT_SwitchRX2TX on SBU1.
- The LRD ***shall*** check for high-speed signal when receiving the LT_SwitchRX2TX. If high speed signal is detected by the LRD on the lane which will switch direction, the LRD ***shall*** wait for no high-speed signal and then perform the direction switch within tLRDSwitch. The LRD ***shall*** assume this is a transition to Asymmetrical because the previous state was Symmetrical.
- The LRD switches its TX2_Out to RX2_IN on receipt of the LT_SwitchACK on SBU1 within tLRDSwitch.

The LRD transmitter and receiver ***shall*** modify their common-mode voltage after receipt of the LT_SwitchRX2TX or LT_SwitchACK if needed. The transmitter and receiver ***shall not*** exceed the V_DC_AC_CONN during the transition assuming the far side termination present. The transmitter and receiver ***shall*** apply terminations after the common-mode voltage ramp if the termination was removed during the common-mode ramp.

- The LRD ***shall not*** forward LFPS until it has completed direction switching.

  Note that if no LT_SwitchACK is received within 1 second, the Link will disconnect by pulling SBTX low tDisconnectTx.

Figure 6-16 *USB4* Symmetric to Asymmetric Transition



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6.1.2.5.4.16.6 *USB4* Gen4 Asymmetric to Symmetric Transitions

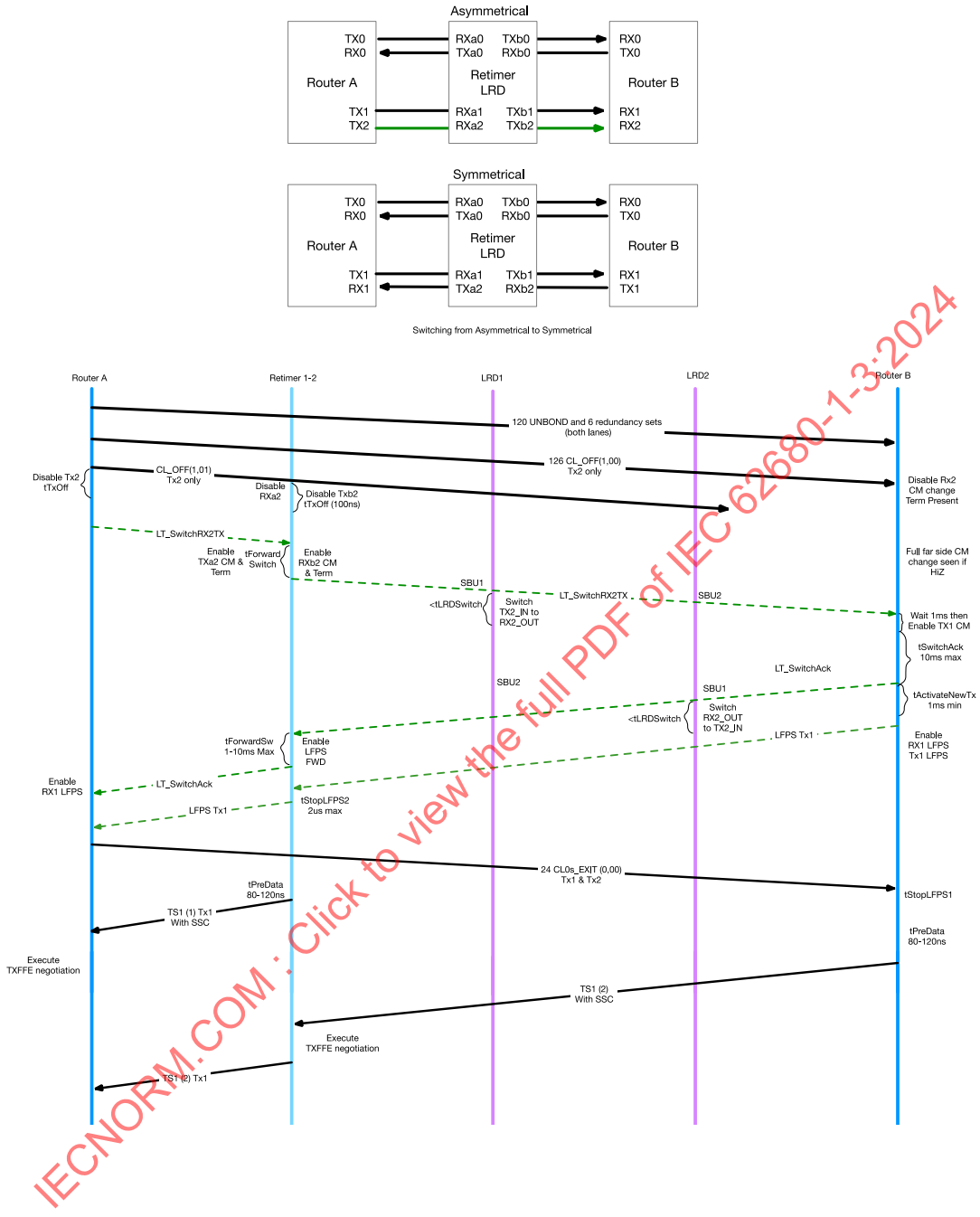
- Figure 6-17 provides an example of the Asymmetric to Symmetric flow for an LRD active cable.
- The LRD transitions from asymmetrical to symmetrical when it snoops LT_SwitchRX2TX or LT_SwitchACK on SBU1.
- The LRD switches its TX2_OUT to a RX_IN on receipt of the LT_SwitchRX2TX on SBU1.
- The LRD ***shall*** check for high-speed signal when receiving the LT_SwitchRX2TX. If high speed signal is detected by the LRD on the lane which will switch direction, the LRD ***shall*** wait for no high-speed signal and then perform the direction switch within tLRDSwitch. The LRD ***shall*** assume this is a transition to Symmetrical because the previous state was Asymmetrical.
- The LRD switches its RX2_Out to TX2_IN on receipt of the LT_SwitchACK on SBU1 within tLRDSwitch.

  The LRD transmitter and receiver ***may*** ramp their common-mode voltage after receipt of the LT_SwitchRX2TX or LT_SwitchACK if needed. The transmitter and receiver ***shall not*** exceed the V_DC_AC_CONN during the transition assuming the far side termination present. The transmitter and receiver ***shall*** apply terminations after the common-mode voltage ramp if the termination was removed during the common-mode ramp.
- The LRD ***shall not*** forward LFPS until it has completed direction switching.

  Note that if no LT_SwitchACK is received within 1s, the Link will disconnect by pulling SBTX low tDisconnectTx.

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Figure 6-17 *USB4* Asymmetric to Symmetric Transition



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6.1.2.5.4.17 Cable Compliance

The LRD in the active cable ***shall*** support snooping the LRD Tuning register as defined in Table 6-21. The Compliance Software only writes to the LRD Tuning Register if it needs to swap Lane1 and Lane2 in the active cable. The Compliance Software first writes to the Router LRD Tuning Register to set Force Lane Reversal=1b with Response Request=1b. The connected Router will then write to the LRD Turning register in the test equipment with the same Force Lane Reversal=1b with Response Request=0. This allows LRD active cables which only snoop SBU1 to snoop the LRD Tuning Register write on the cable plug farthest from the Compliance Software and test equipment.

The Compliance Software then writes to the LRD Tuning register to set Force Lane Reversal=1b with Response Request=0b to inform the local cable plug.

The active cable ***shall*** switch back to normal Lane1 and Lane2 operation on disconnect.

Table 6-21 *USB4* LRD Tuning Register Snooping

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
7	LRD Tuning	0	0	**Response Request** – When this bit is set to 1b, the ***USB4*** Port ***shall*** send a write Command to the LRD Tuning register in the adjacent Router/Re-timer. The write ***shall*** contain the values of the local LRD Tuning register and ***shall*** have the Response Request bit set to 0b. The ***USB4*** Port ***shall*** then set this bit to 0b.	R	0
			1	**Force Lane Reversal** – Identifies whether to override the functional Lane Reversal. 0b: Cable ***shall*** use normal Lane1 and Lane2 operation relative to CC 1b: Cable ***shall*** swap Lane1 and Lane2 Note: Sideband SBU1 and SBU2 ***shall*** remain in normal orientation regardless of the Force Lane Reversal setting.	R	0

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6.1.2.6 Return Loss

Return loss is defined in the ***USB 3.2*** specification.

6.1.3 Mechanical Requirements

All active cables ***shall*** meet the mechanical requirements defined in the Section 3.8.

6.1.3.1 Thermal Requirements

6.1.3.1.1 Thermal Shutdown

All active cables ***shall*** implement a temperature sensor and place the ***USB 3.2*** signals in the eSS.Disabled state when the plug skin temperature reaches the maximum defined in Table 6-22. Active cables ***shall*** indicate they are in thermal shutdown if queried via the ***USB PD Get_Status*** command.

The Thermal Shutdown is cleared by the following events:

- Disconnect, and
- ***USB PD*** Hard Reset.

6.1.3.1.2 Maximum Skin Temperature

Active cable plug's skin temperature ***shall not*** exceed a maximum operating temperature of 30 °C above the ambient temperature for a plastic/rubber housing and 15 °C for a metal housing in any operating mode, when measured at an ambient temperature of 25 °C.

The active cable ***shall*** meet this requirement when tested connected to a port with a motherboard temperature of (ambient + 25 °C).

6.1.3.1.3 Thermal Reporting

Active cables ***shall*** implement reporting their maximum internal operating temperature in the ***USB PD Discover_ID*** Command. Active cables ***shall*** implement reporting their current internal operating temperature in the ***USB PD Get_Status*** Command on SOP' and SOP" when supported. Active cables ***shall*** update their reported Internal Temperature at least every 500 ms.

The plug's Internal Temperature is reported in °C and ***shall*** be monotonic. It is not the plug's skin temperature, but cable manufacturers ***shall*** correlate the maximum internal operating temperature with the maximum plug skin temperature to ensure shutdown when the maximum plug skin temperature is reached.

Sources and/or Sinks ***may*** take action to reduce VBUS current to reduce the cable plug internal operating temperature to below the reported maximum operating temperature. It is recommended Sources and/or Sinks poll the plug's Internal Temperature every 2 seconds.

Table 6-22 Cable Temperature Requirements

Temperature Requirements	
Maximum Internal to Skin Temperature Offset	Design Specific
Maximum Internal Operating Temperature	Design Specific
Maximum Skin Temperature Plastic/Rubber[1]	Ambient + 30 °C
Maximum Skin Temperature Metal[1]	Ambient + 15 °C
Thermal Shutdown Skin Temperature Plastic/Rubber[2]	77 °C
Thermal Shutdown Skin Temperature Metal[2]	60 °C

Notes:
1. When connected to a port with a motherboard temperature that is set to ambient +25 °C.
2. Based on IEC 62368-1.

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6.1.3.2 Plug Spacing

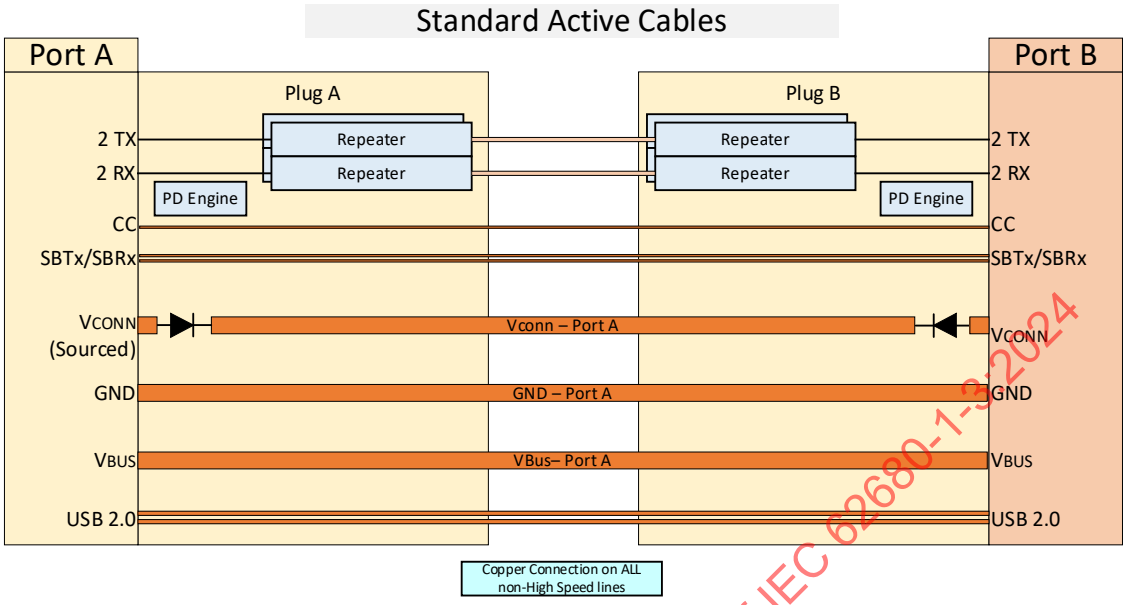
Active cables will support the USB Type-C vertical and horizontal spacing defined Section 3.10.2 when functioning in ***USB 3.2*** x1 operation. However, this spacing ***may*** impose thermal constraints. Appendix D provides system design guidance to minimize the thermal impact due to connector spacing. It is recommended that products designed for ***USB 3.2*** x2 operation with multiple adjacent USB Type-C connectors follow the design guidance in Appendix D to minimize the likelihood the active cable will go into thermal shutdown.

6.2 Additional Specifications for Copper and Hybrid-Optical Active Cables

Active cables include all active element cables including re-timer, re-driver, and hybrid optical-based cables. Hybrid Optical active cables use copper for power and low-speed data and optical for high-speed data.

Active cables minimally support ***USB 3.2*** Gen 2x2. ***USB4*** active cables support ***USB4*** as well as all ***USB 3.2*** rates. All ***USB4*** active cables ***shall*** be interoperable with ***Thunderbolt 3*** as defined in the ***USB4*** Specification.

6.2.1 Active Cable Block Diagram



6.2.2 *USB4* Asymmetric Mode Support

All ***USB4*** Gen4-capable Active Cables ***shall*** support ***USB4*** Asymmetric Mode. The only exception is for OIAC as defined in Section 6.3. This support ***shall*** be reported in the ***USB PD*** Active Cable VDO2 (Bit 1).

6.2.3 Active Cable *USB PD* Requirements

Active cables ***shall*** support ***USB PD*** Revision 3, Version 1.2 or later. Active cables ***shall*** support ***USB PD*** Structured VDMs.

6.2.3.1 SOP' and SOP" Requirements

SOP' and SOP" are fixed in the active cable at the time of manufacture. See Section 4.5.2.4.

Active cables ***shall*** respond to Discover_Identity and ***USB PD Get_Status*** on SOP'. When the SOP'' Controller Present bit is set in the Active Cable VDO, they ***shall*** respond ***USB PD Get_Status*** on SOP'' as well.

6.2.3.2 Cable Status

The ***USB PD Get_Status*** Command is used to discover the current state of the active cable. Cable status ***shall*** be reported on SOP' and ***shall*** also be reported on SOP" when the SOP'' Controller Presence bit is set in the Active Cable VDO.

6.2.4 Active Cable Behaviors in Response to *USB PD* Events

Each cable plug of the short active cable ***shall*** be capable of communicating on SOP' and SOP" if reported in the ***USB PD Discover_Identity*** Command.

6.2.4.1 Data Role Swap

Active cables are transparent to the ***USB PD*** Data Role swap.

6.2.4.2 Power Role Swap

Active cables ***shall*** maintain ***USB 3.2*** signaling during a ***USB PD*** Power Role swap. The source of VCONN is not affected by a Power Role Swap.

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6.2.4.3 VCONN Swap

Active cables ***shall*** maintain ***USB 3.2*** signaling during a ***USB PD*** VCONN swap. During a VCONN Swap, the original VCONN Source continues to supply VCONN for some time after the new VCONN Source begins to supply VCONN. This ensures that VCONN is never dropped.

6.2.4.4 Fast Role Swap

Active cables will drop ***USB 3.2*** signaling as a side-effect of a Fast Role Swap if VCONN is not maintained during the Fast Role Swap.

6.2.5 Active Cable Power Requirements

6.2.5.1 VBUS Requirements

Active cables ***shall*** meet the limits of the IR Drop on VBUS and ground defined in Section 4.4.1.

Active cables ***shall*** provide VBUS and support at least 3 A and ***optionally*** 5 A current.

6.2.5.2 VCONN Requirements

Active Cables ***shall***:

- Meet the VCONN sink requirement defined in Table 4-6, Table 6-6 (U-State Requirements) and Table 6-12 (CLx Requirements).
- Connect VCONN as shown in Sections 6.2.1.

Active cables ***shall*** meet the VCONN requirements specified in Section 4.9.

6.3 Additional Specifications for Optically Isolated Active Cables

Optically Isolated Active Cables (OIACs) key features are that they support longer lengths up to 50 meters and provide electrical isolation between the two ends of the cable.

This specification defines support for the following OIACs:

- ***USB 3.2*** Gen2
- ***USB4*** Gen3 (***USB 3.2*** Gen2, ***USB4*** Gen2, ***TBT3***, and ***USB4*** Gen3)
- ***USB4*** Gen4 (***USB 3.2*** Gen2, ***USB4*** Gen2, ***TBT3***, ***USB4*** Gen3, ***USB4*** Gen4)

They are targeted for Industrial, Machine Vision, Remote Sensor, Pro Video, and Medical applications.

Since no power runs through an OIAC, VCONN must be provided from both ends and ***USB PD*** is required to correctly setup DFP-UFP link. Therefore, an OIAC can only be used to connect a Source DRD to a Source DRD or a Source DRD to a DFP, and at least one of the Sourcing DRDs must start out as a Sourcing DFP and ACCEPT a ***DR_Swap*** request to a UFP. ***USB PD*** Revision 3.0 or higher must be supported on both port partners for an OIAC to function. These requirements are detailed in Section 6.3.2.2 and 6.3.2.3.

OIACs have additional limitations on systems, even when a viable High Speed link has been established, including but not limited to some power saving modes, and features that require ***Alternate Modes*** or ***USB 2.0***, which are not supported by the OIAC. Additional system limitations are defined in Section 6.3.2.

If a connection to a ***USB 2.0*** Device is required at the end of an OIAC, an adapter with a ***USB 3.2*** to ***USB 2.0*** transaction translator and VBUS/VCONN Source ***may*** be connected at the Device side of the cable to convert the ***USB 3.2*** signals to ***USB 2.0*** and provide power to the ***USB 2.0*** Device and the OIAC.

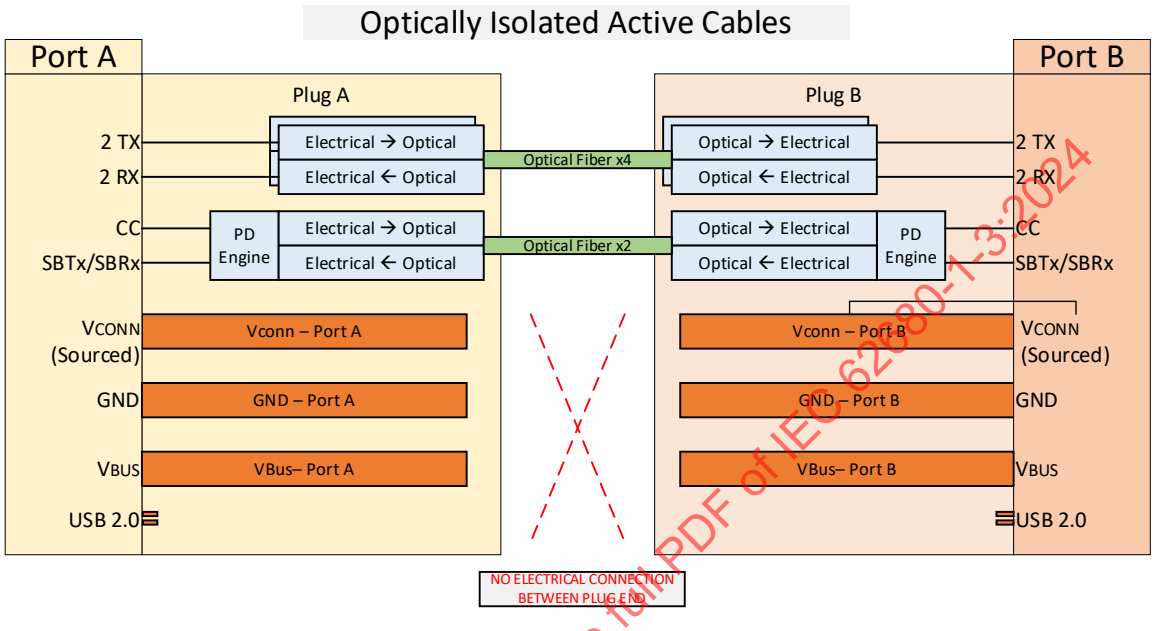
OIACs ***may optionally*** support other ***Alternate Modes***. If an OIAC supports ***Alternate Modes*** that require the use of SBUs, the SBUs ***shall*** be optically isolated.

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6.3.1 OIAC Block Diagrams

OIACs can be implemented in different ways. This section provides one possible implementation example for the ***USB 3.2*** and the corresponding ***USB4*** example. Other implementations can be used, as long as the all the electrical plug specification and characteristics are the same.

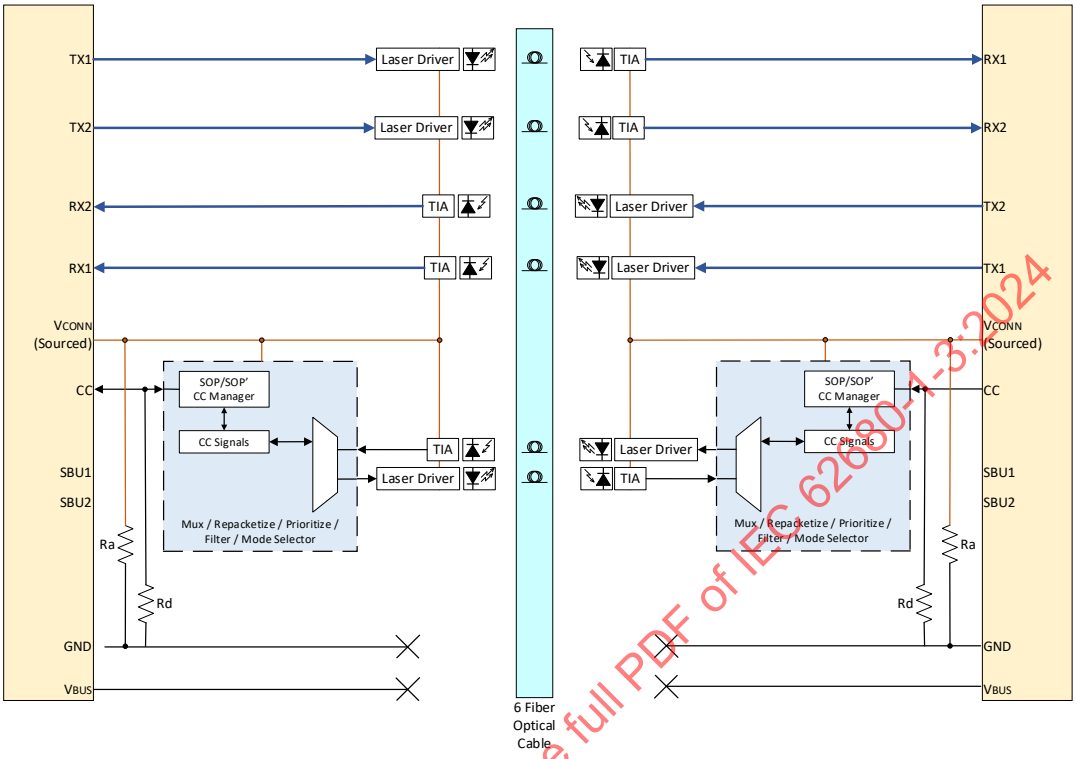
6.3.1.1 Simplified Optically Isolated Active Cable (OIAC) Block Diagram



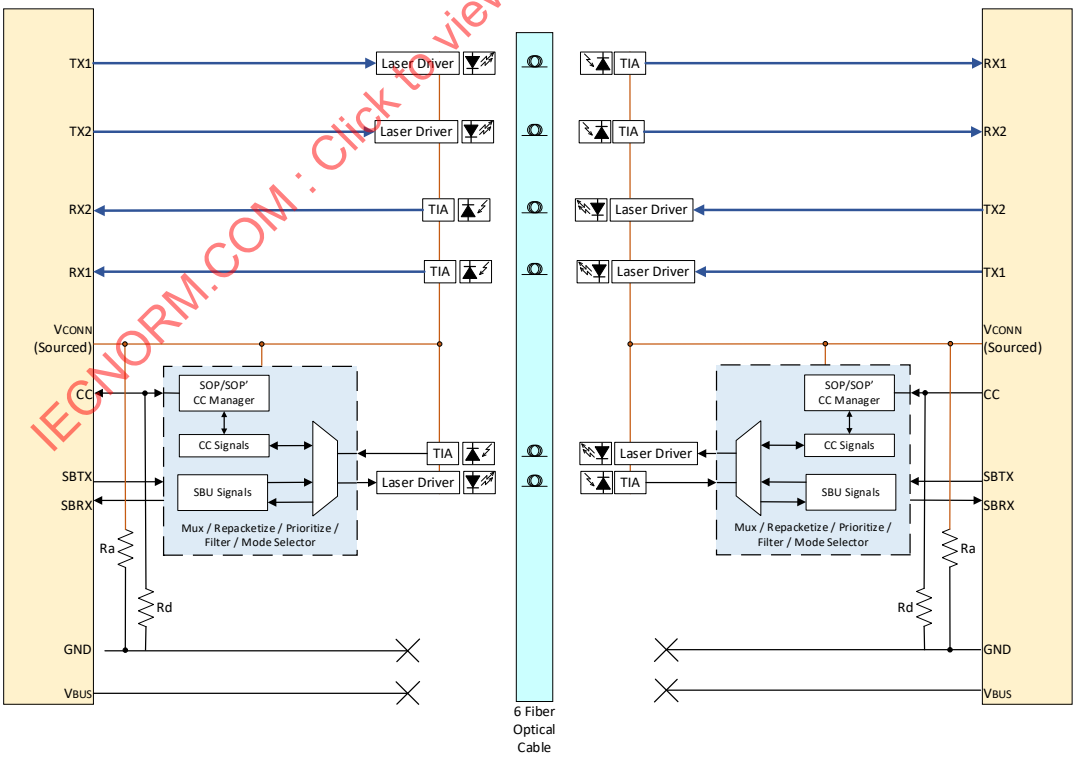
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6.3.1.2 Example – Detailed OIAC Block Diagram – *USB 3.2* Gen2

In this example, SBU lines are unused unless directed to enter an ***Alternate Mode***.



6.3.1.3 Example – Detailed OIAC Block Diagram – *USB4* Gen3/Gen4 Block Diagram



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6.3.2 OIAC Limitations and General Requirements

6.3.2.1 Limitations of OIAC versus Active Cable

The Optically Isolated Active Cable (OIAC) ***shall not*** have any electrical wires running between the two plug ends. There are no electrical wires for VBUS, VCONN, GND, SBx, or ***USB 2.0***.

VBUS, VCONN, and GND are completely isolated on each end of the cable, which means that the host/device must be both self-powered and supply VCONN to the OIAC.

The following features are ***optional***:

- ***DP Alternate Mode***.
- ***USB 2.0***.
- ***USB PD*** Unchunked Messages.
- For ***USB4*** Gen4 OIAC, ***USB4*** Asymmetric Mode.

Cable VCONN CLd/U3 Power Requirement: The OIAC does not reduce the power requirement on VCONN during the CLd/U3 power state. The power consumption for VCONN power @ CL3/U3 ≤ power at CL0/U0. Additional details are in Section 6.3.6.4.3 and Section 6.3.6.5.2.

The above limitations of the OIAC force additional requirements on the Host / Device connected to the OIAC, including be not limited to both VCONN and ***USB PD*** being required on each end of the cable. Additional requirements for the Host and Device and listed in Section 6.3.2.2 and Section 6.3.2.3.

6.3.2.2 Host Requirements

All USB certified hosts ***should*** meet all the requirements to support an OIAC.

However, the minimum requirements are listed here:

1. Source VCONN.
2. Support ***USB PD***.
3. Initialize as a Sourcing DFP.
4. Dual Role Data (*).

(*) Conditional Requirement: In the scenario where the Host and OIAC is connected to Dual Role Data (DRD) Host/Device, at least one of the two (the Host on the near end or Host/Device on the far end) must be able to accept a ***DR_Swap*** when requested. If both ends "***Reject***" (or continuously respond with "***Wait***") then the DFP-UFP link cannot be created, and a USB link will not be established.

6.3.2.3 Device Requirements

There are more device requirements to use an OIAC and a standard USB device. This is because the OIAC does not have a VBUS wire connecting the DFP and the UFP.

The device will need the meet all the following requirements:

1. Source VCONN.
2. Support ***USB PD***.
3. Initialize as a Sourcing DFP.
4. Dual Role Data (*).

(*) Conditional Requirement: In the scenario where the Device and OIAC is connected to Dual Role Data (DRD) Host/Device, at least one of the two (the Device on the near end or Host/Device on the far end)

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must be able to accept a ***DR_Swap*** when requested. If both ends "***Reject***" (or continuously respond with "***Wait***") then the DFP-UFP link cannot be created, and a USB link will not be established.

Note: It is expected that the Device is a DRD Device that can support a ***DR_Swap*** request to a UFP.

6.3.2.4 Additional Limitations with using an OIAC with a Downstream Device (Dock/Hub/Device)

Assuming a ***USB4*** (or ***USB 3.2***) link is established using an OIAC, some features that are normally available with a USB Type-C Full Featured Copper Cable ***may not*** be fully supported in the link including the following:

- Downstream ***USB 2.0*** ports:

  Downstream ***USB 2.0*** ports will not work on a Dock/Hub/Device connected via an OIAC unless the OIAC implements proprietary support for ***USB 2.0***.

- Downstream ***Alternate Modes*** ports:

  Alternate Modes (e.g., ***Thunderbolt 3***, ***DP***) are only supported if the OIAC implements the mode.

6.3.3 OIAC Cable Power Requirements

6.3.3.1 VBUS Requirements

There are no VBUS wires across an OIAC.

6.3.3.2 VCONN Requirements

There is no VCONN wire between the two ends of an OIAC, therefore it is possible for each OIAC plug to consume the entire 1.5 W allocated to VCONN from each port. However, the OIAC must meet all thermal and mechanical requirements of the USB Type-C Active Cable.

OIAC ***shall***:

- Meet the VCONN sink requirement defined in Table 4-6, Table 6-6 (U-State Requirements) and Table 6-12 (CLx Requirements).
- Connect VCONN as shown in Section 6.3.1.

OIAC ***shall*** meet the VCONN requirements specified in Section 4.9.

6.3.3.3 OIAC Power Contract

While OIAC does not have VBUS going through the cable, each OIAC cable plug will have a power contract with their respective ports. This is required for any ***USB PD*** communication, which is needed for the OIAC to properly initialize.

The recommended power contract response for the OIAC is detailed in Section 6.3.4.3.2.1.2.

6.3.4 OIAC *USB PD* Requirements

OIACs ***shall*** support ***USB PD*** Revision 3, Version 1.6 or later. OIACs ***shall*** support ***USB PD*** Structured VDMs.

OIAC ***may*** support Unchunked Messages.

6.3.4.1 SOP' and SOP" Requirements

OIAC ***shall*** respond to ***USB PD Discover_Identity*** and ***USB PD Get_Status*** of SOP'.

SOP" controller is not required in the OIAC, however, a ***USB PD Get_Status*** of SOP' will respond with Thermal Shutdown and temperature information of the worst case of both cable ends. The OIAC will need to internally communicate thermal information between the plug ends and provide that information in the SOP' response.

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OIACs will always have SOP' at the near end and SOP" is the far end with respect to each port. This differs from other Active Cables where SOP' and SOP" are predefined.

6.3.4.2 *USB4* Asymmetric Mode Support

USB4 Gen4-capable OIAC ***may optionally*** support ***USB4*** Asymmetric Mode. This support ***shall*** be reported in the ***USB PD*** Active Cable VDO2 (Bit 1) response.

6.3.4.3 *USB PD* Message Handling

Table 6-23 OIAC *USB PD* Message Handling

Received Message	Local OIAC Plug Response (Sink)
Resets	
Cable Reset	Specified in Section 6.3.4.3.1
Hard Reset	Specified in Section 6.3.4.3.1
Soft Reset	Specified in Section 6.3.4.3.1
Data Reset	Specified in Section 6.3.4.3.1
Locally Handled Messages	
Get_Sink_Capabilities	Specified in Section 6.3.4.3.2.1.1
Source_Capabilites	Specified in Section 6.3.4.3.2.1.2
PR_Swap	Reject (Section 6.3.4.3.2.2)
FR_Swap	Reject (Section 6.3.4.3.2.2)
VCONN_Swap	Reject (Section 6.3.4.3.2.2)
Get_Source_Capabilities	Not Supported (Section 6.3.4.3.2.3)
Get_Source_Capabilites_Extended	Not Supported (Section 6.3.4.3.2.3)
EPR_Get_Source_Capabilities	Not Supported (Section 6.3.4.3.2.3)
EPR_Get_Sink_Capabilites	Not Supported (Section 6.3.4.3.2.3)
BIST	Specified in Section 6.3.4.3.2.4.1
GoodCRC	Specified in Section 6.3.4.3.2.4.2
PS_RDY	Specified in Section 6.3.4.3.2.4.2
GotoMin	Ignore (Section 6.3.4.3.2.4.3)
Conditionally Handled Messages	
Accept	Specified in Section 6.3.4.3.3.1
Reject	Specified in Section 6.3.4.3.3.2
Wait	Specified in Section 6.3.4.3.3.3
All other *USB PD* Message *shall* be allowed to traverse the OIAC	

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6.3.4.3.1 *USB PD* Reset (Hard, Cable, Soft, Data)

All Resets (Cable, Hard, Data, Soft) will be handled the same by the OIAC and all be treated as Hard Reset, which resets VCONN.

For Hard (or Cable) Reset, an OIAC plug ***shall***:

1. Detect the Hard (or Cable) Reset ordered set,
2. Forward "disconnect event" to the remote plug, and
3. Remove ***Rd***.

For Data (or Soft) Reset, an OIAC plug ***shall***:

1. Detect the Data (or Soft) Reset Message,
2. Forward “disconnect event” to the remote plug, and
3. Remove ***Rd***.

At the Remote OIAC Plug:

1. Receive “disconnect event”, and

   Note: Forwarding a “disconnect event,” to the remote plug can be accomplished with a simple internal message or any other means the implemented decides.

2. Remove ***Rd***.

A Hard Reset signal can occur at any time during normal operation of the cable and during the cable initialization. This signal will take precedent over the initialization state machine and immediately forward the Hard Reset Message to the remote plug, using an internal cable message.

6.3.4.3.2 Locally-Handled SOP *USB PD* Messages Received by the OIAC Plug

6.3.4.3.2.1 Specific Responses From the Local OIAC Plug

6.3.4.3.2.1.1 Get_Sink_Capabilities

The OIAC plug ***shall*** respond to this message directly and the suggested response is defined in Table 6-24 and Table 6-25 depending on which phase of the link bring up the OIAC is currently in.

Table 6-24 Recommended OIAC Sink_Capabilities PDO (SOP) on Initial Connection

Bit(s)	Value	Parameter
B31..30	00b	Fixed Supply
B29	0b	Not Dual-Role Power
B28	0b	Not higher capability
B27	0b	Not unconstrained power
B26	1b	USB Communications Capable
B25	0b	Dual-Role Data
B24..23	00b	Fast Role Swap not supported
B22..20	000b	***Reserved***
B19..10	00 0110 0100b	5V in 50mV units
B9..0	00 0000 0000b	Operational current in 10mA units

Table 6-25 Recommended OIAC Sink_Capabilities PDO (SOP) on Active Connection

Bit(s)	Value	Parameter
B31..30	00b	Fixed Supply
B29	0b	Not Dual-Role Power
B28	0b	Not higher capability
B27	0b	Not unconstrained power
B26	1b	USB Communications Capable
B25	As reported from Remote End	Dual-Role Data[1]
B24..23	00b	Fast Role Swap not supported
B22..20	000b	***Reserved***
B19..10	00 0110 0100b	5V in 50mV units
B9..0	00 0000 0000b	Operational current in 10mA units
Note 1: Reflection of far side connection.		

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6.3.4.3.2.1.2 Source_Capabilities

A recommended Sink RDO is provided as an example in Table 6-26 is the same for both the initial connection and when the OIAC is in normal active mode.

The OIAC ***shall*** function when receiving the minimum Source PDO and the OIAC plug will request 5 V at 0 mA.

Table 6-26 Recommended OIAC Active Sink RDO (SOP)

Bit(s)	Value	Parameter
B31	0b	***Reserved***
B20..28	0 0000 0001b	Object Position
B27	0b	No GiveBack flag
B26	0b	No Capabilities Mismatch
B25	1b	USB Communication Capable
B24	1b	USB Suspend
B23	0b	Unchunked Extended Messages
B22..20	000b	***Reserved***
B19..10	0b	Operating Current in 10 mA units[1]
B9..0	0b	Maximum current in 10 mA units[1]
Note 1: Thermal design must be considered.		

6.3.4.3.2.2 "Rejected" Response From the Local OIAC Plug

The OIAC does not have any copper wires, therefore must supply power from each end independently, which makes any type of power swapping not possible. The following messages ***shall*** be intercepted by the OIAC and responded with a "***Reject***."

- ***PR_Swap***.
- ***FR_Swap***.
- ***VCONN_Swap***.

6.3.4.3.2.3 "Non Supported" Response From the Local OIAC Plug

Since the OIAC acting as sink (that must be powered by the local port) on both ends of the cable the following messages are not applicable. The OIAC ***shall*** respond with a "Not Supported."

- ***Get_Source_Cap***.
- ***Get Source_Cap Extended***.
- ***EPR_Get_Source_Cap***.
- ***EPR_Get_Sink_Cap***.

6.3.4.3.2.4 Handled/Ignored by the Local OIAC Plug

6.3.4.3.2.4.1 BIST

BIST is a function that needs to be supported by the OIAC plug. The BIST message from the port ***should*** be intercepted and completely handled by the OIAC plug.

6.3.4.3.2.4.2 GoodCRC, PS_RDY

Both messages, GoodCRC and PS_RDY are confirmation messages that the previous message was successful. They just need to terminate in the OIAC plug.

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6.3.4.3.2.4.3 GotoMin

GotoMin is a message that will just be completely ignored by the OIAC. As this ***should*** have no effect but is required to be terminated in the plug.

6.3.4.3.2.4.4 Soft Reset, Data Reset

See Section 6.3.4.3.1.

6.3.4.3.3 Conditional Response Messages

6.3.4.3.3.1 Accept

The ***Accept*** Message is a Valid response to only the following messages: ***Request***, ***EPR_Request***, ***PR_Swap***, ***DR_Swap***, ***VCONN_Swap***, ***FR_Swap***, ***Soft_Reset***, and ***USB PD Enter_USB***.

The OIAC, as the Sink, will never initiate any type of Power Swap or EPR request, therefore, an ***Accept*** response from the Source for those messages (***EPR_Request***, ***PR_Swap***, ***VCONN_Swap***, ***FR_Swap***) ***should*** never occur.

Soft_Reset will be handled as a reset case and is defined in Section 6.3.4.3.1. There ***should*** never be an ***Accept*** message following a ***Soft_Reset***.

A ***Request*** Message can and will initiate from the OIAC, so an ***Accept*** following that ***Request*** message will need to be processed within the OIAC plug and will not need to traverse the OIAC.

Both a ***DR_Swap*** and ***USB PD Enter_USB*** message can initiate from either end of the OIAC, and therefore ***may*** require an ***Accept*** message to traverse the OIAC.

6.3.4.3.3.2 Reject

The ***USB PD Reject*** message is a Valid response to only the following messages: ***USB PD Request***, ***EPR_Request***, ***PR_Swap***, ***DR_Swap***, ***VCONN_Swap***, and ***Enter_USB***.

The OIAC, as the Sink, will never initiate any type of Power Swap or EPR request, therefore, a ***Wait*** response from the Source for those messages (***EPR_Request***, ***PR_Swap***, ***VCONN_Swap***) ***should*** never occur.

A ***Request*** Message can initiate from the OIAC, so a ***Reject*** following that ***Request*** message will need to be processed within the OIAC plug and ***should not*** need to traverse the OIAC.

Both a ***DR_Swap*** and ***USB PD Enter_USB*** message can initiate from either end of the OIAC, and therefore ***may*** require a ***Reject*** message to traverse the OIAC.

6.3.4.3.3.3 Wait

The ***Wait*** Message is a Valid response to only the following messages: ***Request***, ***EPR_Request***, ***PR_Swap***, ***DR_Swap***, ***VCONN_Swap***, and ***USB PD Enter_USB***.

The OIAC, as the Sink, will never initiate any type of Power Swap or EPR request, therefore, a ***Wait*** response from the Source for those messages (***EPR_Request***, ***PR_Swap***, ***VCONN_Swap***) ***should*** never occur.

A ***Request*** Message can initiate from the OIAC, so a ***Wait*** following that ***Request*** message will need to be processed within the OIAC plug and ***should not*** need to traverse the OIAC.

Both a ***DR_Swap*** and ***USB PD Enter_USB*** message can initiate from either end of the OIAC, and therefore ***may*** require a ***Wait*** message to traverse the OIAC.

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6.3.4.3.4 Other *USB PD* Messages

6.3.4.3.4.1 Get Status SOP'

OIACs are not required to support SOP", however, when reporting to a ***USB PD Get_Status*** message, the OIAC must provide accurate temperature information on the worst case of either cable plug, the higher temperature reading. And it must provide thermal shutdown information of either cable plug.

6.3.4.3.5 Messages That Traverse the OIAC

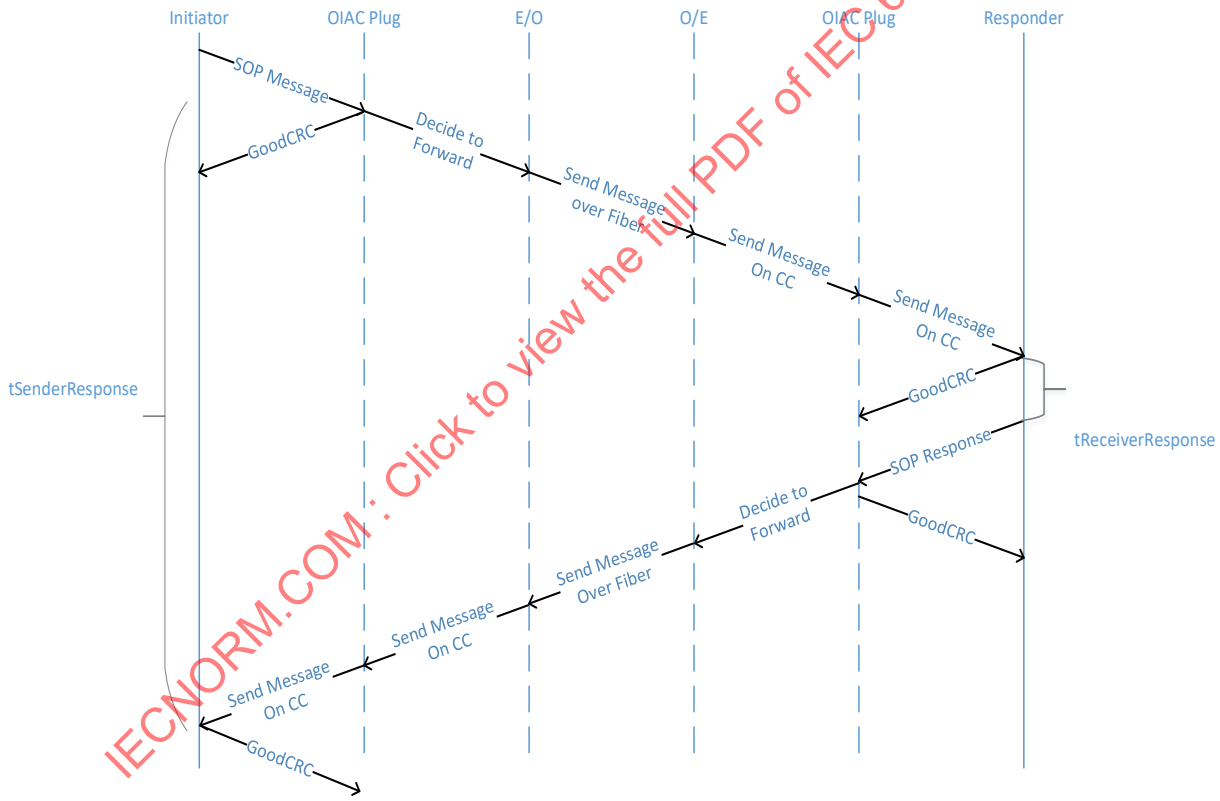
All other ***USB PD*** messages that are not listed in above section are considered "Generic" and will allowed to traverse the OIAC.

6.3.4.3.6 OIAC Cable Status

The ***USB PD Get_Status*** Command is used to discover the current state of the active cable. Cable status ***shall*** be reported on SOP'.

6.3.4.3.7 OIAC *USB PD* Message Forwarding Timing

Figure 6-18 OIAC *USB PD* Message Forwarding



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Table 6-27 OIAC *USB PD* Message Timing

Timer	Value (Min)	Value (Max)	Units	Reference
tDRSwapWait	100		ms	Time to wait if WAIT received before sending another ***DR_Swap***. Defined in the ***USB PD*** Specification.
tForward		4	ms	Time to forward SOP Message one direction in OIAC.
tTransmit		195	µs	Time to send the GoodCRC. Defined in the ***USB PD*** Specification.
tInterFrameGap	25		µs	Time from the end of the last bit of a Frame until the start of the first bit of the next Preamble. Defined in the ***USB PD*** Specification.
tReceiverResponse		15	ms	Time for SOP Receiver to respond. Defined in the ***USB PD*** Specification.
tSenderResponse	27	33	ms	Time for SOP Initiator to receive response. Defined in the ***USB PD*** Specification.
tBootupCRCHoldoff		50	ms	Hold off on GoodCRC until ready to respond with Operational RDO in Phase 3.

Note: The ***USB PD*** specification revision ***shall*** take precedence over this table if any discrepancies exist.

6.3.4.3.8 Internal Cable Messages

All SOP messages ***shall*** be forwarded or terminated as defined in Sections 6.3.4.3.1 and 6.3.4.3.3, and will not be further described in this section.

The messages defined in this section provide ***informative*** guidance on internal messages for OIACs. The actual definition and implementation of each message is left to the implementer.

In this section and Section 6.3.1, there is a defined Plug-A and Plug-B to support ***USB PD*** communication through the OIAC cable. These designations are established at the time of manufacture and are completely internal to the cable. They are used to simplify cable initialization and internal messaging.

6.3.4.3.8.1 MSG_Keep_Alive (*Informative*)

A low duty cycle message that is meant to inform the remote cable plug that the local cable plug is still operational.

A simple example is that only Plug-A will send MSG_Keep_Alive and Plug-B must respond with MSG_Keep_Alive_ACK. Each end will have its own timeout for MSG_Keep_Alive and MSG_Keep_Alive_ACK.

6.3.4.3.8.2 MSG_Keep_Alive_ACK

Acknowledgement message to the MSG_Keep_Alive.

A simple example is that only Plug-A will send MSG_Keep_Alive and Plug-B must respond with MSG_Keep_Alive_ACK. Each end will have its own timeout for MSG_Keep_Alive and MSG_Keep_Alive_ACK.

6.3.4.3.8.3 MSG_Port_Capabilities

This message contains all relevant local port capabilities including but not limited to:

- Chunked/Unchunked capability, and
- DRD/DFP/UFP capabilities.

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6.3.4.3.8.4 MSG_Cable_Config

This message contains the final cable configuration based on known system capabilities.

It will contain both relevant ports' capabilities and the final DFP/UFP roles for the system.

This message will also serve as the signal in Phase 2 for the cable plug to start the reboot process.

6.3.4.3.8.5 MSG_Release_Remote_SourceCap_GoodCRC

This is a synchronization message to attempt to bring up both ports at the same time.

It is used in Phase 3 and is the signal to release the GoodCRC message to the Source Capabilities message from the attached port. At the beginning of Phase 3, after each plug has been rebooted, and depending on the final DFP/UFP role, each plug ***should*** wait for MSG_Release_Remote_SourceCap_GoodCRC before it is allowed to release a GoodCRC in response to a Source_Capabilities message from the port.

6.3.4.3.8.6 MSG_DR_Swap_Init

Initial ***DR_Swap*** sent by Plug-A to Plug-B to perform a ***DR_Swap***.

6.3.4.3.8.7 MSG_DR_Swap_Reject

Plug-B sends this message to report that the initial ***DR_Swap*** was rejected by its attached port.

This is needed by Plug-A to attempt to re-configure the cable such that the port associated to Plug-B can remain a DFP. This is part of the ***DR_Swap*** test in Phase 1, shown in the state diagram transition from M3 to M4 (or M3 to M5). It is also possible that this ***may*** be needed in Phase 3, if the port associated with Plug-B rejects the ***DR_Swap***.

6.3.4.3.8.8 MSG_DR_Swap_Accept

Plug-B sends this message to report that the initial ***DR_Swap*** was accepted by its attached port.

This is needed by Plug-A to continue (M3 to M6 transition) in Phase 1 in the cable initialization.

6.3.4.3.8.9 MSG_Force_Detach

This message is to request the remote plug to disconnect from its attached port. The disconnect method can be done by raising the voltage on the CC line to above ***vRd-Connect*** or removing ***Rd***.

This will cause the remote port to remove VCONN from the remote plug all the circuitry ***should*** be powered down, therefore resetting any action taken by the plug on the CC line to cause the disconnect.

6.3.4.3.8.10 MSG_Reset

This message is to forward a Hard_Reset signal to the remote plug and port.

An internal Hard Reset message ***should*** be responded to with an Acknowledgement.

6.3.4.3.8.11 MSG_Acknowledgement

This message is to acknowledge that a message was received.

This message has been explicitly defined in a few specific cases but can be used more broadly.

6.3.4.3.9 Data Role Swap in Active State (*Informative*)

OIACs ***shall*** support Data Role Swaps on SOP. Each OIAC plug discovers its plug port partner and determines if it is capable of a Data Role Swap during the initialization process described in Section 6.3.5. OIAC cable

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plugs generate internal messages to communicate the ***DR_Swap***, ***Accept***, ***Reject***, and ***Wait*** to the far side of the cable.

- The flow of a successful ***DR_Swap*** is shown in Figure 6-19.
- The flow of a Responder rejecting a ***DR_Swap*** is shown in Figure 6-20.
- The flow of a Responder issuing a ***Wait*** to a ***DR_Swap*** is shown in Figure 6-21. Note: The ***USB PD Wait*** and Retry timers ***shall*** follow all timing requirements in ***USB PD***.
- The flow of an Initiator rejecting a cable plug ***DR_Swap*** due to an ***Accept*** from the Responder is shown in Figure 6-22.
- The flow of an Initiator issuing a ***Wait*** to a cable plug ***DR_Swap*** due to an ***Accept*** from the Responder is shown in Figure 6-23. Note: This does not follow the ***USB PD Wait*** timing, because a Hard Reset is initiated.

Figure 6-19 OIAC Successful Data Role Swap

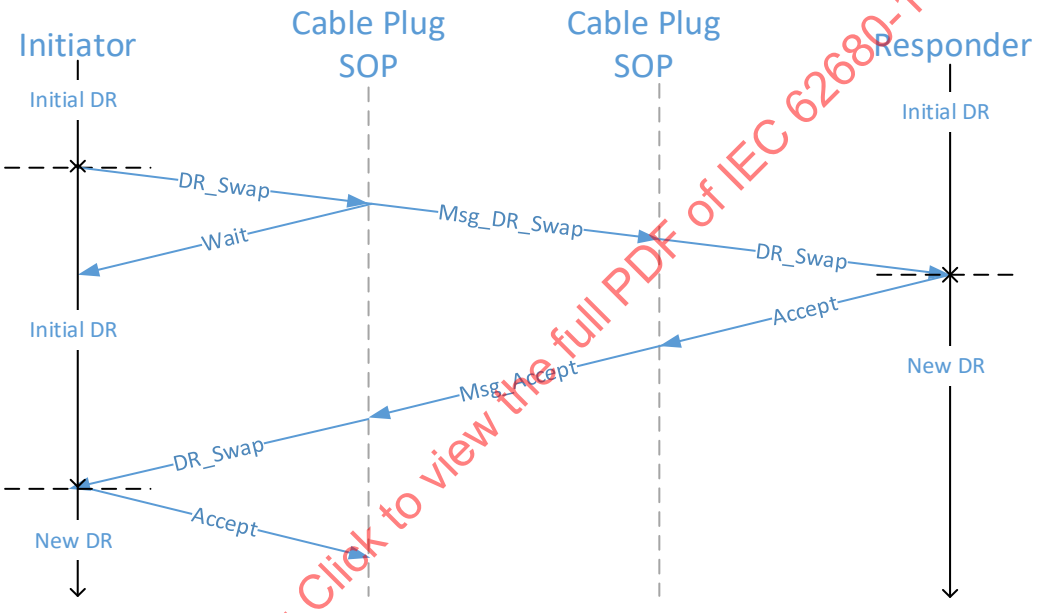
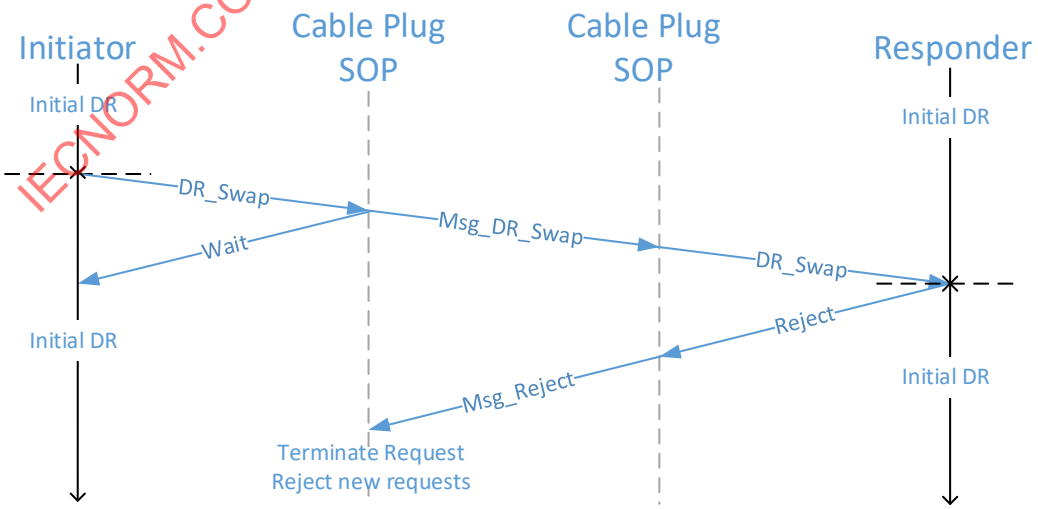


Figure 6-20 OIAC Rejected Data Role Swap



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Figure 6-21 OIAC Wait Data Role Swap

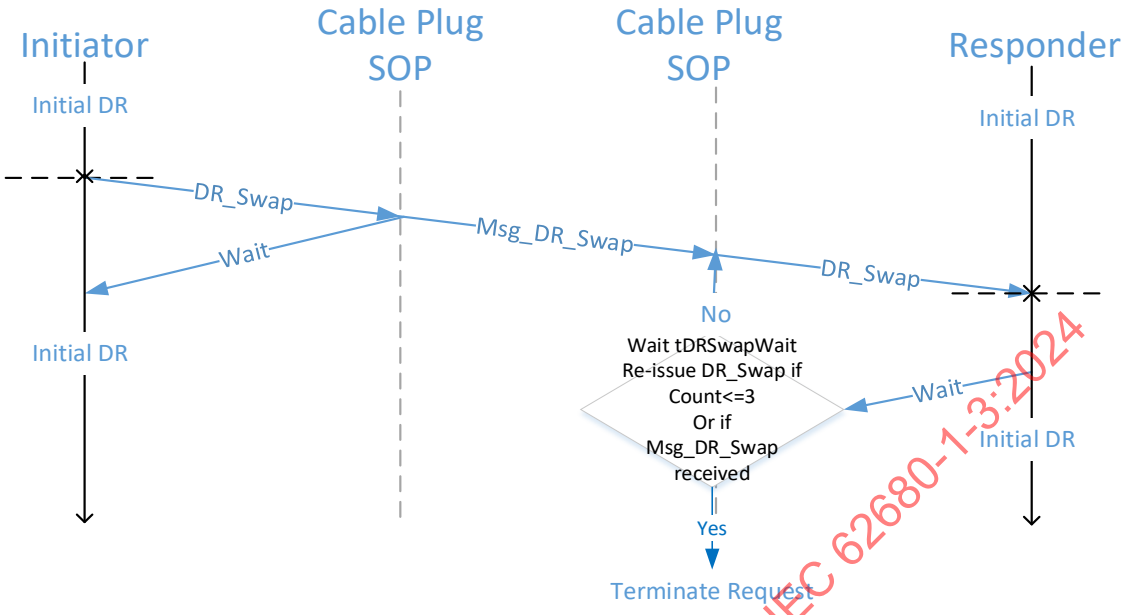
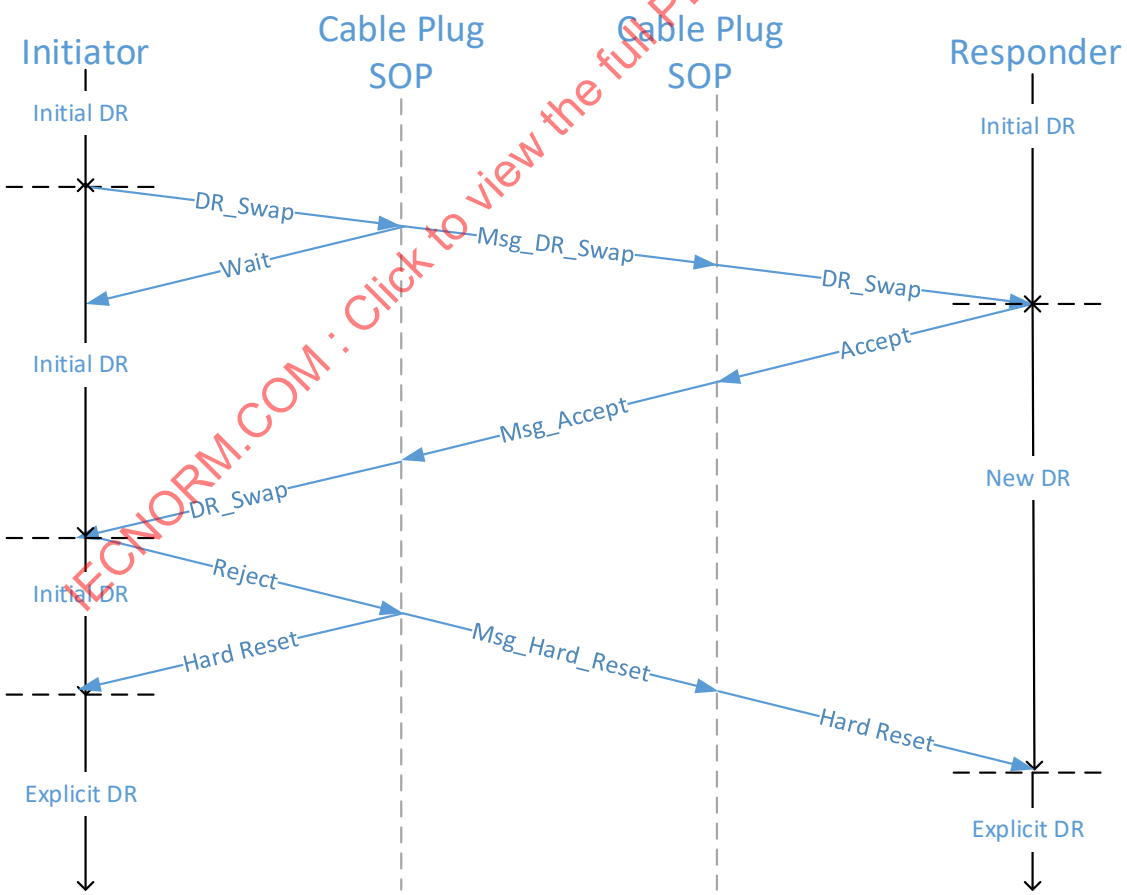
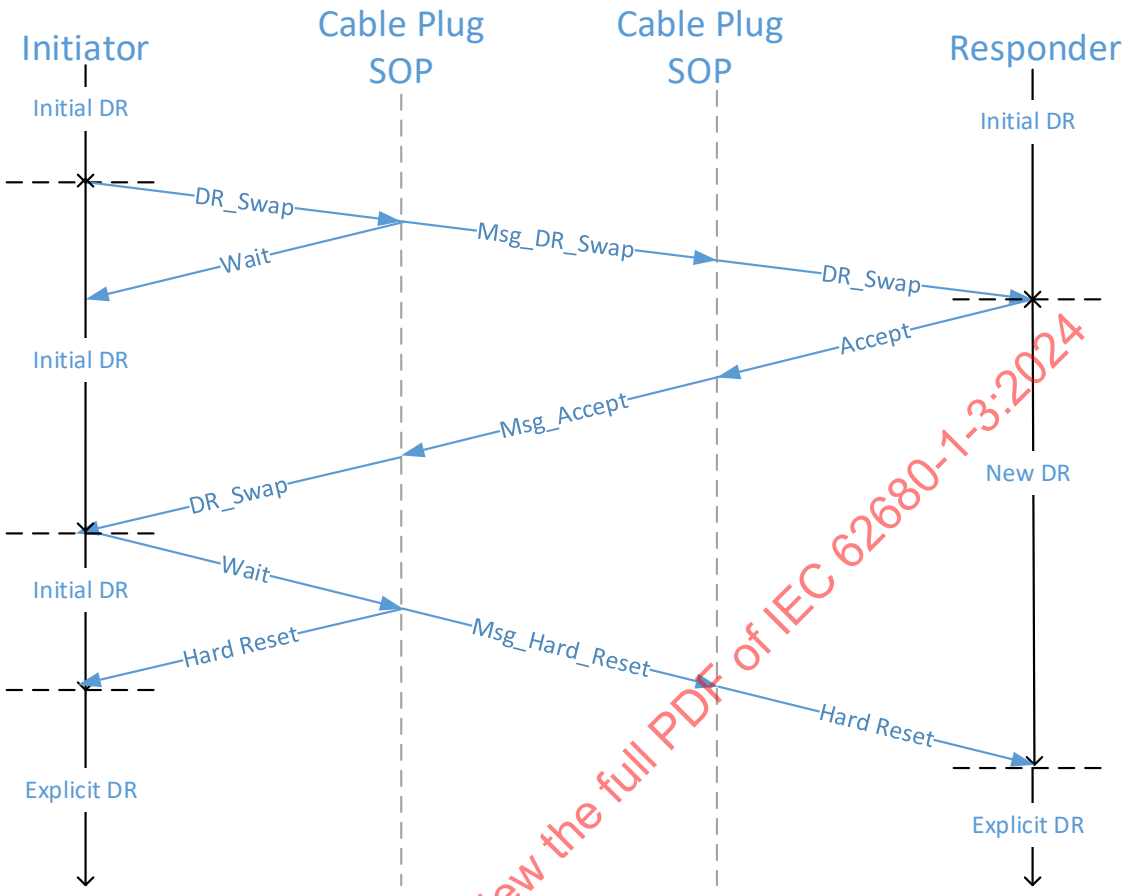


Figure 6-22 OIAC Initiator Reject Data Role Swap



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Figure 6-23 OIAC Initiator Wait Data Role Swap



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6.3.5 OIAC Connection Flow and State Diagrams

This section defines the connection state diagrams for the OIAC. The connection sequence applies to both ***USB 3.2*** and ***USB4*** OIAC. To complete bringing up the ***USB4*** link, the ***USB4*** OIAC is also required to handle all ***USB4***-related messages as defined in ***USB PD***.

OIAC plug defined at time of manufacture as either Plug-A or Plug-B for ***USB PD*** communication. This in no way indicates the plug has more or less capability, rather it allows for a consistent behavior when making the initial end to end connection.

The OIAC communicates using ***USB PD*** with its plug partners to determine the partner capabilities. The OIAC performs a series of connect/disconnects to establish the correct UFP/DFP data role for the cable plug. The possible combinations for ports and cable plugs is defined in Table 6-28.

The connection and establishment of data roles is performed in three phases.

Table 6-28 Port and Plug Capabilities

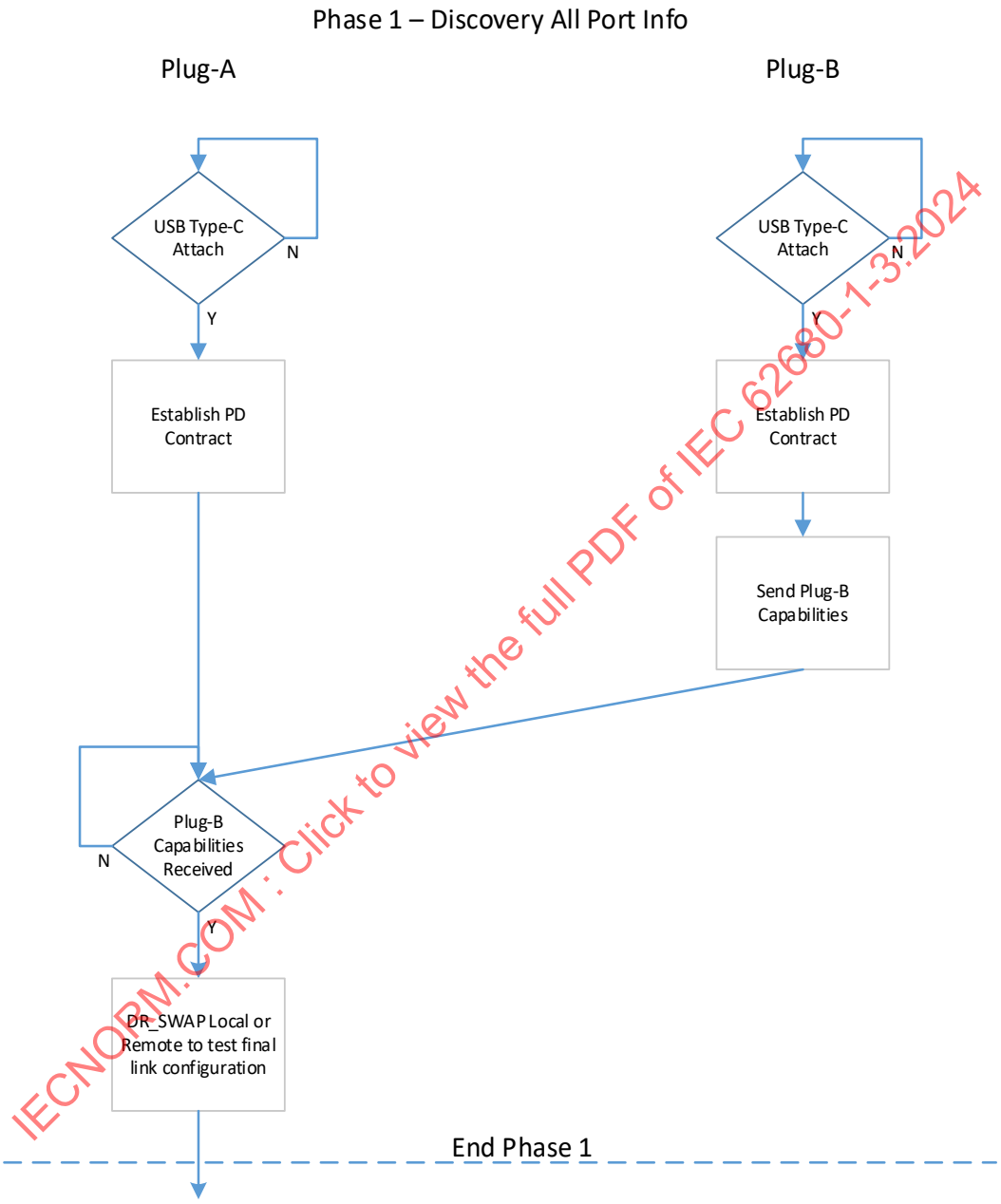
Host/Device Port Capabilities	Cable Configuration		Host/Device Port Capabilities
	Plug-A Role	Plug-B Role	
DRD	DFP	UFP	DRD
DFP	UFP	DFP	DRD
DRD	DFP	UFP	DFP
DFP	Billboard		DFP
Any	Billboard if possible		UFP
UFP	Billboard if possible		Any

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6.3.5.1 OIAC Connection Flow – Discovery – Phase 1

The OIAC cable plugs discover the capabilities of their port partners in the Discovery Phase.

Figure 6-24 OIAC Discovery – Phase 1



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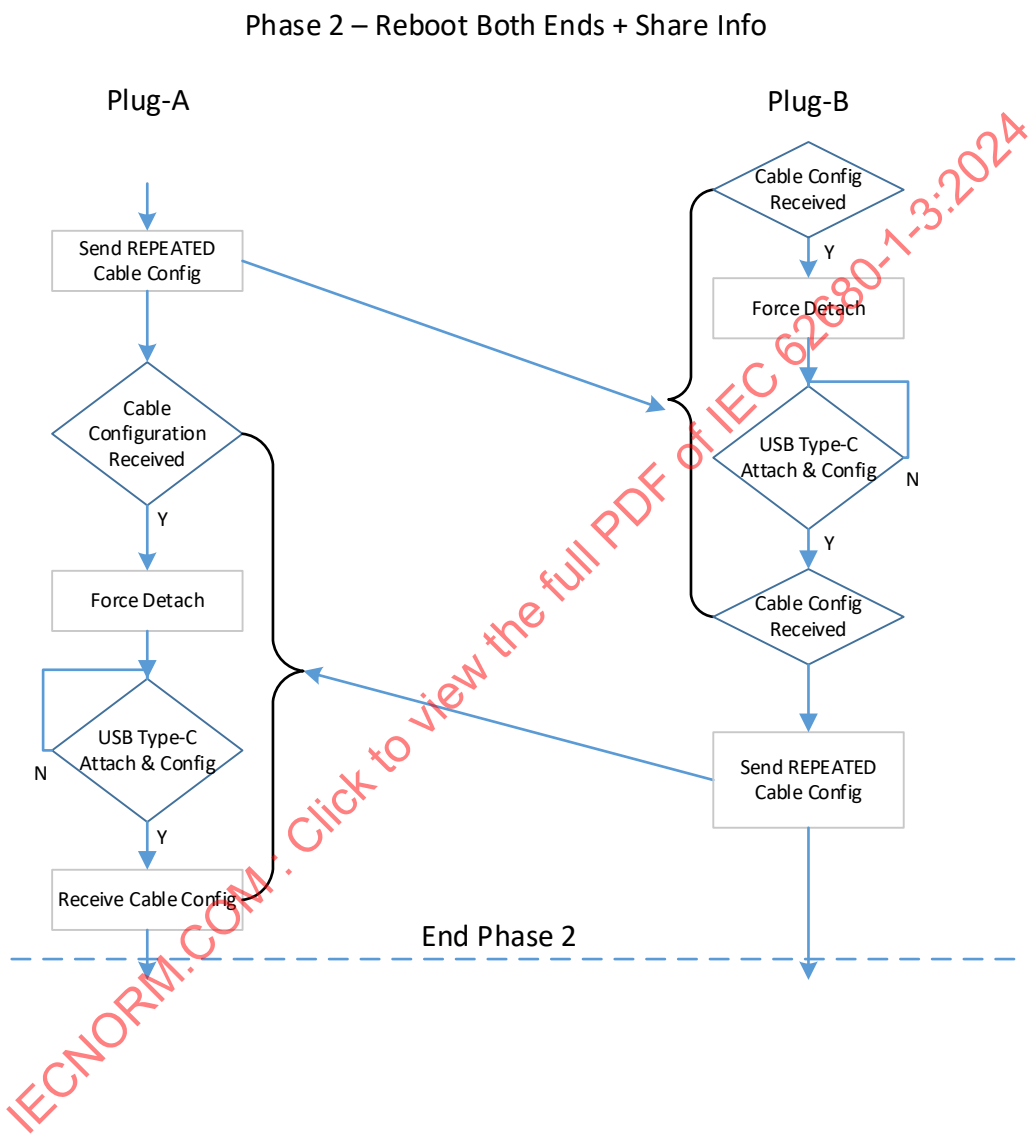
6.3.5.2 OIAC Connection Flow – Reboot – Phase 2

The OIAC cable plugs forward the capabilities of their plug partners and perform disconnect/reconnect.

- Plug-A will always start by repeatedly sending “MSG_Cable_Config” to Plug-B to start reboot.
- Plug-B Reboots.

- Plug-B sees “MSG_Cable_Config” and holds off on SourceCap GoodCRC until it is allowed to release it.
- Plug-B sends “MSG_Cable_Config” to Plug-A.
- Plug-A Reboots.
- Plug-A sees “MSG_Cable_Config” and holds off on SourceCap GoodCRC until it is allowed to release it.

Figure 6-25 OIAC Reboot – Phase 2



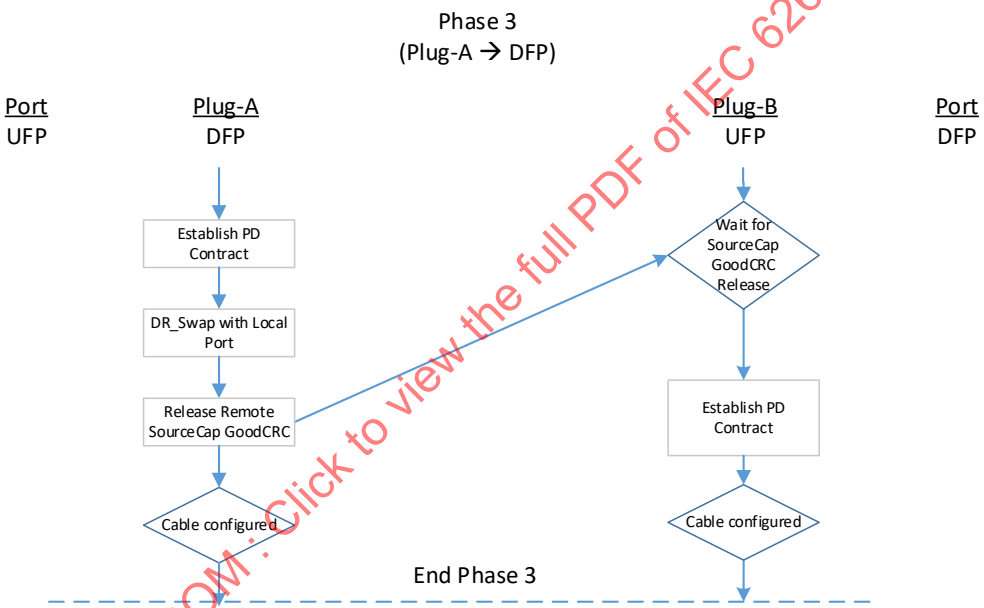
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6.3.5.3 OIAC Connection Flow – Configuration – Phase 3

The OIAC Plug-A determines DFP/UFP roles for Plug-A and Plug-B. Plug-A releases the PLUG to be configured as the DFP and initiates a ***DR_Swap***. The side that issues the ***DR_Swap*** send a ***DR_Swap*** and releases the other side SourceCap GoodCRC.

Figure 6-26 OIAC Plug-A Configured as DFP – Phase 3

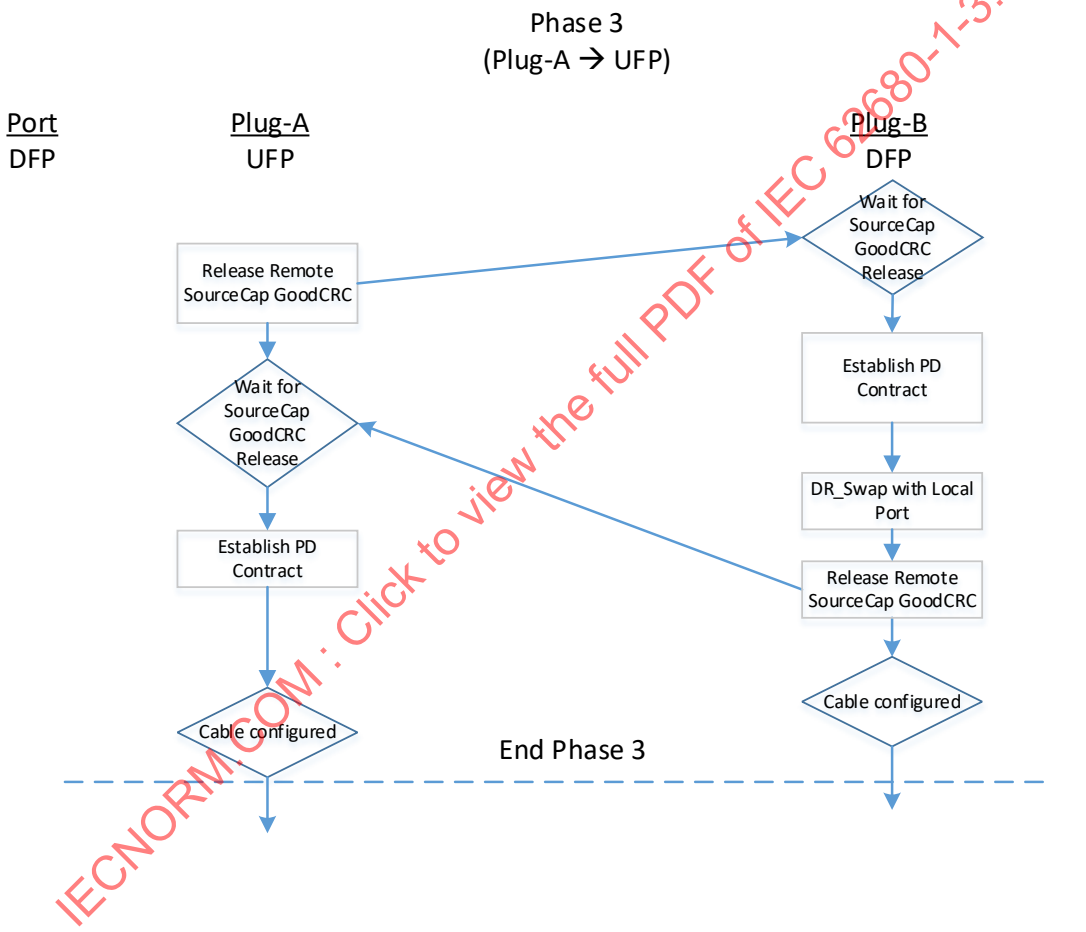
Host/Device Port		Cable			Host/Device Port
		Plug-A	Plug-B		
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any



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Figure 6-27 OIAC Plug-A Configured as UFP – Phase 3

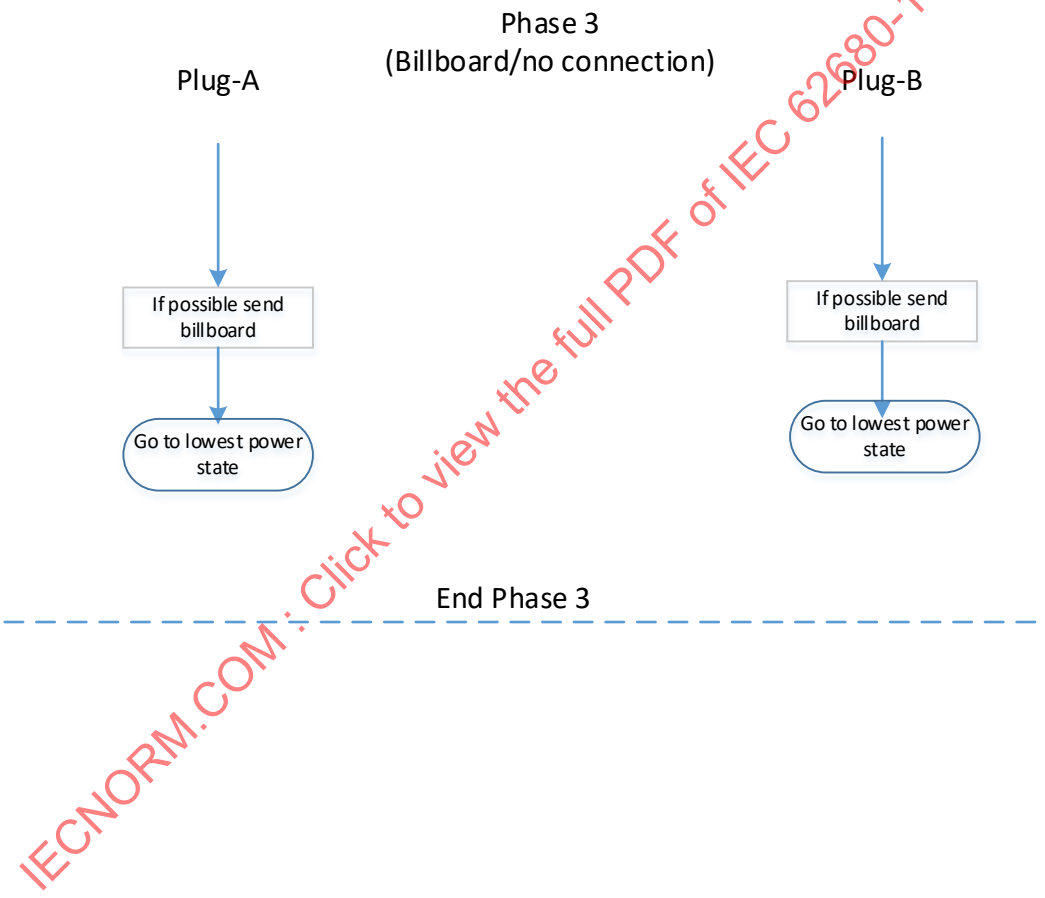
Host/Device Port		Cable			Host/Device Port
		Plug-A	Plug-B		
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any



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Figure 6-28 OIAC Plug-A No Connection Possible Billboard – Phase 3

Host/Device Port		Cable			Host/Device Port
		Plug-A	Plug-B		
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any

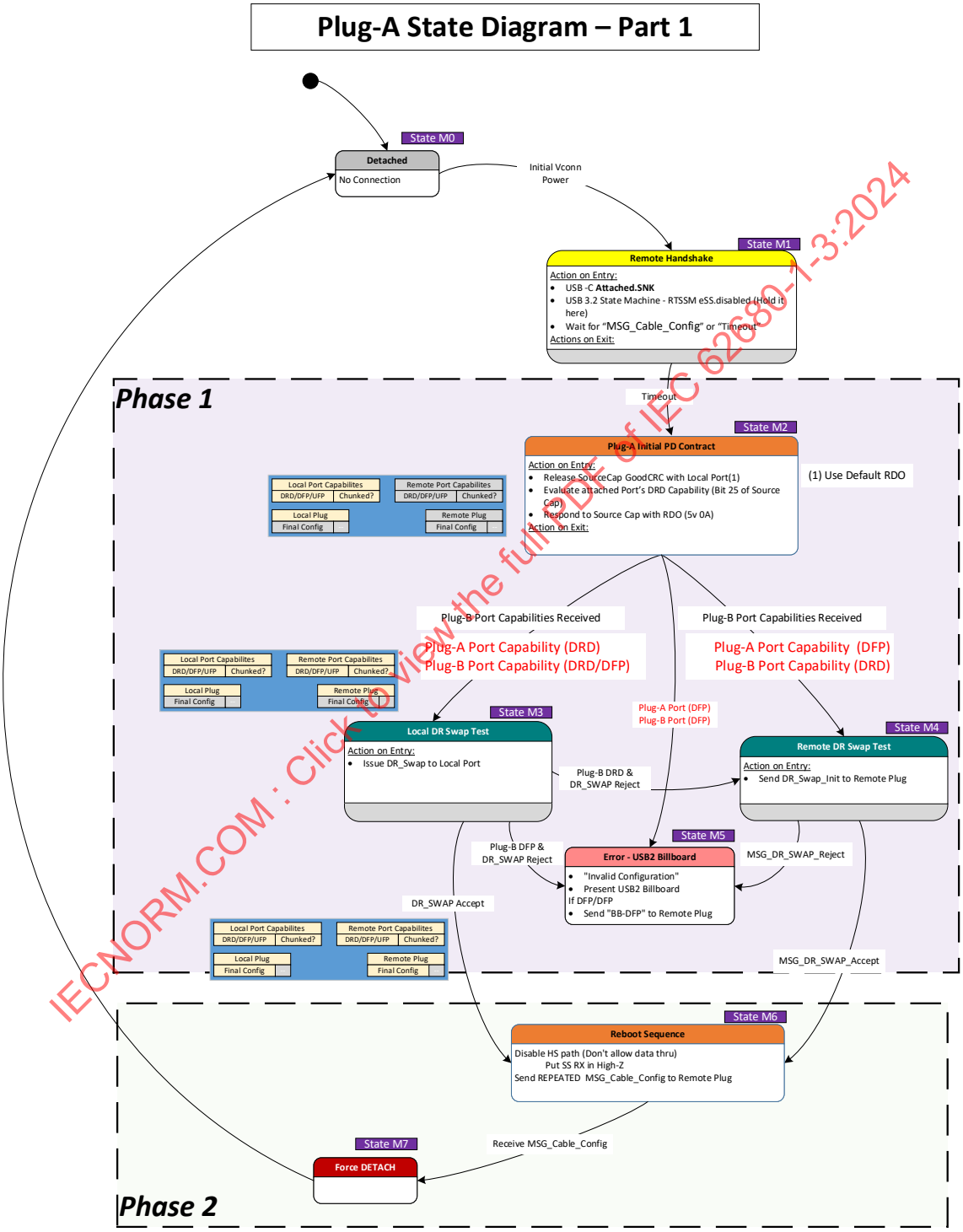


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6.3.5.4 OIAC Connection State Diagram Plug-A

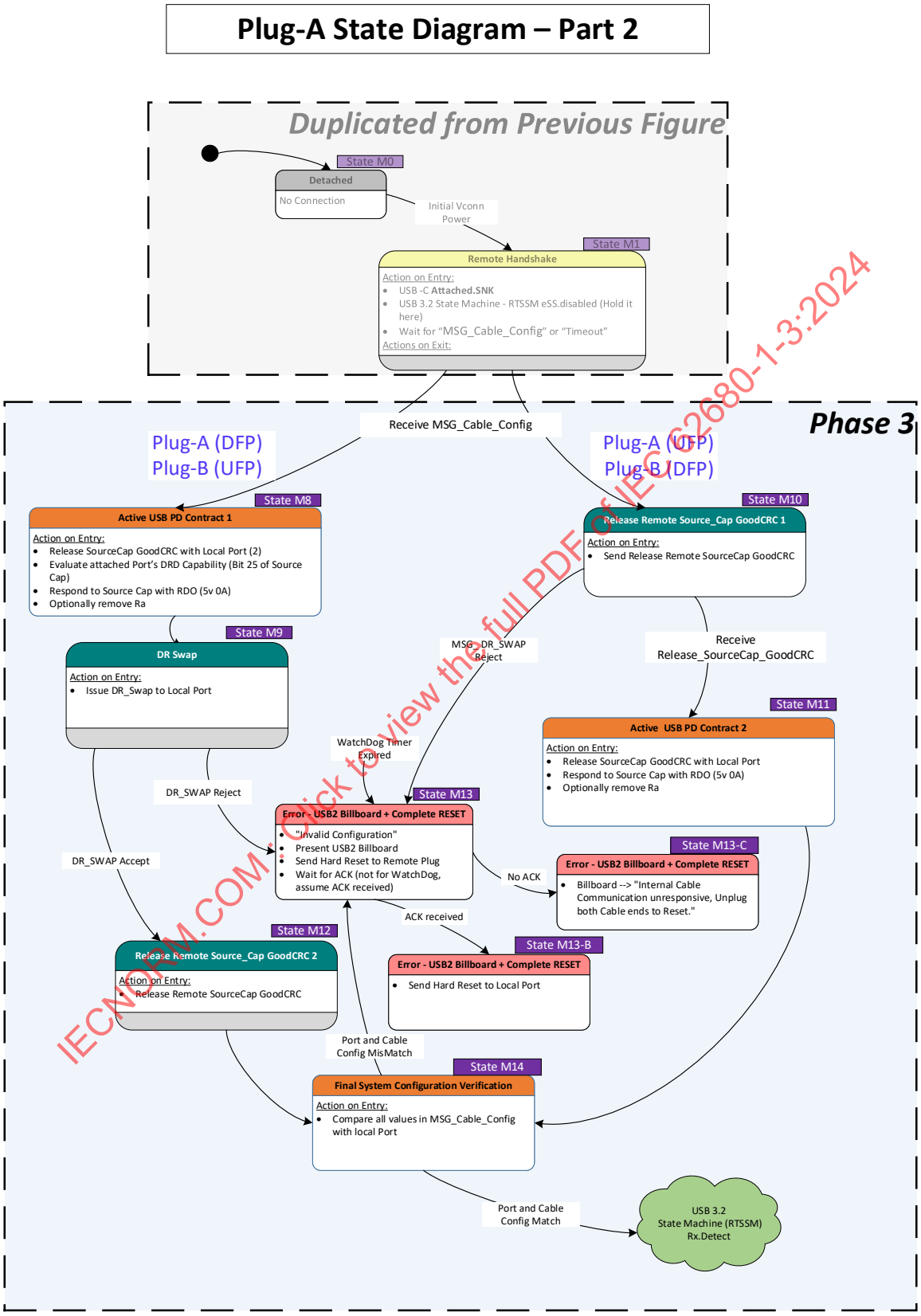
The following sections detail a possible OIAC state diagram for Plug-A.

Figure 6-29 OIAC Plug-A State Diagram Part 1 (Phase 1 and 2)



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Figure 6-30 OIAC Plug-A State Diagram Part 2 (Phase 3)



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6.3.5.4.1 Detached State (M0)

The plug is in ***Detached*** (M0) when no power is applied. The plug transitions to ***Remote Handshake*** (M1) when VCONN is applied.

6.3.5.4.2 Remote Handshake State (M1)

The plug is waiting for the "Timeout" timer expiration or a "MSG_Cable_Config" message from Plug-B.

Recommended Timeout time = ~100ms

The Timeout time is dependent on the duty cycle of Plug-B's Repeat Port Capabilities messages and the maximum cable latency.

The plug starts in the ***USB 3.2*** RTSSM eSS.Disabled and remains in eSS.Disabled until cable initialization is complete at the end of Phase 3.

6.3.5.4.2.1 Entry to Remote Handshake

The plug enters ***Attached.SNK*** followed by entry to ***Remote Handshake*** (M1).

6.3.5.4.2.2 Exit from Remote Handshake

The plug transitions to:

- ***Plug-A Initial PD Contract*** (M2) when the "Timeout" timer has expired,
- ***Active USB PD Contract 1*** (M8) upon receipt of a "MSG_Cable_Config" message when Plug-A resolves to a DFP and Plug-B will resolve to a UFP, or
- ***Release Remote Source_Cap GoodCRC 1*** (M10) upon receipt of a "MSG_Cable_Config" message when Plug-A resolves to a UFP and Plug-B will resolve to a DFP.

6.3.5.4.3 Plug-A Initial PD Contract State (M2)

When the plug is in ***Plug-A Initial PD Contract***, the plug has established an initial ***USB PD*** contract and evaluated its local port's DRD capability.

6.3.5.4.3.1 Entry to Plug-A Initial PD Contract State

On Entry to ***Plug-A Initial PD Contract***, the plug ***shall***:

1. Send a GoodCRC in response to a Source Capabilities message from the local attached port
2. Evaluate the local attached port's DRD capability (as indicated in the Source Capabilities message)
3. Respond to the Source Capabilities message with the "default" RDO specified in Section 6.3.4.3.2.1.2.

6.3.5.4.3.2 Exit from Plug-A Initial PD Contract State

The OIAC plug ***shall*** transition to:

- ***Local DR Swap Test*** (M3) upon receipt of a MSG_Port_Capabilities where the Plug-A port is a DRD and the Plug-B port is either a DRD or DFP,
- ***Remote DR Swap Test*** (M4) upon receipt of a MSG_Port_Capabilities where the Plug-A port is a DFP and the Plug-B port is DRD, or
- ***Error – USB2 Billboard*** (M5) upon determination both Plug-A and Plug-B are connected to DFPs.

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6.3.5.4.4 Local DR Swap Test State (M3)

The ***Local DR Swap Test*** is a test to ensure that the Plug-A port that is defined as a DRD will accept a ***DR_Swap*** request.

6.3.5.4.4.1 Entry to Local DR Swap Test State

On entry to ***Local DR Swap Test***, the plug ***shall*** issue ***DR_Swap*** request to its local port.

If the local port responds to the DR Swap with "***Wait***," then the plug ***shall*** follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state ***Error – USB2 Billboard*** (M5).

6.3.5.4.4.2 Exit from Local DR Swap Test State

The OIAC plug ***shall*** transition to:

- ***Remote DR Swap Test*** (M4) upon receipt of a ***Reject*** and the Plug-B port reported that it is a DRD,
- ***Error – USB2 Billboard*** (M5) upon receipt of a ***Reject*** and the Plug-B port reported that it is a DFP, or
- ***Reboot Sequence*** (M6) upon receipt of an ***Accept***.

6.3.5.4.5 Remote DR Swap Test State (M4)

The ***Remote DR Swap Test*** is a test to ensure that the Plug-B port that is defined as a DRD will accept a ***DR_Swap*** request.

6.3.5.4.5.1 Entry to Remote DR Swap Test State

On entry to ***Remote DR Swap Test***, the plug ***shall*** issue a DR_Swap_Init to the remote plug.

6.3.5.4.5.2 Exit from Remote DR Swap Test State

The OIAC plug ***shall*** transition to:

- ***Reboot Sequence*** (M6) upon receipt of a MSG_DR_Swap_Accept, or
- ***Error – USB2 Billboard*** (M5) upon receipt of a MSG_DR_Swap_Reject.

6.3.5.4.6 Error – USB2 Billboard (M5)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: A DFP only device connected to one of the plugs."

6.3.5.4.6.1 Entry to Error – USB2 Billboard

On entry ***Error – USB2 Billboard***, the plug ***shall*** issue present a Billboard message over ***USB 2.0*** and then power down to its lowest possible state.

6.3.5.4.6.2 Exit from Error – USB2 Billboard

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power.

6.3.5.4.7 Reboot Sequence State (M6)

When the plug is in the ***Reboot Sequence***, it will disable the High Speed Data path and start to initiate a remote plug reboot.

6.3.5.4.7.1 Entry to Reboot Sequence State

On entry to Reboot Sequence, the plug ***shall***:

1) Disable the HS path by changing the SS RX termination to High-Z.

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2) Determine and store the final System Configuration for this link.
    a. The System Configuration will contain:
        i. Host/Device Port information
        ii. Final Plug-A/Plug-B roles
            1. If coming from State M3
                a. Plug-A → DFP (***DR_Swap***)
                b. Plug-B → UFP
            2. If coming from State M4
                a. Plug-A → UFP
                b. Plug-B → DFP (***DR_Swap***)
            3. If coming from State M9
                a. Plug-A → UFP
                b. Plug-B → DFP (***DR_Swap***)
3) Continuously send "MSG_Cable_Config" message to the remote plug.

6.3.5.4.7.2 Exit from Reboot Sequence State

The OIAC plug ***shall*** transition to the ***Force Detach*** (M7) when a "MSG_Cable_Config" message is received that matches the final configuration that Plug-A sent to Plug-B.

6.3.5.4.8 Force Detach State (M7)

The plug ***shall*** transition to ***SRC.Open*** on both CC and VCONN and maintain this state for at least ***tSRCDisconnect***.

6.3.5.4.8.1 Entry to Force Detach State

On entry to ***Force Detach***, the plug ***shall*** raise the voltage on the CC-wire above ***vRd-Connect***.

6.3.5.4.8.2 Exit from Force Detach State

The plug transitions to ***Detached*** upon exit from ***Force Detach***.

6.3.5.4.9 Active *USB PD* Contract 1 State (M8)

Active USB Contract 1 is where OIAC Plug-A creates at ***USB PD*** contract with the local port.

6.3.5.4.9.1 Entry to *USB PD* Contract 1 State

The OIAC plug ***shall*** follow the steps listed below:

1. Begin responding to ***USB PD*** messages from its port partner with GoodCRCs.
2. Evaluate Fixed 5V PDO in the Source Capabilities message to check if its port partner is a DRD.
3. Request for a 5 V @ 0 A power contract.
4. May remove ***Ra*** to save power.

6.3.5.4.9.2 Exit from *USB PD* Contract 1 State

The plug transitions to the ***DR Swap*** (M9) when it receives an ***Accept*** followed by a PS_RDY message from its port partner.

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6.3.5.4.10 DR Swap State (M9)

The ***DR Swap*** is used to set the final data role of the OIAC's Plug-A and signal to the OIAC Plug-B to complete its configuration.

6.3.5.4.10.1 Entry to DR Swap State

The OIAC plug ***shall*** issue a ***DR_Swap*** to its port partner.

If the local port responds to the ***DR_Swap*** with "***Wait***," then the plug ***shall*** follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state ***Error – USB2 Billboard*** (M5).

6.3.5.4.10.2 Exit from DR Swap State

If the ***DR_Swap*** message is responded to with:

- An ***Accept***, it ***shall*** transition to the ***Release Remote Source_Cap GoodCRC 2 State*** (M12), or
- A ***Reject*** it ***shall*** transition to the ***Error - USB2 Billboard + Complete Reset*** (M13).

6.3.5.4.11 Release Remote Source_Cap GoodCRC 1 State (M10)

The OIAC is waiting for Release_Remote_Source_Cap_GoodCRC to better synchronize the power on of the two OIAC plug ends.

6.3.5.4.11.1 Entry to Release Remote Source_Cap GoodCRC 1 State

The OIAC plug ***shall*** release the Remote SourceCap GoodCRC.

6.3.5.4.11.2 Exit from Release Remote Source_Cap GoodCRC 1 State

The OIAC plug ***shall*** transition to:

- ***Active USB PD Contract 2 State*** (M11), when a "MSG_ Release_Remote_SourceCap_GoodCRC" message is received, or
- ***Error – USB2 Billboard + Complete Reset*** (M13) upon receipt of a MSG_DR_Swap_Reject.

6.3.5.4.12 Active *USB PD* Contract 2 State (M11)

Active USB Contract 2 is where OIAC Plug-A creates at ***USB PD*** contract with the local port and ***should*** end with viable link.

6.3.5.4.12.1 Entry to Active *USB PD* Contract 2 State

The OIAC plug ***shall*** follow the steps listed below:

1. Begin responding to ***USB PD*** messages from its port partner with GoodCRCs.
2. Request a 5 V @ 0 A power contract.
3. May remove ***c*** to save power.

6.3.5.4.12.2 Exit from Active *USB PD* Contract 2 State

The plug ***shall*** transition to ***Final System Configuration Verification*** (M13) for final system verification.

6.3.5.4.13 Release Remote Source_Cap GoodCRC 2 State (M12)

OIAC Source Plug configuration is completed, and the ***USB 3.2*** begins looking for a connection.

6.3.5.4.13.1 Entry to Release Remote Source_Cap GoodCRC 2 State

The OIAC plug ***shall*** release the Remote SourceCap GoodCRC.

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6.3.5.4.13.2 Exit from Release Remote Source_Cap GoodCRC 2 State

The plug ***shall*** transition to ***Final System Configuration Verification*** (M13) for final system verification.

6.3.5.4.14 Error – USB2 Billboard + Complete Reset (M13)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: An invalid configuration occurred. Full link will be reset."

6.3.5.4.14.1 Entry to Error – USB2 Billboard + Complete Reset

On entry Error – USB2 Billboard + Complete Reset, the plug ***shall***:

1) Present a USB2 Billboard message
2) Send a MSG_Hard_Reset to the remote Plug
3) Wait for Hard Reset Ack from Remote Plug (Unless entry is from an expired WatchDog Timer, in which case, go directly to M13-B)

   Received ACK (State M13-B):

4) Send Hard Reset to the Local Port

   Did NOT receive ACK (State M13-C):

5) Present USB2 Billboard Message: "Error: Internal Cable Communication Error. Unplug both cable ends to reset."

6.3.5.4.14.2 Exit from Error – USB2 Billboard + Complete Reset

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power from each port.

6.3.5.4.14.3 Watchdog Timer Entry

A watchdog timer ***should*** be implemented for internal cable messages that require a response. The watchdog timer will also provide an entry to an ***Error State*** (M13) if the far end plug is unresponsive for any reason.

There are a few states where the watchdog timer ***shall not*** be implemented including but not limited to M2, where it is possible that only a single end of the OIAC is connected and M6, where the reboot sequence can take a few seconds.

6.3.5.4.15 Final System Configuration Verification (M14)

Final System Configuration Verification is used to do one final check there were no unforeseen changes the local port and the final cable configuration defined by Plug-A.

6.3.5.4.15.1 Entry to Final System Configuration Verification

The OIAC plug ***shall*** check all values in the MSG_Cable_Config match that of the current local port's configuration.

6.3.5.4.15.2 Exit from Final System Configuration Verification

The plug ***shall*** transition to:

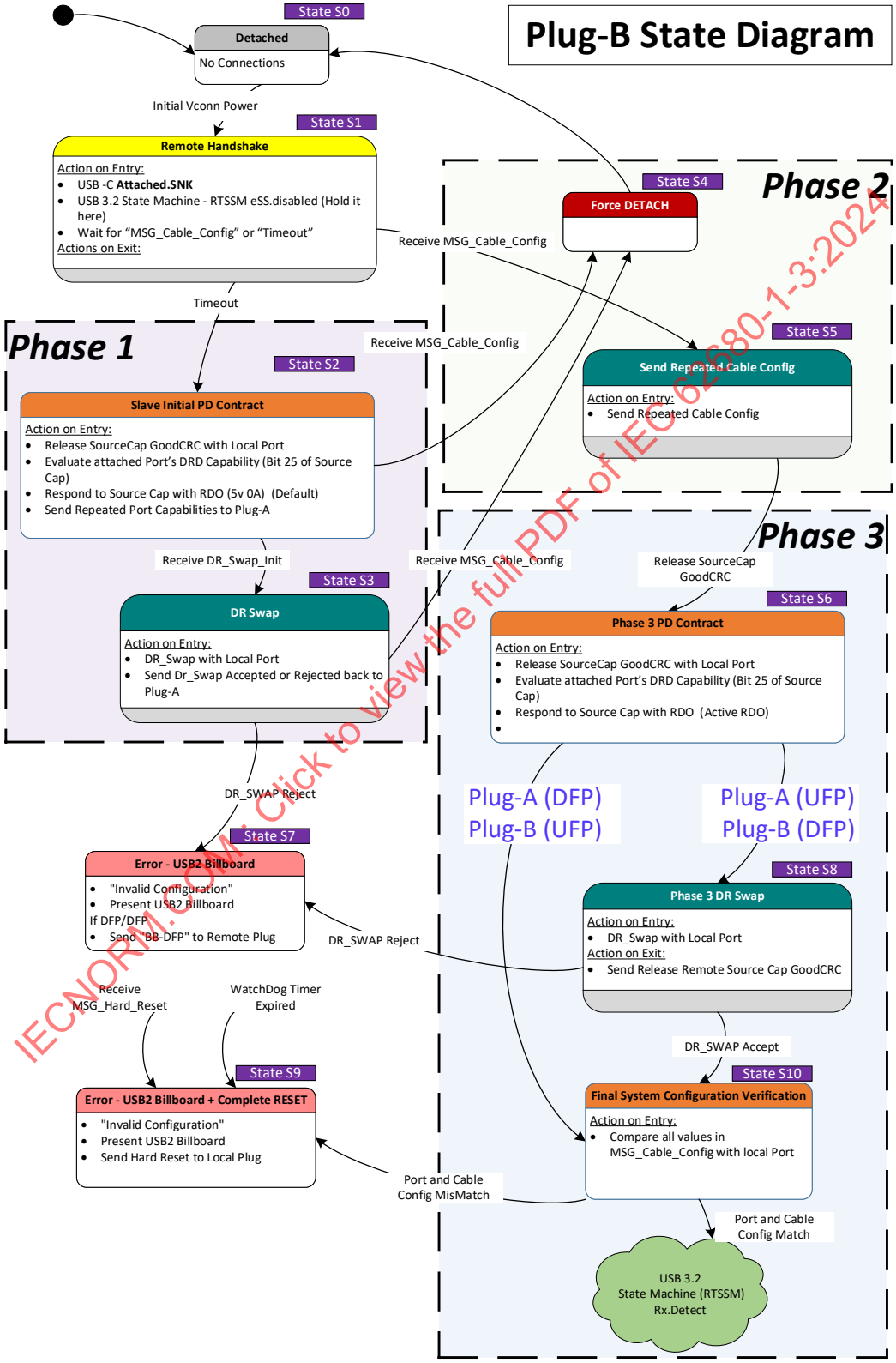
- ***Rx.Detect***, and start far-end receiver termination detection and the ***USB 3.2*** RTSSM State Machine after a successful match of the MSG_Cable_Config and the local port's configuration, or
- ***Error - USB2 Billboard + Complete RESET*** (State M14) after unsuccessful match of the MSG_Cable_Config and the local port's configuration.

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6.3.5.5 OIAC Connection State Diagram Plug-B

The following sections detail a possible OIAC state diagram for Plug-B.

Figure 6-31 OIAC Plug-B State Diagram



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6.3.5.5.1 Detached State (S0)

The plug is in ***Detached*** (S0) when no power is applied. The plug transitions to ***Remote Handshake*** (S1) when VCONN is applied.

6.3.5.5.2 Remote Handshake State (S1)

The plug is waiting for the "Timeout" timer expiration or a "MSG_Cable_Config" message from Plug-A.

Recommended Timeout time = ~100ms

The Timeout time is dependent on the duty cycle of the Plug-A's Repeat MSG_Cable_Config messages and the maximum cable latency.

6.3.5.5.2.1 Entry to Remote Handshake State

The plug enters ***Attached.SNK*** followed by entry to ***Remote Handshake*** (S1).

The plug starts in the ***USB 3.2*** RTSSM eSS.Disabled and remains in eSS.Disable until cable initialization is complete at the end of Phase 3.

6.3.5.5.2.2 Exit from Remote Handshake State

The plug transitions to:

- ***Plug-B Initial PD Contract*** (S2) when the "Timeout" timer has expired, or
- ***Send Repeated Cable Config*** (S5) upon receipt of a "MSG_Cable_Config" message.

6.3.5.5.3 Plug-B Initial PD Contract (S2)

The plug takes the following actions in the order defined:

1. Send a GoodCRC in response to a Source Capabilities message from the local attached port.
2. Evaluate the local attached port's DRD Capability (as indicated in the Source Capabilities message).
3. Send the initial RDO (5 V/0 A) and negotiate an explicit power contract.
4. Send "MSG_Port_Capabilities" to Plug-A. The plug ***shall*** continue to send "MSG_Port_Capabilities" until it exits this state.

6.3.5.5.3.1 Entry to Plug-B Initial PD Contract

The plug enters ***Plug-B Initial PD Contract*** (S2) upon "Timeout" timer expiration.

6.3.5.5.3.2 Exit from Plug-B Initial PD Contract

The plug transitions to:

- ***DR Swap*** (S3) upon receipt of a "DR_Swap_Init" message from Plug-A, or
- ***Force Detach*** (S4) upon receipt of a "MSG_Cable_Config" message from Plug-A.

6.3.5.5.4 DR Swap (S3)

The plug determines if a ***DR_Swap*** can be performed with the local attached port or Plug-A configured itself.

6.3.5.5.4.1 Entry to DR Swap

Upon entry into DR Swap (S3) the plug ***shall***:

1. Send ***DR_Swap*** message to the local attached port.
2. Send MSG_DR_Swap_Accept when the plug receives ***Accept*** message from the local attached port.

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3. Send MSG_DR_Swap_Reject when the plug receives ***Reject*** message from the local attached port.

If the local port responds to the DR Swap with "***Wait***," then the plug ***shall*** follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state ***Error – USB2 Billboard*** (S7).

6.3.5.5.4.2 Exit from DR Swap

The plug ***shall*** transition to:

- ***Error – USB2 Billboard*** (S7) upon rejection of the local attached port ***DR_Swap***, or
- ***Force Detach*** (S4) upon receipt of a "MSG_Cable_Config" message from Plug-A.

6.3.5.5.5 Force Detach (S4)

The plug ***shall*** transition to ***SRC.Open*** on both CC and VCONN and maintain this state for at least ***tSRCDisconnect***.

6.3.5.5.5.1 Entry to Force Detach

The plug enters ***Force Detach*** (S4) upon receipt of a "MSG_Cable_Config"" message from Plug-A.

6.3.5.5.5.2 Exit from Force Detach

The plug transitions to ***Detached*** (S0) upon exit from ***Force Detach***.

6.3.5.5.6 Send Repeated Cable Config (S5)

The plug repeatedly sends "MSG_Cable_Config" messages in this state to inform Plug-A of the configuration of the local attached port.

6.3.5.5.6.1 Entry to Send Repeated Cable Config

The plug enters ***Repeated Cable Config*** (S5) upon receipt of a "MSG_Cable_Config" message from Plug-A.

6.3.5.5.6.2 Exit from Send Repeated Cable Config

The plug transitions to ***Phase 3 PD Contract*** (S6) upon receipt of a "Release SourceCap GoodCRC" message from the Plug-A port.

6.3.5.5.7 Phase 3 PD Contract (S6)

The plug performs the following actions in this state:

1. Send a GoodCRC in response to a Source Capabilities message from the local attached port.
2. Evaluate the attached local attached port's DRD Capability (as indicated in the Source Capabilities message).
3. Send the initial RDO (5 V/0 A) in response to the Source Capabilities message and negotiate an explicit power contract.

6.3.5.5.7.1 Entry to Phase 3 PD Contract

The plug enters ***Phase 3 PD Contract*** upon receipt of a "Release SourceCap GoodCRC" message from Plug-A.

6.3.5.5.7.2 Exit from Phase 3 PD Contract

The plug transitions to:

- ***Final System Configuration Verification*** (S10) for final system verification upon determination Plug-A is acting as a DFP and it is acting as a UFP, or
- ***Phase 3 DR Swap*** (S8) upon determination Plug-A is acting as a UFP and it is acting as a DFP.

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6.3.5.5.8 Error – USB2 Billboard (S7)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: “Error: A DFP only device connected to one of the plugs.”

6.3.5.5.8.1 Entry to Error – USB2 Billboard

The plug transitions to this state upon rejection of a ***DR_Swap*** by the local attached port.

6.3.5.5.8.2 Exit from Error – USB2 Billboard

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power.

6.3.5.5.9 Phase 3 DR Swap (S8)

The plug issues a ***DR_Swap*** with its local attached port in this state.

6.3.5.5.9.1 Entry to Phase 3 DR Swap

The plug enters ***Phase 3 DR Swap*** upon determination Plug-A is connected as a UFP and Plug-B ***should*** connect as a DFP.

6.3.5.5.9.2 Exit from Phase 3 DR Swap

The plug ***shall*** transition to:

- ***Final System Configuration Verification*** (S10) for final system verification after successful completion of the ***DR_Swap*** with the local attached port, or
- ***Error – USB2 Billboard*** (S7) after unsuccessful completion of the ***DR_Swap*** with the local attached port.

6.3.5.5.10 Error – USB2 Billboard + Complete RESET (S9)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: “Error: An invalid configuration occurred. Full link will be reset.”

6.3.5.5.10.1 Entry to Error – USB2 Billboard + Complete RESET

On entry ***Error – USB2 Billboard + Complete RESET***, the plug ***shall***:

1. Present a USB2 Billboard message.
2. Send Hard_Reset to the Local Plug.

6.3.5.5.10.2 Exit from Error – USB2 Billboard + Complete RESET

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power.

6.3.5.5.10.3 Watchdog Timer Entry

A watchdog timer ***should*** be implemented for internal cable messages that require a response. The watchdog timer will also provide an entry to an ***Error State*** (M13) if the far end plug is unresponsive for any reason.

There are a few states where the watchdog timer ***shall not*** be implemented including but not limited to S5, where the reboot sequence can take a few seconds.

6.3.5.5.11 Final System Configuration Verification (S10)

The ***Final System Configuration Verification*** is used to one final check there were no unforeseen changes to the local port and the final cable configuration defined by Plug-A.

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6.3.5.5.11.1 Entry to Final System Configuration Verification

The OIAC plug ***shall*** check all values in the MSG_Cable_Config match that of the current local port's configuration.

6.3.5.5.11.2 Exit from Final System Configuration Verification

The plug ***shall*** transition to:

- ***Rx.Detect***, and start far-end receiver termination detection and the ***USB 3.2*** RTSSM State Machine after a successful match of the MSG_Cable_Config and the local port's configuration, or
- ***Error – USB2 Billboard + Complete RESET*** (State S9) after unsuccessful match of the MSG_Cable_Config and the local port's configuration.

6.3.6 Additional Electrical Requirements for OIAC

6.3.6.1 Shielding Effectiveness Requirement

OIACs ***shall*** meet the shielding effectiveness requirement defined in Section 3.7.7 and Figure 3-65.

6.3.6.2 Low Speed Signal Requirements

6.3.6.2.1 CC Channel Requirements

OIACs ***shall*** meet the Low-Speed Signal Requirements in Section 3.7.2.6.

6.3.6.2.2 SBU Requirements

6.3.6.2.2.1 *USB 3.2*

OIACs are not required to support SBU1/2 for ***USB 3.2*** support.

6.3.6.2.2.2 Alternate Modes

OIACs ***may*** support SBUs for ***Alternate Modes***. SBUs are not usable until the cable has entered an ***Alternate Mode***. OIACs which support SBU signals ***shall*** meet the requirements of the ***Alternate Mode***(s) supported. Definition of the SBU requirements for ***Alternate Modes*** is outside the scope of this specification..

6.3.6.2.2.3 *USB4*

OIACs ***shall*** support SBTX and SBRX for ***USB4*** support. No additional support for SBU1/2 signaling is required.

OIAC SBU wires operating as ***USB4*** SBTX and SBRX ***shall*** meet the same voltage swing requirements as Active Cables as defined in Table 6-3.

6.3.6.3 *USB 2.0*

OIACs are not required to support ***USB 2.0***, therefore ***USB 2.0*** is not expected to work across an OIAC.

The OIAC will take action to reset the link when the USB Device drops from ***USB 3.2*** to ***USB 2.0***.

During the initial connection the OIAC ***shall*** present as a ***USB 2.0*** DFP and provide a 15K Ohm pull down on the D+/D– pins on both ends of the cable. The cable plug ***shall not*** issue a ***USB 2.0*** Reset in this state.

The OIAC cable plug ***shall*** issue a ***USB 2.0*** Reset upon detecting a ***USB 2.0*** connection on D+/D– (LS, FS, or HS ***USB 2.0*** connection). The cable plug ***shall*** issue a ***USB 2.0*** Bus Reset by pulling D+ and D– low for at least 50 ms.

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The OIAC ***shall*** implement a tDisableCount counter to determine how many times the cable has transitioned from ***USB 3.2*** to ***USB 2.0***. The tDisableCount counter ***shall*** be reset to zero on either condition:

- Power on Reset of the OIAC, or
- Successful transition to ***USB 3.2*** U0.

The OIAC ***shall*** present and latch a ***USB 2.0*** billboard when the tDisableCount counter reaches three.

6.3.6.4 *USB 3.2*

OIAC ***shall*** meet the requirements in this section regardless of length. OIACs ***shall*** incorporate AC-coupling from the plug to repeater on both the ***USB 3.2*** TX and RX signals. OIACs ***shall*** provide a discharge path for discharging the AC-coupling capacitors in the cable on unplug per ***USB 3.2***.

6.3.6.4.1 *USB 3.2* Power-on and Rx.Detect

OIAC ***shall*** have the same power-on and far-end receiver termination as defined for the Active Cable defined in Section 6.1.2.4.2.

OIACs ***shall*** reflect the receiver terminations across the cable to replicate the behavior of a passive cable.

6.3.6.4.2 OIAC Legacy Adapter

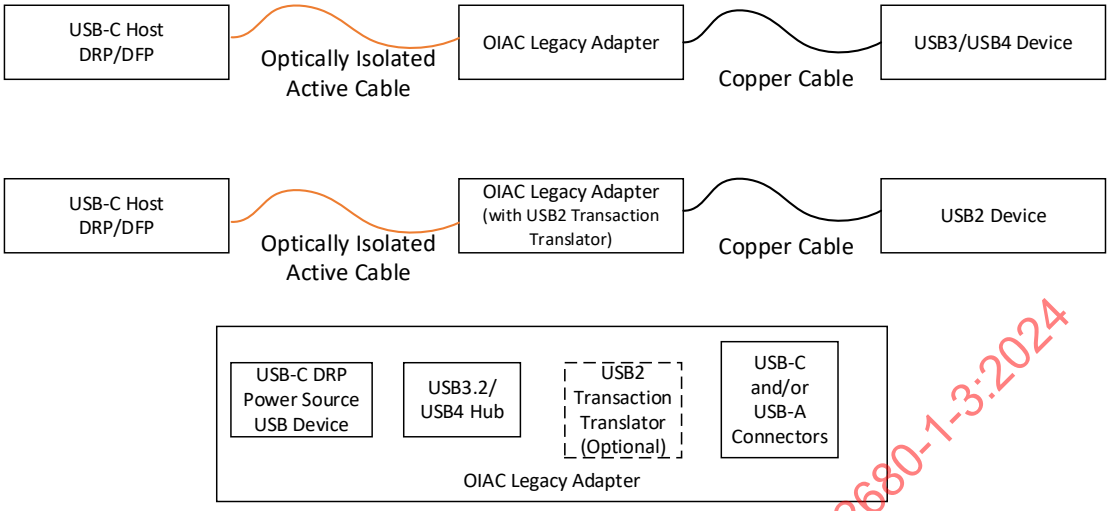
The OIAC Legacy Adapter is specified here to provide a way to connect to a ***USB 3.2*** or ***USB4*** device that does not support OIACs. This adapter will need to be in place between the OIAC and the device.

The OIAC Adapter requires the following capabilities:

1. USB Type-C DRP/Source (Self-Powered) on the upward facing port connected to the OIAC,
2. Self-Powered
    a. Needs to power the upstream OIAC
    b. Needs to be able to power the downstream device
3. ***USB PD*** on the upward facing port connected to the OIAC,
4. ***USB 3.2*** Hub
5. ***Optional***: ***USB4*** Hub
6. ***Optional***: ***USB 2.0*** to ***USB 3.2*** transaction translator on the downstream facing port (only needed if connecting to ***USB 2.0***-only devices, hubs, or hosts).

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Figure 6-32 Illustration of Usages for OIAC that Require an Adapter or Hub



6.3.6.4.3 *USB 3.2* U-State Power Requirements

OIACs ***shall*** meet the VCONN power requirements for ***USB 3.2*** operation in Table 6-29. These requirements are for the entire cable not just a cable plug.

Table 6-29 *USB 3.2* U-State Requirements

State	Maximum VCONN Power Consumption	Power Consumption Notes
U0	1.0 W single-lane 1.5 W dual-lane	Applies to POLLING.LFPS, TRAINING, and RECOVERY states.
U1	≤ U0 power	Forwarding LFPS is required
U2	≤ U0 power	Forwarding LFPS is required
U3	≤ U0 power	Steady state power. eMarker in sleep.
Rx.Detect	≤ U0 power	Rx.Detect period ***may*** be lengthened when no ***USB 3.2*** terminations have been detected. eMarker in sleep.
eSS.Disabled	≤ U0 power	***USB 3.2*** is disabled. eMarker in sleep.

6.3.6.4.4 *USB 3.2* U-State Exit Latency

USB 3.2 U-State Exit Latency is TBD.

6.3.6.4.5 Signal Swing

OIACs ***shall*** meet the same electrical characteristics for ***USB 3.2*** Signal Swing as an Active Cable defined in Section 6.1.2.4.6.

6.3.6.5 *USB4*

The Optically Isolated Active Cable for ***USB4*** is defined as a Linear Optical Active Cable. As such, the electrical LRD requirements in Section 6.1.2.5.4 will generally apply to a ***USB4*** OIAC.

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6.3.6.5.1 AC Coupling Capacitors

OIAC ***shall*** include AC-coupling capacitance between 135 nF and 265 nF inside their plugs placed at the output transmit path and between 300 nF and 363 nF at the input receive path. Discharge resistors between 200 KΩ and 242 KΩ ***shall*** be placed at the input receive path. See Figure 3-3 in the ***USB4*** specification for a diagram of the AC-coupling capacitors and discharge resistors.

6.3.6.5.2 *USB4* CL-State Power Requirements for OIAC

OIACs are not required to meet the same CL-State power requirements as defined for Active Cables (Section 6.1.2.5.2).

OIACs ***shall*** meet the VCONN power requirements for ***USB4*** operation in Table 6-30. These requirements are for the entire cable, not just a cable plug.

Table 6-30 *USB4* CL-State Requirements for OIAC

State	Maximum VCONN Power Consumption	Power Consumption Notes
CL0	1.5 W	Applies to training states and CL0.
CL0s	≤ CL0 power	
CL1	≤ CL0 power	
CL2	≤ CL0 power	
CLd	≤ CL0 power	Steady state power.

6.3.6.6 Return Loss

Return loss is defined in the ***USB 3.2*** specification.

6.3.7 Additional Mechanical Requirements for OIAC

The mechanical specifications for OIACs are the same as all other Active Cables (see Section 6.1.3). Additional requirements for OIACs are provided in this section.

6.3.7.1 Thermal

6.3.7.1.1 Thermal Shutdown

OIACs ***shall*** billboard in shutdown to both ports, regardless of which end of the cable plug is in thermal shutdown. For example: "Error: The Optical Cable has experienced a thermal shutdown."

6.3.7.1.2 Thermal Reporting

The OIAC ***shall*** implement reporting their maximum internal operating temperature in the ***USB PD*** **Discover_ID** Command.

The OIAC ***shall*** report their current internal operating temperature (of the higher of the two cable plugs) in the ***USB PD Get_Status*** Command on SOP'.

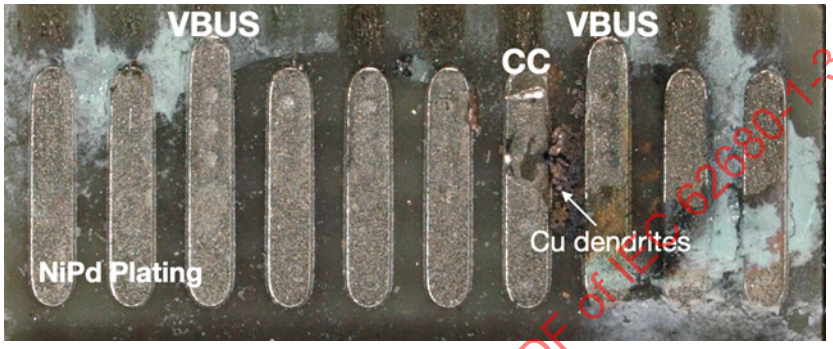
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A Liquid Corrosion Mitigation Mode

A.1 Overview

Ingress of every day liquids with electrolytes (sweat, soda, tap water, salt water, pool water, etc.) into the USB Type-C connector can easily corrode the connector pins when exposed to the liquid with electrical bias in the connector (VBUS, CC, etc.). The liquid forms a bridge between pins and when the voltage difference between the pins is high enough (above a few hundred millivolts), the exposed metal will dissolve into free ions and these ions will migrate from one pin to another. When these dissolved ions move and form oxides, they can lead to open or high impedance due to surface residue or partial metal pin material loss or they can lead to shorts due to various mechanisms like dendrite growth or metal-based particle depositions on plastic surface.

Figure A-1 Electrolytic Liquid Corrosion Example



When in a connected state, VBUS is 4.75 V – 50.4 V and CC/VCONN is 0.2 V – 5.5 V. Likewise, in an unconnected state, a Source or DRP will pull the CC pin to 3 V – 5.5 V. This results in always-present voltage bias that will corrode pins when exposed to electrolytic liquids.

The ***Liquid Corrosion Mitigation Mode*** is an optional normative mode that eliminates or reduces the rate of corrosion by removing or forcing the bias voltages in the connector to a voltage as close to 0 V as possible.

A.2 Detail

If a liquid detection scheme is employed by a device with a USB Type-C port, the port state can be directed to the ***CorrosionMitigation*** state by first going through ***ErrorRecovery***. In the ***CorrosionMitigation*** state, the port shall pull low with a resistance on both CC1 and CC2 less than or equal to the Maximum Impedance of ***Ra*** as specified in Table 4-29. The port should pull low with a resistance stronger than ***Ra*** to pull the voltage as low as possible. The lower the voltage, the lower the rate of corrosion. Figure A-2 and Figure A-3 show the Corrosion Mitigation pull-down resistance for any port in the ***CorrosionMitigation*** state when connected to a Source. Alternatively, for solutions with the ability to only pull one pin low at a time, this resistance can be applied to only one of the CC pins while the other CC pin is kept open. Figure A-4 shows the pull-down resistance and open with this method. When this alternative approach is used, the voltage on the open CC pin shall be monitored to detect the presence of a pull-up from an attached Source (CC is ***SNK.Rp***) due to a plug event with a cable or device in the opposite orientation. When the pull-up is detected, the Sink shall swap the pull-down and open between the CC pins.

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Figure A-2 Corrosion Mitigation in Pull-Up/Pull-Down CC Model

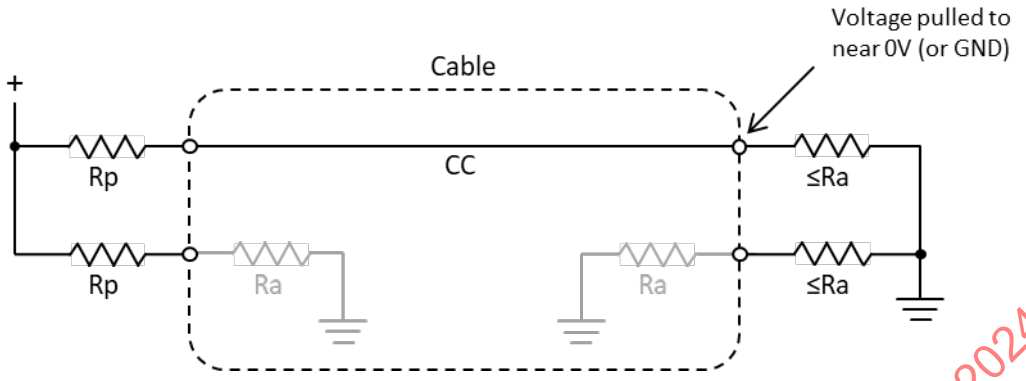


Figure A-3 Corrosion Mitigation in Current Source/Pull-Down CC Model

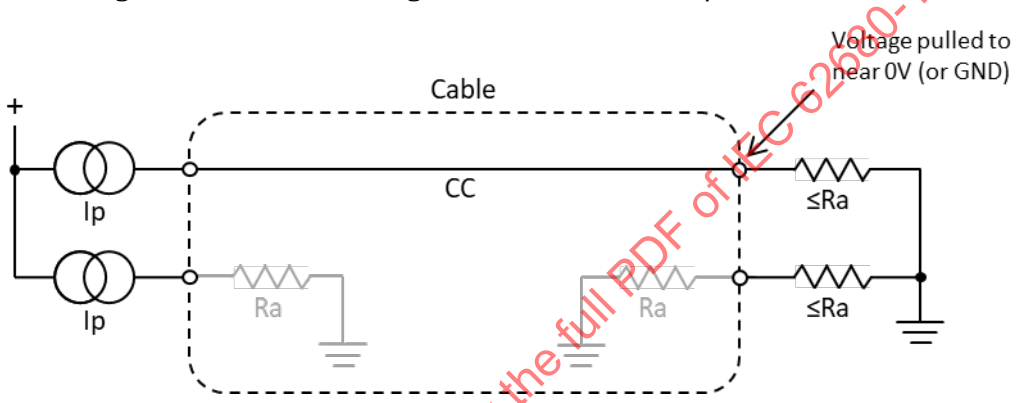
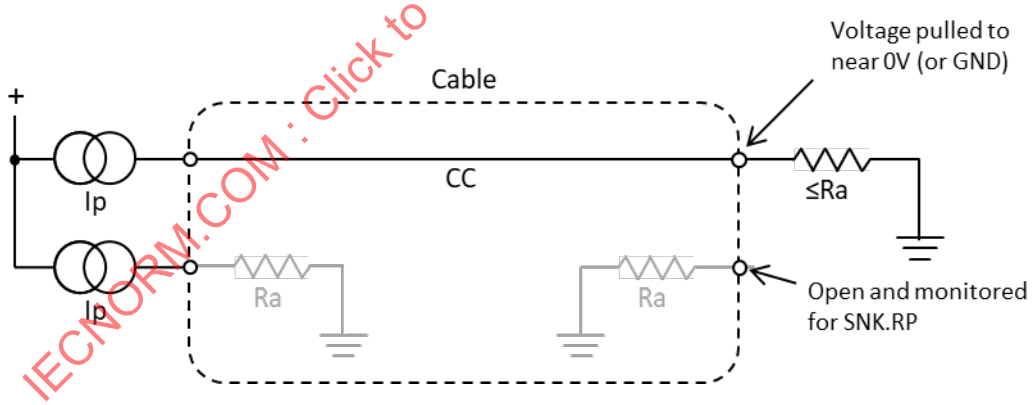


Figure A-4 Corrosion Mitigation in Current Source/Pull-Down CC Model with Alternate Mitigation



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When a Source or DRP connects to a port in the ***CorrosionMitigation*** state, it will move to the ***AttachWait.SRC*** state (two ***Ra*** detected), stay in the ***Unattached.SRC*** state (Source with single ***Ra*** detected), or continue DRP toggling (DRP with single ***Ra*** detected) until the ***CorrosionMitigation*** state is exited by the port partner. In these states, V_{BUS} and V_{CONN} are at 0 V, and the CC pin will be pulled low by the attached resistance of the port partner. All other pins should be open or pulled low. This will hold all voltages in the port low enough to stop or greatly reduce the rate of corrosion. Once a liquid condition is no longer detected, the port should be directed to exit the ***CorrosionMitigation*** state.

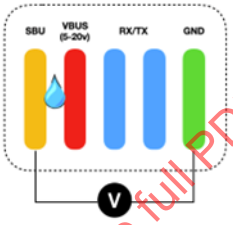
A.3 Liquid Detection Methods

Multiple methods exist to detect liquid in a port. Three possible methods are described, but this is not an exhaustive list. Other methods may be developed and used.

A.3.1 Liquid Measurement Method

Liquid may be detected by measuring the effect of leakage through the liquid between pins. The voltage on a pin can be measured to determine if there is a connection through this liquid to another pin. Figure A-5 shows an example of this measurement using one of the SBU pins. When the port is dry, the measurement pin should be biased to a known level based on the bias circuitry chosen. When the port is wet, DC voltages or signals may couple on the measurement pin which can be read by comparator or ADC. To use the method, various liquids should be characterized with the planned connector (metal, plating, spacing, etc.). Note, this method has low complexity, but may have only moderate sensitivity (accuracy of detection) to liquids resulting in some missed detections based on the amount of and type of liquid. This method may also have a high rate of missed detects due to the variation of the voltages to which the leakage may be connected (i.e., VBUS and CC). This method may also produce higher levels of false detections (other contaminants, high levels of coupling, etc.).

Figure A-5 Liquid Detection by Leakage Measurement

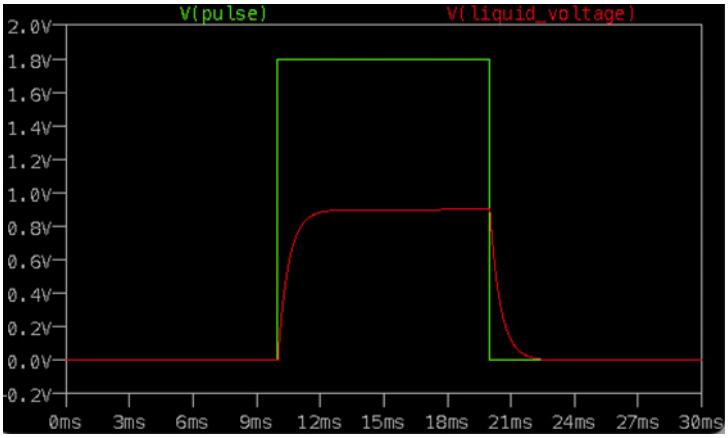


A.3.2 Pulsed Measurement Method

Liquid may be detected by measuring the effect of driving a pulse onto the measurement pin through a series resistance. The rise and fall behavior of the pin can be measured with a timer and comparator to determine the time it takes to cross a certain threshold. Figure A-6 shows an example of this measurement. When the port is dry, the pin voltage will pass the threshold quickly. When the port is wet, loading from the liquid and adjacent pins will cause a slower voltage rise or fall. Like the leakage measurement method, to use the pulsed measurement method, various liquids should be characterized with the planned connector (metal, plating, spacing, etc.). Note, this method is slightly more complex, but can also have only moderate sensitivity to liquids. Some missed detections based on the amount of, and type of liquid may still occur. This method may also miss detections due to other pulsed signals within the port like DRP toggling. This method may also produce false detections but at a reduced rate from the leakage measurement method.

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Figure A-6 Liquid Detection by Pulsed Measurement



A.3.3 Impedance Measurement Method

Liquid may be detected by measuring the impedance of a measurement pin. This can be done by various methods. One example method is an I-V measurement that measures both the amplitude and phase shift from a known “dry” condition. Wet or Dry conditions can be determined by the measurement impedance characteristics of the port with the liquid. Like the previous measurement methods, to use the pulsed measurement method, various liquids should be characterized with the planned connector (metal, plating, spacing, etc.). Note, this method is much more complex, but has higher sensitivity and lower false detections. Figure A-7 through Figure A-11 show examples of this measurement on various liquids taken with a Keysight E4990A impedance analyzer sweeping from 20Hz to 1MHz. Table A-1 shows the conditions for the measurements shown.

Table A-1 Example Measurement Test Conditions

Item	Model	Description
Connector	JAE DX07S024JJ2R1300	USB Type-C receptacle, 24 pin SMD
Liquid Dispense	Various	0.5-10µL micropipette
Equipment	Keysight E4990A	Impedance Analyzer
Artificial Sweat	1700-0020	Pickering Laboratories Artificial Eccrine Perspiration Stabilized

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Figure A-7 Example Measurement of a Dry Port

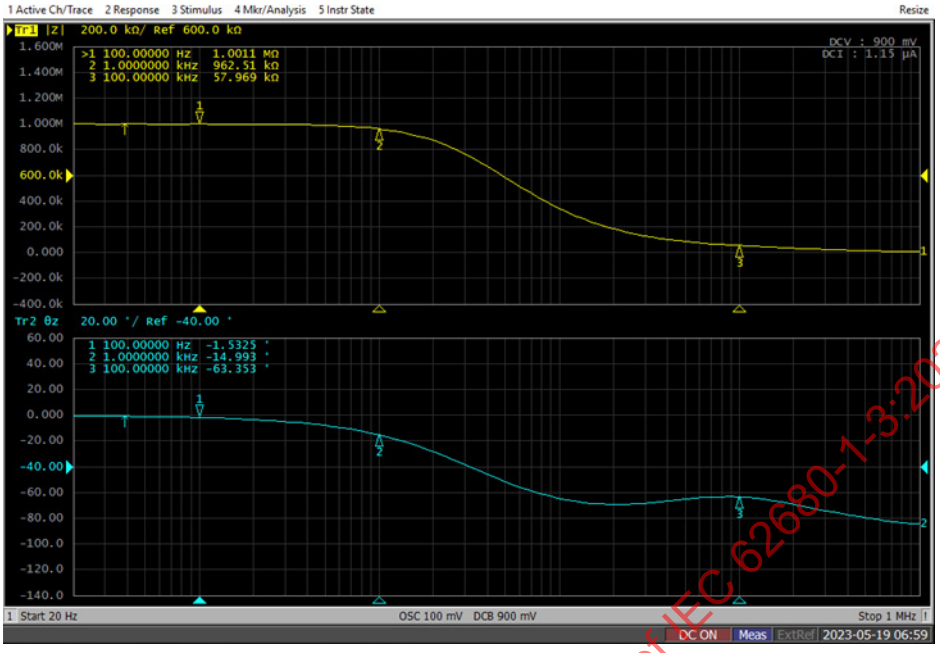
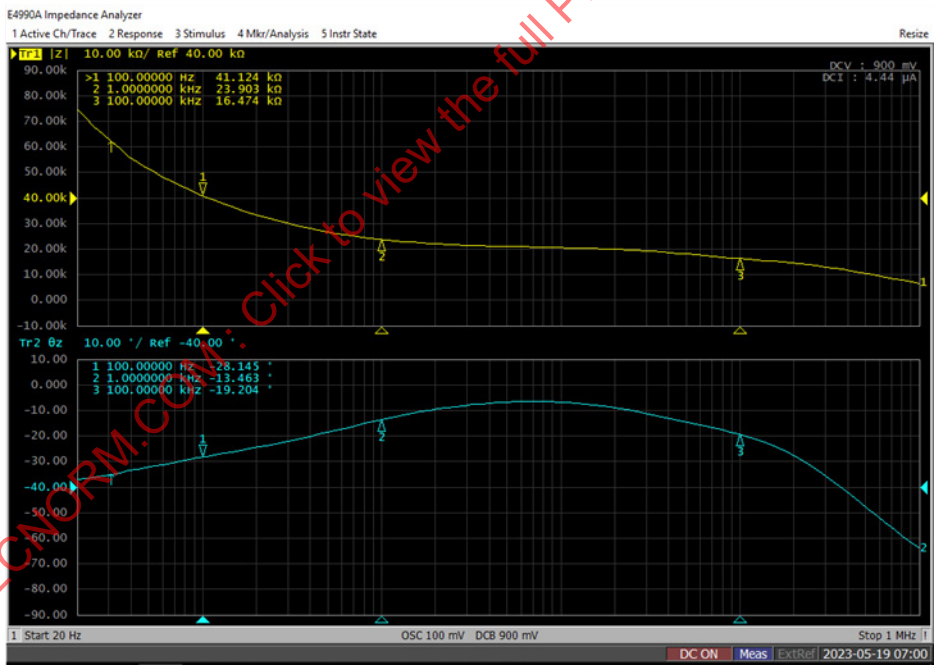


Figure A-8 Example Measurement of a Port with Reverse Osmosis Water



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Figure A-9 Example Measurement of a Port with Tap Water

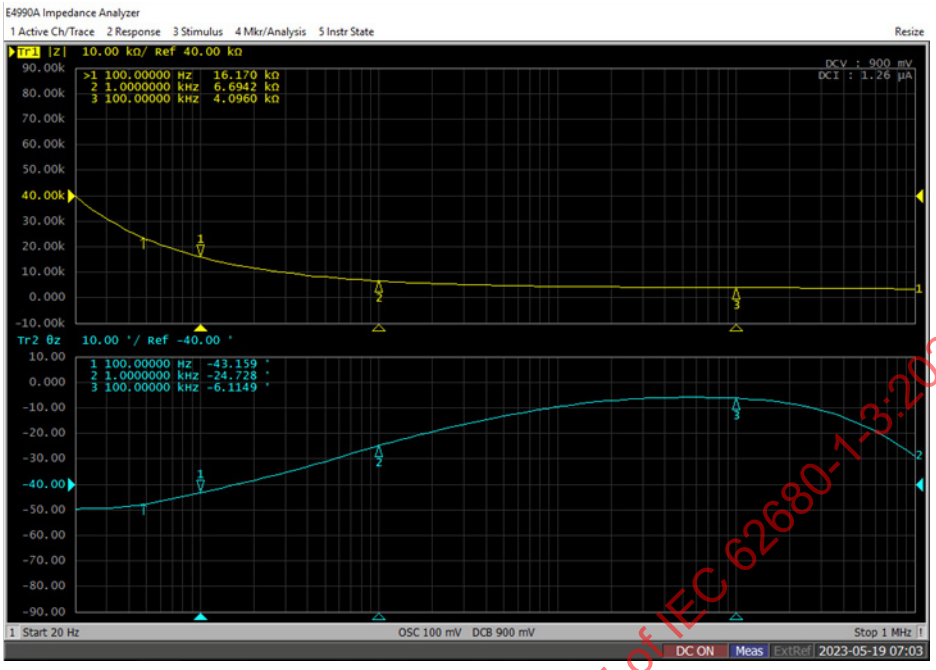
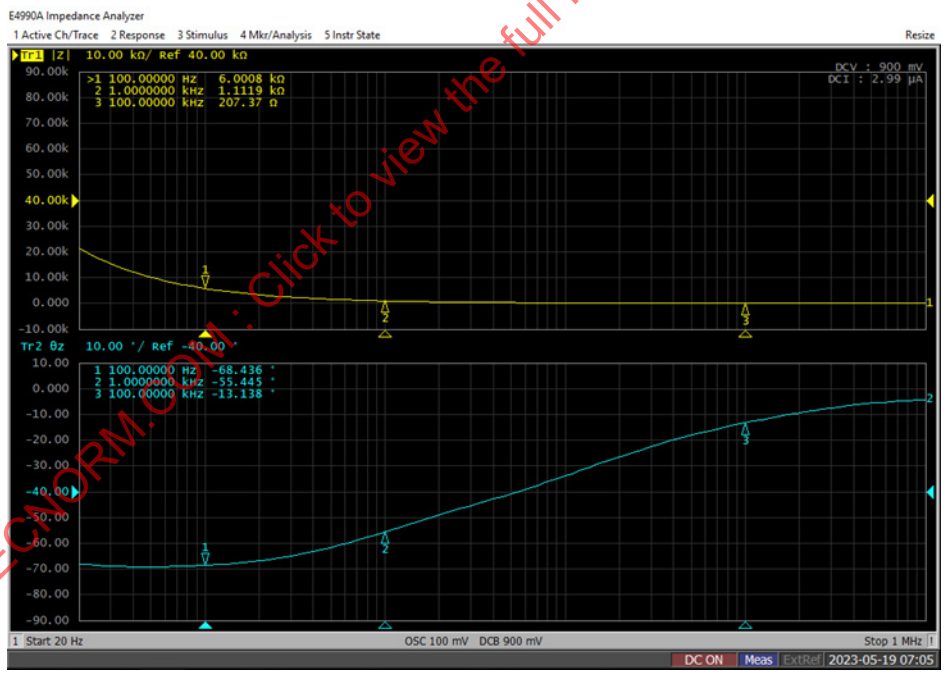
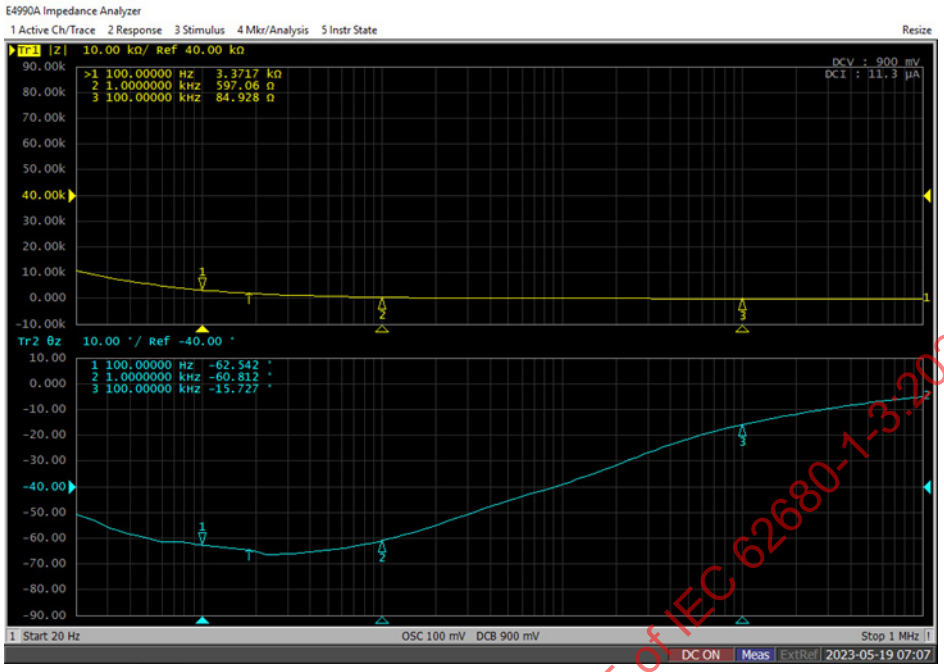


Figure A-10 Example Measurement of a Port with Artificial Sweat



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Figure A-11 Example Measurement of a Port with Ocean Water



A.4 Liquid Detection Pins in the Connector

Liquid may be detected by utilizing unused pin(s) in the connector or by adding dedicated pin(s)/pad(s) into the connector.

Key options and design areas that need attention.

1. When adding pin(s)/pad(s) to the connector, requirements found in Section 3.2.1 shall still be met.
2. This specification does not define standard locations for liquid detection pin(s)/pad(s). Figure A-12 shows a reference area within a receptacle where dedicated liquid detection (LD) pin(s)/pad(s) may be added. This region is between the normative pin mating area and the EMC pad. Utilizing this area for liquid detection pin(s)/pad(s) avoids interfering with either the normative plug pins or the EMC springs. It is recommended that the connector designer define the liquid detection pin(s)/pad(s) tolerances such that these pin(s)/pad(s) stay in the liquid detect zone in worse case tolerance.
3. Figure A-13 shows a reference receptacle with a liquid detection pad along the full width of the receptacle pins. Note, the reference receptacle shown is a PCB tongue with the ground mating locations on the metal frame encapsulating the edge.
4. Figure A-14 shows a reference receptacle with dedicated liquid detection pins between each VBUS and the adjacent CC and SBU pins. In this example, the liquid detection pins have been placed where typical corrosion damage is observed and where the connector is functionally most sensitive to shorts (impedance reduction) due to corrosion. Figure A-15 shows a view of an example surface mount footprint with the added pins. This can be applied to a vertical-mount, right-angle mount, or mid-mound receptacle.
5. Placement of the liquid detection pad or pins can affect the signal performance of the high-speed signaling path. The resulting shape and spacing of the high-speed pins should be analyzed to ensure it meets the signaling requirements of the high-speed protocol being used in the design. Interference of the high-speed signals from the liquid detection pin(s)/pad(s) due to the liquid detection method should also be analyzed.

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Figure A-12 Example Liquid Detect Pin(s)/Pad(s) Location Area

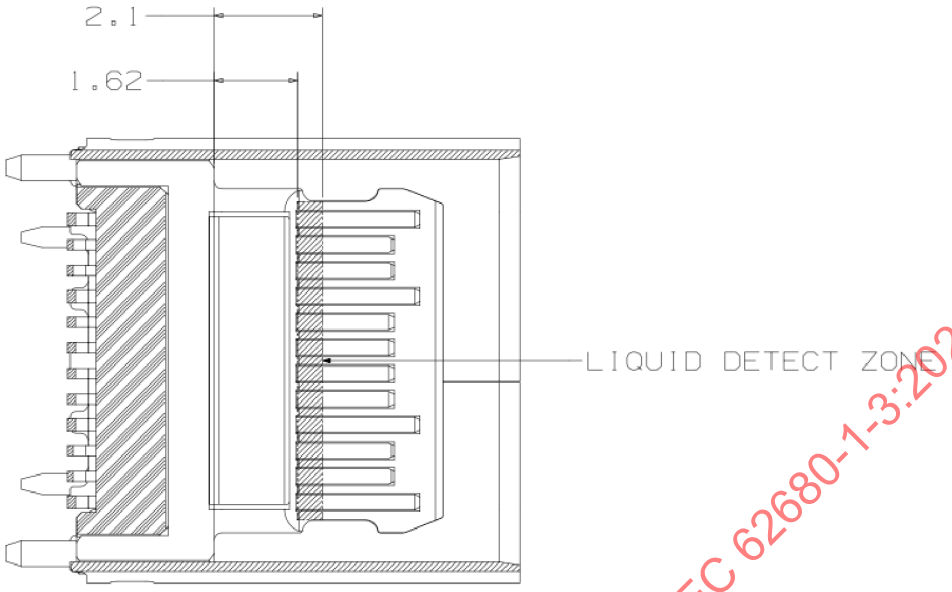
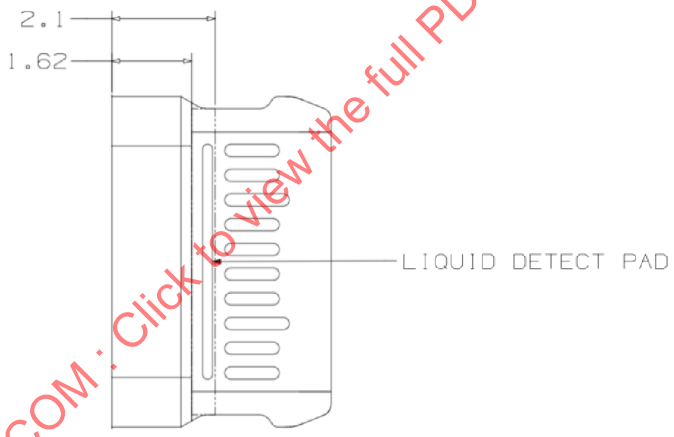


Figure A-13 Example Liquid Detect Pad Along All Connector Pins



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Figure A-14 Example Liquid Detect Pins Adjacent to VBUS/SBU/CC

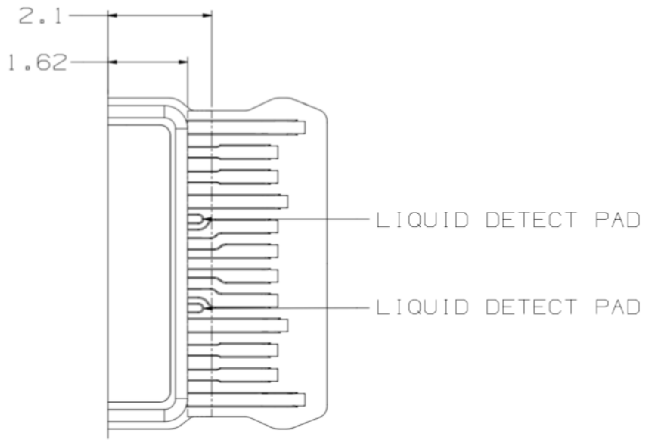
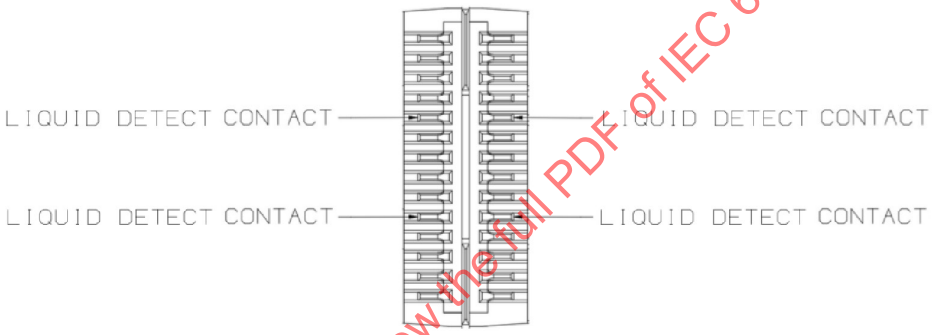


Figure A-15 Example Liquid Detect Connector Surface Mount View



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B Debug Accessory Mode

B.1 Overview

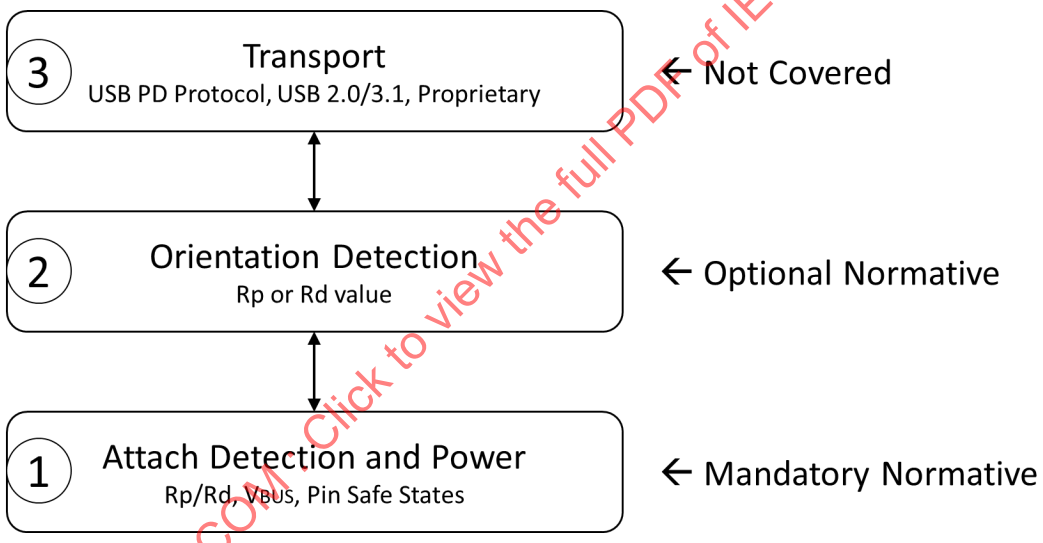
This appendix covers the functional requirements for the USB Type-C ***Debug Accessory Mode*** (***DAM***), ***Debug and Test System*** (DTS), and ***Target System*** (TS). The USB Type-C connector is ideal for the debug of closed-chassis, form-factor devices. Debug covers many areas, ranging from detailed JTAG Test Access Port (TAP)-level debug in a lab to high-level debug of software applications in production. Lab debug requires early debug access to hardware registers soon after reset, whereas software debug uses kernel debuggers, etc. to access software state. ***Debug Accessory Mode*** in USB Type-C enables debug of closed-chassis, form-factor devices by re-defining the USB Type-C ports for debug purposes.

Basic debug requirements are defined as a standard feature, and additional debug features ***may*** be added as per vendor specifications.

B.2 Functional

The USB Type-C ***Debug Accessory Mode*** follows a layered structure as shown in Figure B-1, defining the minimum physical layer for Attach, Detection and Power. Orientation detection is ***optional normative***. The transport layer is left proprietary and is not covered in this document.

Figure B-1 USB Type-C Debug Accessory Layered Behavior



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B.2.1 Signal Summary

Figure B-2 shows the pin assignments of the DTS plug that are used to support DAM. The pins highlighted in yellow are those available to be configured for debug signals. Both CC1 and CC2 are used for current advertisement and ***optional*** orientation detection.

Figure B-2 DTS Plug Interface

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2-	VBUS	SBU1	D-	D+	CC1	VBUS	TX1-	TX1+	GND
GND	TX2+	TX2-	VBUS	CC2	D+	D-	SBU2	VBUS	RX1-	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

The DTS and TS must follow the USB Safe State as defined in the ***USB PD*** specification at all times (whether in DAM or not).

B.2.2 Port Interoperability

Table B-1 summarizes the expected results when interconnecting a DTS Source, Sink or DRP port to a TS Source, Sink or DRP port.

Table B-1 DTS to TS Port Interoperability

	DTS Source	DTS Sink	DTS DRP
TS Sink	Functional	Non-Functional[1]	Functional
TS Sink w/ Accessory Support	Functional	Non-Functional[1]	Functional
TS DRP	Functional	Functional	Functional
TS Source	Non-Functional[1]	Functional	Functional

Note 1: In the cases where no function results, neither port ***shall*** be harmed by this connection. Following the USB Safe State ensures this.

B.2.3 Debug Accessory Mode Entry

The typical flow for the configuration of the interface in the general case of a DTS to a TS is as follows:

1. Detect a valid connection between the DTS (Source, Sink, or DRP) and TS (Source, Sink, or DRP)
2. ***Optionally*** determine orientation of the plug in the receptacle
3. ***Optionally*** establish ***USB PD*** communication over CC for advanced power delivery negotiation and ***Alternate Modes***. ***USB PD*** communication is allowed only if the ***optional*** orientation of the plug is determined.
4. Establish test access connections with the available USB Type-C signals

The DTS DRP will connect as either a Source or a Sink, but its state diagram gives preference to the Source role.

B.2.3.1 Detecting a Valid DTS-to-TS Connection

The general concept for setting up a valid connection between a DTS and TS is based on being able to detect the typical USB Type-C termination resistances. However, detecting a ***Debug Accessory Mode*** connection requires that both CC pins must detect a pull-up (***Rp***) or pull-down (***Rd***) termination. A USB Type-C Cable does not pass both CC wires so a receptacle to receptacle ***Debug Accessory Mode*** connection cannot be detected.

A DTS is only allowed to connect to a TS that is presenting either ***Rp***/***Rp*** or ***Rd***/***Rd***. Otherwise, the TS does not support ***Debug Accessory Mode***.

To detect either an ***Rp***/***Rp*** or ***Rd***/***Rd***, the DTS must be a captive cable or a direct-attach device with a USB Type-C plug and the TS must have a USB Type-C receptacle.

B.2.4 Connection State Diagrams

This section provides reference connection state diagrams for CC-based behaviors of the DTS. The TS connection state diagrams are found in Section 4.5.2.

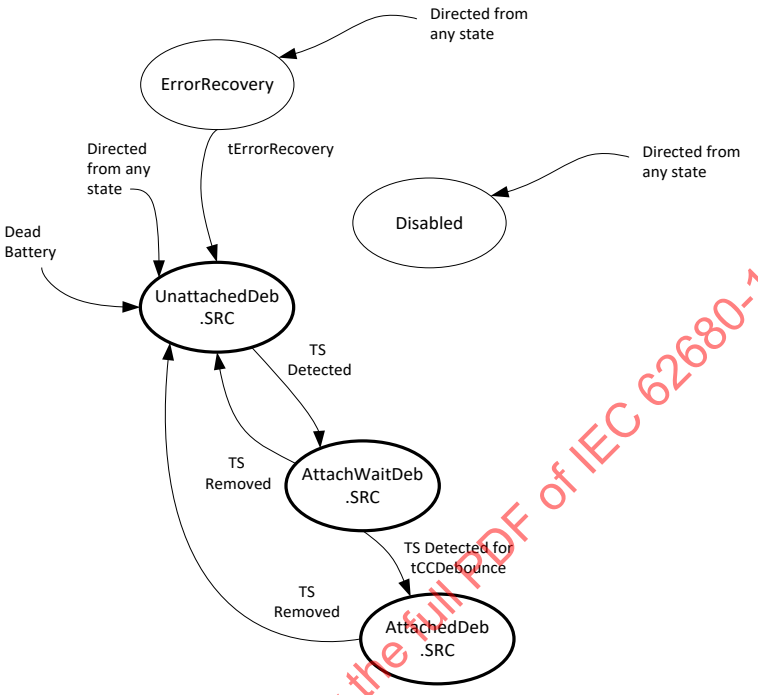
Refer to Section B.2.4.1 for the specific state transition requirements related to each state shown in the diagrams.

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Refer to Section B.2.4.3 for a description of which states are mandatory for each port type and a list of states where ***USB PD*** communication is permitted.

Figure B-3 illustrates a connection state diagram for a DTS Source.

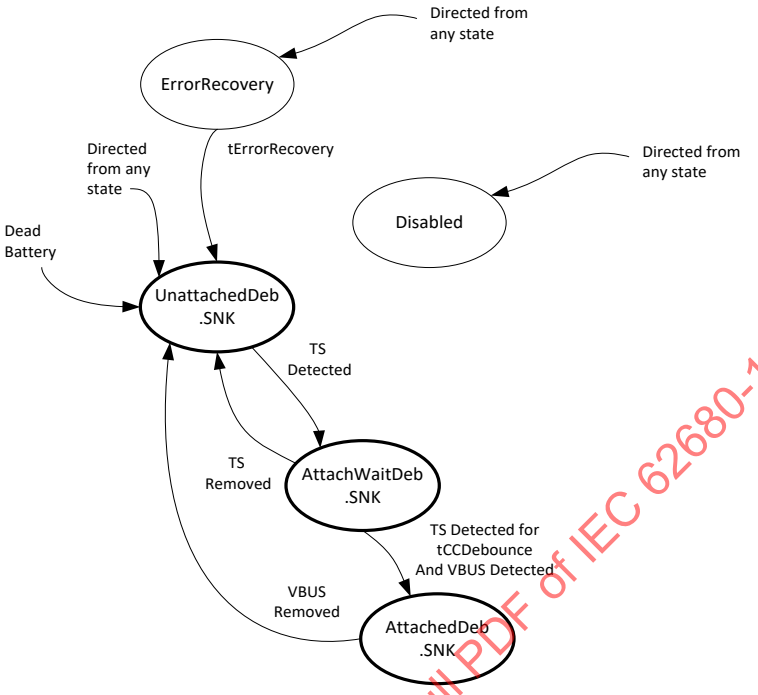
Figure B-3 Connection State Diagram: DTS Source



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Figure B-4 illustrates a connection state diagram for a simple DTS Sink.

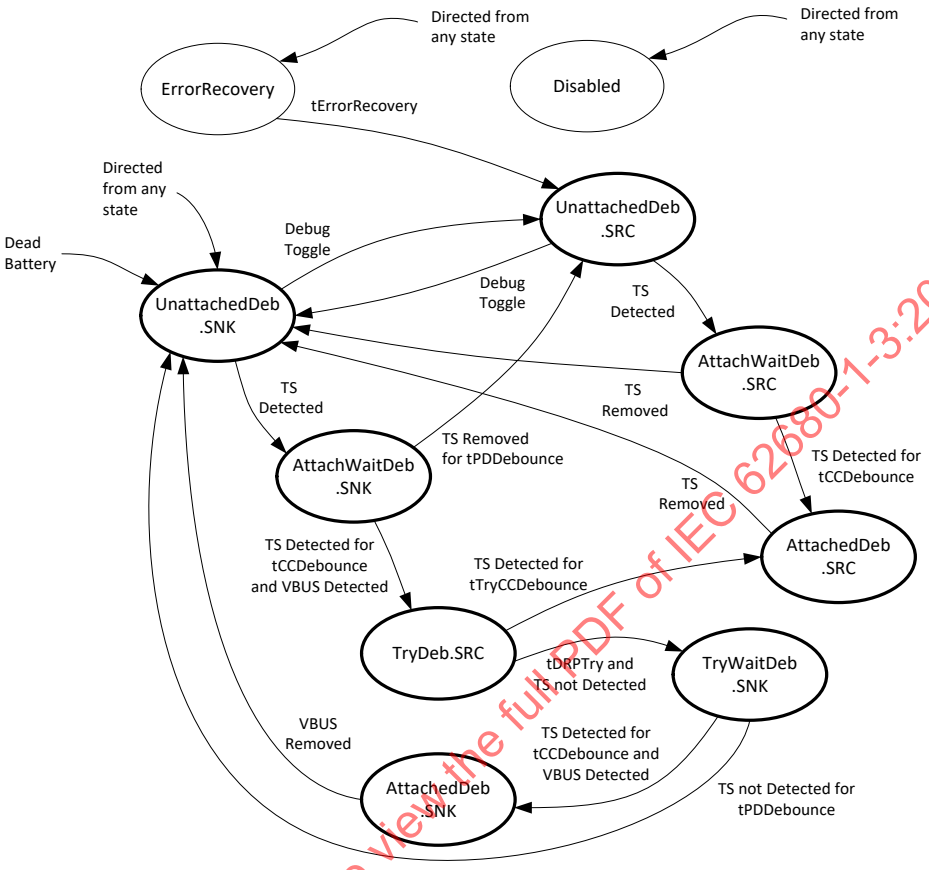
Figure B-4 Connection State Diagram: DTS Sink



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Figure B-5 illustrates a connection state diagram for a DTS DRP.

Figure B-5 Connection State Diagram: DTS DRP



B.2.4.1 Connection State Machine Requirements

The DTS state machine requirements follow those outlined in Section 4.5.2.2 for the general USB Type-C state machines with the additional following states defined.

Note, VCONN ***shall not*** be driven by any DTS or TS port in any state.

B.2.4.1.1 ErrorRecovery State

This state appears in Figure B-3, Figure B-4, and Figure B-5.

The ***ErrorRecovery*** state is where the DTS cycles its connection by removing all terminations from the CC pins for ***tErrorRecovery*** followed by transitioning to the appropriate ***UnattachedDeb.SNK*** or ***UnattachedDeb.SRC*** state based on DTS type.

The DTS ***should*** transition to the ***ErrorRecovery*** state from any other state when directed.

A DTS ***may*** choose not to support the ***ErrorRecovery*** state. If the ***ErrorRecovery*** state is not supported, the DTS ***shall*** be directed to the ***Disabled*** state if supported. If the ***Disabled*** state is not supported, the DTS ***shall*** be directed to either the ***UnattachedDeb.SNK*** or ***UnattachedDeb.SRC*** states.

A DTS Sink ***shall*** transition to ***UnattachedDeb.SNK*** after ***tErrorRecovery***.

A DTS Source ***shall*** transition to ***UnattachedDeb.SRC*** after ***tErrorRecovery***.

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A DTS DRP ***shall*** transition to ***UnattachedDeb.SRC*** after ***tErrorRecovery***.

B.2.4.1.2 UnattachedDeb.SNK State

This state appears in Figure B-4 and Figure B-5.

When in the ***UnattachedDeb.SNK*** state, the DTS is waiting to detect the presence of a TS Source.

A DTS with a dead battery ***shall*** enter this state while unpowered.

B.2.4.1.2.1 UnattachedDeb.SNK Requirements

The DTS ***shall not*** drive VBUS.

Both CC pins ***shall*** be independently terminated to ground through ***Rd***.

B.2.4.1.2.2 Exiting from UnattachedDeb.SNK State

The DTS ***shall*** transition to ***AttachWaitDeb.SNK*** when a TS Source connection is detected, as indicated by the ***SNK.Rp*** state on both of its CC pins.

A DTS DRP ***shall*** transition to ***UnattachedDeb.SRC*** within ***tDRPTransition*** after the state of one or both CC pins is ***SNK.Open*** for ***tDRP*** – ***dcSRC.DRP*** · ***tDRP***, or if directed.

B.2.4.1.3 AttachWaitDeb.SNK State

This state appears in Figure B-4 and Figure B-5.

When in the ***AttachWaitDeb.SNK*** state, the DTS has detected the ***SNK.Rp*** state on both CC pins and is waiting for VBUS.

B.2.4.1.3.1 AttachWaitDeb.SNK Requirements

The requirements for this state are identical to ***UnattachedDeb.SNK***.

B.2.4.1.3.2 Exiting from AttachWaitDeb.SNK State

A DTS Sink ***shall*** transition to ***UnattachedDeb.SNK*** when the state of one or both CC pins is ***SNK.Open*** for at least ***tPDDebounce***.

A DTS DRP ***shall*** transition to ***UnattachedDeb.SRC*** when the state of one or both CC pins is ***SNK.Open*** for at least ***tPDDebounce***.

A DTS Sink ***shall*** transition to ***AttachedDeb.SNK*** when neither CC pin is ***SNK.Open*** after ***tCCDebounce*** and VBUS is detected.

A DTS DRP ***shall*** transition to ***TryDeb.SRC*** when neither CC pin is ***SNK.Open*** after ***tCCDebounce*** and VBUS is detected.

B.2.4.1.4 AttachedDeb.SNK State

This state appears in Figure B-4 and Figure B-5.

When in the ***AttachedDeb.SNK*** state, the DTS is attached and operating as a DTS Sink.

B.2.4.1.4.1 AttachedDeb.SNK State Requirements

This mode is for debug only.

The port ***shall not*** drive VBUS.

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The port ***shall*** provide an ***Rd*** as specified in Table 4-17 on both CC pins if orientation is not needed. See Section B.2.6 for orientation detection.

The port ***shall*** monitor to detect when VBUS is removed.

If the DTS needs to establish ***USB PD*** communications, it ***shall*** do so only after entry to this state. In this state, the DTS takes on the initial ***USB PD*** role of UFP/Sink.

The DTS ***shall*** connect the debug signals for ***Debug Accessory Mode*** operation only after entry to this state.

The DTS ***may*** follow the DAM ***Sink Power Sub-State*** behavior specified in Section B.2.4.2.

B.2.4.1.4.2 Exiting from AttachedDeb.SNK State

A DTS ***shall*** transition to ***UnattachedDeb.SNK*** when VBUS is no longer present.

B.2.4.1.5 UnattachedDeb.SRC State

This state appears in Figure B-3 and Figure B-5.

When in the ***UnattachedDeb.SRC*** state, the DTS is waiting to detect the presence of a TS Sink.

B.2.4.1.5.1 UnattachedDeb.SRC Requirements

The DTS ***shall not*** drive VBUS.

The DTS ***shall*** source current on both CC pins independently.

The DTS ***shall*** provide a unique ***Rp*** value on each CC pin as specified in Section B.2.4.2.

B.2.4.1.5.2 Exiting from UnattachedDeb.SRC State

The DTS ***shall*** transition to ***AttachWaitDeb.SRC*** when the ***SRC.Rd*** state is detected on both CC pins.

A DTS DRP ***shall*** transition to ***UnattachedDeb.SNK*** within ***tDRPTransition*** after ***dcSRC.DRP · tDRP***, or if directed.

B.2.4.1.6 AttachWaitDeb.SRC State

This state appears in Figure B-3 and Figure B-5.

The ***AttachWaitDeb.SRC*** state is used to ensure that the state of both of the CC pins is stable after a TS Sink is connected.

B.2.4.1.6.1 AttachWaitDeb.SRC State Requirements

The requirements for this state are identical to ***UnattachedDeb.SRC***.

B.2.4.1.6.2 Exiting from AttachWaitDeb.SRC State

The DTS ***shall*** transition to ***AttachedDeb.SRC*** when VBUS is at ***vSafe0V*** and the ***SRC.Rd*** state is detected on both of the CC pins for at least ***tCCDebounce***.

A DTS Source ***shall*** transition to ***UnattachedDeb.SRC*** and a DTS DRP to ***UnattachedDeb.SNK*** when the ***SRC.Open*** state is detected on either of the CC pins.

B.2.4.1.7 AttachedDeb.SRC State

This state appears in Figure B-3 and Figure B-5.

When in the ***AttachedDeb.SRC*** state, the DTS is attached and operating as a DTS Source.

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B.2.4.1.7.1 AttachedDeb.SRC State Requirements

The DTS ***shall*** provide a unique ***Rp*** value on each CC pin as specified in Section B.2.4.2.

The DTS ***shall*** supply VBUS current at the level it advertises. See Section B.2.6.1.1 for advertising current level.

The DTS ***shall*** supply VBUS within ***tVBUSON*** of entering this state, and for as long as it is operating as a power source.

If the DTS needs to establish ***USB PD*** communications, it ***shall*** do so only after entry to this state. The DTS ***shall not*** initiate any ***USB PD*** communications until VBUS reaches ***vSafe5V***. In this state, the DTS takes on the initial ***USB PD*** role of DFP/Source.

The DTS ***shall*** connect the debug signals for ***Debug Accessory Mode*** operation only after entry to this state.

B.2.4.1.7.2 Exiting from AttachedDeb.SRC State

A DTS Source ***shall*** transition to ***UnattachedDeb.SRC*** when the ***SRC.Open*** state is detected on either CC pin.

A DTS DRP ***shall*** transition to ***UnattachedDeb.SNK*** when ***SRC.Open*** is detected on either CC pin.

A DTS ***shall*** cease to supply VBUS within ***tVBUSOFF*** of exiting ***AttachedDeb.SRC***.

B.2.4.1.8 TryDeb.SRC State

This state appears in Figure B-5.

When in the ***TryDeb.SRC*** state, the DTS DRP is querying to determine if the TS is also a DRP, to favor the DTS taking the Source role.

B.2.4.1.8.1 TryDeb.SRC State Requirements

The DTS ***shall not*** drive VBUS.

The DTS ***shall*** source current on both CC pins independently.

The DTS ***shall*** provide a unique ***Rp*** value on each CC pin as specified in Section B.2.4.2.

B.2.4.1.8.2 Exiting from TryDeb.SRC State

The DTS ***shall*** transition to ***AttachedDeb.SRC*** when the ***SRC.Rd*** state is detected on both CC pins for at least ***tTryCCDebounce***.

The DTS ***shall*** transition to ***TryWaitDeb.SNK*** after ***tDRPTry*** if the state of both CC pins is not ***SRC.Rd***.

B.2.4.1.9 TryWaitDeb.SNK State

This state appears in Figure B-5.

When in the ***TryWaitDeb.SNK*** state, the DTS has failed to become a DTS Source and is waiting to attach as a DTS Sink.

B.2.4.1.9.1 TryWaitDeb.SNK State Requirements

The DTS ***shall not*** drive VBUS.

Both CC pins ***shall*** be independently terminated to ground through ***Rd***.

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B.2.4.1.9.2 Exiting from TryWaitDeb.SNK State

The DTS ***shall*** transition to ***AttachedDeb.SNK*** when neither CC pin is ***SNK.Open*** after ***tCCDebounce*** and VBUS is detected.

The DTS ***shall*** transition to ***UnattachedDeb.SNK*** when the state of one of the CC pins is ***SNK.Open*** for at least ***tPDDebounce*** or if VBUS is not detected within ***tPDDebounce***.

B.2.4.2 Power Sub-State Requirements

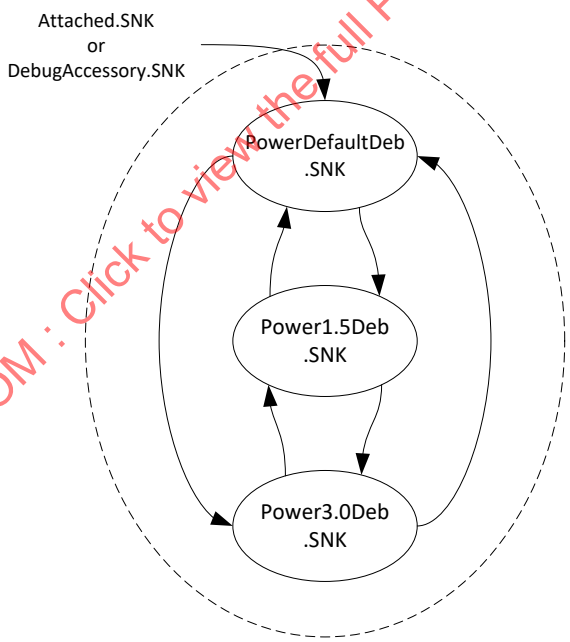
B.2.4.2.1 TS Sink Power Sub-State Requirements

When in the ***DebugAccessory.SNK*** state and the DTS Source is supplying default VBUS, the TS Sink ***shall*** operate in one of the sub-states shown in Figure B-6. The initial TS Sink Power Sub-State is PowerDefaultDeb.SNK. Subsequently, the TS Sink Power Sub-State is determined by the DTS Source's USB Type-C current advertisement determined by the ***Rp*** value on each CC pin as shown in Table B-2. The TS Sink in the attached state ***shall*** remain within the TS Sink Power Sub-States until either VBUS is removed, or a ***USB PD*** contract is established with the Source.

The TS Sink is only required to implement TS Sink Power Sub-State transitions if the TS Sink wants to consume more than default USB current.

Note, a TS Source will not use the values in Table B-2. A TS Source will present the same ***Rp*** on each CC pin using the standard ***Rp*** value for the desired current advertisement.

Figure B-6 TS Sink Power Sub-States



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Table B-2 Rp/Rp Charging Current Values for a DTS Source

Mode of Operation	CC1	CC2
Default USB Power	***Rp*** for 3 A	***Rp*** for 1.5 A
USB Type-C Current @ 1.5 A	***Rp*** for 1.5 A	***Rp*** for Default
USB Type-C Current @ 3 A	***Rp*** for 3 A	***Rp*** for Default

B.2.4.2.2 PowerDefaultDeb.SNK Sub-State

This sub-state supports DAM Sinks consuming current within the lowest range (default) of Source-supplied current.

B.2.4.2.2.1 PowerDefaultDeb.SNK Sub-State Requirements

The port ***shall*** draw no more than the default USB power from VBUS. See Section 4.6.2.1.

If the DTS Sink wants to consume more than the default USB power, it ***shall*** monitor ***vRd*** on both CC pins to determine if more current is available from the Source.

B.2.4.2.2.2 Exiting from PowerDefaultDeb.SNK Sub-State

For any change on CC indicating a change in allowable power, the DAM Sink ***shall not*** transition until the new ***vRd*** voltages on each CC pin have been stable for at least ***tRpValueChange***.

For ***vRd*** voltages on the CC pins indicating 1.5 A mode, the DAM Sink ***shall*** transition to the Power1.5Deb.SNK Sub-State.

For ***vRd*** voltages on the CC pins indicating 3 A mode, the DAM Sink ***shall*** transition to the Power3.0Deb.SNK Sub-State.

B.2.4.2.3 Power1.5Deb.SNK Sub-State

This sub-state supports DAM Sinks consuming current within the two lower ranges (default and 1.5 A) of DAM Source-supplied current.

B.2.4.2.3.1 Power1.5Deb.SNK Sub-State Requirements

The DAM Sink ***shall*** draw no more than 1.5 A from VBUS.

The DAM Sink ***shall*** monitor both ***vRd*** voltages while it is in this sub-state.

B.2.4.2.3.2 Exiting from Power1.5Deb.SNK Sub-State

For any change on the CC pins indicating a change in allowable power, the DAM Sink ***shall not*** transition until the new ***vRd*** voltages on both CC pins have been stable for at least ***tRpValueChange***.

For ***vRd*** voltages on the CC pins indicating Default USB Power mode, the port ***shall*** transition to the PowerDefaultDeb.SNK Sub-State and reduce its power consumption to the new range within ***tSinkAdj***.

For ***vRd*** voltages on the CC pins indicating 3 A mode, the port ***shall*** transition to the Power3.0Deb.SNK Sub-State.

B.2.4.2.4 Power3.0Deb.SNK Sub-State

This sub-state supports DAM Sinks consuming current within all three ranges (default, 1.5 A and 3.0 A) of DAM Source-supplied current.

B.2.4.2.4.1 Power3.0Deb.SNK Sub-State Requirements

The port ***shall*** draw no more than 3.0 A from VBUS.

The port ***shall*** monitor both ***vRd*** voltages while it is in this sub-state.

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B.2.4.2.4.2 Exiting from Power3.0Deb.SNK Sub-State

For any change on the CC pins indicating a change in allowable power, the port ***shall not*** transition until the new ***vRd*** voltages on both CC pins have been stable for at least ***tRpValueChange***.

For ***vRd*** voltages on the CC pins indicating Default USB Power mode, the port ***shall*** transition to the PowerDefaultDeb.SNK Sub-State and reduce its power consumption to the new range within ***tSinkAdj***.

For ***vRd*** voltages on the CC pins indicating 1.5 A mode, the DAM Sink ***shall*** transition to the Power1.5Deb.SNK Sub-State.

B.2.4.2.5 DTS Sink Power Sub-State Requirements

A DTS Sink follows the same power sub-states defined in Section 4.5.2.3. The TS Source will be advertising current with a standard ***Rp*** value that is the same for each CC pin. If ***optional*** orientation detection is performed, the DTS Sink will only be able to determine the ***Rp*** value from the CC pin that is set for ***USB PD*** communication.

B.2.4.3 Connection State Summary

Table B-3 defines the mandatory and ***optional*** states for each type of port. For states allowing ***USB PD*** communication, DAM connections requiring ***USB PD*** communication ***shall*** determine orientation by the steps described in Section B.2.6.

Table B-3 Mandatory and Optional States

	DTS Source	DTS Sink	DTS DRP	*USB PD* Communication and/or Debug Signal Activity
UnattachedDeb.SNK	***N/A***	Mandatory	Mandatory	Not Permitted
AttachWaitDeb.SNK	***N/A***	Mandatory	Mandatory	Not Permitted
AttachedDeb.SNK	***N/A***	Mandatory	Mandatory	Permitted
UnattachedDeb.SRC	Mandatory	***N/A***	Mandatory	Not Permitted
AttachWaitDeb.SRC	Mandatory	***N/A***	Mandatory	Not Permitted
AttachedDeb.SRC	Mandatory	***N/A***	Mandatory	Permitted
TryDeb.SRC	***N/A***	***N/A***	Mandatory	Not Permitted
TryWaitDeb.SNK	***N/A***	***N/A***	Mandatory	Not Permitted

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B.2.5 DTS Port Interoperability Behaviors

This section describes interoperability behavior between DTS ports and TS ports.

B.2.5.1 DTS Port to TS Port Interoperability Behaviors

The following sub-sections describe typical port-to-port interoperability behaviors for the various combinations of DTS and TS Sources, Sinks and DRPs as presented in Table B-1.

B.2.5.1.1 DTS Source to TS Sink Behavior

The following describes the behavior when a DTS Source is connected to a TS Sink.

1. DTS Source and TS Sink in the unattached state.

2. DTS Source transitions from ***UnattachedDeb.SRC*** to ***AttachedDeb.SRC*** through ***AttachWaitDeb.SRC***.
    - DTS Source detects the TS Sink's pull-downs on both CC pins and enters ***AttachWaitDeb.SRC***. After ***tCCDebounce*** it then enters ***AttachedDeb.SRC***.
    - DTS Source turns on VBUS.
3. TS Sink transitions from ***Unattached.SNK*** to ***DebugAccessory.SNK*** through ***AttachWait.SNK***.
    - TS Sink in ***Unattached.SNK*** detects the DTS Source's pull-ups on both CC pins and enters ***AttachWait.SNK***. After that state persists for ***tCCDebounce*** and it detects VBUS, it enters ***DebugAccessory.SNK***.
4. While the DTS Source and TS Sink are in the attached state:
    - DTS Source adjusts both ***Rp*** values as needed for offered current.
    - TS Sink detects and monitors ***vRd*** on the CC pins for available current on VBUS and performs any orientation required.
    - DTS Source monitors both CC pins for detach and when detected on either pin, enters ***UnattachedDeb.SRC***.
    - TS Sink monitors VBUS for detach and when detected, enters ***Unattached.SNK***.

B.2.5.1.2 DTS Source to TS DRP Behavior

The following describes the behavior when a DTS Source is connected to a TS DRP.

1. DTS Source and TS DRP in the unattached state.
    - TS DRP alternates between ***Unattached.SRC*** and ***Unattached.SNK***.
2. DTS Source transitions from ***UnattachedDeb.SRC*** to ***AttachedDeb.SRC*** through ***AttachWaitDeb.SRC***.
    - DTS Source detects the TS DRP's pull-downs on both CC pins and enters ***AttachWaitDeb.SRC***. After ***tCCDebounce*** it then enters ***AttachedDeb.SRC***.
    - DTS Source turns on VBUS.
3. TS DRP transitions from ***Unattached.SNK*** to ***DebugAccessory.SNK*** through ***AttachWait.SNK***.
    - TS DRP in ***Unattached.SNK*** detects the DTS Source's pull-ups on both CC pins and enters ***AttachWait.SNK***. After that state persists for ***tCCDebounce*** and it detects VBUS, it enters ***DebugAccessory.SNK***.
4. While the DTS Source and TS DRP are in their respective attached states:
    - DTS Source adjusts both ***Rp*** values as needed for offered current.
    - TS DRP detects and monitors ***vRd*** on both CC pins for available current on VBUS and performs any orientation required.
    - DTS Source monitors both CC pins for detach, and when detected, enters ***UnattachedDeb.SRC***.
    - TS DRP monitors VBUS for detach and when detected, enters ***Unattached.SNK*** (and resumes toggling between ***Unattached.SNK*** and ***Unattached.SRC***).

B.2.5.1.3 DTS Sink to TS Source Behavior

The following describes the behavior when a DTS Sink is connected to a TS Source.

1. TS Source and DTS Sink in the unattached state.
2. TS Source transitions from ***Unattached.SRC*** to ***UnorientedDebugAccessory.SRC*** through ***AttachWait.SRC***.
    - TS Source detects the DTS Sink's pull-downs on both CC pins and enters ***AttachWait.SRC***. After ***tCCDebounce***, it enters ***UnorientedDebugAccessory.SRC***.

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- TS Source turns on VBUS.

3. DTS Sink transitions from ***UnattachedDeb.SNK*** to ***AttachedDeb.SNK*** through ***AttachWaitDeb.SNK***.
   - DTS Sink in ***UnattachedDeb.SNK*** detects the TS Source's pull-ups on both CC pins and enters ***AttachWaitDeb.SNK***.
   - DTS Sink in ***AttachWaitDeb.SNK*** detects that the pull-ups on both CC pins persist for ***tCCDebounce*** and it detects VBUS. It enters ***AttachedDeb.SNK***.
   - DTS sink determines advertised current from ***vRd*** on either CC pin.
4. If orientation supported, DTS Sink adjusts ***Rd*** on the non-CC communication pin as needed for orientation detection.
5. If orientation supported, TS Source detects change in ***vRd*** of one of the CC pins and transitions from ***UnorientedDebugAccessory.SRC*** to ***OrientedDebugAccessory.SRC*** and performs any orientation required.
6. While the TS Source and DTS Sink are in the attached state:
   - If orientation is supported, DTS sink determines any change in advertised current from ***vRd*** of the CC pin that has been set as the CC communication pin.
   - TS Source monitors both CC pins for detach and when detected, enters ***Unattached.SRC***.
   - DTS Sink monitors VBUS for detach and when detected, enters ***UnattachedDeb.SNK***.

B.2.5.1.4 DTS Sink to TS DRP Behavior

The following describes the behavior when a DTS Sink is connected to a TS DRP.

1. DTS Sink and TS DRP in the unattached state.
   - TS DRP alternates between ***Unattached.SRC*** and ***Unattached.SNK***.
2. TS DRP transitions from ***Unattached.SRC*** to ***UnorientedDebugAccessory.SRC*** through ***AttachWait.SRC***.
   - TS DRP in ***Unattached.SRC*** detects both CC pull-downs of DTS Sink in ***UnattachedDeb.SNK*** and enters ***AttachWait.SRC***.
   - TS DRP in ***AttachWait.SRC*** detects that the pull-downs on both CC pins persist for ***tCCDebounce***. It then enters ***UnorientedDebugAccessory.SRC*** and turns on VBUS.
3. DTS Sink transitions from ***UnattachedDeb.SNK*** to ***AttachedDeb.SNK*** through ***AttachWaitDeb.SNK***.
   - DTS Sink in ***UnattachedDeb.SNK*** detects the TS DRP's pull-ups on both CC pins and enters ***AttachWaitDeb.SNK***. After that state persists for ***tCCDebounce*** and it detects VBUS, it enters ***AttachedDeb.SNK***.
   - DTS sink determines advertised current from ***vRd*** on either CC pin.
7. If orientation is supported, DTS Sink adjusts ***Rd*** on the non-CC communication pin as needed for orientation detection.
8. If orientation supported, TS DRP detects change in ***vRd*** on one of the CC pins and transitions to ***OrientedDebugAccessory.SRC*** and performs the required orientation.
9. While the TS DRP and DTS Sink are in the attached state:
   - If orientation is supported, DTS sink determines any change in advertised current from ***vRd*** of the CC pin that has been set as the CC communication pin.
   - TS DRP monitors both CC pins for detach and when detected, enters ***Unattached.SNK***.
   - DTS Sink monitors VBUS for detach and when detected, enters ***UnattachedDeb.SNK***.

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B.2.5.1.5 DTS DRP to TS Sink Behavior

The following describes the behavior when a DTS DRP is connected to a TS Sink.

1. DTS DRP and TS Sink in the unattached state.
   - DTS DRP alternates between ***UnattachedDeb.SRC*** and ***UnattachedDeb.SNK***.
2. DTS DRP transitions from ***UnattachedDeb.SRC*** to ***AttachedDeb.SRC*** through ***AttachWaitDeb.SRC***.
   - DTS DRP in ***UnattachedDeb.SRC*** detects both of the CC pull-downs of TS Sink enters ***AttachWaitDeb.SRC***.
   - DTS DRP in ***AttachWaitDeb.SRC*** detects that the pull-downs on both CC pins persist for ***tCCDebounce***. It then enters ***AttachedDeb.SRC***.
   - DTS DRP turns on VBUS.
3. TS Sink transitions from ***Unattached.SNK*** to ***DebugAccessory.SNK*** through ***AttachWait.SNK***.
   - TS Sink in ***Unattached.SNK*** detects the DTS DRP's pull-ups on both CC pins and enters ***AttachWait.SNK***.
   - TS Sink in ***AttachWait.SNK*** detects that the pull-ups on both CC pins persist for ***tCCDebounce*** and it detects VBUS. It enters ***DebugAccessory.SNK***.
4. While the DTS DRP and TS Sink are in their respective attached states:
   - DTS DRP adjusts ***Rp*** as needed for offered current.
   - TS Sink detects and monitors ***vRd*** on the CC pins for available current on VBUS and performs any orientation required.
   - DTS DRP monitors both CC pins for detach and when detected, enters ***UnattachedDeb.SNK***.
   - TS Sink monitors VBUS for detach and when detected, enters ***Unattached.SNK***.

B.2.5.1.6 DTS DRP to TS DRP Behavior

The following describes the behavior when a DTS DRP is connected to TS DRP.

Case #1:

1. Both DRPs in the unattached state.
   - DTS DRP alternates between ***UnattachedDeb.SRC*** and ***UnattachedDeb.SNK***.
   - TS DRP alternate between ***Unattached.SRC*** and ***Unattached.SNK***.
2. DTS DRP transitions from ***UnattachedDeb.SRC*** to ***AttachWaitDeb.SRC***.
   - DTS DRP in ***UnattachedDeb.SRC*** detects both CC pull-downs of TS DRP in ***Unattached.SNK*** and enters ***AttachWaitDeb.SRC***.
3. TS DRP transitions from ***Unattached.SNK*** to ***AttachWait.SNK***.
   - TS DRP in ***Unattached.SNK*** detects both CC pull-ups of DTS DRP and enters ***AttachWait.SNK***.
4. DTS DRP transitions from ***AttachWaitDeb.SRC*** to ***AttachedDeb.SRC***.
   - DTS DRP in ***AttachWaitDeb.SRC*** continues to see both CC pull-downs of TS DRP for ***tCCDebounce***, enters ***AttachedDeb.SRC*** and turns on VBUS.
5. TS DRP transitions from ***AttachWait.SNK*** to ***DebugAccessory.SNK***.
   - TS DRP detects DTS DRP's pull-ups on both CC pins for ***tCCDebounce*** and detects VBUS and enters ***DebugAccessory.SNK***.
   - TS DRP detects and monitors ***vRd*** on the CC pins for available current on VBUS and performs any orientation required.

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6. While the TS DRP and DTS DRP are in the attached state:
    - TS DRP monitors VBUS for detach and when detected, enters ***Unattached.SNK***.
    - DTS DRP monitors both CC pins for detach and when detected, enters ***UnattachedDeb.SNK***.

Case #2:

1. Both DRPs in the unattached state.
    - DTS DRP alternates between ***UnattachedDeb.SRC*** and ***UnattachedDeb.SNK***.
    - TS DRP alternates between ***Unattached.SRC*** and ***Unattached.SNK***.
2. DTS DRP transitions from ***UnattachedDeb.SNK*** to ***AttachWaitDeb.SNK***.
    - DTS DRP in ***UnattachedDeb.SNK*** detects both CC pull-ups of TS DRP in ***Unattached.SRC*** and enters ***AttachWaitDeb.SNK***.
3. TS DRP transitions from ***Unattached.SRC*** to ***UnorientedDebugAccessory.SRC*** through ***AttachWait.SRC***.
    - TS DRP in ***Unattached.SRC*** detects both CC pull-downs of DTS DRP and enters ***AttachWait.SRC***.
    - TS DRP in ***AttachWait.SRC*** continues to see both CC pull-downs of TS DRP for ***tCCDebounce***, enters ***UnorientedDebugAccessory.SRC*** and turns on VBUS.
4. DTS DRP transitions from ***AttachWaitDeb.SNK*** to ***TryDeb.SRC***.
    - DTS DRP in ***AttachWaitDeb.SNK*** continues to see both CC pull-ups of TS DRP for ***tCCDebounce*** and detects VBUS, enters ***TryDeb.SRC***.
5. TS DRP transitions from ***UnorientedDebugAccessory.SRC*** to ***Unattached.SNK***.
    - TS DRP in ***UnorientedDebugAccessory.SRC*** detects the removal of both CC pull-downs of DTS DRP and enters ***Unattached.SNK***.
6. TS DRP transitions from ***Unattached.SNK*** to ***AttachWait.SNK***.
    - TS DRP in ***Unattached.SNK*** detects both CC pull-ups of DTS DRP and enters ***AttachWait.SNK***.
7. DTS DRP transitions from ***TryDeb.SRC*** to ***AttachedDeb.SRC***.
    - DTS DRP in ***TryDeb.SRC*** detects both CC pull-downs of TS DRP for ***tTryCCDebounce*** and enters ***AttachedDeb.SRC***.
    - DTS DRP turns on VBUS.
8. TS DRP transitions from ***AttachWait.SNK*** to ***DebugAccessory.SNK***.
    - TS DRP detects DTS DRP's pull-ups on both CC pins for ***tCCDebounce*** and detects VBUS and enters ***DebugAccessory.SNK***.
9. While the DTS DRP and TS DRP are in their respective attached states:
    - DTS DRP adjusts ***Rp*** as needed for offered current.
    - TS DRP detects and monitors ***vRd*** on the CC pins for available current on VBUS and performs any orientation required.
    - DTS DRP monitors both CC pins for detach and when detected, enters ***UnattachedDeb.SNK***.
    - TS DRP monitors VBUS for detach and when detected, enters ***Unattached.SNK***.

B.2.5.1.7 DTS DRP to TS Source Behavior

The following describes the behavior when a DTS DRP is connected to TS Source.

1. DTS DRP and TS Source in the unattached state.

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- DTS DRP alternates between ***UnattachedDeb.SRC*** and ***UnattachedDeb.SNK***.
- TS Source in ***Unattached.SRC***.

2. DTS DRP transitions from ***UnattachedDeb.SNK*** to ***AttachWaitDeb.SNK***.
   - DTS DRP in ***UnattachedDeb.SNK*** detects pull-ups on both CC pins and enters ***AttachWaitDeb.SNK***.
3. TS Source transitions from ***Unattached.SRC*** to ***UnorientedDebugAccessory.SRC*** through ***AttachWait.SRC***.
   - TS Source in ***Unattached.SRC*** detects both CC pull-downs of DTS DRP and enters ***AttachWait.SRC***.
   - TS Source in ***AttachWait.SRC*** continues to see both CC pull-downs of DTS DRP for ***tCCDebounce***, enters ***UnorientedDebugAccessory.SRC*** and turns on VBUS.
4. DTS DRP transitions from ***AttachWaitDeb.SNK*** to ***TryDeb.SRC***.
   - DTS DRP in ***AttachWaitDeb.SNK*** continues to see both CC pull-ups of TS DRP for ***tCCDebounce*** and detects VBUS, enters ***TryDeb.SRC***.
5. TS Source transitions from ***UnorientedDebugAccessory.SRC*** to ***Unattached.SRC***.
   - TS Source in ***UnorientedDebugAccessory.SRC*** detects the removal of both CC pull-downs of DTS DRP and enters ***Unattached.SRC***.
6. DTS DRP transitions from ***TryDeb.SRC*** to ***TryWaitDeb.SNK***.
   - After ***tDRPTry***, DTS DRP does not see pull-downs on both CC pin and enters ***TryWaitDeb.SNK***
7. TS Source transitions from ***Unattached.SRC*** to ***UnorientedDebugAccessory.SRC***.
   - TS Source in ***Unattached.SRC*** detects pull-downs on both CC pins and enters ***AttachWait.SRC***.
   - TS Source continues to detect pull-downs on both CC pins for ***tCCDebounce*** and enters ***UnorientedDebugAccessory.SRC*** and outputs VBUS.
8. DTS DRP transitions from ***TryWaitDeb.SNK*** to ***AttachedDeb.SNK***.
   - DTS DRP sees pull-ups on both CC pins for ***tCCDebounce*** and detects VBUS and enters ***AttachedDeb.SNK***.
   - If orientation required, DTS DRP adjusts ***Rd*** on the non-CC communication pin as needed for orientation detection
9. If orientation supported, TS Source detects change in ***vRd*** on one of the CC pins and transitions to ***OrientedDebugAccessory.SRC*** and performs the required orientation.
10. While the TS Source and DTS DRP are in the attached state:
    - If orientation is supported, DTS DRP determines any change in advertised current from ***vRd*** of the CC pin that has been set as the CC communication pin.
    - TS Source monitors both CC pins for detach and when detected, enters ***Unattached.SRC***.
    - DTS DRP monitors VBUS for detach and when detected, enters ***UnattachedDeb.SNK***.

B.2.5.2 DTS Port to non-DAM TS Port Interoperability Behaviors

The following sub-sections describe the non-functional port-to-port interoperability behaviors for the various combinations of DTS and TS Sources, Sinks, and DRPs that do not support DAM.

B.2.5.2.1 DTS Source to non-DAM TS Sink Behavior

The following describes the behavior when a DTS Source is connected to a non-DAM TS Sink.

1. DTS Source and TS Sink in the unattached state.

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2. DTS Source transitions from ***UnattachedDeb.SRC*** to ***AttachedDeb.SRC*** through ***AttachWaitDeb.SRC***.
    - DTS Source detects the non-DAM TS Sink's pull-downs on both CC pins and enters ***AttachWaitDeb.SRC***. After ***tCCDebounce*** it then enters ***AttachedDeb.SRC***.
    - DTS Source turns on VBUS.
3. Non-DAM TS Sink transitions from ***Unattached.SNK*** to ***AttachWait.SNK***.
    - Non-DAM TS Sink in ***Unattached.SNK*** detects the DTS Source's pull-ups on both CC pins and enters ***AttachWait.SNK***.
    - Non-DAM TS Sink continues to detect pull-ups on both CC pins and stays in ***AttachWait.SNK*** because it does not support DAM (will not enter ***Attached.SNK*** because it does not detect ***SNK.Open*** on either pin).
4. While the DTS Source and non-DAM TS Sink are in their final state:
    - DTS Source adjusts ***Rp*** as needed for offered current.
    - Non-DAM TS Sink ***may*** draw USB default current from DTS Source as permitted by Section 4.5.2.3 but will not enter DAM.
    - DTS Source monitors both CC pins for detach and when detected, enters ***UnattachedDeb.SRC***.
    - Non-DAM TS Sink monitors both CC pins for detach and when detected, enters ***Unattached.SNK***.

B.2.5.2.2 DTS Source to non-DAM TS DRP Behavior

The following describes the behavior when a DTS Source is connected to a non-DAM TS DRP.

1. DTS Source and non-DAM TS DRP in the unattached state.
    - Non-DAM TS DRP alternates between ***Unattached.SRC*** and ***Unattached.SNK***.
2. DTS Source transitions from ***UnattachedDeb.SRC*** to ***AttachedDeb.SRC*** through ***AttachWaitDeb.SRC***.
    - DTS Source detects the non-DAM TS Sink's pull-downs on both CC pins and enters ***AttachWaitDeb.SRC***. After ***tCCDebounce*** it then enters ***AttachedDeb.SRC***.
    - DTS Source turns on VBUS.
3. Non-DAM TS DRP transitions from ***Unattached.SNK*** to ***AttachWait.SNK***.
    - Non-DAM TS DRP in ***Unattached.SNK*** detects the DTS Source's pull-ups on both CC pins and enters ***AttachWait.SNK***.
    - Non-DAM TS DRP continues to detect pull-downs on both CC pins and stays in ***AttachWait.SNK*** because it does not support DAM (will not enter ***Attached.SNK*** because it does not detect ***SNK.Open*** on either pin)
4. While the DTS Source and non-DAM TS DRP are in their final state:
    - DTS Source adjusts ***Rp*** as needed for offered current.
    - Non-DAM TS DRP ***may*** draw USB default current from DTS Source as permitted by Section 4.5.2.3 but will not enter DAM.
    - DTS Source monitors both CC pins for detach and when detected, enters ***UnattachedDeb.SRC***.
    - Non-DAM TS DRP monitors both CC pins for detach and when detected, enters ***Unattached.SRC***.

B.2.5.2.3 DTS Sink to non-DAM TS Source Behavior

The following describes the behavior when a DTS Sink is connected to a non-DAM TS Source.

1. Non-DAM TS Source and DTS Sink in the unattached state.

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2. Non-DAM TS Source transitions from ***Unattached.SRC*** to ***AttachWait.SRC***.
    - Non-DAM TS Source detects the DTS Sink's pull-downs on both CC pins and enters ***AttachWait.SRC***.
    - Non-DAM TS Source continues to detect pull-downs on both CC pins and stays in ***AttachWait.SRC*** because it does not support DAM (will not enter ***Attached.SRC*** because it does not detect ***SRC.Rd*** on only one CC pin).
3. DTS Sink transitions from ***UnattachedDeb.SNK*** to ***AttachWaitDeb.SNK***.
    - DTS Sink in ***UnattachedDeb.SNK*** detects the non-DAM TS Source's pull-ups on both CC pins and enters ***AttachWaitDeb.SNK***.
    - DTS Sink remains in ***AttachWaitDeb.SNK*** because it does not detect VBUS.
4. While the non-DAM TS Source and DTS Sink are in their final state:
    - Non-DAM TS Source monitors both CC pins for detach and when detected, enters ***Unattached.SRC***
    - DTS Sink monitors VBUS for attach and both CC pins for detach and enters ***UnattachedDeb.SNK*** when both CC pins go to ***SNK.Open***.

B.2.5.2.4 DTS Sink to non-DAM TS DRP Behavior

The following describes the behavior when a DTS Sink is connected to a non-DAM TS DRP.

1. DTS Sink and non-DAM TS DRP in the unattached state.
    - Non-DAM TS DRP alternates between ***Unattached.SRC*** and ***Unattached.SNK***.
    - DTS Sink in ***UnattachedDeb.SNK***.
2. Non-DAM TS DRP transitions from ***Unattached.SRC*** to ***AttachWait.SRC***.
    - Non-DAM TS DRP detects the DTS Sink's pull-downs on both CC pins and enters ***AttachWait.SRC***.
    - Non-DAM TS DRP continues to detect pull-downs on both CC pins and stays in ***AttachWait.SRC*** because it does not support DAM (will not enter ***Attached.SRC*** because it does not detect ***SRC.Rd*** on only one CC pin).
3. DTS Sink transitions from ***UnattachedDeb.SNK*** to ***AttachWaitDeb.SNK***.
    - DTS Sink in ***UnattachedDeb.SNK*** detects the non-DAM TS DRP's pull-ups on both CC pins and enters ***AttachWaitDeb.SNK***.
    - DTS Sink remains in ***AttachWaitDeb.SNK*** because it does not detect VBUS.
4. While the non-DAM TS DRP and DTS Sink are in their final state:
    - Non-DAM TS DRP monitors both CC pins for detach and when detected, enters ***Unattached.SNK***.
    - DTS Sink monitors VBUS for attach and both CC pins for detach and enters ***UnattachedDeb.SNK*** when both CC pin go to ***SNK.Open***.

B.2.5.2.5 DTS DRP to non-DAM TS Sink Behavior

The DTS DRP to non-DAM TS Sink behavior follows the flow in Section B.2.5.2.1.

B.2.5.2.6 DTS DRP to non-DAM TS DRP Behavior

The DTS DRP to non-DAM TS DRP behavior follows the flows in Section B.2.5.2.2 and Section B.2.5.2.4 depending on the role forced by the non-DAM TS DRP.

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B.2.5.2.7 DTS DRP to non-DAM TS Source Behavior

The following describes the behavior when a DTS DRP is connected to non-DAM TS Source.

1. DTS DRP and non-DAM TS Source in the unattached state.
   - DTS DRP alternates between ***UnattachedDeb.SRC*** and ***UnattachedDeb.SNK***.
   - Non-DAM TS Source in ***Unattached.SRC***.
2. DTS DRP transitions from ***UnattachedDeb.SNK*** to ***AttachWaitDeb.SNK***.
   - DTS DRP in ***UnattachedDeb.SNK*** detects pull-ups on both CC pins and enters ***AttachWaitDeb.SNK***.
3. Non-DAM TS Source transitions from ***Unattached.SRC*** to ***AttachWait.SRC***.
   - Non-DAM TS Source in ***Unattached.SRC*** detects pull-downs on both CC pins and enters ***AttachWait.SRC***.
   - Non-DAM TS Source continues to detect pull-downs on both CC pins and stays in ***AttachWait.SRC*** because it does not support DAM (will not enter ***Attached.SRC*** because it does not detect ***SRC.Rd*** on only one CC pin).
   - DTS Sink remains in ***AttachWaitDeb.SNK*** because it does not detect VBUS.
5. While the non-DAM TS Source and DTS DRP are in their final state:
   - Non-DAM TS Source monitors both CC pins for detach and when detected, enters ***Unattached.SRC***.
   - DTS DRP monitors VBUS for attach and both CC pins for detach and enters ***UnattachedDeb.SRC*** when both CC pin go to ***SNK.Open***.

B.2.5.2.8 DTS Sink to non-DAM TS Sink with Accessory Support Behavior

The following describes the behavior when a DTS Sink is connected to a non-DAM USB Type-C TS Sink with Accessory Support.

1. DTS Sink and non-DAM TS Sink with Accessory Support (“non-DAM TS Sink” for the remainder of this flow) in the unattached state.
   - Non-DAM TS Sink alternates between ***Unattached.SNK*** and ***Unattached.Accessory***.
   - DTS Sink in ***UnattachedDeb.SNK***.
2. Non-DAM TS Sink transitions from ***Unattached.Accessory*** to ***AttachWait.Accessory***.
   - Non-DAM TS Sink detects the DTS Sink’s pull-downs on both CC pins and enters ***AttachWait.Accessory***.
   - Non-DAM TS Sink continues to detect pull-downs on both CC pins and enters USB Type-C ***Debug Accessory Mode***.
3. DTS Sink transitions from ***UnattachedDeb.SNK*** to ***AttachWaitDeb.SNK***.
   - DTS Sink in ***UnattachedDeb.SNK*** detects the non-DAM TS Sinks pull-ups on both CC pins and enters ***AttachWaitDeb.SNK***.
   - DTS Sink remains in ***AttachWaitDeb.SNK*** because it does not detect VBUS.
4. While the non-DAM TS DRP and DTS Sink are in their final state:
   - Non-DAM TS Sink monitors both CC pins for detach and when detected, enters ***Unattached.SNK***.
   - DTS Sink monitors both CC pins for detach and enters ***UnattachedDeb.SNK*** when both CC pins go to ***SNK.Open***.

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B.2.6 Orientation Detection

Orientation detection is ***optional normative***. A USB Type-C port supporting ***Debug Accessory Mode*** is not required to perform orientation detection. If orientation detection is required, this method ***shall*** be followed.

B.2.6.1 Orientation Detection using Rd and/or Rp Values

In this ***optional normative*** flow, the DTS ***shall*** always initiate an orientation detection sequence, independent of its role as Source, Sink, or DRP. This means that the TS must detect this orientation sequence and perform multiplexing to orient and connect the port signals to the proper channels as well as determine the proper CC pin for ***USB PD*** communication.

B.2.6.1.1 Orientation Detection with DTS as a Source

When the DTS is presenting an ***Rp***, it ***shall*** present asymmetric ***Rp*** values (Rp1/Rp2) on CC1/CC2 to indicate orientation to the TS. The DTS as a source ***shall*** indicate a weaker resistive value on CC2. Table B-2 shows the values of ***Rp*** resistance on each CC pin to indicate orientation and advertise the USB Type-C current available on VBUS. See Table 4-27 for the ***Rp*** resistance ranges.

Once the TS sink enters the ***DebugAccessory.SNK*** state, after the ***vRd*** on both CC pins is stable for ***tRpValueChange***, it will orient its signal multiplexor based on the detected orientation indicated by the relative voltages of the CC pins. The CC pin with the greater voltage is the plug CC pin, which establishes the orientation of the DTS plug in the TS receptacle and also indicates the ***USB PD*** CC communication wire. The TS Sink cannot perform ***USB PD*** communication or connect any orientation-sensitive debug signals until orientation is determined.

B.2.6.1.2 Orientation Detection with DTS as a Sink

When the DTS is a sink, it ***shall*** follow a two-step approach.

1. The DTS sink ***shall*** present ***Rd***/***Rd*** on the CC pins of the debug accessory plug. This will put the system into ***Debug Accessory Mode***
2. Once the DTS sink enters ***AttachedDeb.SNK*** state, it ***shall*** present a resistance to GND of ≤ ***Ra*** on B5 (CC2)

The asymmetric signaling is detected by the TS Source in the ***UnorientedDebugAccessory.SRC*** state. Once Detected, the TS Source will move to the ***OrientedDebugAccessory.SRC***. Once the TS source enters the ***OrientedDebugAccessory.SRC*** state, after the ***SRC.Ra*** level is detected on one of the CC pins, it will orient its signal multiplexor based on the detected orientation indicated by the relative voltages of the CC pins. The CC pin with the greater voltage is the plug CC pin, which establishes the orientation of the DTS plug in the TS receptacle and also indicates the ***USB PD*** CC communication wire. The TS Source cannot perform ***USB PD*** communication or connect any orientation-sensitive debug signals until orientation is determined.

B.3 Security/Privacy Requirements

Debug port(s) typically provide system access beyond the normal operation of USB hardware and protocol. Additional protection against unintended use is needed. The design must incorporate appropriate measures to prohibit unauthorized access or modification of the unit under test and to prevent exposure of private user data on the unit under test. The method of protection is not explicitly defined in this specification.

The vendor ***shall*** assert as part of USB compliance certification that:

- The device has met the requirement to protect the system's security and user's privacy in its vendor-specific implementation of the port, and
- The device requires the user to take an explicit action to authorize access to or modification of the unit.

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C USB Type-C Digital Audio

C.1 Overview

One of the goals of USB Type-C is to help reduce the number of I/O connectors on a host platform. One connector type that could be eliminated is the legacy 3.5 mm audio device jack. A USB Type-C digital audio solution based on native USB protocol is a simple solution and is interoperable with both the host platform and audio device being connected directly without the need for adapters and operates seamlessly through existing USB topologies (e.g., through hubs and docks).

This appendix is for the ***optional normative*** definition of digital audio support on USB Type-C-based products. Any USB Audio Class product, having either a USB Type-C plug or receptacle, and whether it is a host system, typically an audio source, and an audio device, typically an audio sink, ***shall*** meet the requirements of this appendix in addition to all other applicable USB specification requirements.

C.2 USB Type-C Digital Audio Specifications

USB Type-C Digital Audio (TCDA), when implemented per this specification, ***shall*** be compliant with either the USB Audio Device Class 1.0, 2.0, 3.0 or 4.0 specifications as listed below. While allowed, basing a TCDA on USB Audio Device Class 1.0 or USB Audio Device Class 3.0 is not recommended. As USB Audio Device Class 4.0 improves power efficiency by providing new selective configuration tools and supporting burst mode audio data transfers, supports new CODEC types and data formats for consumer audio applications, and provides numerous extensions to support various changes in the core specification, its use is *strongly recommended*.

USB Audio Device Class 1.0 (*not recommended*) including:

- USB Device Class Definition for Audio Devices, Release 1.0
- USB Device Class Definition for Audio Data Formats, Release 1.0
- USB Device Class Definition for Audio Terminal Types, Release 1.0

USB Audio Device Class 2.0 including:

- USB Device Class Definition for Audio Devices, Release 2.0
- USB Device Class Definition for Audio Data Formats, Release 2.0
- USB Device Class Definition for Audio Terminal Types, Release 2.0

USB Audio Device Class 3.0 (*not recommended*) including:

- USB Device Class Definition for Audio Devices, Revision 3.0
- USB Device Class Definition for Audio Data Formats, Release 3.0
- USB Device Class Definition for Audio Terminal Types, Release 3.0
- USB Device Class Definition for Basic Audio Functions, Release 3.0

USB Audio Device Class 4.0 including:

- USB Device Class Definition for Audio Devices, Revision 4.0

USB Audio Device Class 3.0 specifications include the definition of basic audio function profiles (Basic Audio Device Definition, BADD). TCDA devices based on USB Audio Device Class 3.0 will implement one of the defined profiles. TCDA-capable hosts based on USB Audio Device Class 3.0 will recognize and typically implement all of the profiles that are relevant to the capabilities and usage models for the host.

TCDA devices ***shall*** fall into one of the following two configurations:

- a traditional VBUS-powered USB device that has a USB Type-C receptacle for use with a standard USB Type-C cable, or
- a ***VCONN-Powered USB Device*** (***VPD***) that has a captive cable with a USB Type-C plug (including thumb drive style products).

USB Type-C plug-based TCDA devices ***shall not*** be implemented as a variant of the USB Type-C ***Analog Audio Adapter Accessory*** (Appendix A in USB Type-C specifications prior to Release 2.3).

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D Thermal Design Considerations for Active Cables

D.1 Introduction

USB Type C active cables use active circuitry to realize a longer link than passive cables and to maintain the electrical performance at high speed data transmission (***USB 3.2*** or ***USB4***). The additional power dissipation due to active components in the plug over-mold, creates a thermal challenge to passively dissipate power from its active components off the limited outer surface area of cable over-mold. Furthermore, the VBUS current, up to 5 A for power delivery, generates joule heat from the conductors along VBUS and GND lines, including copper wires, solder joints, contact pins insides connectors and copper traces on paddle board.

This appendix provides some case studies, based on ***USB 3.2*** active cable designs, to show the thermal impacts of certain factors affecting the maximum over-mold surface temperature TS such as IC power inside over-mold (PO), thermal boundary, VBUS current level, and port to port spacing. The case study provided is for a specific mechanical design of the cable. When a different mechanical design (geometry, or material, etc.) are used, these impacts need further investigation. The methodology of the study is thermal modeling. The modeling results have been validated for some cases (1.5 W PO and 5A VBUS) with lab test results within ± 3 °C, but not for all cases. Note that this appendix is not a full factorial or complete Design of Experiment (DOE) study and whether there is interaction among any of these factors are not covered here.

To meet thermal requirements specified in Section 6.1.3.1, as well as the junction temperature T_J requirement of any active components, an active cable ***should*** be carefully designed to facilitate the desired heat flow paths. A desirable thermal resistance between powered IC to over-mold surface is achieved when neither T_S nor T_J exceeds their specifications. This appendix focuses solely on T_S as output of the study, as the T_J requirement varies depending on the IC requirements.

It is recommended that system integrator such as host or device designer ***should*** take into consideration the heat transferred to or from an active cable in the system level thermal analysis.

Nomenclature used in this appendix:

- T_A = ambient temperature (°C)
- T_J = junction temperature (°C)
- T_S = plug over-mold outer surface maximum temperature (°C)
- T_{MB} = motherboard/thermal boundary temperature (°C)
- P_O = active component power (W) inside the over-mold that directly plugged in the host or device at each end of cable.

D.2 Model

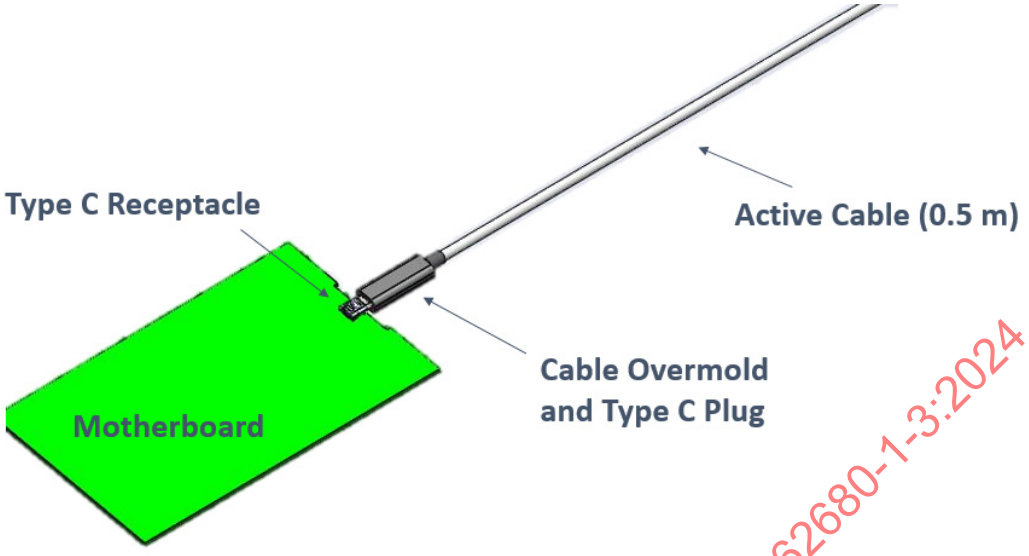
D.2.1 Assumptions

A system model was built which includes a half active cable with one over-mold on the end, a mated pair of connectors (plug and receptacle) and a motherboard as its host or device side thermal boundary. The model assumes the cable is symmetric with VCONN power to be equally divided and each end of cable consumes half of VCONN power for the active components.

It is a Computational Fluid Dynamics (CFD) model with heat transfer of conduction, natural convection, and radiation. The emissivity of the plug over-mold and cable jacket is assumed to be 0.92 and the connector metal surfaces is assumed to be 0.05.

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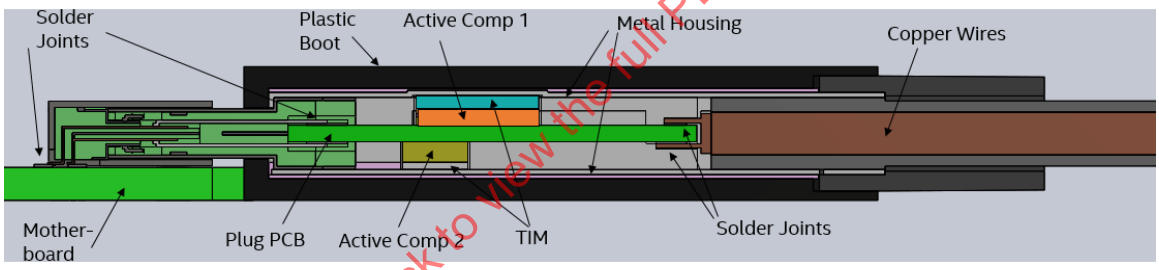
Figure D-1 Active Cable Model (Single Port, Top Mount Receptacle)



D.2.2 Model Architecture

The specific system and cable architecture used in the model is shown below.

Figure D-2 Model Architecture



The simplified cable model uses a pure copper cable, representing a typical short active cable, with total cross section of the copper conductors being about 3.8 mm^2.

The cable model incorporates a plastic boot for the over-mold which allows a higher surface temperature threshold than some other materials such as metal or glass. The over-mold length in the study was 35 mm.

In this specific cable design, two active components are surface mounted on plug PCB (or paddle board). Thermal Interface Material (TIM) are placed between "hot components" and "heat spreading material" such as metal housings to reduce thermal resistance between component junctions to ambient. Metal shells help to reduce Ts by spreading heat across the over-mold surface and avoid hot spots.

The plug PCB and motherboard are assumed to be FR4 based material. The motherboard is a bulk model assumed to be at a constant temperature without a point heat source on it. The receptacle is top mounted on the motherboard in single port and horizontal stacked cases, Figure D-6; and is vertically mounted in vertical stack up cases, Figure D-4 and Figure D-5.

D.2.3 Heat Sources

Main heat sources include:

- Active component power such as re-timer, voltage regulator, etc.; the overall power inside over-mold is P_O, which is about half of VCONN power consumed by the full cable.

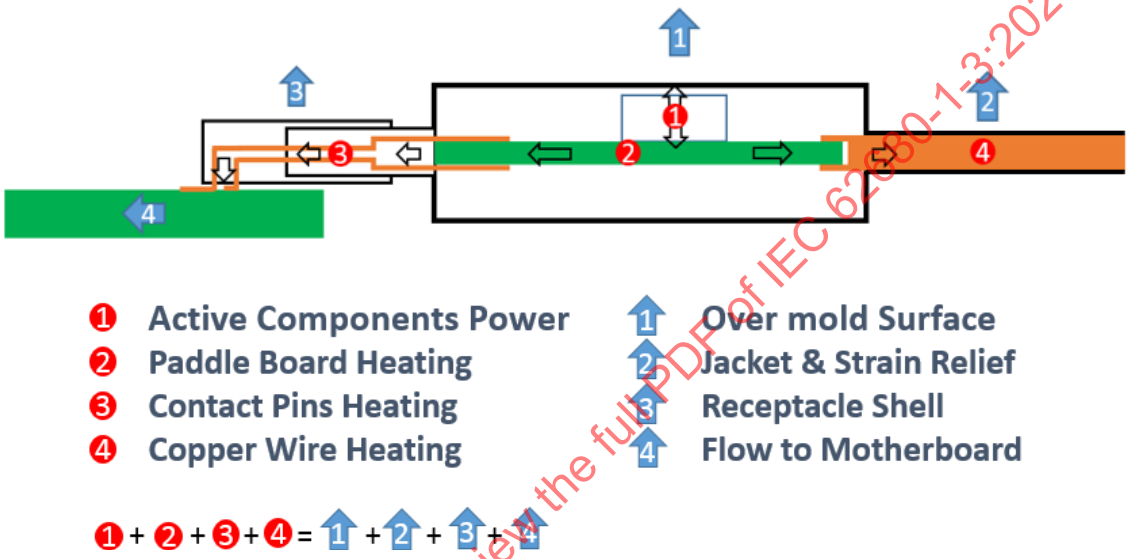
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- Joule heat from the any conductor that carries high current, e.g., raw cable VBUS and GND copper wire, the plug PCB copper traces, contact pins of connectors, etc.

D.2.4 Heat Flow

The main power sources and heat flow paths are illustrated in Figure D-3. The overall heat generated from the cable is mainly dissipated from over-mold surfaces, cable jacket and path to motherboard. The higher thermal resistance of one heat path, the more heat it will "push off" to other heat paths and the more risk that active component junction is overheated. Since heat flow to motherboard is not a desired path from the perspective of system design, cable and over-mold design are critical to achieve balanced heat dissipation paths so not to violate either T_S or T_J requirements.

Figure D-3 Heat Sources and Heat Flow Paths



The overall heat generated from the cable ***should*** be consistent with the overall power dissipated by the cable. An example of half a 1.0 m active cable consuming 1.5 W and sourcing 5 A VBUS is shown below:

Table D-1 Heat Sources and Heat Dissipation Example (1.5 W cable and 5 A)

(a) Heat Sources

Index	Heat Source	Power (W)
1	Active Components	0.750
2	Pin Heating	0.330
3	PCB Heating	0.135
4	Cable Heating	0.805
	Total Power Generation:	2.020

(b) Heat Dissipation

Index	Heat Dissipation	Power (W)
1	Plug Surface	0.500
2	Cable & SR	1.120
3	Receptacle	0.050
4	Flow to Motherboard	0.350
	Total Power Dissipation:	2.020

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D.3 *USB 3.2* Single-Lane Active Cable

Based on the assumption that VCONN power consumption is equally split between two ends of the cable and the 1 W maximum VCONN power dissipation in the USB Type-C active cable (See Table 4-5), active component power in each end or over-mold power (P_O) can go up to 0.5 W in a ***USB 3.2*** active cable.

D.3.1 *USB 3.2* Single-Lane Active Cable Design Considerations

The active cable designer ***should*** design for T_S less than 30 °C above T_A in the condition where thermal boundary T_{MB} is of 25 °C above T_A per Section 6.1.3.1.

D.3.1.1 *USB 3.2* Single-Lane Active Cable in a Single Port Configuration

An active cable connected to a single port in a host or device can take full advantage of the overall plug surface area for heat dissipation. Table D-2 shows that when P_O is 0.5 W, it is achievable to keep the plug over-mold surface temperature T_S of a single cable below the requirement, at both 3 A and 5 A VBUS, assuming the motherboard temperature is no higher than (T_A +25) °C.

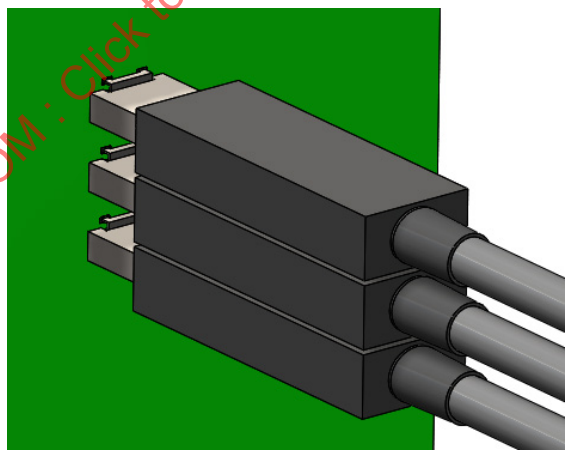
Table D-2 *USB 3.2* Active Cable Design Single Port Case Study at 35 °C Ambient and 60 °C Thermal Boundary (Single Lane)

	3 A VBUS	5 A VBUS
T_S (°C)	57	60

D.3.1.2 *USB 3.2* Single-Lane Active Cable in a Multiple Port Configuration

When multi-port connector spacing is small, there is heat transfer between cables resulting in heat dissipation through natural convection being less effective than in the single port case. Radiation is also less effective due to the proximity of hot surfaces. This section lists a few typical 3-port configurations to show the impacts of receptacle spacing to the thermal performance of an active cable. For Figure D-4 and Figure D-5 minimum spacing center to center is 7 mm; for Figure D-6 it is 12.85 mm.

Figure D-4 Vertically Stacked Horizontal Connectors 3x1 Configuration (VERT)



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Figure D-5 Horizontally Stacked Vertical Connectors 1x3 Configuration (HZ90)

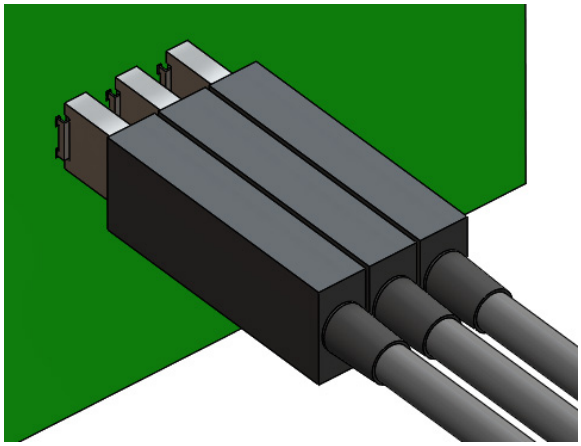
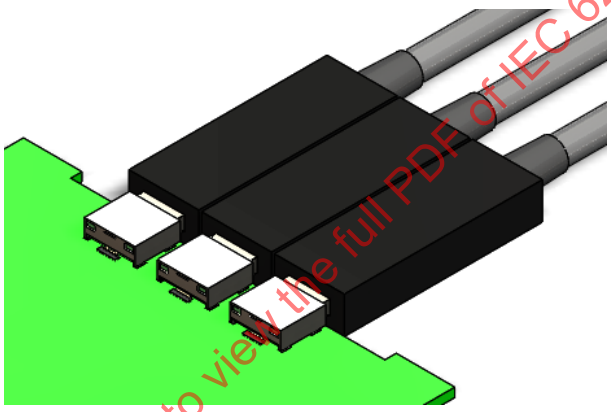


Figure D-6 Horizontally Stacked Horizontal Connectors 1x3 Configuration (HORZ)



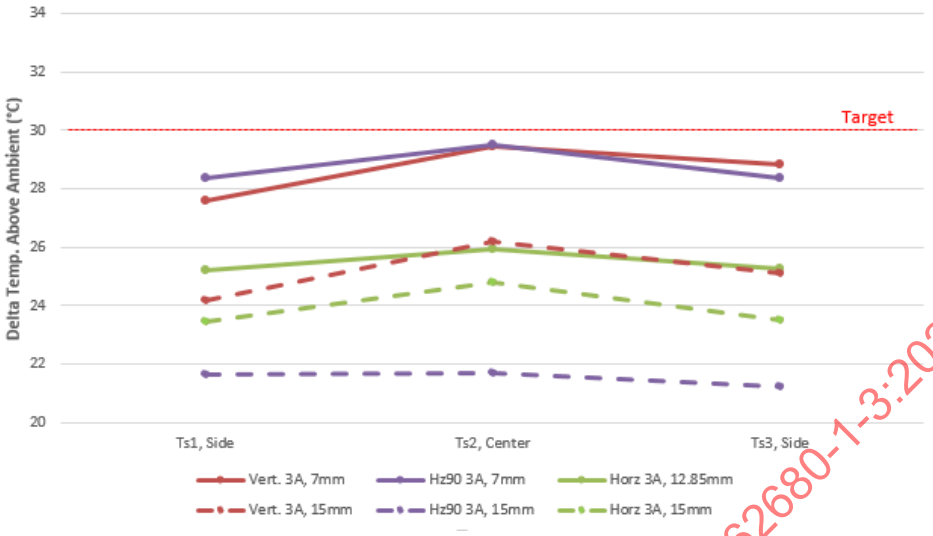
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D.3.1.2.1 *USB 3.2* Single-Lane 3A Active Cable in a 3-Port Configuration

When three active cables are stacked up, the port in the center position is usually in the worst situation for heat transfer. Figure D-7 shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three ***USB 3.2*** 3A cables are plugged on a 60 °C motherboard in 35°C ambient.

In all 3-port configurations shown in Figure D-4, Figure D-5, and Figure D-6, it is achievable to keep the all three plug over-mold surface temperature T_S below the requirement, at 3 A V_{BUS}, assuming the motherboard temperature is no higher than (T_A +25) °C. Specific cable design ***should*** be tested and validated because the margin of center port in VERT and HZ90 is less than 1 °C at minimum port spacing in thermal modeling.

Figure D-7 *USB 3.2* Single-Lane 3A Active Cable in a 3-Port Configuration



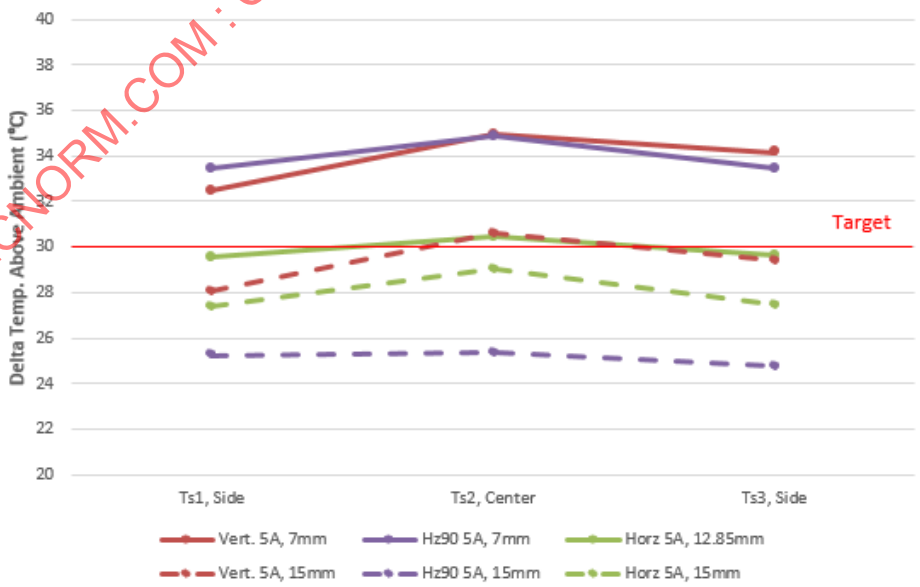
D.3.1.2.2 *USB 3.2* Single-Lane 5A Active Cable in a 3-Port Configuration

Figure D-8 shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three ***USB 3.2*** 5A cables are plugged on a 60 °C motherboard in 35 °C ambient.

All solid lines indicate the minimum spacing cases and dash lines the enlarged spacing cases. Center port is the worst case in all configurations. Three 5A cables at VERT and HZ90 configurations at minimum spacing could exceed the (T_A +30 °C) specification by up to 5 °C. HORZ configuration marginally meet spec on side ports but failed on center port.

Enlarging spacing between ports greatly reduce T_S. Especially in HZ90 configuration, spacing from 7 mm to 15 mm reduced T_S by about 8 °C.

Figure D-8 *USB 3.2* Single-Lane 5A Active Cable in a 3-Port Configuration



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D.4 Dual-Lane Active Cables

USB 3.2 and ***USB4*** defines two lanes of USB high-speed data and in dual-lane operation typically has higher active component power consumption than ***USB 3.2*** single-lane Gen2 active cables. Higher power could heat up the over-mold and raise T_S above user comfort zone when plugging or unplugging the cable.

USB 3.2 and ***USB4*** dual-lane active cable ***may*** consume up to 1.5 W of power from VCONN. This compares with the 1 W allowed for ***USB 3.2*** single-lane active cables.

Section D.4.1 shows T_S resulting from 0.75 W over-mold power P_O in a 1.5 W dual-lane ***USB 3.2*** active cable for a certain design, in both single-port and multiple-port configurations. Results reveal that a thermal solution is necessary to meeting cable design requirements, especially in multiple-port configuration.

Both over-mold power P_O and thermal boundary of the cable T_{MB} have impacts on T_S. The correlation of three are studied in Section D.4.1.2 which helps system and cable designer to take both factors into consideration.

D.4.1 *USB 3.2* Dual-Lane Active Cable Design Considerations

The cable designer ***should*** design for T_S of the over-mold less than 30 °C above T_A in the condition where thermal boundary T_{MB} is of 25 °C above T_A per Section 6.1.3.1.

D.4.1.1 *USB 3.2* Dual-Lane Active Cable in a Single Port Configuration

An active cable connected to a single port in a host or device can take full advantage of the overall plug surface area for heat dissipation. Table D-3 shows that when P_O is 0.75 W, it is achievable to keep the plug over-mold surface temperature T_S of a single cable below (T_A +30) °C at both 3 A and 5 A VBUS, assuming the motherboard temperature is no higher than (T_A +25) °C.

Table D-3 *USB 3.2* Active Cable Design Single Port Case Study at 35 °C Ambient and 60 °C Thermal Boundary (Dual Lane)

	3 A VBUS	5 A VBUS
T_S (°C)	61	64

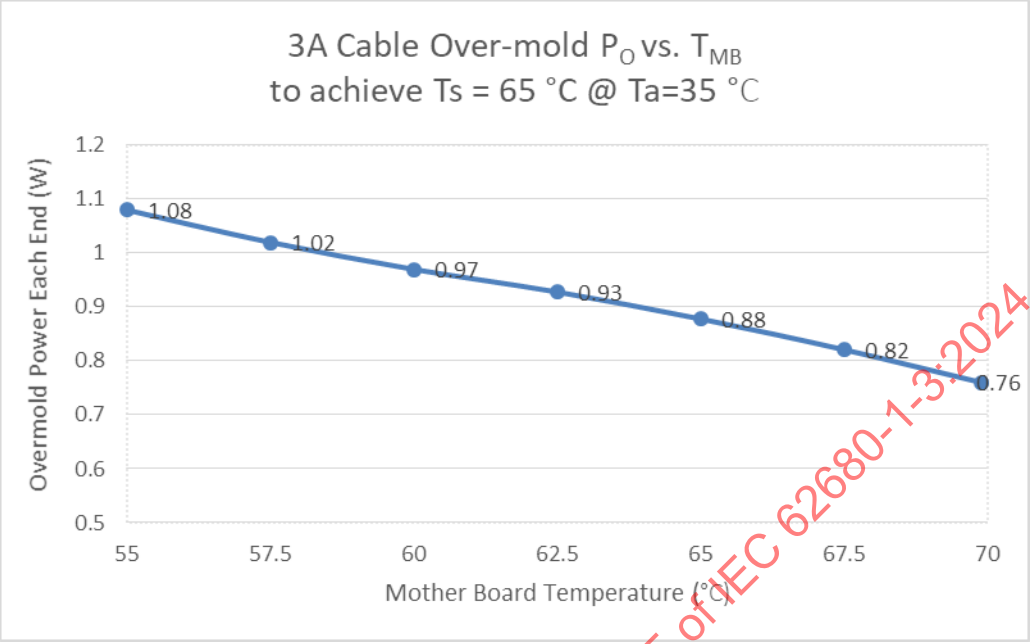
In 5 A VBUS case, T_S is much closer to specified limit than 3 A VBUS case (Section D.3.1.1), so test and verification of thermal design is highly recommended.

D.4.1.2 Impact of Over-mold Power P_O and Thermal Boundary Temperature T_{MB}

In Figure D-9, the area under graph indicates the combination of over-mold power P_O and thermal boundary temperature T_{MB} that can achieve T_S < (T_A +30) °C in a single port configuration in a 3 A VBUS application.

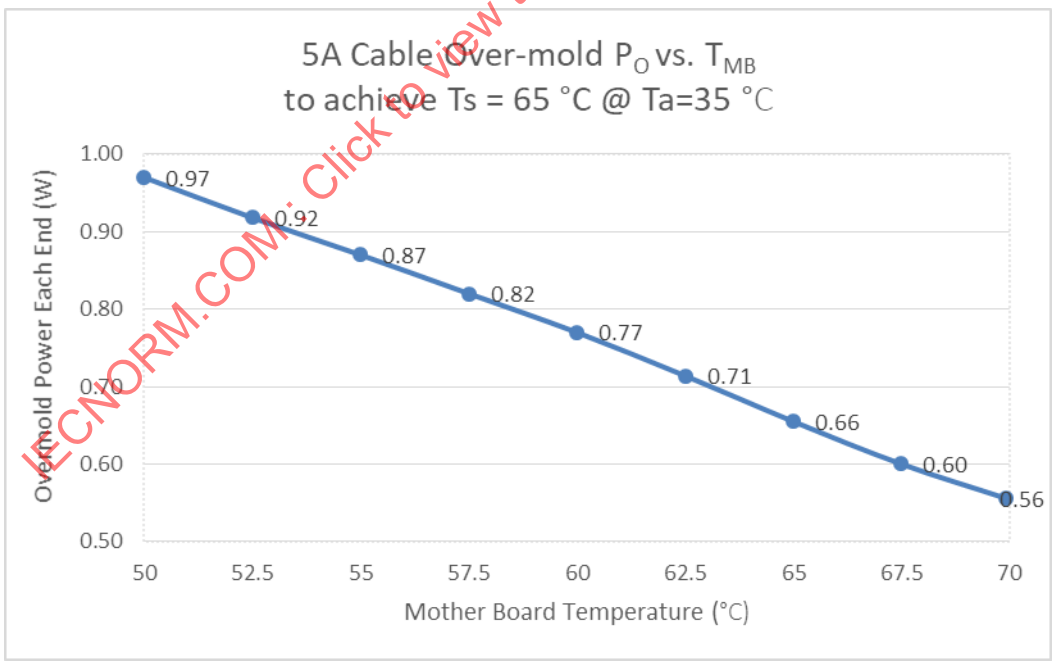
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Figure D-9 Impact of Overmold Power P_O and Thermal Boundary Temperature T_{MB} at 3 A VBUS in a Single Port Configuration



In Figure D-10, the area under graph indicates the combination of over-mold power P_O and thermal boundary temperature T_{MB} that can achieve $T_S < (T_A + 30)$ °C in a single port configuration in a 5 A VBUS application.

Figure D-10 Impact of Overmold Power P_O and Thermal Boundary Temperature T_{MB} at 5 A VBUS in a Single Port Configuration



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D.4.1.3 Dongle Cable

When overall active component power is higher than the maximum over-mold power P_O that could meet T_S requirement, cable ***may*** be re-designed to move the thermal load away from the USB Type-C plug over-mold such as in a dongle cable as illustrated in Figure D-11.

Figure D-11 *USB 3.2* Active Cable Dongle Design (One End Shown)



The cable ***should*** be designed so that the over-mold directly plugged in the host or device dissipates no more than maximum P_O and extra heat is migrated to another part of the cable such as a dongle, so neither extra heat will flow into host and device, nor over-mold surface temperature is too hot for users to touch.

D.4.2 *USB 3.2* Dual-Lane Active Cable in a Multiple Port Configuration

Multi-port connector spacing results in less effective heat dissipation by natural convection and radiation. This section lists a few typical 3-port configurations to show the impacts of receptacle spacing to the thermal performance of ***USB 3.2*** active cables. Naming of configurations used in this section are the same as in Section D.3.1.2.

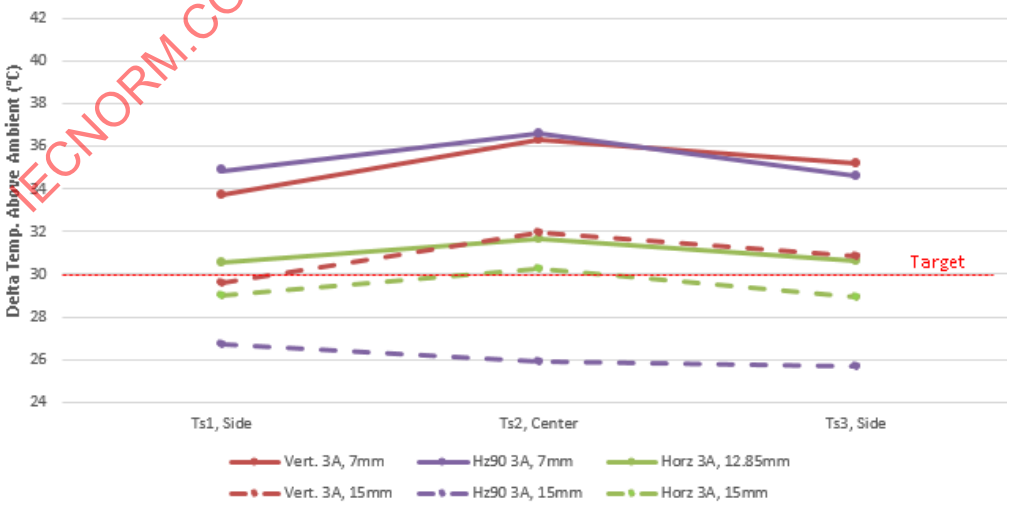
D.4.2.1 *USB 3.2* Dual-Lane 3A Active Cable in a 3-Port Configuration

Figure D-12 shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three ***USB 3.2*** dual-lane 3A V_{BUS} and 1.5 W cables are plugged on a 60 °C motherboard in 35 °C ambient. The port in the center position is usually in the worst situation for heat transfer.

All solid lines indicate the minimum spacing cases and dash lines the enlarged spacing cases. Center port is the worst case in all configurations. T_S of center port in VERT and HZ90 configurations at minimum spacing could be more than 6 °C over the (T_A +30 °C) specification and in HORZ configuration about 2 °C over specification.

Enlarging spacing between ports could greatly reduce T_S. Especially in HZ90 configuration, spacing from 7 mm to 15 mm reduced T_S by about 11 °C, which helps to reduce T_S to meet specification.

Figure D-12 *USB 3.2* Dual-Lane 3A Active Cable in a 3-Port Configuration



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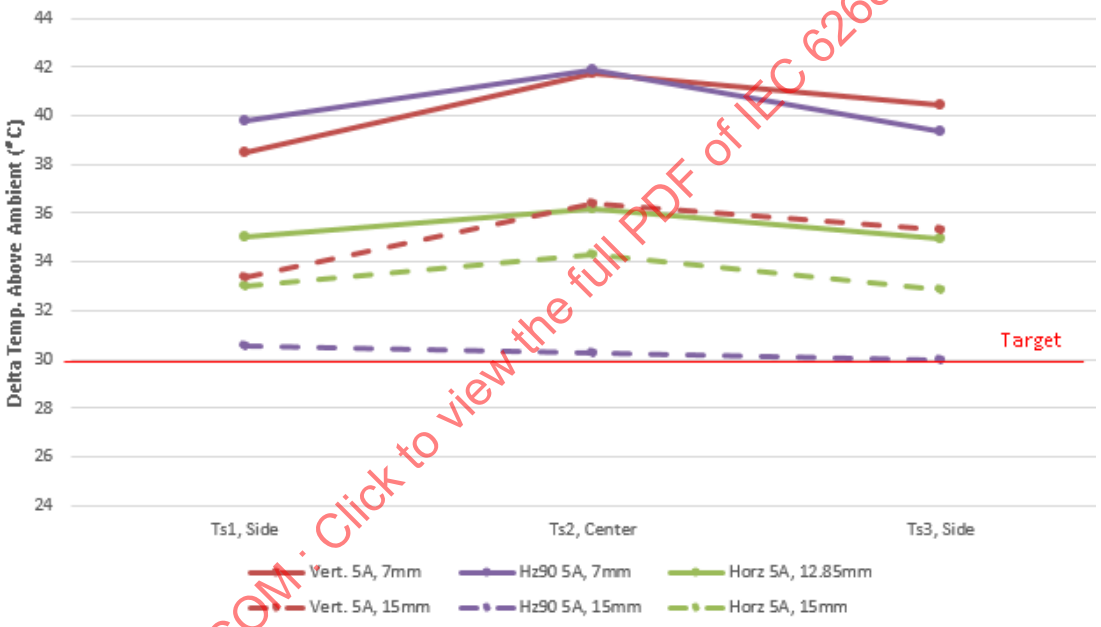
D.4.2.2 *USB 3.2* Dual-Lane 5A Active Cable in a 3-Port Configuration

Figure D-13 shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three ***USB 3.2*** dual-lane 5 A V_{BUS} and 1.5 W cables are plugged on a 60 °C motherboard in 35 °C ambient. The T_S port in the center position is still the highest of all three in all cases.

In all 3-port configurations listed in Figure D-4, Figure D-5, and Figure D-6, plug over-mold surface temperature T_S of all three ports have exceeded the requirement, at 5 A V_{BUS}, assuming the motherboard temperature is at (T_A +25) °C. T_S of center port in VERT and HZ90 configurations at minimum spacing are the highest, near 12 °C over the (T_A +30 °C) specification and in HORZ configuration about 6 °C over specification.

Enlarging spacing between ports could help reduce T_S. The largest reduction is seen in HZ90 configuration, which is near 12 °C and it brings T_S back close to target, when spacing is enlarged from 7 mm to 15 mm. However, when port spacing is not sufficient to bring T_S down to desired range, further design options in cable and host/device ***should*** be investigated.

Figure D-13 *USB 3.2* Dual-Lane 5A Active Cable in a 3-Port Configuration



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D.5 *USB 3.2* Host and Device Design Considerations

Multi-port ***USB 3.2*** systems ***should*** follow the connector minimum spacing requirement defined in Section 3.10.2.

From heat flow schematics (Section D.2.4), when flow path 1 (over-mold surface dissipation) is less effective due to the limited spacing between cables, more heat would flow to motherboard and cable. It is recommended that system designer evaluate the heat flow to the system in a system level thermal analysis and provide a heat solution at the system level to reduce the motherboard temperature at these ports if necessary.

D.5.1 Heat Spreading or Heat Sinking from Host or Device

Proper thermal solutions ***may*** be needed on a host or device to meet cable thermal requirements. Below are examples of placement of thermal interface material on host or device USB Type-C receptacle connector to spread heat or conduct heat away from chassis. This is to help either direct heat away from active components inside cable plug or limit amount of heat from flowing from host or device into the cable plug.

Both would prevent the increased junction temperature of active components and increased cable plug surface temperature over the finger touch temperature limit. The heat management solutions shown below are not limited to certain type or size.

Figure D-14 Example: Additional Heat Spreader on Receptacle in Host or Device

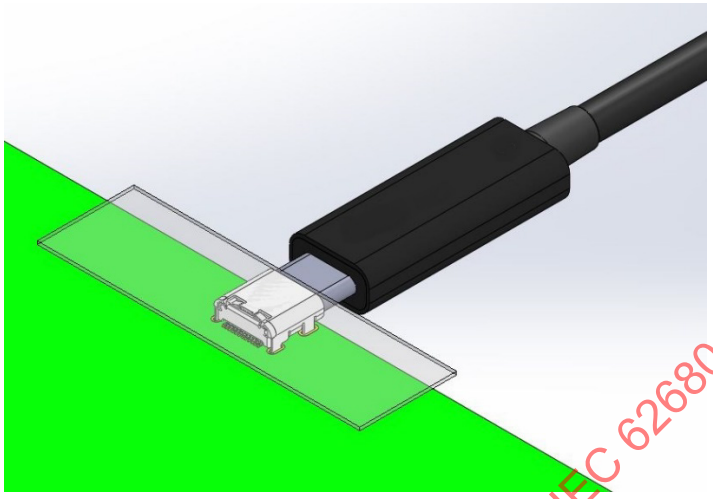
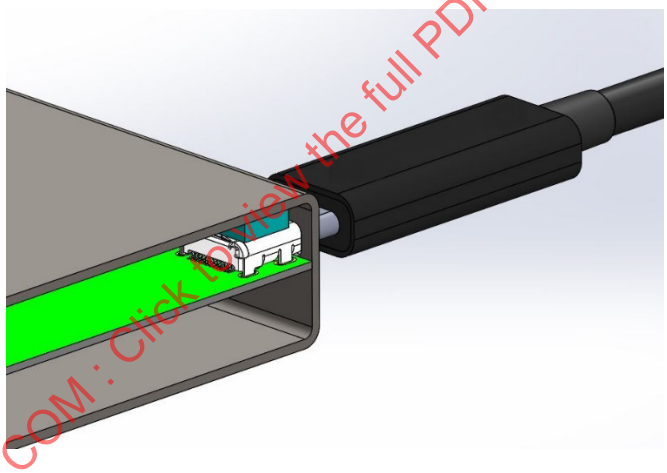


Figure D-15 Example: Heat Sinking on Chassis of Host or Device



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D.5.2 Motherboard Temperature Control

Motherboard as a thermal boundary for the cable, could impact the thermal performance of cable greatly. Lowered mother temperature especially the area local around the receptacles could help reduce plug surface temperature T_S and component junction temperature T_J. See more discussion in Section D.4.1.1.

D.5.3 Wider Port Spacing for Multi-Port Applications

Wider spacing between receptacle connectors, especially when no additional heat sinking is available, is recommended for multiport application. Section D.3.1.2.1 and section D.3.1.2.2 show the impact from adjustment of port spacing.

D.5.4 Power Policies

To be added in a future update.

E Alternate Modes

All hosts and devices (except chargers and clearly marked charge-through ports) using a USB Type-C receptacle ***shall*** expose a USB interface (minimally ***USB 2.0***). In the case where the host or device ***optionally*** supports ***Alternate Modes***:

- The host and device ***shall*** use ***USB Power Delivery*** Structured Vendor Defined Messages (Structured VDMs) to discover, configure and enter/exit modes to enable ***Alternate Modes***.
- The device is strongly encouraged to provide equivalent functionality over ***USB 3.2*** and/or ***USB 2.0*** where such exists for best user experience.
- Where no equivalent functionality is implemented, the device ***shall*** provide a USB interface exposing a ***USB Billboard Device Class*** used to provide information needed to identify the device. A device is not required to provide a USB interface exposing a ***USB Billboard Device Class*** for non-user facing modes (e.g., diagnostic modes).

As ***Alternate Modes*** do not traverse the USB hub topology, they ***shall*** only be used between a host connected directly to a device.

There are ***Alternate Mode*** devices that look like a USB hub – the downstream facing ports of such devices are USB Type-C receptacles that support ***Alternate Modes***. These devices are referred to as ***Alternate Mode*** expanders:

- The ***Alternate Mode*** port expander's downstream facing USB Type-C receptacles ***shall*** expose a ***USB 2.0*** interface.

An ***Alternate Mode*** port expander with the capability to pass SuperSpeed USB through its upstream facing port ***should*** expose SuperSpeed USB on its downstream facing USB Type-C receptacles.

E.1 Alternate Mode Architecture

The ***USB Power Delivery*** Structured VDMs are defined to extend the functionality a device exposes. Only Structured VDMs ***shall*** be used to alter the USB functionality or reconfigure the pins the USB Type-C Connector exposes. Structured VDMs provide a standard method to identify the modes a device supports and to command the device to enter and exit a mode. The use of Structured VDMs is in addition to the normal ***USB PD*** messages used to manage power. Structured VDMs ***may*** be interspersed within the normal ***USB PD*** messaging stream, however they ***shall not*** be inserted in the middle of an ongoing PD power negotiation.

The Structured VDMs consist of a request followed by a response. The response is either a successful completion of the request (ACK), an indication that the device needs time before it can service a request (BUSY), or a rejection of the request (NAK). A host and device do not enter a mode when either a NAK or BUSY is returned.

Multiple modes ***may*** exist and/or function concurrently. For example, a Structured VDM ***may*** be used to manage an active cable at the same time that another Structured VDM is used to manage the device so that both the cable and device are operating in a compatible mode.

E.2 Alternate Mode Requirements

The host and device ***shall*** negotiate a ***USB PD*** Explicit Contract before Structured VDMs ***may*** be used to discover or enter an ***Alternate Mode***.

The ACK ***shall*** be sent after switching to the ***Alternate Mode*** has been completed by the UFP for Enter Mode and Exit Mode requests. See Section 6.4.4 in the ***USB Power Delivery*** Specification. On initial connect, a UFP that reassigns pins when in its ***Alternate Mode*** ***shall*** hold off exposing ***USB 2.0*** speed identification (Section 7.1.5 of the ***USB 2.0*** specification) and ***USB 3.2*** receiver terminations until completing entry (including any pin reassignments) into the ***Alternate Mode*** or the ***tAMETimeout*** has expired.

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If a device fails to successfully enter an ***Alternate Mode*** within ***tAMETimeout*** then the device ***shall*** minimally expose a ***USB 2.0*** interface (***USB Billboard Device Class***) that is powered by VBUS. If the device additionally supports ***USB4***, then the device ***should*** defer exposing a ***USB 2.0*** interface (***USB Billboard Device Class***) due to an ***Alternate Mode*** timeout until the ***USB4*** discovery and entry process has completed (See Section 5.2.2).

When a device offers multiple modes, especially where multiple ***Alternate Mode*** definitions are needed in order to be compatible with multiple host-side implementations, successfully entering an ***Alternate Mode*** ***may*** be predicated on only one of the available modes being successfully recognized by a host. In this case, the device is not required to expose but ***may*** still expose a ***USB Billboard Device Class*** interface to indicate to the host the availability and status of the modes it supports.

The host ***may*** send an Enter Mode after ***tAMETimeout***. If the device enters the mode, it ***shall*** respond with an ACK and discontinue exposing the ***USB Billboard Device Class*** interface. The device ***may*** expose the ***USB Billboard Device Class*** interface again with updated capabilities.

The current supplied over VCONN ***may*** be redefined by a specific ***Alternate Mode***, but the power ***shall not*** exceed the current rating of the pin (See Section 3.7.8.4).

E.2.1 Alternate Mode Pin Reassignment

Figure E-1 illustrates the only pins that ***shall*** be available for functional reconfiguration in a full-featured cable. The pins highlighted in yellow are the only pins that ***shall*** be reconfigured.

Figure E-1 Pins Available for Reconfiguration over the Full-Featured Cable

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

Figure E-2 illustrates the only pins that ***shall*** be available for functional reconfiguration in direct connect applications such as a cradle dock, captive cable, or a detachable notebook. The pins highlighted in yellow are the only pins that ***shall*** be reconfigured. Five additional pins are available because this configuration is not limited by the cable wiring.

Figure E-2 Pins Available for Reconfiguration for Direct Connect Applications

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

The ***USB 2.0*** data pins (A6, A7) ***shall*** remain connected to the USB host controller during entry, while in and during exit of an ***Alternate Mode*** except in the case of a direct connect application that remaps A6 and A7. Direct connect applications that remap A6 and A7 through the use of an ***Alternate Mode*** ***shall*** provide a USB Billboard Class device that is presented if the remapped ***Alternate Mode*** is not entered within ***tAMETimeout***.

E.2.2 Alternate Mode Electrical Requirements

Signaling during the use of ***Alternate Modes*** ***shall*** comply with all relevant cable assembly, adapter assembly and electrical requirements of Chapter 3.

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Several requirements are specified in order to minimize risk of damage to the USB transmitters and receivers in a USB host or device when operating in an ***Alternate Mode***:

- If pin pairs B11, B10 (RX1) and A11, A10 (RX2) are used on a captive cable, they ***shall*** be AC coupled either before or in the USB Type-C plug.
- If pin pairs B11, B10 (RX1) and A11, A10 (RX2) are used on a USB Type-C receptacle, they ***may*** be AC coupled and discharged per ***USB 3.2*** before the receptacle.
- AC coupling on pin pairs A2, A3 (TX1) and B2, B3 (TX2) as defined for SuperSpeed USB signaling per ***USB 3.2 shall*** be used for ***Alternate Mode*** signaling.
- Signals being received at the USB Type-C receptacle ***shall not*** exceed the value specified for $V_{TX\text{-}DIFF\text{-}PP}$ in Table 6-18 of the ***USB 3.2*** specification.
- Direct Connect applications that remap pins A6 and A7 ***shall*** place pins A6 and A7 in a hi-Z state before transmitting the ***USB PD*** Enter_Mode command to the Sink. The Source ***shall not*** enable the alternate use of the A6 and A7 pins until an ACK has been received by the Source. In the event of a failure to enter the ***Alternate Mode*** after transmission of the ***USB PD Enter_Mode*** command, the Source ***shall*** restore pins A6 and A7 to the ***normative USB 2.0*** operation.

Direct connect applications ***shall*** ensure that any stubs introduced by repurposing the extra D+/D− pair do not interfere with USB communication with compliant hosts that short the pairs of pins together on the receptacle. This can be ensured by placing the ***Alternate Mode*** switch close to the plug, by adding inductors to eliminate the stubs at ***USB 2.0*** frequencies, by AC-terminating the long stubs to remove reflections at the cost of attenuated signal, or by other means.

When in an ***Alternate Mode***, activity on the SBU lines ***shall not*** interfere with ***USB PD*** BMC communications or interfere with detach detection.

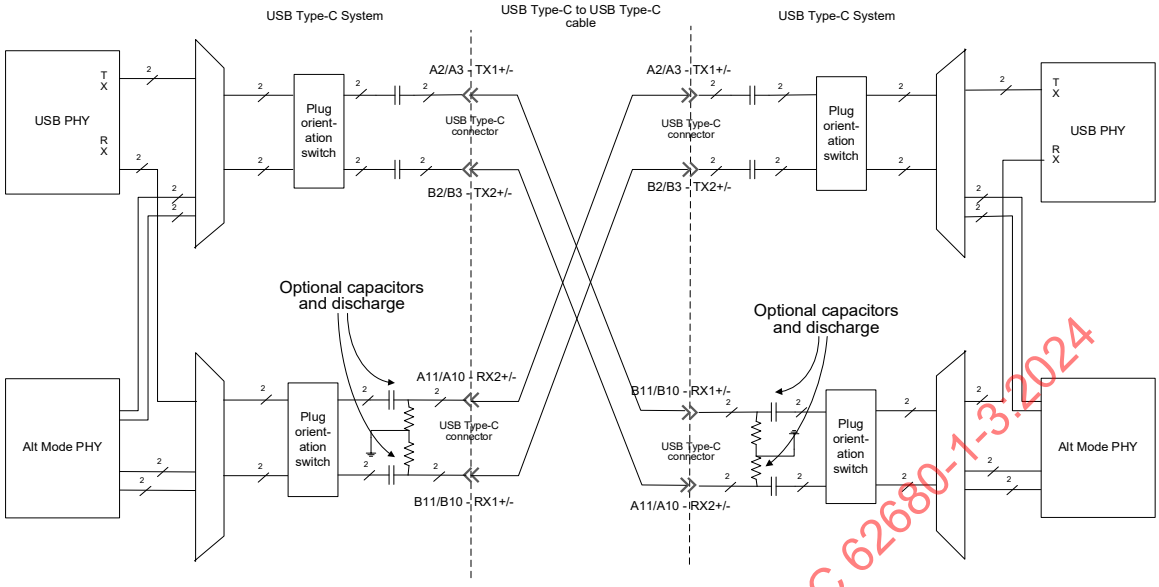
The AC coupling requirement are the same as defined in the ***USB 3.2*** specification. The TX signals ***shall*** be AC coupled within the system before the physical connector. The RX signals ***may*** be DC coupled or AC coupled and discharged within the system.

It ***should*** be noted that the AC coupling capacitor is placed in the system next to the USB Type-C receptacle, so that the system components (the orientation switch, the ***Alternate Mode*** selection multiplexer, and other system components) operate within the common mode limits set by the local PHY. This applies, in the SuperSpeed USB operation, to both the transmit path and the receive path within the local system. The receive path is isolated from the common mode of the port partner by the AC coupling capacitors that are implemented on the TX path in the port partner.

Figure E-3 shows the key components in a typical ***Alternate Mode*** implementation using a USB Type-C to USB Type-C full featured cable. This implementation meets the AC coupling requirements, as the capacitors required to be in or before the USB Type-C plug are implemented behind the TX pins in the port partner.

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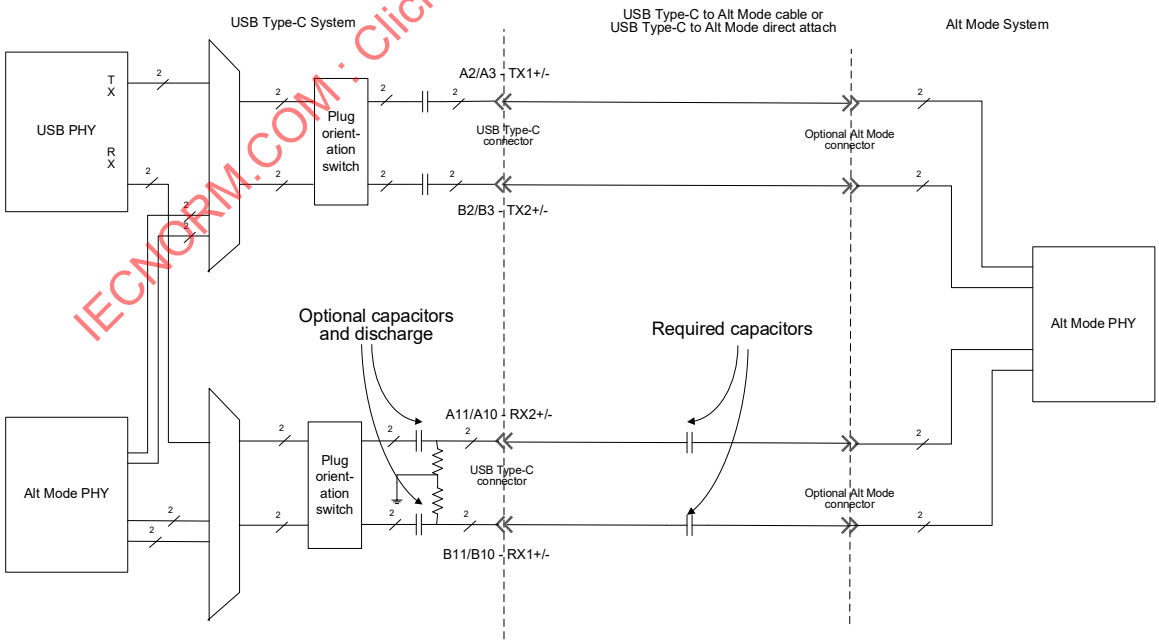
Figure E-3 Alternate Mode Implementation using a USB Type-C to USB Type-C Cable



In the case where the ***Alternate Mode*** System is required to implement DC blocking capacitors within the system between active system components and the ***Alternate Mode*** connector, then this provides the necessary isolation and further capacitors in the USB Type-C to ***Alternate Mode*** adapter cable are not necessary and ***may*** indeed impair signal integrity.

Figure E-4 shows the key components in a typical ***Alternate Mode*** implementation using either a USB Type-C to ***Alternate Mode*** connector cable, or a USB Type-C ***Alternate Mode*** Direct Attach device. In both cases it is necessary that the system path behind the RX pins on the USB receptacle be isolated from external common mode. This requirement is met by incorporating capacitors in or behind the USB Type-C plug on the ***Alternate Mode*** cable or ***Alternate Mode*** device.

Figure E-4 Alternate Mode Implementation using a USB Type-C to Alternate Mode Cable or Device



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The USB Safe State is defined by the ***USB PD*** specification. The USB Safe State defines an electrical state for the SBU1/2 and TX/RX for DFPs, UFPs, and Active Cables when transitioning between USB and an ***Alternate Mode***. SBU1/2 and TX/RX must transition to the USB Safe State before entering to or exiting from an ***Alternate Mode***. Table E-1 defines the electrical requirements for the USB Safe State. See the ***USB PD*** Specification for more detail on entry/exit mechanisms to the USB Safe State.

Table E-1 USB Safe State Electrical Requirements

	SBU1/2	TX[1,2]	RX[2]	A6/A7/B6/B7[4]
Common-mode voltage	0 to 1.5 V	0 to 1.5 V	0 to 1.5 V	0 to 1.5 V
Impedance to ground[3]	< 4 MΩ	< 4 MΩ	25 KΩ – 4 MΩ	< 4 MΩ

Notes:

1. TX common-mode voltage is defined on the integrated circuit side of the AC coupling capacitors.
2. Unused TX and RX signals ***should*** transition to USB Safe State if wired to the connector but not used.
3. The DFP and UFP ***shall*** provide a discharge path to ground in USB Safe State when a connection to the USB Type-C receptacle is present.
4. Applies to docking solutions/direct connect applications that redefine pins A6, A7, B6 and B7.

E.3 Parameter Values

Table E-2 provides the timeout requirement for a device that supports ***Alternate Modes*** to enable a ***USB Billboard Device Class*** interface when none of the modes supported by the device are successfully recognized and configured by the DFP to which the device is attached.

Table E-2 USB Billboard Device Class Availability Following Alternate Mode Entry Failure

	Maximum	Description
tAMETimeout	1000 ms	The time between a Sink attach until a ***USB Billboard Device Class*** interface is exposed when an ***Alternate Mode*** is not successfully entered.

While operating in an ***Alternate Mode***, the signaling ***shall not*** cause noise ingression onto USB signals operating concurrently that exceeds the **Vnoise** parameters given in Table E-3.

Table E-3 Alternate Mode Signal Noise Ingression Requirements

	Limit	Bandwidth
VNOISE on BMC during BMC Active	30 mV	100 ns time constant filter
VNOISE on BMC during BMC Idle	100 mV	100 ns time constant filter
VNOISE on D+/D– (Single-ended)	40 mV	500 MHz
VNOISE on D+/D– (Differential)	10 mV	500 MHz

Note: Each VNOISE parameter is the max noise ingression level allowed onto the respective interface that is due to two SBU aggressors from the ***Alternate Mode*** signaling, under respective worse case scenarios. The coupling between SBU_A/SBU_B and CC within a USB Type-C cable ***shall*** meet the requirement described in Section 3.7.2.6.4. The coupling between SBU_A/SBU_B and USB D+/D– within a USB Type-C cable ***shall*** meet the requirement described in Section 3.7.2.6.5.

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E.4 Example Alternate Mode – USB DisplayPort™ Dock

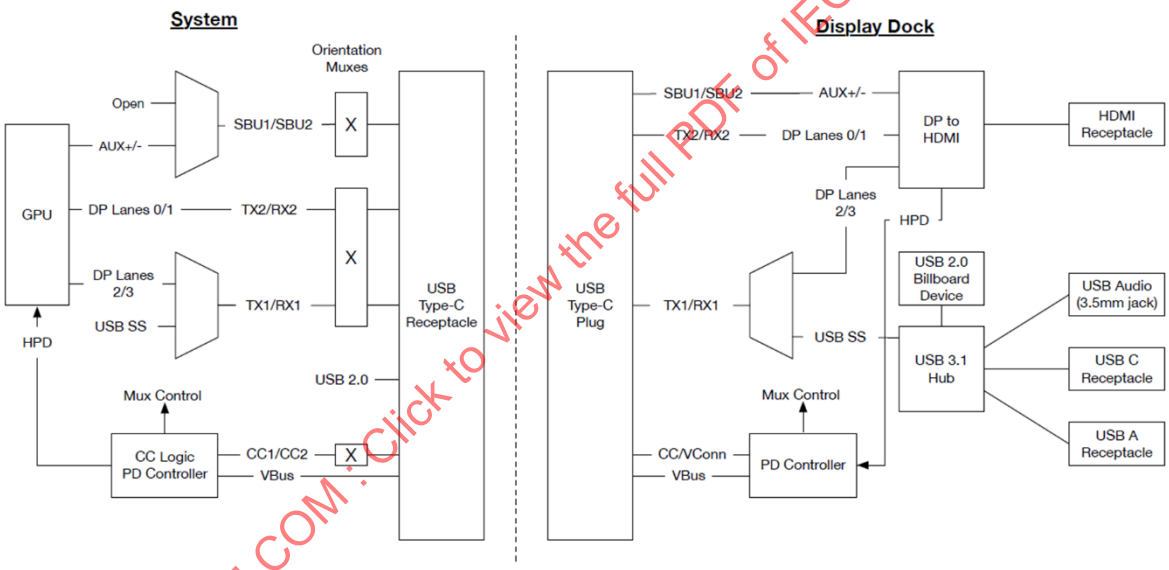
This example illustrates the use of Structured VDMs to expose and access functionality beyond the basic functionality defined by the USB Type-C Connector. The device uses its USB Type-C connector to make connection when placed in a cradle dock. This example only illustrates the functional connections.

E.4.1 USB DisplayPort™ Dock Example

- The cradle dock provides mechanical alignment and attachment in addition to those provided by the USB Type C connector allowing for only one orientation eliminating the need for an orientation MUX in the dock.
- The dock and system use ***USB PD*** to manage charging and power.
- The dock uses ***DisplayPort*** to drive a ***DisplayPort***-to-***HDMI*** adapter to support connecting an ***HDMI*** monitor.
- The dock has a USB hub that exposes two external USB ports and attached internal USB Devices, e.g., a USB audio Device (a 3.5 mm audio jack), and a USB Billboard Device.

Figure E-5 illustrates the USB ***DisplayPort*** Dock example in a block diagram form.

Figure E-5 USB DisplayPort Dock Example



The system uses ***USB PD*** Structured VDMs to communicate with the dock to discover that it supports a compatible ***Alternate Mode***. The system then uses a Structured VDM to enter the dock mode. Since ***USB PD*** is used, it ***may*** also be used to negotiate power for the system and dock. In this example, the SuperSpeed USB signals allow the dock to work as a USB-only dock when attached to a system that does not fully support the dock or even ***USB PD***.

E.4.2 Functional Overview

The following summarizes the behavior resulting from attaching the example USB ***DisplayPort*** Dock for three likely host system cases.

1. Host system does not support ***USB PD*** or supports ***USB PD*** without Structured VDMs
    - The host does not support ***USB PD***, or supports ***USB PD*** but not Structured VDMs, so it will not look for SVIDs using the Structured VDM method.
    - The host will discover the USB hub and operate as it would when connected to any USB hub.

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- Since the host will not send an Enter Mode command, after ***tAMETimeout*** the dock will expose a ***USB Billboard Device Class*** interface that the host will enumerate. The host then reports to the user that an unsupported Device has been connected, identifying the type of Device from the ***USB Billboard Device Class*** information.

2. Host system supports ***USB PD*** and Structured VDMs but does not support this specific USB ***DisplayPort*** Dock
   - The host discovers the USB hub and operates as it would when connected to any USB hub.
   - The Host looks for SVIDs that it recognizes. The VID associated with this USB ***DisplayPort*** Dock ***may*** or ***may not*** be recognized by the Host.
   - If that VID is recognized by the Host, the Host then requests the modes associated with this VID. The mode associated with this USB ***DisplayPort*** Dock is not recognized by the Host.
   - Since the host does not recognize the mode as being supported hence will not send the Enter Mode command, after ***tAMETimeout*** the dock will expose a ***USB Billboard Device Class*** interface that the host will enumerate. The host then reports to the user that an unsupported Device has been connected, identifying the type of Device from the ***USB Billboard Device Class*** information.

3. Host system supports this specific USB ***DisplayPort*** Dock
   - The Host looks for SVIDs that it recognizes. The VID associated with this USB ***DisplayPort*** Dock is recognized by the Host.
   - The Host then requests the modes associated with this VID. The mode associated with this USB/Display Dock is recognized by the Host.
   - Since this mode is recognized as supported, the Host uses the Enter Mode command to reconfigure the USB Type-C receptacle and enter the USB ***DisplayPort*** Dock mode.
   - The USB ***DisplayPort*** Dock ***may optionally*** expose the ***USB Billboard Device Class*** interface to provide additional information to the OS.

E.4.3 Operational Summary

The following summarizes the basic process of discovery through configuration when the USB ***DisplayPort*** Dock is attached to the Host.

1. Host detects the presence of a device (CC pins) and the connector orientation.
2. Host applies default VBUS.
3. Host applies VCONN because the dock presents ***Ra***.
4. Host uses ***USB PD*** to make power contract with the USB ***DisplayPort*** Dock.
5. Host runs the Discover Identify process.
   a. Sends ***Discover Identity*** message.
   b. Receives an ACK message with information identifying the cable.
6. Host runs the Discover SVIDs process.
   a. Sends Discover SVID message.
   b. Receives an ACK message with list of SVIDs for which the Dock device has modes.
7. Host runs the Discover Modes process.
   a. Sends Discover Modes VDM for the VIDs previously discovered.
   b. Receives an ACK message with a list of modes associated with each VID.

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c. If USB ***DisplayPort*** Dock mode is not found, dock will timeout and present the ***USB Billboard Device Class*** interface and the OS will inform the user of the error – *Done*.

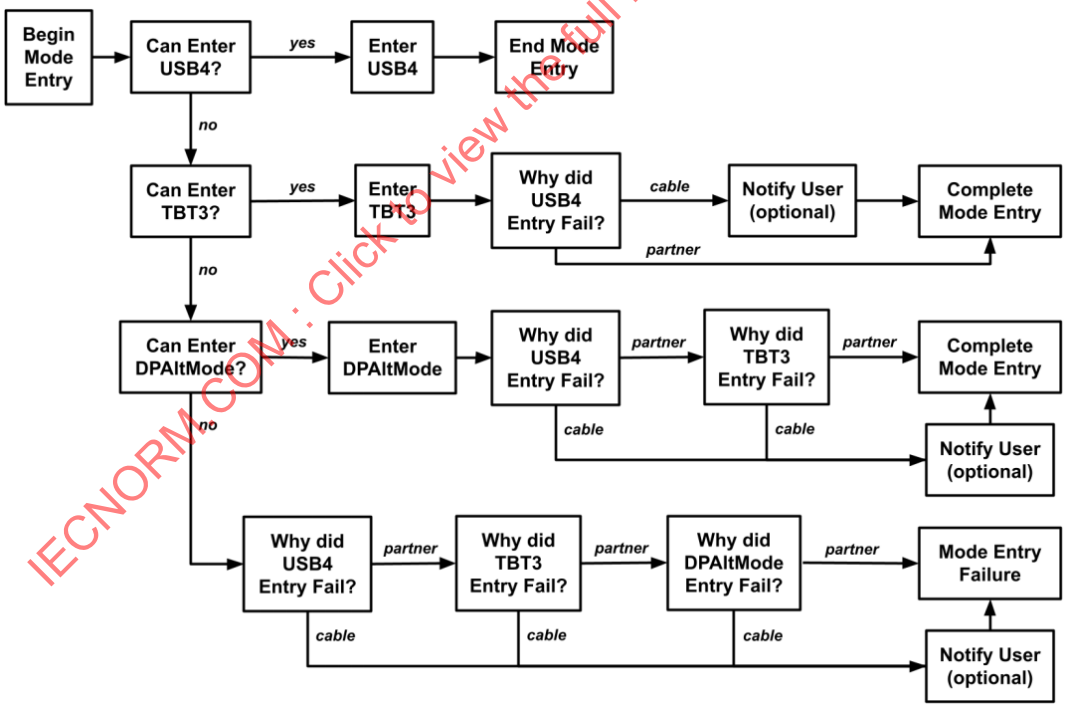
d. Else …

8. Host runs the Enter Mode process.
   a. Sends Enter Mode VDM with VID and USB ***DisplayPort*** Dock mode.
   b. Receives an ACK message – Host is now attached to the USB ***DisplayPort*** Dock and supports ***DisplayPort*** signaling to interface additional functions in combination with USB signaling.
9. Host stays in the USB ***DisplayPort*** Dock mode until.
   a. Explicitly exited by an Exit Mode VDM.
   b. System physically disconnected from the USB ***DisplayPort*** Dock.
   c. Hard Reset on ***USB PD***.
   d. VBUS is removed.

E.5 Example Alternate Mode Entry Flow with Cable Warnings

A single USB Type-C port ***may*** support multiple ***Alternate Modes*** if it is acting as a DFP. Which ***Alternate Mode*** the port enters depends on two factors. Firstly, what the port, partner and cable can support. Secondly, how the DFP's ***Alternate Modes*** are prioritized. Figure E-6 gives an example of how an ***Alternate Mode*** entry flow ***may*** work for a DFP ***USB4*** port with notifications to warn the user when a cable is preventing ***Alternate Mode*** entry.

Figure E-6 *USB4* DFP Mode Entry Flow Example



The port in this system example supports ***USB4***, ***Thunderbolt 3 Alternate Mode*** and ***DisplayPort Alternate Mode***. These ***Alternate Modes*** are mutually exclusive because they use pin reassignment as detailed in Section E.2.1. The port will prioritize entering ***USB4***, followed by ***Thunderbolt 3 Alternate Mode***, and then ***DisplayPort Alternate Mode***. It will only attempt ***Thunderbolt 3 Alternate Mode*** discovery if ***USB4*** discovery fails. It will only attempt ***DisplayPort Alternate Mode*** discovery if both ***USB4*** discovery and ***Thunderbolt 3 Alternate Mode*** discovery fail.

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E.5.1 Operational Summary

This subsection describes how the DFP ***USB4*** port in this example attempts ***Alternate Mode*** discovery and entry when a USB Type-C device has been connected. Before attempting any ***Alternate Mode*** entry, both the partner and cable need to have completed ***USB PD*** discovery. For each ***Alternate Mode***, the DFP will attempt a discovery flow to determine if it can enter that ***Alternate Mode*** with the attached partner and cable. It will only enter an ***Alternate Mode*** after successfully completing the mode discovery flow.

1. The DFP attempts ***USB4*** discovery defined in Section 5.1 and illustrated in Figure 5-1.
    a. If successful, the DFP enters ***USB4*** and completes mode entry.
2. If the DFP fails ***USB4*** discovery, it attempts ***Thunderbolt 3 Alternate Mode*** discovery defined in Appendix F and illustrated in Figure F-1.
    a. If successful, the DFP enters ***Thunderbolt 3 Alternate Mode***.
    b. ***Optionally***, the DFP can check why ***USB4*** discovery failed and inform the user. Figure E-6 illustrates a case where the user is notified when ***USB4*** discovery fails due to the cable.
    c. After entering ***Thunderbolt 3 Alternate Mode***, the DFP completes mode entry.
3. If the DFP fails ***Thunderbolt 3 Alternate Mode*** discovery, it will attempt ***DisplayPort Alternate Mode*** discovery described in Section E.4.3.
    a. Unlike ***USB4*** and ***Thunderbolt 3 Alternate Mode***, ***DisplayPort Alternate Mode*** does not explicitly define cable conditions required for mode entry. A DFP ***should*** still check the cable to confirm it supports a sufficient data rate for ***DP*** signals as a condition of ***DisplayPort Alternate Mode*** discovery. While this will prevent entering ***DisplayPort Alternate Mode*** with a cable that ***should not*** work for connecting displays, it will also prevent mode entry in cases where non-compliant cables would work for connecting displays but do not have a proper eMarker. Figure E-6 shows a case where cable checks are part of the ***DisplayPort Alternate Mode*** discovery and entry.
    b. If ***DisplayPort Alternate Mode*** entry succeeds, the DFP can ***optionally*** check why ***USB4*** and ***Thunderbolt 3 Alternate Mode*** discovery failed and inform the user.
    c. If ***DisplayPort Alternate Mode*** entry failed, the DFP can ***optionally*** check why ***USB4***, ***Thunderbolt 3 Alternate Mode*** and ***DisplayPort Alternate Mode*** discovery failed and notify the user.
    d. After attempting discovery for all modes and entering the highest priority mode that successfully finished its discovery flow, the DFP completes mode entry.

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F Thunderbolt™ 3 Compatibility Discovery and Entry

The ***USB4*** specification includes defined support for compatibility between ***USB4*** products that are designed to interoperate with existing ***Thunderbolt™ 3*** (***TBT3***) products. This appendix documents the ***normative*** methodology to discover and enter into ***TBT3*** between two port partners – this methodology relies on ***Alternate Mode*** protocol as defined in Appendix E of this specification and the ***USB Power Delivery*** specification.

Thunderbolt 3 technology is organized into two primary product categories: hosts and devices. Most ***TBT3*** devices include at least one upstream and one downstream port although a ***TBT3*** device ***may*** include more than one downstream port in a manner similar to a hub or no downstream ports in a manner similar to a peripheral.

F.1 *TBT3* Compatibility Mode Functional Requirements

In order to successfully interoperate with existing ***TBT3*** products, the functional requirements in the following subsections must be met.

F.1.1 *TBT3*-Compatible Power Requirements

Before two ***TBT3***-compatible port partners can enter ***TBT3*** mode, a ***USB PD*** explicit power contract ***shall*** be established.

F.1.2 *TBT3*-Compatible Host Requirements

All ***TBT3***-compatible host ports ***shall*** meet the following requirements.

- Support DRP operation.
- If resolved to a UFP, use ***USB PD DR_Swap*** to attempt to switch into the DFP data role when DFP is preferred.
- If resolved to a DFP, do not accept ***USB PD DR_Swap*** to remain in the DFP data role when DFP is preferred.

F.1.3 *TBT3*-Compatible Device Upstream Requirements

F.1.3.1 Self-Powered Device

The ***TBT3***-compatible upstream port of a self-powered device ***shall*** meet the following requirements.

- Support DRP operation.
- Prefer Sink/UFP through the implementation and use of ***Try.SNK*** as needed.
- If resolved to a DFP, accept ***USB PD DR_Swap*** to switch into the UFP data role.

F.1.3.2 Bus-Powered Device

The ***TBT3***-compatible upstream port of a bus-powered device ***shall*** meet the following requirements.

- Support Sink/UFP operation.
- Reject ***USB PD DR_Swap*** to remain in the UFP data role.

F.1.4 *TBT3*-Compatible Device Downstream Requirements

F.1.4.1 Self-Powered Device

The ***TBT3***-compatible downstream port of a self-powered device ***shall*** meet the following requirements.

- Support DRP operation.
- Prefer Source/DFP through the implementation and use of ***Try.SRC*** as needed.

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- If resolved to a DFP, do not accept ***USB PD DR_Swap*** to switch into the DFP data role.

F.1.4.2 Bus-Powered Device

The ***TBT3***-compatible downstream port of a bus-powered device ***shall*** meet the following requirements.

- Support Sink.

F.1.5 *TBT3*-Compatible Self-Powered Device Without Predefined Upstream Port Rules

A ***TBT3***-compatible device port ***may*** behave as either a downstream or upstream port based on its connection state to a ***TBT3***-compatible host as described below.

- When no ***TBT3***-compatible host is connected, the USB Type-C ports ***shall***:
  - Prefer to be configured as a UFP.
  - Implement and use ***Try.SNK*** as needed to get into the UFP state.
  - If resolved to a DFP, initiate, or accept ***USB PD DR_Swap*** to switch to the UFP data role.
  - Accept ***USB PD DR_Swap*** to switch to the DFP data role.
  - When resolved to a UFP, identify this port as being connected to the host.
    - Put the remaining downstream ports into the ***ErrorRecovery*** state.
- After a ***TBT3***-compatible host is initially connected, the remaining downstream USB Type-C ports ***shall***:
  - Implement and use ***Try.SRC*** as needed to get into the DFP state.
  - Issue a Hard Reset if a ***USB PD DR_Swap*** is received when both a connection is present, and an ***Alternate Mode*** is in place.
  - Issue a ***USB PD DR_Swap*** to switch to the DFP data role if a connection is present but no ***Alternate Mode*** has been entered (this includes performing a disconnect/reconnect on the port).
  - Accept ***USB PD DR_Swap*** to switch to the DFP data role if a connection is present but no ***Alternate Mode*** has been entered (this includes performing a disconnect/reconnect on the port).
- When a ***TBT3***-compatible host that was identified as a host is disconnected, the downstream USB Type-C ports ***shall***:
  - Enter the ***ErrorRecovery*** state.
  - Behave as if no host is connected.

F.1.6 *TBT3*-Compatible Devices with a Captive Cable

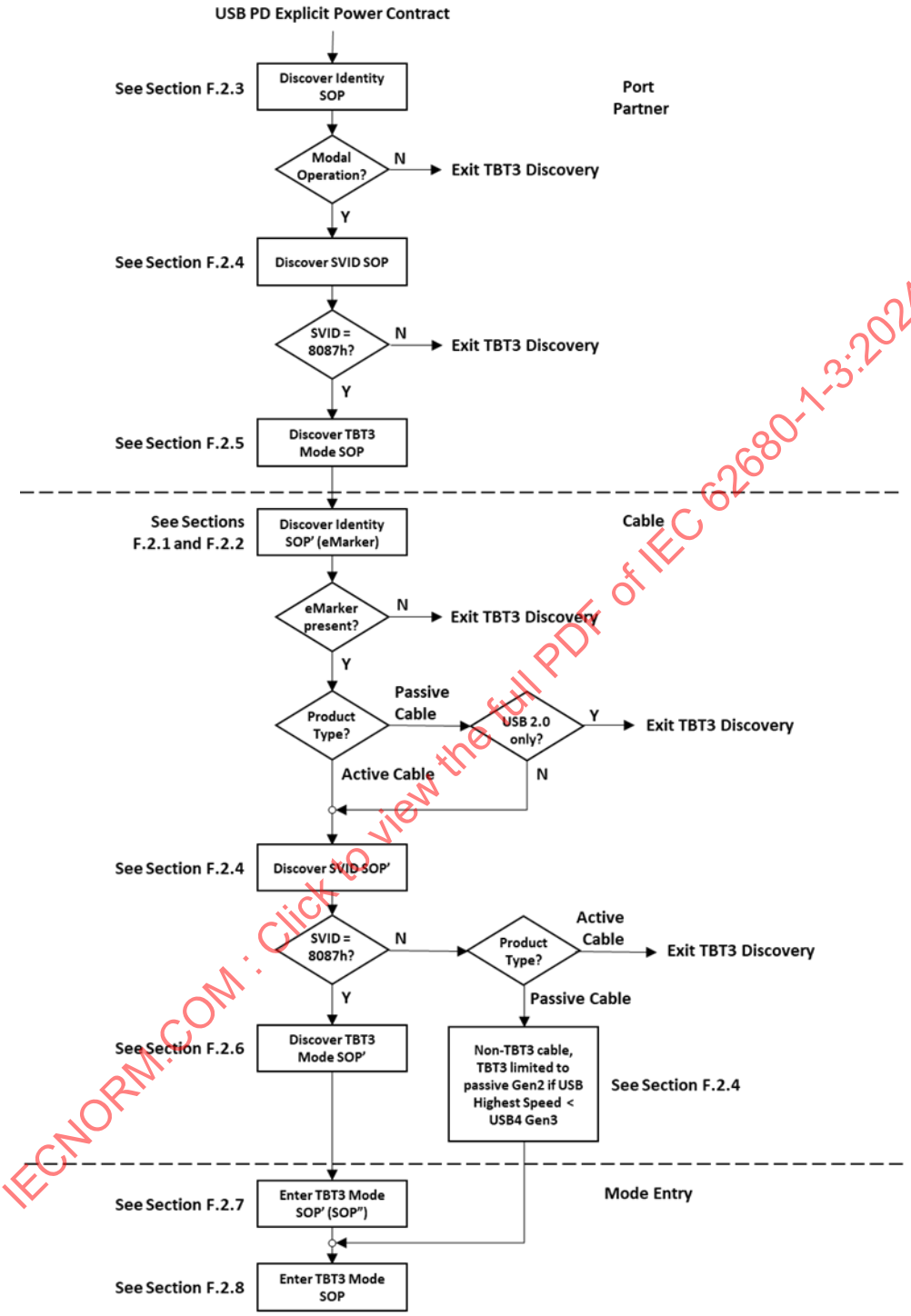
TBT3-compatible devices with a captive cable ***shall*** respond to ***USB PD*** messages both SOP and SOP'.

F.2 *TBT3* Discovery and Entry Flow

Figure F-1 describes the flow for a ***TBT3***-compatible DFP port to discover and enter into the ***TBT3*** Compatibility Mode of ***USB4*** with a connected UFP. For each functional block, refer to the sub-sections identified for additional details.

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Figure F-1 *TBT3* Discovery Flow



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F.2.1 *TBT3* Passive Cable Discover Identity Responses

Table F-1, along with Table F-2 and Table F-3, defines the expected ***Discover Identity*** VDO responses for a ***TBT3*** passive cable. In fields where multiple values are listed, cable responses ***may*** vary to match the specific connected cable's capabilities.

Table F-1 *TBT3* Passive Cable Discovery Identity VDO Responses

Message Header						
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**	**Spec Revision**	**Rsvd**	**Message Type**
0	5…6	0…7	1 = Cable Plug	10b or 01b	0	1111b
VDM Header						
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00001b

Bit(s)	Value	Parameter
ID Header VDO		
B31	0	USB Communications Capable as USB Host
B30	0	USB Communications Capable as a USB Device
B29…27	011b = Passive Cable	Product Type (Cable Plug)
B26	1 = Modal Operation	Modal Operation Supported
B25…23	000b	Product Type (DFP)
B22…16	0	***Reserved***
B15…0	Per vendor	USB Vendor ID
Cert Stat VDO		
B31…0	0x00000000…0xFFFFFFFF	XID assigned by ***USB-IF***
Product VDO		
B31…16	0x0000…0xFFFF	USB Product ID
B15…0	0x0000…0xFFFF	bcdDevice
Passive Cable VDO		
Depending on ***USB PD*** Specification Revision: See Table F-2 for ***USB PD*** Revision 2.0 or Table F-3 for ***USB PD*** Revision 3.0		

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Table F-2 *TBT3* Passive Cable VDO for *USB PD* Revision 2.0, Version 1.3

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	0001b – <10ns (~1m) 0010b – 10ns to 20ns (~2m)	Cable Latency
B12…11	00b = VCONN not required	Cable Termination Type
B10	0 = Fixed	SSTX1 Directionality Support
B9	0 = Fixed	SSTX2 Directionality Support
B8	0 = Fixed	SSRX1 Directionality Support
B7	0 = Fixed	SSRX2 Directionality Support
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4	1 = Yes	VBUS through cable
B3	0 = No	SOP" controller present
B2…0	010b = [***USB 3.1***] Gen1 and Gen2	SuperSpeed USB Signaling Support

Table F-3 *TBT3* Passive Cable VDO for *USB PD* Revision 3.0, Version 1.2

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…21	000b = Version 1.0	VDO Version
B20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	0001b – <10ns (~1m) 0010b – 10ns to 20ns (~2m)	Cable Latency
B12…11	00b = VCONN not required	Cable Termination Type
B10…9	00b = 20V	Maximum VBUS Voltage
B8…7	00b	***Reserved***
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4…3	00b	***Reserved***
B2…0	010b = [***USB 3.2***] Gen1 and Gen2	SuperSpeed USB Signaling Support

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F.2.2 *TBT3* Active Cable Discover Identity Responses

Table F-4, along with Table F-5, Table F-6 and Table F-7, defines the expected ***Discover Identity*** VDO responses for a ***TBT3*** active cable. In fields where multiple values are listed, cable responses ***may*** vary to match the specific connected cable's capabilities.

Table F-4 *TBT3* Active Cable Discovery Identity VDO Responses

Message Header						
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**	**Spec Revision**	**Rsvd**	**Message Type**
0	5…6	0…7	1 = Cable Plug	10b or 01b	0	11111b
VDM Header						
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00001b

Bit(s)	Value	Parameter
ID Header VDO		
B31	0	USB Communications Capable as USB Host
B30	0	USB Communications Capable as a USB Device
B29…27	100b = Active Cable	Product Type (Cable Plug)
B26	1 = Modal Operation Supported	Modal Operation Supported
B25…23	000b	Product Type (DFP)
B22…16	0	***Reserved***
B15…0	Per vendor	USB Vendor ID
Cert Stat VDO		
B31…0	0x00000000…0xFFFFFFFF	XID assigned by ***USB-IF***
Product VDO		
B31…16	0x0000…0xFFFF	USB Product ID
B15…0	0x0000…0xFFFF	bcdDevice
Active Cable VDO 1		
Depending on ***USB PD*** Specification Revision: See Table F-5 for ***USB PD*** Revision 2.0 or Table F-6 for ***USB PD*** Revision 3.0		
Active Cable VDO 2		
Applicable only for ***USB PD*** Revision 3.0 – See Table F-7		

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Table F-5 *TBT3* Active Cable VDO for *USB PD* Revision 2.0, Version 1.3

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	0001b – <10ns (~1m)	Cable Latency
B12…11	11b = Both ends Active, VCONN required	Cable Termination Type
B10	0 = Fixed	SSTX1 Directionality Support
B9	0 = Fixed 1= Configurable	SSTX2 Directionality Support
B8	0 = Fixed 1 = Configurable	SSRX1 Directionality Support
B7	0 = Fixed 1 = Configurable	SSRX2 Directionality Support
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4	1 = Yes	VBUS through cable
B3	0 = No 1 = Yes	SOP' controller present
B2…0	010b = [***USB 3.1***] Gen1 and Gen2	SuperSpeed USB Signaling Support

Table F-6 *TBT3* Active Cable VDO 1 for *USB PD* Revision 3.0, Version 1.2

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…21	010b = Version 1.2	VDO Version
B20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	xxxxb (e.g., 0010b – 10ns to 20ns (~2m))	Cable Latency
B12…11	11b = Both ends Active, VCONN required	Cable Termination Type
B10…9	00b = 20V	Maximum VBUS Voltage
B8	1 = Yes	SBU Supported
B7	0 = Passive 1 = Active	SBU Type
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4	0 = No 1 = Yes	VBUS through cable
B3	0 = No 1= Yes	SOP' controller present
B2…0	010b = [***USB 3.2***] Gen1 and Gen2	SuperSpeed USB Signaling Support

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Table F-7 *TBT3* Active Cable VDO 2 for *USB PD* Revision 3.0, Version 1.2

Bit(s)	Value	Parameter
B31…24	xxxxxxxxb (e.g., 10101010b = 170 °C)	Maximum Operating Temperature
B23…16	xxxxxxxxb (e.g., 11010010b = 210 °C)	Shutdown Temperature
B15	0	***Reserved***
B14…12	000b ≥ 10 mW	U3 Power
B11	0	U3 to U0 Transition mode
B10…8	000b	***Reserved***
B7…6	00b	***USB 2.0*** Hub Hops Consumed
B5	0 = Supported	***USB 2.0*** Supported
B4	0 = Supported	SuperSpeed Supported
B3	1 = two lanes	SuperSpeed Lanes Supported
B2	0	***Reserved***
B1…0	00b = Gen1 01b = Gen2	SuperSpeed Signaling

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F.2.3 *TBT3* Device Discover Identity Responses

Table F-8 defines the expected ***Discover Identity*** VDO responses for a ***TBT3*** device. In fields where multiple values are listed, device responses ***may*** vary to match the specific connected device's capabilities.

Table F-8 *TBT3* Device Discovery Identity VDO Responses

Message Header						
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**	**Spec Revision**	**Rsvd**	**Message Type**
0	4	0…7	0 = UFP	10b or 01b	0	1111b
VDM Header						
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00001b

Bit(s)	Value	Parameter
ID Header VDO		
B31	0 or 1	USB Communications Capable as USB Host
B30	0 or 1	USB Communications Capable as a USB Device
B29…27	001b = PDUSB Hub 010b = PDUSB Peripheral 101b = Alternate Mode Adapter (AMA) 110b = VCONN-Powered USB Device (VPD)	Product Type (UFP)
B26	1 = Modal Operation Supported	Modal Operation Supported
B25…23	001b = PDUSB Hub 010b = PDUSB Host 100b = Alternate Mode Controller (AMC)	Product Type (DFP)
B22…16	0	***Reserved***
B15…0	Per vendor	USB Vendor ID
Cert Stat VDO		
B31…0	0x00000000…0xFFFFFFFF	XID assigned by ***USB-IF***
Product VDO		
B31…16	0x0000…0xFFFF	USB Product ID
B15…0	0x0000…0xFFFF	bcdDevice

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F.2.4 *TBT3* Discover SVID Responses

Table F-9 defines the expected Discover SVID VDO responses for a ***TBT3*** device or cable.

Table F-9 *TBT3* Discover SVID VDO Responses

Message Header						
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**	**Spec Revision**	**Rsvd**	**Message Type**
0	3	0…7	0 = UFP	10b or 01b	0	1111b
VDM Header						
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00010b

Bit(s)	Value	Parameter
VDO 1		
B31…16	0x8087 = Intel/***TBT3***	SVID 0
B15…0	0xFF01 = VESA DP (if supported)	SVID 1
VDO 2		
B31…16	0x0000 – 0xFFFF (normally the cable manufacturer VID)	SVID 2
B15…0	0x0000 (normally)	SVID 3

If the Intel/***TBT3*** SVID of 0x8087 is not returned in response to the Discover SVID command, the cable is a Non-***TBT3*** cable.

If a Non-***TBT3*** cable's Product Type is Active Cable, it ***shall*** be regarded as not compatible with ***TBT3***, and ***TBT3*** Discovery ***shall*** exit.

If a Non-***TBT3*** cable's Product Type is Passive Cable, the USB Highest Speed field in the cable's Passive Cable VDO ***shall*** determine ***TBT3*** functionality and speed. If USB Highest speed is "***USB4*** Gen3" or higher, the cable ***shall*** be regarded as a ***TBT3*** capable cable at Gen3 performance. If USB Highest speed is "***USB 3.2*** Gen1" or "***USB 3.2***/***USB4*** Gen2", it ***shall*** be regarded as a ***TBT3*** capable cable limited to passive Gen2 performance. If USB Highest Speed indicates "***USB 2.0***-only, No SuperSpeed", ***TBT3*** Discovery ***shall*** exit.

Note: Legacy ***TBT3*** platforms ***may not*** recognize ***USB4*** Gen3 or higher passive cables that don't also include the ***TBT3*** Passive Cable ***Discover Identity*** VDOs. When this happens, the ***USB4*** Gen3 or higher passive cable will still function but will only be used at Gen2 speeds.

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F.2.5 *TBT3* Device Discover Mode Responses

Table F-10 defines the expected Discover Mode VDO responses for a ***TBT3*** device. In fields where multiple values are listed, device responses ***may*** vary to match the specific connected device's capabilities.

Table F-10 *TBT3* Device Discover Mode VDO Responses

Message Header						
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**	**Spec Revision**	**Rsvd**	**Message Type**
0	2	0…7	0 = UFP	10b or 01b	0	1111b

VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	001b	0	00011b

Bit(s)	Value	Parameter
***TBT3* SOP VDO**		
B31	0 = Not supported 1 = Supported	Vendor specific B1
B30	0 = Not supported 1 = Supported	Vendor specific B0
B29…27	000b	***Reserved***
B26	0 = Not supported 1 = Supported	Intel specific B0
B25…17	000000000b	***Reserved***
B16	0 = ***TBT3*** Adapter 1 = TBT2 Legacy Adapter	TBT Adapter
B15…0	0x0001 = TBT Mode	TBT Alternate Mode

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F.2.6 *TBT3* Cable Discover Mode Responses

Table F-11 defines the expected Discover Mode VDO responses for a ***TBT3*** cable. In fields where multiple values are listed, cable responses ***may*** vary to match the specific connected cable's capabilities.

Table F-11 *TBT3* Cable Discover Mode VDO Responses

Message Header						
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**	**Spec Revision**	**Rsvd**	**Message Type**
0	2	0…7	1 = Cable Plug	10b or 01b	0	1111b

VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	001b	0	00011b

Bit(s)	Value	Parameter
	***TBT3* SOP' VDO**	
B31…26	00000000b	***Reserved***
B25	0 = Passive cable 1 = Active cable	Active_Passive
B24	0b	***Reserved***
B23	0 = Active with bi-directional LSRX[1] communication or when Passive 1 = Active with uni-directional LSRX[1] communication	Active Cable Plug Link Training
B22	0 = Not re-timer 1 = Re-timer	Re-timer
B21	0 = Non-Optical 1 = Optical	Cable Type
B20…19	00b = 3rd Gen Non-Rounded TBT 01b = 3rd & 4th Gen Rounded and Non-Rounded TBT 10b…11b = ***Reserved***	TBT_Rounded_Support
B18…16	000b = ***Reserved*** 001b = USB3.1 Gen1 Cable (10 Gbps TBT support) 010b = 10 Gbps (***USB 3.2*** Gen1 and Gen2 passive cables) 011b = 10 Gbps and 20 Gbps (TBT 3rd Gen active cables and 20 Gbps passive cables) 100b…111b = ***Reserved***	Cable Speed
B15…0	0x0001 = TBT Mode	TBT Alternate Mode

Notes:
1. LSRX in ***TBT3*** is the same communication channel as SBRX in ***USB4***.

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F.2.7 *TBT3* Cable Enter Mode Command

Table F-12 defines the Enter Mode Command that ***shall*** be sent to the SOP' (and if needed the SOP") of an active ***TBT3*** cable to enable the cable for ***TBT3*** operation.

Table F-12 *TBT3* Cable Enter Mode Command

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	1	0…7	1 = Cable Plug		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	000b	0	00100b

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F.2.8 *TBT3* Device Enter Mode Command

Table F-13 defines the Enter Mode Command that ***shall*** be sent to the SOP of a ***TBT3*** device to enable the device for ***TBT3*** operation.

Table F-13 *TBT3* Device Enter Mode Command

Message Header						
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**	**Spec Revision**	**Rsvd**	**Message Type**
0	2	0…7	0 = UFP	10b or 01b	0	1111b

VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	000b	0	00100b

Bit(s)	Value	Parameter
	***TBT3* SOP VDO**	
B31	0 = Not supported 1 = Supported	Vendor specific B1
B30	0 = Not supported 1 = Supported	Vendor specific B0
B29…27	000b	***Reserved***
B26	0 = Not supported 1 = Supported	Intel specific B0
B25	0 = Passive cable 1= Active cable	Active_Passive
B24	0 = ***TBT3*** Adapter 1 = TBT2 Legacy Adapter	TBT Adapter
B23	0 = Active with bi-directional LSRX[1] communication or when Passive 1 = Active with uni-directional LSRX[1] communication	Active Cable Link Training
B22	0 = Not re-timer 1 = Re-timer	Re-timer
B21	0 = Non-Optical 1 = Optical	Cable Type
B20…19	00b = 3rd Gen Non-Rounded TBT 01b = 3rd & 4th Gen Rounded and Non-Rounded TBT 10b…11b = ***Reserved***	TBT_Rounded_Support
B18…16	000b = ***Reserved*** 001b = USB3.1 Gen1 Cable (10 Gbps TBT support) 010b = 10 Gbps (***USB 3.2*** Gen1 and Gen2 passive cables) 011b = 10 Gbps and 20 Gbps (TBT 3rd Gen active cables and 20 Gbps passive cables) 100b…111b = ***Reserved***	Cable Speed
B15…0	0x0001 = TBT Mode	TBT Alternate Mode

Notes:
1. LSRX in ***TBT3*** is the same communication channel as SBRX in ***USB4***.

The values to be used when sending the ***TBT3*** Device Enter Mode command to the SOP of a ***TBT3*** device are determined based on information retained from earlier in the discovery flow as follows:

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- B31 and B30: return the values received in the B31 and B30 fields of the ***TBT3*** Device Discover Mode Response.
- B26: return the value received in the B26 field of the ***TBT3*** Device Discover Mode Response.
- B25: return the value received in the B25 field of the ***TBT3*** Cable Discover Mode Response.
- B24: return the value received in the B16 field of the ***TBT3*** Device Discover Mode Response.
- B23: if using a ***TBT3*** cable, return the value received in the B23 field of the ***TBT3*** Cable Discover Mode Response, otherwise set to 0.
- B22: if using a ***TBT3*** cable, return the value received in the B22 field of the ***TBT3*** Cable Discover Mode Response, otherwise set to 0.
- B21: if using a ***TBT3*** cable, return the value received in the B21 field of the ***TBT3*** Cable Discover Mode Response, otherwise set to 0.
- B20…19: if using a ***TBT3*** cable, return the value received in the B20…19 field of the ***TBT3*** Cable Discover Mode Response, otherwise set to 00b.
- B18…16: if using a ***TBT3*** cable, return the value received in the B18…16 field of the ***TBT3*** Cable Discover Mode Response, otherwise set to 010b.

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F.2.9 *TBT3* Cable Functional Difference Summary

Table F-14 provides a summary of existing ***TBT3*** cables and the unique functional differences between them.

Table F-14 *TBT3* Cable Functional Difference Summary

Cable	Function					SOP' Configuration					
						ID Header VDO	Discover Mode (8087)				
	USB2	USB3	*TBT3* Limitations	*USB4*	DP	Passive/ Active B29…27	Re-timer B22	Passive/ Active B25	Uni/Bi Directional LSRX[1] B23	Rounded/ none B20…19	Optical/ none B21
Passive	Yes	Yes		Yes	Yes	011b	0b	0b	***N/A*** (0b)	***N/A*** (0b)	0b
TBT3 Re-timer	Yes	No	***TBT3*** Legacy[3]	No	No	100b	1b	0b	0b	00b	0b
USB4 Re-Timer (with ***TBT3***)	Yes	Yes		Yes	***Optional***	100b	1b	0b/1b	1b	01b	0b
USB4 Re-Driver (with ***TBT3***)	Yes	Yes		Yes	***Optional***	011b[2]	0b	1b	1b	01b	0b
TBT3 Limit Optical	No	No	No CLx No CC[4]	No	No	100b	0b	0b	1b	00b	1b
Linear Optical Re-Driver	No	Yes		Yes	No	100b	0b	1b	1b	01b	1b

Notes:
1. LSRX in ***TBT3*** is the same communication channel as SBRX in ***USB4***.
2. This cable is an active cable, however, to support backward combability with ***TBT3*** legacy devices, B29…27 ***should*** be set to 011b.
3. Per ***USB4*** Chapter 13 definition.
4. This cable does not support end-to-end ***USB PD*** communication.

Notes:

1. ***TBT3*** Re-timer cables only support ***TBT3*** and does not support ***USB4*** operation.
2. All other re-timer cables are as defined in Chapter 6.
3. Limit Optical cables are as defined in Chapter 6 as optically-isolated active cables.

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G Extracting Pulse Response from Sampled Data and Calculating Non-Linearity Noise

The following procedure is used to determine the linear fit pulse response and error for Linear Re-Driver (LRD) based cables.

1. The transmitter ***shall*** be configured to transmit PRBS15 pattern (as defined in ***USB4*** Specification section 4.2.1.3.4).

2. Extract the linear fit pulse from the measured waveform using the parameters specified in Table G-1.

3. Define an input pattern x(n) to be a single PRBS period of length Nseq and an output signal to be the captured waveform y(n), sampled at M times the signal baud rate.

4. Average the captured waveform at intervals of 2 PRBS repetitions (2·N·M samples) for filtering out uncorrelated noise.

5. Correlate the averaged waveform and the reference input pattern for extracting output signal y1(n) aligned to the input pattern x(n) (N·M samples).

6. Concatenate the post-cursor input pattern corresponding to the first waveform sample at the left of the input vector x(n), and the pre-cursor input pattern corresponding to the last waveform sample at the right of the input vector as following:

$$x_1[n] = [\{x(N\text{-}Npost+1), x(N\text{-}Npost+2), \ldots, x(N)\}, \{x(1), x(2), \ldots, x(N)\}, \{x(1), x(2), \ldots, x(Npre)\}]$$

7. Zero pad x1(n) to yield xz(n) such that M-1 zeros are inserted between each adjacent entry, before the first entry and after the last entry of x1(n).

8. Present the output signal y1(n) as the convolution of xz(n) and FIR filter h(n) containing Ntaps·M coefficients:

$$y_1(n) = \sum_{k=0}^{N_{taps} \cdot M} x_z(n-k) \cdot h(k)$$

and in matrix representation:

$$y_1^{[(N_{seq} \cdot M)\ x\ 1]} = X_z^{[(N_{seq} \cdot M)\ x\ (N_{taps} \cdot M)]} \cdot h^{[(N_{taps} \cdot M)\ x\ 1]}$$

$$X_z = \begin{bmatrix} x_z(N_{taps} \cdot M) & x_z(N_{taps} \cdot M - 1) & \ldots & x_z(3) & x_z(2) & x_z(1) \\ x_z(N_{taps} \cdot M + 1) & x_z(N_{taps} \cdot M) & \ldots & x_z(4) & x_z(3) & x_z(2) \\ x_z(N_{taps} \cdot M + 2) & x_z(N_{taps} \cdot M + 1) & \ldots & x_z(5) & x_z(4) & x_z(3) \\ & \vdots & & & \vdots & \\ x_z(N_{seq} \cdot M) & x_z(N_{seq} \cdot M - 1) & \ldots & x_z(N_{seq} \cdot M - N_{taps} \cdot M + 1) & & \end{bmatrix}$$

9. Extract the filter h coefficients by applying least-squares fitting:

$$h = [X_z^T \cdot X_z]^{-1} \cdot X_z^T \cdot y_1$$

where the superscript "T" denotes the matrix transpose operation.

10. Extract the linear fitting error waveform:

$$e = y_1 - X_z \cdot h$$

11. Since *e* has M phases, need to calculate *e* for each phase.

    a. Align the *e* vector to be in length of M*N

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b. Create a matrix $E^{[NxM]}$ such as $E = \begin{bmatrix} e_1 & e_2 & \dots & e_M \\ e_{M+1} & e_{M+2} & \dots & e_{2M} \\ e_{2M+1} & e_{2M+2} & \dots & e_{3M} \\ \vdots & & & \vdots \\ e_{NM+1} & e_{NM+2} & \dots & e_{NM+M} \end{bmatrix}$

c. Calculate the standard deviation of each phase. $e_{std} = std(E)$

d. $\sigma_e = \max(e_{std})$

e. The value ***should*** be normalized to the input swing: $\sigma_e = \frac{0.4}{TX_{amp}} \cdot \sigma_e$

The following parameters ***shall*** be used in the linear fit pulse calculation:

Table G-1 Linear Fit Pulse Extraction Parameters

Parameter	Value
Ntaps	100
Npost	Ntaps – Npre – 1
Npre	5
M	8

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H *USB PD* High-Voltage Design Considerations

This appendix considers the impact of having higher voltages across the USB Type-C interface. It addresses contact lifetime and product safety when the USB Type-C cable gets unplugged while high-voltage operation is still enabled. It is applicable for the ***USB Power Delivery*** defined Extended Power Range (EPR) voltages (28 V – 48 V) and the Standard Power Range (SPR) at 20 V when supply current is high.

H.1 Potential for Arcing Damage During Cable Withdrawal

Arcing can occur when the connector is unplugged if the voltage differential across the gap between the plug and receptacle VBUS contacts is greater than 12 volts. Figure H-1 shows examples of the damage that could result from arcing.

Figure H-1 Arcing Damage to USB Type-C VBUS Contacts



The following conditions can result in arcing when the cable is withdrawn:

1. Source
   - Voltage regulation when the load is suddenly removed.
2. Sink
   - Length of time for the Sink to hold the voltage on its VBUS contact.
3. Cable
   - The inductive kick on VBUS occurs in sub-100 ns.
   - Ringing on VBUS occurs in microseconds.
   - The loss of IR voltage drop from the source to the plug due to load removal occurring in 0.1 to 1 µs.

An arc can be formed when the voltage difference between the Source and Sink across the gap between connector contacts is as low as 12 volts. The arcing voltage of 12 volts only applies within a gap distance of less than 7.5 – 10 µm at normal atmospheric pressures. Above this gap distance, the arcing voltage increases significantly. Assuming 12 volts across the entire range provides a significant margin for analysis and application.

H.2 Arcing During USB Type-C Cable Withdrawal

There are two separate mechanisms that can create the voltage differential necessary to arc and with enough current can potentially damage contacts through excessive heating.

1. Inductive kickback
2. Sink discharge

Even before either of these mechanisms occur, there is initial heating because of all the current being channeled through a very small contact point where the power density creates enough heat to potentially melt metal.

Inductive Kickback

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The first arcing mechanism is due to inductive kickback which can readily create a voltage delta of 12 volts or more. This event starts at contact break and lasts less than approximately 100 ns. Inductive kickback induced arcing occurs at any VBUS voltage – it happens regardless of the starting DC voltage on VBUS. This arcing has not been seen to cause long term damage to USB Type-C cables in the past as the current is likely too low to super heat the metal (beyond forming a temporary micron-sized molten bridge) to a point where it is permanently destructive. Calculating the energy of the inductive arc as ½ Li^2 results in approximately 5 µjoules which is too low of an energy to damage the metal and correlates well with observation over the lifetime of USB Type-C connections in practice.

Sink Discharge

The second mechanism creating a voltage differential that can result in arcing is due to the discharge of the voltage at the Sink-side VBUS contact while the Source-side VBUS contact remains high. This arcing mechanism is the one with the most potential to create and sustain an arc at high enough current to heat and damage the connector contacts.

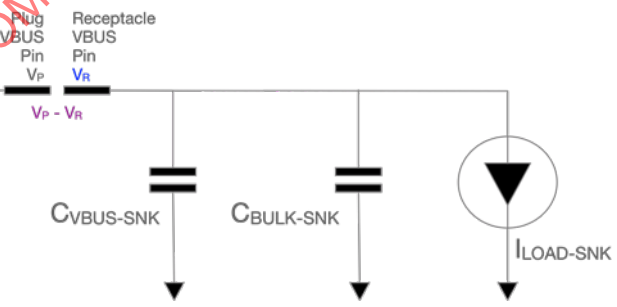
This analysis will assume that the disconnect occurs at the Sink end of a cable, but a disconnect at the Source end has the same effect.

When the disconnect occurs, the Source will continue to supply power until it detects that the Sink has been disconnected which ***may*** take up to 650 ms (***tVBUSOFF***). The VBUS contact voltage on the Source-side ***may*** quickly (~1 µs) step up in voltage due to load regulation and the elimination of any IR voltage drop through the cable. At the same time, the Sink-side contact voltage will discharge due to the load current until the Sink detects the disconnect and removes the load. This creates a voltage difference that is increasing in time.

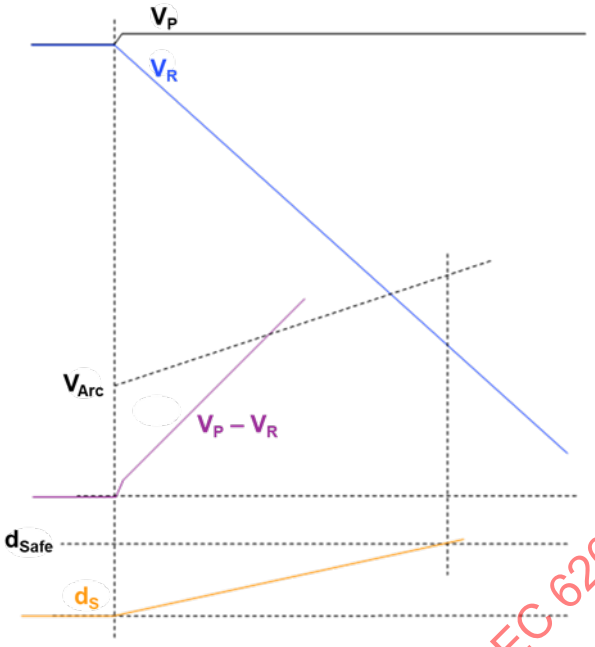
The withdrawal velocity is a factor in whether an arc will occur or not. If it is fast enough, then there is insufficient time to reach the voltage differential needed to form an arc. In practice, the withdrawal rate ***may not*** always be fast enough to keep the differential voltage below the threshold of arcing. In essence, there is a race between the contacts reaching a safe distance such that arcing will not occur at the voltages within the USB Type-C range and the voltage differential between the pins reaching the arcing voltage of 12 V.

Figure H-2 shows the potential for arcing due to Sink Discharge. At disconnect, the Source-side plug contact voltage V_P increases in voltage while the Sink-side receptacle contact starts decreasing in voltage, thus the differential voltage across the contact gap begins increasing. Note, the discharge rate of the Sink-side contact voltage is determined by the Sink load current and the Sink VBUS and ***USB PD*** bulk capacitance (***cSnkBulkPd***).

Figure H-2 Arcing Due to Discharge



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In Figure H-2, the graph shows the voltage difference V_P–V_R reaching the potential arcing voltage V_{Arc} before the contact separation d_S reaches the safe distance d_{Safe}. This would result in an arc forming and damaging the pins if the current is sufficient.

The calculated energy of this event if V_{Arc} is 15 Volts for example for 1 ms would result in 75 milli-joules which will boil the surface of the contacts resulting in significant damage.

H.3 Mitigating Arcing Damage During Cable Withdrawal Due to Sink Discharge

The goal of arcing mitigation is not necessarily to entirely prevent arcing but to prevent damage to the connector pins due to arcing that ***may*** still occur. An arc ***may*** occur without damaging the connector pins if the energy of the arcing is sufficiently low. Experimental data suggests that arcing with a current less than 1 A does not generate enough heat to damage the connector pins.

To mitigate arcing damage due to Sink discharge, the voltage between the disconnected contacts must not reach the arcing voltage of 12 volts until the distance between the contacts reaches a safe distance or the current sinking capability of the Sink must be sufficiently low at the time of arcing. The actual arcing voltage increases significantly as the gap distance increases and is not constant and has been seen to range from 12 volts at 0 µm gap distance to as high as 300 volts with a gap distance of 7.5 – 10 µm. Assuming the minimum of 12 volts throughout gives margin and is a practical design target. Likewise, the safe distance is somewhere between 7.5 – 10 µm therefore assuming 20 µm for the following analyses gives plenty of margin.

To help mitigate arcing due to Sink discharge, the Sink ***should*** manage the discharge slew rate in combination with detecting the disconnection and internally disconnecting its load. Given that it is practical, a Sink design could solely focus on limiting the slew rate to a safe level versus designing with a functional balance between the load capacitance and the time needed to detect the disconnect and remove the device's primary load. However, unplug speed and resulting distance by a human is statistical. This means that the extraction speed

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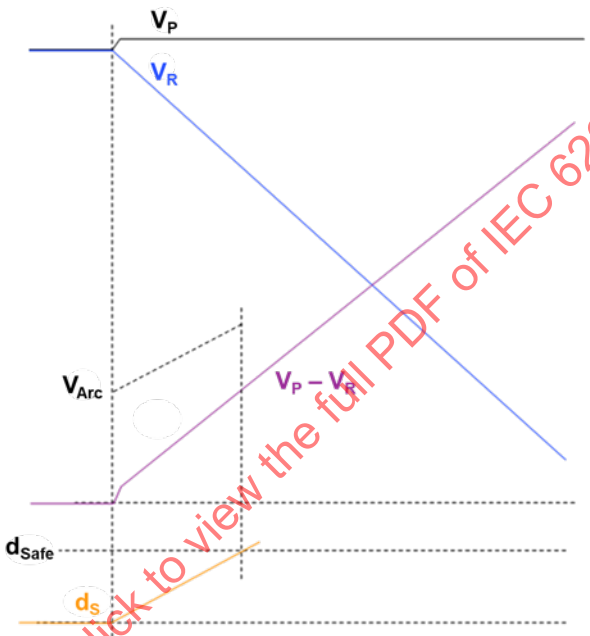
has a statistical chance to be very slow relative to the discharge time and has a statistical chance to stop at an unsafe distance. This means that there will always be observed arcing with enough unplug events.

The best approach is to limit the Sink discharge rate so that an arcing voltage will not be reached. While limiting the discharge speed in the Sink does mitigate the chance of an arc by itself, it ***should*** be used in conjunction with removing the load current. Both approaches are discussed in the following examples.

H.3.1 Limiting Sink Discharge Rate

Figure H-3 shows that arcing is prevented when the discharge rate of the Sink VBUS is slow enough such that the voltage difference V_P–V_R between the contacts does not reach the arcing voltage V_{Arc} before the contact distance dS reaches the safe distance d_{Safe}.

Figure H-3 Arcing Prevention During Sink Discharge by Limiting Slew Rate



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The slew rate of the Sink VBUS discharge is set by the max load current in the Sink and the bulk capacitance on VBUS in the Sink. Increasing the bulk capacitance slows the discharge rate. With some limited testing, the disconnect velocity of a properly designed USB Type-C connector with retention springs has been observed to be as slow as 90 mm/s. It is assumed that there will be little degradation over lifetime due to the required minimum breaking force of the connector. The time to reach the safe distance d_S of 20 µm with a breaking velocity of 90 mm/s is 220 µs. For the timing requirement in Section 4.6.2.6, 250 µs is specified therefore in this analysis, the Sink must not discharge at a rate such that 12 V is reached before 250 µs after disconnect.

Note, the plug VBUS voltage will increase immediately at disconnect when there is load current. It must be assumed that the plug VBUS voltage ***may*** increase from being at the minimum Sink VBUS voltage for the ***USB PD*** contract at disconnect to the maximum Sink VBUS voltage of the ***USB PD*** contract minus the 750 mV defined in ***vSinkPD_min***. This means that at disconnect, as the discharge of the Sink VBUS begins, the differential voltage ***may*** start anywhere between VSinkPD_max – VSinkPD_min.

A. Example of preventing arcing by slew rate limitation for a 20 Volt *USB PD* fixed contract with a max 5 A load current:

d_S = 20 µm = Safe distance to precent arcing.

V_E = 90 mm/s = Minimum contact breaking velocity.

V_{Arc} = 12 V = Minimum Arcing Voltage.

VSinkPD_max = 20 V x 1.05 = 21 V = Maximum Sink voltage at disconnect.

VSinkPD_min = 20 V x 0.95 – 750mV = 18.25V = Minimum Sink voltage at disconnect.

VDis = VSinkPD_max – VSinkPD_min = 2.75V = Maximum voltage between the contacts at disconnect.

I_{Load} = 5 A.

tSafe = d_S/ V_E = 250 µs = Time to reach the safe distance.

dV max = V_{Arc} – V_{Dis} = 12 V – 2.75 V = 9.25 V = Maximum discharge voltage before reaching V_{Arc}.

dV / dt = dV max / t_{Safe} = 9.25 V / 250 µs = 37 mV / µs = Maximum slew rate.

C_{Bulk} = I_{Load} / (dV / dT) = 5 A / 37 mV/µs = 135 µF.

In this first example, the Sink Bulk Capacitance to prevent the arcing voltage from being reached before the contacts are at a safe distance is 135 µF.

B. Example of preventing arcing by slew rate limitation for a *USB PD* EPR 48V contract operating at 48 V with a max 5 A load current:

In this example, the analysis is essentially the same as the first example but using the highest voltage request for the given EPR voltage range, in this case 48 volts.

With all other parameters and assumptions remaining the same, the follow adjustments are made:

VSinkPD_max = 48 V x 1.05 = 50.4 V.

VSinkPD_min = 48 V x 0.95 – 750mV = 44.85 V.

V_{Dis} = VSinkPD_max – VSinkPD_min = 5.55 V.

dV max = V_{Arc} – V_{Dis} = 12 V – 5.55 V = 6.45 V

dV / dt = dV max / t_{Safe} = 6.45 V / 250 µs = 25.8 mV / µs.

C_{Bulk} = I_{Load} / (dV / dT) = 5 A / 25.8 mV/µs = 194 µF.

In this second example, the Sink Bulk Capacitance to prevent the arcing voltage from being reached before the contacts are at a safe distance is 194 µF.

Note, due to the nature of ***USB PD*** contracts, the starting differential voltage between the contacts V_{Dis} at disconnect increases with increasing nominal or variable contract. This results in the dV max being lower as contract voltage gets higher. Thus, higher contract voltages will need to slow down the slew rate with higher C_{Bulk} or lower I_{Load}.

H.3.2 Load Removal

Quickly detecting the disconnect and reducing the Sink's primary load is an alternative to simply relying on managing the slew rate via adjusting the load capacitance. Based on the Sink requirements given in Section 4.6.2.6, the method analysis that follows is for detecting disconnect by the Sink based on monitoring the VBUS voltage for a drop to below the defined value for ***vSinkDisconnectPD*** and disconnecting the Sink's primary load to reduce the current that flows through the arc if an arc occurs.

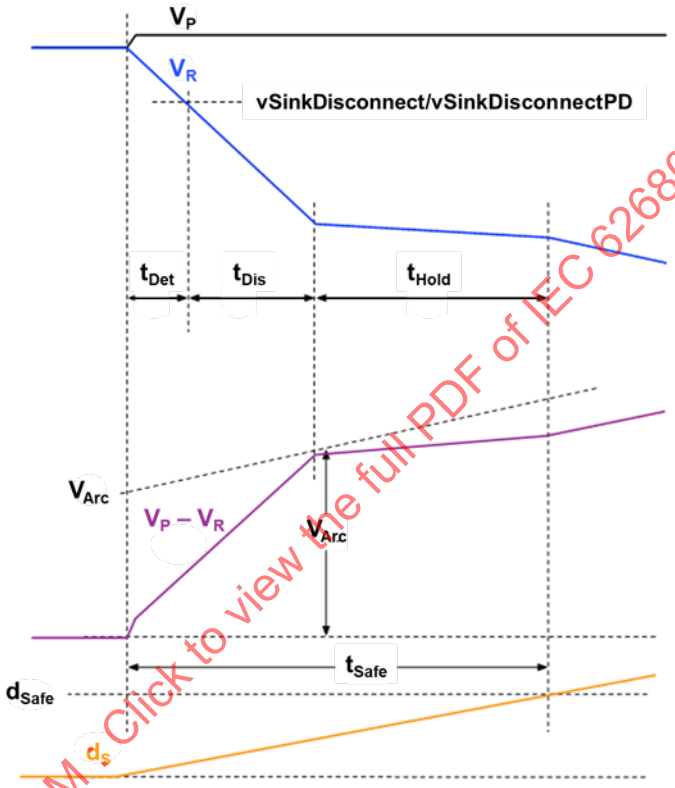
Note: As a secondary method and in addition to monitoring the VBUS voltage for disconnect, monitoring the CC voltage ***may*** give the earliest indication of disconnection – this is due to the CC contacts separating before the VBUS contacts in the connector design. The amount of time between VBUS and CC contact breaks depends

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upon the relative distance between the VBUS contact and the CC contact in the receptacle and the extraction speed. To make CC detection of the unplug most effective, a receptacle with a distance of at least 0.3 mm ***should*** be used (see Figure 3-1). For example, a system with at least 100 µF operational capacitance that only transmits mandatory ***USB PD*** messages (durations < 1.6 ms) and debounces the CC pin for no more than 200 µs will detect the detach before the VBUS contact breaks if it uses a 0.3 mm receptacle.

Figure H-4 shows an alternative to increasing the capacitance relative to the load current. In this example, the Sink detects the disconnect using ***vSinkDisconnect*** or ***vSinkDisconnectPD*** depending on the contract type to disconnect the load before V_{Arc} is reached.

Figure H-4 Arcing Prevention During Sink Discharge by Load Removal



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In this example, three timings are introduced. t_{Det} is the time from disconnect to reaching the minimum detection voltage. t_{Dis} is the remaining time for the Sink VBUS to discharge after reaching the minimum detection voltage t_{Det}. The sink must remove the load current within t_{Dis} to stop the discharge before the differential voltage between the contacts reaches V_{Arc}. tHold is the remaining time the discharge of VBUS must be halted or reduced such that V_{Arc} is not reached until t_{Safe} is has expired.

A. Example of preventing arcing by load removal for a 20 Volt *USB PD* fixed contract with a max 5 A load current:

In this analysis, some values are identical to the Limiting Sink Discharge example.

d_S = 20 µm.

V_E = 90 mm/s.

V_{Arc} = 12 V.

VSinkPD_max = 21 V.

VSinkPD_min = 18.25 V.

V_{Dis} = 2.75 V.

I_{Load} = 5 A.

t_{Safe} = 250 µs.

dV max = 9.25 V – 1 V = Maximum discharge voltage with 1 V margin before reaching V_{Arc}.

In this case, 1 V margin has been added to ensure that the sink disconnects before reaching V_{Arc}.

C_{Bulk} = 20 µF = Bulk capacitance in Sink.

In this case, C_{Bulk} is chosen to be lower than the previously calculated minimum bulk capacitance to prevent arcing by slow discharge.

dV / dt = I_{Load} / C_{Bulk} = 5 A / 20 µF = 250 mV/µs = Maximum slew rate.

Based on this maximum slew rate, the sum of (t_{Det} + t_{Dis}) can be calculated. The voltage detector and load disconnect switch can vary by implementation but the sum of these two processes needs to occur within this calculated total.

(t_{Det} + t_{Dis}) = dV max / (dV / dt) = 8.25 V / 250 mV/µs = 33 µs = time from contact disconnect to removing the load.

t_{Hold} = t_{Safe} – (t_{Det} + t_{Dis}) = 250 µs – 33 µs = 217 µs.

In this example, to prevent arcing when the bulk capacitance is 20 µF, which is not enough to keep the differential voltage between the contacts from reaching the arcing voltage V_{Arc} before the contacts reach a safe distance, the load must be removed within 33 µs after V_{BUS} contacts start to disconnect and must be held from reaching the arcing voltage for another 217 µs.

B. Example of preventing arcing by load removal for a *USB PD* EPR 48V contract operating at 48 V with a max 5 A load current:

In this example, the analysis is essentially the same as the first example but using the highest voltage request for the given EPR voltage range, in this case 48 volts. In this example, the bulk capacitance used has been increased to better illustrate balancing the mitigation approach between limiting Sink discharge rate and Sink load removal.

With all other parameters and assumptions remaining the same, the follow adjustments are made:

VSinkPD_max = 48 V x 1.05 = 50.4 V.

VSinkPD_min = 48 V x 0.95 – 750mV = 44.85 V.

V_{Dis} = VSinkPD_max – VSinkPD_min = 5.55 V.

dV max = V_{Arc} – V_{Dis} – 1 V = 12 V – 5.55 V – 1 V= 5.45 V (includes the 1 V margin)

C_{Bulk} = 100 µF = Bulk capacitance in Sink.

dV / dt = I_{Load} / C_{Bulk} = 5 A / 100 µF = 50 mV/µs

(t_{Det} + t_{Dis}) = dV max / (dV / dt) = 5.45 V / 50 mV/µs = 109.0 µs

t_{Hold} = t_{Safe} – (t_{Det} + t_{Dis}) = 250 µs – 109.0 µs = 141.0 µs.

The slew rate in this example assumes the bulk capacitance is 100 µF resulting in the load removal to be completed within 109.0 µs and the needed hold time of 141.0 µs.

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If the bulk capacitance were to be increased to 194 µF as calculated in the limiting Sink discharge rate Example B in Section H.3.1, the slew rate would decrease to 25.8 mV/µs resulting in the load removal needing to be completed within 211.2 µs and the hold time decreased to 38.8 µs.

H.3.3 Limiting Source Current Capability

To further aid in mitigating the chance of damage from an arc, the Source ***should*** monitor for disconnect and remove the sourcing capability as well as source bulk capacitance as quickly as possible. Since the source does not have a mechanism to see the sink-side voltage, it has no direct way to determine when it ***should*** have the source and bulk capacitance disconnected from VBUS. The faster the removal of the source and bulk capacitance, the less chance there is for damage from an arc.

The simplest mechanism for detecting the disconnect is the defined monitoring of the CC voltage. Note, when the source is transmitting ***USB PD*** traffic, it cannot detect the disconnect with the CC voltage until the transmitted packet is finished. ***USB PD*** transmission from the source ***should*** be a relatively low percentage of connect time resulting in a statistically low chance of hitting this scenario. Combined with the Sink properly removing the load current for arc mitigation further reduces the chance. Another mechanism for detecting disconnect would be to monitor the load drop on VBUS. A disconnect load drop is much faster than the allowed load step from a sink defined in ***USB PD***. Detection circuity can be added that distinguishes the faster load drop such that the disconnect can be detected during ***USB PD*** traffic transmission.

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I *USB PD* Encoding Guidelines for USB Type-C Product Types

This appendix provides guidance for the use of the UFP and DFP product types and UFP and DFP VDO responses for USB Type-C product examples. Refer to Section 6.4.4.3.1 (***Discover Identity***) in the ***USB Power Delivery*** specification for more information.

I.1 USB Type-C Product Type Definitions and *USB PD* Encodings

When establishing a USB Type-C connection, the ***Discover Identity*** command ***may*** be received over the link between the two products being connected. It ***should*** be noted that an Explicit Contract must already exist between the port partners before the ***Discover Identity*** command ***may*** be initiated by either product.

The product that receives a ***Discover Identity*** Command responds with a ***Discover Identity*** Command ACK which will contain multiple pieces of information including the Product Types for its UFP, DFP or both (depending on applicability) and its UFP VDO, DFP VDO or both (depending on applicability). The encoding information described below and used in the tables that follow is only a portion of the overall Command ACK response – refer to the ***USB PD*** specification for the complete ***Discover Identity*** Command ACK response requirements.

When a product has multiple USB Type-C ports, these definitions are specific to the port that is being queried by its port partner. Typically, a product with multiple ports will expose the same functionality across all of its ports but there are some situations where this isn't the case, for example, a hub will describe its upstream port differently than its collection of downstream ports. In some cases, a port ***may*** have a special purpose that is not equivalent to the other exposed ports, for example, a user-identifiable port dedicated to charging a product whereas the other port or ports have data capabilities.

In this appendix, the following ***Discover Identity*** Command ACK response items are included.

- **UFP Product Types** (Ref. ***USB PD*** Section 6.4.4.3.1.1.3)
  - **Undefined** (000b) – The responding port is not a UFP, i.e., it has no device function or device controller connected to this port. This port also does not consume power although it ***may*** connect as a Sink for the purpose of establishing a functional relationship with a Source.
  - **PDUSB Hub** (001b) – The responding port has only upstream hub functionality connected to this port. No other device function or device controller is connected to this port. The response needs to also include a UFP VDO.
  - **PDUSB Peripheral** (010b) – The responding port has at least one device function or device controller connected to this port. The response needs to also include a UFP VDO.
  - **PSD** (011b) – The responding port has no data functionality but does consume power via this port.

- **DFP Product Types** (Ref. ***USB PD*** Section 6.4.4.3.1.1.6)
  - **Undefined** (000b) – The responding port is not a DFP, i.e., it had no host controller or hub downstream functionality connected to this port. This port also does not supply power to its port partner.
  - **PDUSB Hub** (001b) – The responding port has downstream hub functionality. The response needs to also include a DFP VDO.
  - **PDUSB Host** (010b) – The responding port has a host controller connected to this port. The response needs to also include a DFP VDO.
  - **Power Brick** (011b) – The responding port has no data functionality but does supply power via this port. The response needs to also include a DFP VDO.

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- **UFP VDO – Device Capability** (Ref. ***USB PD*** Section 6.4.4.3.1.4)
  - ***USB 2.0* Device Capable** – The responding port has at least one ***USB 2.0*** device function or device controller. This bit is specific to all device function types except a ***USB 2.0*** Billboard Device Class function. When the ***USB 3.2*** Device Capable bit is set, this bit is required to be set as well. When the ***USB4*** Device Capable bit is set, this bit ***may*** or ***may not*** be set depending on if at least one of the ***USB4*** Device Capable functions maps to a ***USB 2.0*** Device Class function.
  - ***USB 2.0* Billboard only** – this bit is specific to the presence or not of a ***USB 2.0*** Billboard Device Class function. Other ***USB 2.0*** Device Capable functions ***may*** or ***may not*** exist, and if such a function does exist, the ***USB 2.0*** Device Capable bit will be used to indicate this.
  - ***USB 3.2* Device Capable** – The responding port has at least one ***USB 3.2*** device function or device controller. When the ***USB4*** Device Capable bit is set, this bit ***may*** or ***may not*** be set depending on if at least one of the ***USB4*** Device Capable functions maps to a ***USB 3.2*** Device Class function.
  - ***USB4* Device Capable** – The responding port is connected to the upstream port of a ***USB4*** device router with one or more ***USB4*** peripheral functions (CL, ***USB3***, ***DisplayPort*** or ***PCIe***).

- **UFP VDO – Highest Speed** (Ref. ***USB PD*** Section 6.4.4.3.1.4)
  - 000b = ***USB 2.0* only**, no SuperSpeed USB support.
  - 001b = ***USB 3.2* Gen1** – ***USB 2.0*** is also supported.
  - 010b = ***USB 3.2* Gen2 / *USB4* Gen2** – ***USB 2.0*** and ***USB 3.2*** Gen1 are also supported. This encoding is used both for ***USB 3.2*** Gen2 or ***USB4*** Gen2 products, and if for a ***USB4*** Gen2 product, ***USB 3.2*** Gen2 is also supported.
  - 011b = ***USB4* Gen3** – ***USB 2.0***, ***USB 3.2*** Gen1, ***USB 3.2*** Gen2 and ***USB4*** Gen2 are also supported.

- **DFP VDO – Host Capability** (Ref. ***USB PD*** Section 6.4.4.3.1.5)
  - ***USB 2.0* Host Capable** – The responding port is connected to the downstream side of a ***USB 2.0*** host controller. When either the ***USB 3.2*** Host Capable or ***USB4*** Host Capable bits are set, this bit is required to be set as well.
  - ***USB 3.2* Host Capable** – The responding port is connected to the downstream side of a ***USB 3.2*** host controller. When the ***USB4*** Host Capable bit is set, this bit is required to be set as well.
  - ***USB4* Host Capable** – The responding port is connected to the downstream side of a ***USB4*** host or device router.

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I.2 *USB PD* Encoding Guidelines Tables

Table I-1 lists examples of USB Type-C-based products and provides brief clarifying notes for each. All of the included product examples implement ***USB PD*** as either a Source, Sink or both, and will use ***USB PD*** for other functional configuration (***USB4***, ***Alternate Modes***, etc.) as appropriate to the product. This list of examples is not exhaustive and other valid combinations of features can also be described by the available ***USB PD*** encodings. Products that don't implement ***USB PD*** are not relevant to these guidelines.

Table I-2 lists the same examples (in the same order as Table I-1) and provides the recommended ***USB PD*** encoding information for the UFP and DFP Product Types along with the UFP and DFP VDOs fields associated with those product types.

Notes for these tables:

1. DC = USB Device Controller. This controller provides access to either ***USB 2.0***, ***USB 3.2*** or ***USB4*** peripheral functionality when the port is operating in its UFP data role.

2. Upstream and Downstream are in reference to the physical port locations on either a hub or dock product. By definition, a hub has only one identifiable upstream port and will have one or more downstream ports. Docks included here are hubs with extended functionality.
3. For product types: PSDs are power sinks only and don't support a UFP data connection; Power Bricks are power sources only and don't support a DFP data connection.

Table I-1 USB Type-C Product Example Clarifying Notes

Product Example	Notes
USB 3.2 **Host – no DC (e.g., Desktop PC)**	Typical of a Desktop PC that provides power to attached peripherals. This product has no UFP device controller functionality, nor does it consume power via the port.
USB 3.2 **Host – no DC – power consumer**	Typical of a notebook PC that can provide power to attached peripherals but also can consume power over this port from either a hub, dock or charger. This product has no UFP device controller functionality.
USB 3.2 **Host –** ***USB 2.0*** **DC**	This product has user-visible ***USB 2.0***-based UFP device controller functionality. This product ***may*** or ***may not*** consume power over this port from either a hub, dock or charger.
USB 3.2 **Host –** ***USB 3.2*** **DC**	This product has user-visible ***USB 3.2***-based UFP device controller functionality that also will function over a ***USB 2.0*** connection. This product ***may*** or ***may not*** consume power over this port from either a hub, dock or charger.
USB4 **Host – no DC (e.g., Desktop PC)**	Typical of a Desktop PC that provides power to attached peripherals. This product has no UFP device controller functionality, nor does it receive power via the port. Even though this host does not consume power, it will still behave as a DRP in order to be able to establish a ***USB4*** data connection with another ***USB4*** Host.
USB4 **Host – no DC – power consumer**	Typical of a notebook PC that can provide power to attached peripherals but also can consume power over this port from either a hub, dock, or charger. This product has no UFP device controller functionality.
USB4 **Host –** ***USB 2.0*** **DC**	This product has user-visible ***USB 2.0***-based UFP device controller functionality. This product ***may*** or ***may not*** consume power over this port from either a hub, dock or charger.
USB4 **Host –** ***USB 3.2*** **DC**	This product has user-visible ***USB 3.2***-based UFP device controller functionality that also will function over a ***USB 2.0*** connection. This product ***may*** or ***may not*** consume power over this port from either a hub, dock or charger.
USB4 **Host –** ***USB4*** **DC**	This product has user-visible ***USB4***-based UFP device router functionality and that functionality is also available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection. This product ***may*** or ***may not*** consume power over this port from either a hub, dock, or charger.
USB4 **Host –** ***USB4*** **DC – partial USB equiv.**	This product has user-visible ***USB4***-based UFP device router functionality and only a portion of this functionality is available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection. This product ***may*** or ***may not*** consume power over this port from either a hub, dock, or charger.
USB4 **Host –** ***USB4*** **DC – no USB equiv.**	This product has user-visible ***USB4***-based UFP device router functionality and none of this functionally is available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection. This product ***may*** or ***may not*** consume power over this port from either a hub, dock, or charger.
USB 3.2 **Peripheral**	This product provides one or more user-visible functions. Power for this product is provided either over the USB Type-C connection or by a separate power supply not associated with the USB connection. This product is not capable of supplying power to the other product.

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Product Example	Notes
***USB 3.2* Peripheral – power provider**	This product provides one or more user-visible functions. Power for this product is provided either over the USB Type-C connection or by a separate power supply not associated with the USB connection. This product is also capable of supplying power to the other product.
***USB4* Peripheral**	This product provides one or more user-visible functions, and that functionality is also available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection. Power for this product is provided either over the USB Type-C connection or by a separate power supply not associated with the USB connection. This product is not capable of supplying power to the other product.
***USB4* Peripheral – power provider**	This product provides one or more user-visible functions, and that functionality is also available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection. Power for this product is provided either over the USB Type-C connection or by a separate power supply not associated with the USB connection. This product is also capable of supplying power to the other product.
***USB4* Peripheral – partial USB equiv.**	This product provides one or more user-visible functions and only a portion of this functionality is available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection. Power for this product is provided either over the USB Type-C connection or by a separate power supply not associated with the USB connection. This product is not capable of supplying power to the other product.
***USB4* Peripheral – no USB equiv.**	This product provides one or more user-visible functions and none of this functionality is available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection. Power for this product is provided either over the USB Type-C connection or by a separate power supply not associated with the USB connection. This product is not capable of supplying power to the other product.
***USB 3.2* Hub (Upstream)**	This is the dedicated upstream port of a ***USB 3.2*** hub.
***USB 3.2* Hub (Upstream) – power provider**	This is the dedicated upstream port of a ***USB 3.2*** hub. This port can also supply power.
***USB 3.2* Hub (Downstream)**	This is one of the downstream ports of a ***USB 3.2*** hub.
***USB 3.2* Hub (Downstream) – power consumer**	This is one of the downstream ports of a ***USB 3.2*** hub. This port can also consume power.
***USB4* Hub (Upstream)**	This is the dedicated upstream port of a ***USB4*** hub.
***USB4* Hub (Upstream) – power provider**	This is the dedicated upstream port of a ***USB4*** hub. This port can also supply power.
***USB4* Hub (Downstream)**	This is one of the downstream ports of a ***USB4*** hub.
***USB4* Hub (Downstream) – power consumer**	This is one of the downstream ports of a ***USB4*** hub. This port can also consume power.
***USB4* Dock (Upstream)**	This is the dedicated upstream port of a ***USB4***-based dock that includes a ***USB4*** hub with one or more downstream USB Type-C ports. This product provides one or more user-visible functions, and that functionality is also available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection.
***USB4* Dock (Upstream) – power provider**	This is the dedicated upstream port of a ***USB4***-based dock that includes a ***USB4*** hub with one or more downstream USB Type-C ports. This product provides one or more user-visible functions, and that functionality is also available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection. This port can also supply power.
***USB4* Dock (Upstream) – partial USB equiv.**	This is the dedicated upstream port of a ***USB4***-based dock that includes a ***USB4*** hub with one or more downstream USB Type-C ports. This product provides one or more user-visible functions and that only a portion of this functionality is available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection.

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Product Example	Notes
***USB4* Dock (Upstream) – power provider - partial USB equiv.**	This is the dedicated upstream port of a ***USB4***-based dock that includes a ***USB4*** hub with one or more downstream USB Type-C ports. This product provides one or more user-visible functions and only a portion of this functionality is available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection. This port can also supply power.
***USB4* Dock (Upstream) – no USB equiv.**	This is the dedicated upstream port of a ***USB4***-based dock that includes a ***USB4*** hub with one or more downstream USB Type-C ports. This product provides one or more user-visible functions and that none of this functionality is available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection.
***USB4* Dock (Upstream) – power provider – no USB equiv.**	This is the dedicated upstream port of a ***USB4***-based dock that includes a ***USB4*** hub with one or more downstream USB Type-C ports. This product provides one or more user-visible functions and that none of this functionality is available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection. This port can also supply power.
***USB4* Dock (Downstream)**	This is one of the downstream ports of a ***USB4*** dock that includes a ***USB4*** hub.
***USB4* Dock (Downstream) – power consumer**	This is one of the downstream ports of a ***USB4*** dock that includes a ***USB4*** hub. This port can also supply power.
USB Type-C Charger	This product's only function is to be a ***USB PD*** power source.
USB Type-C Power Bank	This product's primary function is to be a ***USB PD*** power source using an internal battery as its source of power. The product also consumes power to charge its internal battery or pass power through to another port of the product.
***USB PD*-based Power Sinking Device**	This product has no USB data functionality and only uses power supplied over a ***USB PD*** connection for its non-USB purpose.

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Table I-2 *USB PD* Encoding Guidelines for Example Products

Product Examples	UFP Product Type		DFP Product Type		UFP Device Cap and Highest Speed										DFP Host Capability		
	Type	VDO Required	Type	VDO Required	*USB 2.0* Device	*USB 2.0* Billboard	*USB 3.2* Device	*USB4* Device	000b = *USB 2.0* only	001b = Gen1	010b = Gen2	011b = Gen3	100b...111b = Reserved		*USB 2.0* Host	*USB 3.2* Host	*USB4* Host
USB 3.2 Host – no DC (e.g., Desktop PC)	Undefined	None	Undefined	None											1	1	0
USB 3.2 Host – no DC – power consumer	PSD		PDUSB Host												1	1	0
USB 3.2 Host – *USB 2.0* DC	PDUSB Peripheral		PDUSB Host		1	0	0	0			000b				1	1	0
USB 3.2 Host – *USB 3.2* DC	PDUSB Peripheral		PDUSB Host		1	0	1	0			001b or 010b				1	1	0
USB4 Host – no DC (e.g., Desktop PC)	Undefined	None	PDUSB Host	None											1	1	1
USB4 Host – no DC – power consumer	PSD		PDUSB Host												1	1	1
USB4 Host – *USB 2.0* DC	PDUSB Peripheral		PDUSB Host		1	0	0	0			000b				1	1	1
USB4 Host – *USB 3.2* DC	PDUSB Peripheral		PDUSB Host		1	0	1	0			001b or 010b				1	1	1
USB4 Host – *USB4* DC	PDUSB Peripheral		PDUSB Host		1	0	1	1			010b or 011b				1	1	1
USB4 Host – *USB4* DC – partial USB equiv.	PDUSB Peripheral		PDUSB Host		1	0	1	1			010b or 011b				1	1	1
USB4 Host – *USB4* DC – no USB equiv.	PDUSB Peripheral		PDUSB Host		0	1	0	1			010b or 011b				1	1	1
USB 3.2 Peripheral	PDUSB Peripheral		Undefined		1	0	1	0			001b or 010b						
USB 3.2 Peripheral – power provider	PDUSB Peripheral		Power Brick		1	0	1	0			001b or 010b				0	0	0
USB4 Peripheral	PDUSB Peripheral		Undefined		1	0	1	1			010b or 011b						
USB4 Peripheral – power provider	PDUSB Peripheral		Power Brick		1	0	1	1			010b or 011b				0	0	0
USB4 Peripheral – partial USB equiv.	PDUSB Peripheral		Undefined		1	0	1	1			010b or 011b						
USB4 Peripheral – no USB equiv.	PDUSB Peripheral		Undefined		0	1	0	1			010b or 011b						

Notes:
1. DC = USB Device Controller (UFP)
2. Upstream and Downstream are in reference to the physical port locations.
3. For product types: PSDs are power sinks only; Power Bricks are power sources only.

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Table I-2 *USB PD* Encoding Guidelines for Example Products, cont.

Product Examples	UFP Product Type		DFP Product Type		UFP Device Cap and Highest Speed									DFP Host Capability		
	Type	VDO Required	Type	VDO Required	*USB 2.0* Device	*USB 2.0* Billboard	*USB 3.2* Device	*USB4* Device	000b = *USB 2.0* only	001b = Gen1	010b = Gen2	011b = Gen3	100b…111b = Reserved	*USB 2.0* Host	*USB 3.2* Host	*USB4* Host
USB 3.2 Hub (Upstream)	Undefined	None	Undefined	None	1	0	1	0	001b or 010b							
USB 3.2 Hub (Upstream) – power provider	PDUSB Hub	UFP VDO	Power Brick	DFP VDO	1	0	1	0	001b or 010b					0	0	0
USB 3.2 Hub (Downstream)	PDUSB Peripheral	UFP VDO	PDUSB Hub	DFP VDO										1	1	0
USB 3.2 Hub (Downstream) – power consumer	PSD	None	PDUSB Hub	DFP VDO										1	1	0
USB4 Hub (Upstream)	PDUSB Hub	UFP VDO	Undefined	None	1	0	1	1	010b or 011b							
USB4 Hub (Upstream) – power provider	PDUSB Hub	UFP VDO	Power Brick	DFP VDO	1	0	1	1	010b or 011b					0	0	0
USB4 Hub (Downstream)	Undefined	None	PDUSB Hub	DFP VDO										1	1	1
USB4 Hub (Downstream) – power consumer	PSD	None	PDUSB Hub	DFP VDO										1	1	1
USB4 Dock (Upstream)	PDUSB Peripheral	UFP VDO	Undefined	None	1	0	1	1	010b or 011b							
USB4 Dock (Upstream) – power provider	PDUSB Peripheral	UFP VDO	Power Brick	DFP VDO	1	0	1	1	010b or 011b					0	0	0
USB4 Dock (Upstream) – partial USB equiv.	PDUSB Peripheral	UFP VDO	Undefined	None	1	0	1	1	010b or 011b							
USB4 Dock (Upstream) – power provider - partial USB equiv.	PDUSB Peripheral	UFP VDO	Power Brick	DFP VDO	1	0	1	1	010b or 011b					0	0	0
USB4 Dock (Upstream) – no USB equiv.	PDUSB Peripheral	UFP VDO	Undefined	None	0	1	0	1	010b or 011b							
USB4 Dock (Upstream) – power provider – no USB equiv.	PDUSB Peripheral	UFP VDO	Power Brick	DFP VDO	0	1	0	1	010b or 011b					0	0	0
USB4 Dock (Downstream)	Undefined	None	PDUSB Hub	DFP VDO										1	1	1
USB4 Dock (Downstream) – power consumer	PSD	None	PDUSB Hub	DFP VDO										1	1	1

Notes:
1. DC = USB Device Controller (UFP)
2. Upstream and Downstream are in reference to the physical port locations.
3. For product types: PSDs are power sinks only; Power Bricks are power sources only.

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Table I-2 *USB PD* Encoding Guidelines for Example Products, cont.

Product Examples	UFP Product Type		DFP Product Type		UFP Device Cap and Highest Speed					DFP Host Capability		
	Type	VDO Required	Type	VDO Required						*USB4* Host	*USB 3.2* Host	*USB 2.0* Host
					USB 2.0 Device	*USB 2.0* Billboard	*USB 3.2* Device	*USB4* Device	000b = *USB 2.0* only			
USB Type-C Charger	Undefined	None	Undefined	None						0	0	0
	PDUSB Hub	UFP VDO	PDUSB Hub	DFP VDO								
	PDUSB Peripheral	UFP VDO	PDUSB Host	DFP VDO								
	PSD	None	Power Brick	DFP VDO								
USB Type-C Power Bank	Undefined		Power Brick						001b = Gen1	0	0	0
USB PD-based Power Sinking Device	PSD		Undefined						010b = Gen2			
									011b = Gen3			
									100b...111b = Reserved			

Notes:
1. DC = USB Device Controller (UFP)
2. Upstream and Downstream are in reference to the physical port locations.
3. For product types: PSDs are power sinks only; Power Bricks are power sources only.

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I.3 Detailed Examples

This section includes a number of detailed examples drawn from the list of product examples listed in Table I-1 and using the guidance provided by Table I-2. This set of examples was chosen to provide additional explanatory comments and for pointing out some notable characteristics.

All of the product examples fall into one of the following USB Type-C power and data role categories:

1. **Sink / UFP** – this product can only consume power and be a UFP in a data connection.
2. **Source / DFP** – this product can only supply power and be a DFP in a data connection.
3. **DRP (Source or Sink) / Not DRD (UFP)** – this product can supply or consume power and only be a UFP in a data connection.
4. **DRP (Source or Sink) / Not DRD (DFP)** – this product can supply or consume power and only be a DFP in a data connection.
5. **DRP (Source or Sink) / DRD** – this product can supply or consume power and be either a UFP or DFP in a data connection.

I.3.1 *USB 3.2* Host – no DC – Power Consumer : DRP (Source or Sink) / Not DRD (DFP)

The following summarizes the connection results for connecting this product to any of the five distinct product power/data role combinations:

	***USB 3.2* Host – no DC – power consumer**	
	DRP (Source or Sink)	**Not DRD (DFP)**
Sink / UFP	Source	DFP
Source / DFP	Sink	No connect
DRP / Not DRD (UFP)	Source or Sink	DFP
DRP / Not DRD (DFP)	Source or Sink	No connect
DRP / DRD	Source or Sink	DFP

This ***USB 3.2*** host is typical of a notebook PC that when connected to a charger or power-sourcing hub, dock or peripheral, can sink power using ***USB PD***. As this product has no UFP device controller functionality, it will not establish a data connection to any other product that isn't in a UFP data role.

As this host can sink power, the UFP Product Type is set to PSD and no UFP VDO is needed.

The DFP Product Type is set to PDUSB Host and the DFP VDO indicates that is supports ***USB 2.0*** and ***USB 3.2*** Host Capabilities.

I.3.2 *USB 3.2* Peripheral – Power Provider : DRP (Source or Sink) / Not DRD (UFP)

The following summarizes the connection results for connecting this product to any of the five distinct product power/data role combinations:

	***USB 3.2* Peripheral – power provider**	
	DRP (Source or Sink)	**Not DRD (UFP)**
Sink / UFP	Source	No connect
Source / DFP	Sink	UFP
DRP / Not DRD (UFP)	Source or Sink	No connect
DRP / Not DRD (DFP)	Source or Sink	UFP
DRP / DRD	Source or Sink	UFP

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This ***USB 3.2*** peripheral is unusual in that goes beyond a traditional peripheral by being able to supply power to a connected host, hub or dock that is capable of consuming power over the connection. An example might be a ***USB 3.2***-based dock where all of its functional capabilities connect in the UFP role after the Source/Sink relationship with its port partner are established via USB Type-C and ***USB PD*** connection protocol. If this peripheral ends up in the Source power role, the use of a ***USB PD*** Data Role Swap will be used to correctly establish the UFP data role of the peripheral's port.

The UFP Product Type is set to PDUSB Peripheral and the UFP VDO indicates ***USB 2.0*** and ***USB 3.2*** device capabilities and the highest ***USB 3.2*** speed of either Gen1 (001b) or Gen2 (010b).

As this peripheral can supply power, the DFP Product Type is set to Power Brick and the DFP VDO indicates no support for any of the USB Host Capabilities (***USB 2.0***, ***USB 3.2*** or ***USB4***).

I.3.3 *USB4* Host – Power Consumer : DRP (Source or Sink) / Not DRD (DFP)

The following summarizes the connection results for connecting this product to any of the five distinct product power/data role combinations:

	USB4 **Host – no DC – power consumer**	
	DRP (Source or Sink)	**Not DRD (DFP)**
Sink / UFP	Source	DFP
Source / DFP	Sink	No connect or ***USB4****
DRP / Not DRD (UFP)	Source or Sink	DFP
DRP / Not DRD (DFP)	Source or Sink	No connect or ***USB4****
DRP / DRD	Source or Sink	DFP

* If the port partner is also a ***USB4*** DFP.

This ***USB4*** host is similar to the ***USB 3.2*** host described earlier (see I.3.1) but differs with regard to how it works with other hosts, hubs or docks depending on the data capabilities of those other products. Both host examples do not include UFP data role support but the ***USB4*** host is capable of communicating with another ***USB4*** host as an inter-domain link even as it does not include any USB device controller functionality.

To enable two ***USB4*** DFPs to discover and establish the ***USB4*** data connection, the ***USB4*** discovery and entry process of the Source will discover the DFP VDO of the Sink which will indicate ***USB4*** Host Capability and as long as the cable also supports ***USB4***, the ***USB4*** data connection will be enabled. Following that, the ***USB4*** Connection Manager of each host will discover the inter-domain link and enable the host-to-host data connections supported by the application layer.

As this host can sink power, the UFP Product Type is set to PSD and no UFP VDO is needed.

The DFP Product Type is set to PDUSB Host and the DFP VDO indicates that it supports ***USB 2.0***, ***USB 3.2*** and ***USB4*** Host Capabilities.

I.3.4 *USB4* Host – *USB4* DC – Partial or no USB Equivalent : DRP (Source or Sink) / DRD

The following summarizes the connection results for connecting this product to any of the five distinct product power/data role combinations:

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	***USB4* Host – *USB4* DC**	
	DRP (Source or Sink)	**DRD**
Sink / UFP	Source	DFP
Source / DFP	Sink	UFP
DRP / Not DRD (UFP)	Source or Sink	DFP
DRP / Not DRD (DFP)	Source or Sink	UFP
DRP / DRD	Source or Sink	DFP or UFP

This ***USB4*** host differs from the ***USB4*** host described earlier (see I.3.3) in that it does include some ***USB4***-based UFP device functionality and therefore is a DRD. This specific example is included here to illustrate what is needed if only a portion of this device functionally is available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection.

When this example host is connected to another ***USB4*** host, its device functionality is fully available to the other host via functions that are connected to one or more of the available ***USB4*** tunneling protocols (***USB***, ***DisplayPort*** or ***PCIe***). But when this host is connected to either a ***USB 2.0*** or ***USB 3.2*** host, some or all of the ***USB4***-based device functionality is not available because it doesn't map to one of the existing USB Device Classes – in this case, the example host is required to expose a Billboard Device Class function specific to the missing functionality on the ***USB 2.0*** interface when in the UFP data role.

As this host has device controller functionality in a UFP data role, the UFP Product Type is set to PDUSB Peripheral and the UFP VDO indicates ***USB4*** device capabilities and the highest ***USB4*** speed of either Gen2 (010b) or Gen3 (011b).

Additionally, since this host supports only partial or no USB equivalent functionality when connected to a non-***USB4*** host, the UFP VDO will indicate what USB equivalent functionality is supported (***USB 2.0*** or ***USB 3.2***) along with providing a ***USB 2.0*** Billboard or indicate only the presence of a ***USB 2.0*** Billboard. The following lists the possible UFP VDO Device Capabilities combinations for this example.

***USB 2.0* Device**	***USB 2.0* Billboard**	***USB 3.2* Device**	***USB4* Device**	**Interpretation of the *USB4* host's UFP Device Capabilities**
0	1	0	1	None of the ***USB4*** device functionality maps to either ***USB 2.0*** or ***USB 3.2*** Device Class equivalents.
1	0	0	1	At least some of the ***USB4*** device functionality maps to ***USB 2.0*** Device Class equivalents but none maps to ***USB 3.2*** Device Class equivalents.
1	0	1	1	At least some of the ***USB4*** device functionality maps to ***USB 2.0*** and ***USB 3.2*** equivalents.

The DFP Product Type is set to PDUSB Host and the DFP VDO indicates that is supports ***USB 2.0***, ***USB 3.2*** and ***USB4*** Host Capabilities.

I.3.5 *USB4* Peripheral : UFP (Sink)

The following summarizes the connection results for connecting this product to any of the five distinct product power/data role combinations:

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	***USB4* Peripheral**	
	Sink	**UFP**
Sink / UFP	No connect	No connect
Source / DFP	Sink	UFP
DRP / Not DRD (UFP)	Sink	No connect
DRP / Not DRD (DFP)	Sink	UFP
DRP / DRD	Sink	UFP

This ***USB4*** peripheral provides one or more user-visible functions and that functionally is also available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection. Power for this product is provided either over the USB Type-C connection or by a separate power supply not associated with the USB connection.

The UFP Product Type is set to PDUSB Peripheral and the UFP VDO indicates ***USB 2.0***, ***USB 3.2*** and ***USB4*** device capabilities and the highest ***USB4*** speed of either Gen2 (010b) or Gen3 (011b).

As this peripheral can only sink power and has no DFP data functionality, the DFP Product Type is set to Undefined and no DFP VDO is needed.

I.3.6 *USB4* Dock (Upstream) – Power Provider : DRP (Source or Sink) / Not DRD (UFP)

The following summarizes the connection results for connecting this product to any of the five distinct product power/data role combinations:

	***USB4* Dock (Upstream) – power provider**	
	DRP (Source or Sink)	**Not DRD (UFP)**
Sink / UFP	Source	No connect
Source / DFP	Sink	UFP
DRP / Not DRD (UFP)	Source or Sink	No connect
DRP / Not DRD (DFP)	Source or Sink	UFP
DRP / DRD	Source or Sink	UFP

This is the dedicated upstream port of a ***USB4***-based dock that includes a ***USB4*** hub with one or more downstream USB Type-C ports along with one or more user-visible functions and that functionally is also available when the port is operating in either a ***USB 2.0*** or ***USB 3.2*** connection. This upstream port can also supply power.

This dock's upstream port UFP Product Type is set to PDUSB Peripheral and the UFP VDO indicates ***USB 2.0***, ***USB 3.2*** and ***USB4*** device capabilities and the highest ***USB4*** speed of either Gen2 (010b) or Gen3 (011b).

Since this dock's upstream port can also source power but has no DFP data role functionality, its DFP Product Type is Power Brick and the DFP VDO indicates no support for any of the USB Host Capabilities (***USB 2.0***, ***USB 3.2*** or ***USB4***).

I.3.7 *USB4* Hub (Downstream) – DFP (Source)

The following summarizes the connection results for connecting this product to any of the five distinct product power/data role combinations:

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	***USB4* Hub (Downstream) – power provider**	
	Source	**DFP**
Sink / UFP	Source	DFP
Source / DFP	No connect	No connect
DRP / Not DRD (UFP)	Source	DFP
DRP / Not DRD (DFP)	Source	No connect or ***USB4****
DRP / DRD	Source	DFP

* If the port partner is also a ***USB4*** DFP.

This is one of the downstream ports of a ***USB4*** hub.

When a USB host product is connected to a ***USB4*** hub downstream port, it functions similarly to ***USB 2.0*** and ***USB 3.2*** hub downstream ports by not establishing a data connection when that host is only ***USB 2.0*** or ***USB 3.2*** capable. If that USB host product is capable of ***USB4***, the ***USB4*** hub will use its ***USB4*** discovery and entry process to discover the DFP VDO of the attached ***USB4*** host and as long as the cable also supports ***USB4***, the ***USB4*** data connection will be enabled.

To enable two ***USB4*** DFPs to discover and establish the ***USB4*** data connection, the. Following that, the ***USB4*** Connection Manager of each host will discover the inter-domain link and enable the host-to-host data connections supported by the application layer

Since this hub's downstream port does not support receiving power nor does it offer any UFP data functionality in a UFP data role, the UFP Product Type is set to Undefined.

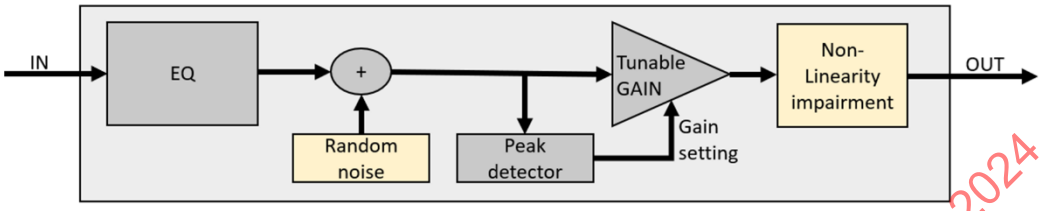
This hub's downstream port DPF Product Type is set to PDUSB Hub and the DFP VDO indicates support for all USB Host Capabilities (***USB 2.0***, ***USB 3.2*** and ***USB4***).

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J Design Assumptions for the *USB4* Gen4 LRD Cable Specification

This appendix describes the design assumptions that were used during the spec development of the ***USB4*** LRD cable. The description here is ***informative*** only and might be used as a reference for design and/or system simulations.

This is the LRD IC model used for the spec development:



The following parameters were assumed:

1. Reference CTLE is given by:

$$H(s) = \omega_{p2} \cdot \frac{S + 10^{\frac{A_{DC}}{20}} \cdot \omega_{p1}}{(S + \omega_{p1}) \cdot (S + \omega_{p2})}$$

   a. Where:

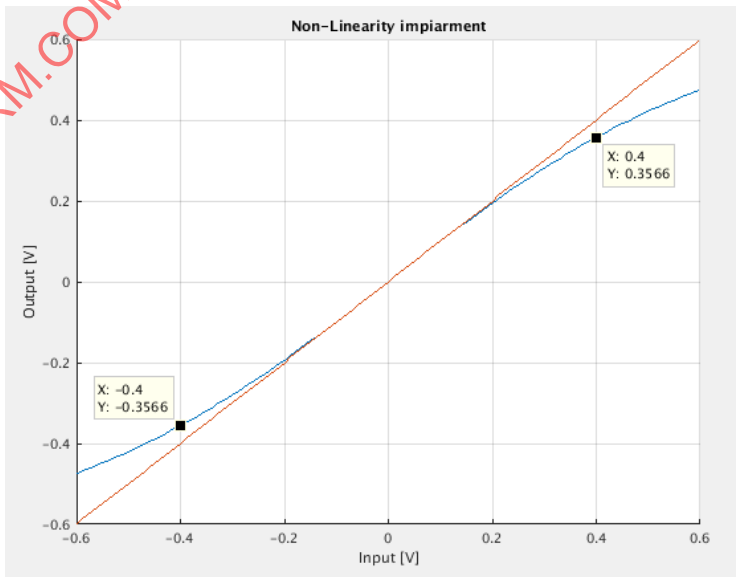
      i. A_{DC} is the DC gain (in dB)

      ii. S is the frequency in Laplace domain

      iii. $\omega_{p1} = 2 \cdot \pi \cdot 4.26e9 \ \frac{rad}{sec}$

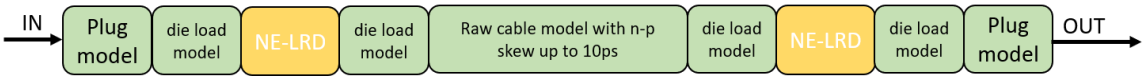
      iv. $\omega_{p2} = 2 \cdot \pi \cdot 20e9 \ \frac{rad}{sec}$

2. Random noise injection with 1.2 mV
3. Tunable gain controlled by peak detector with threshold set to 700 mV-pp
4. Gain limit of 8 dB
5. Non-linearity modeling with 1.53 · tanh(1/1.53)
   a. This reflects 1 dB compression point of 800 mV-pp (reference to input)



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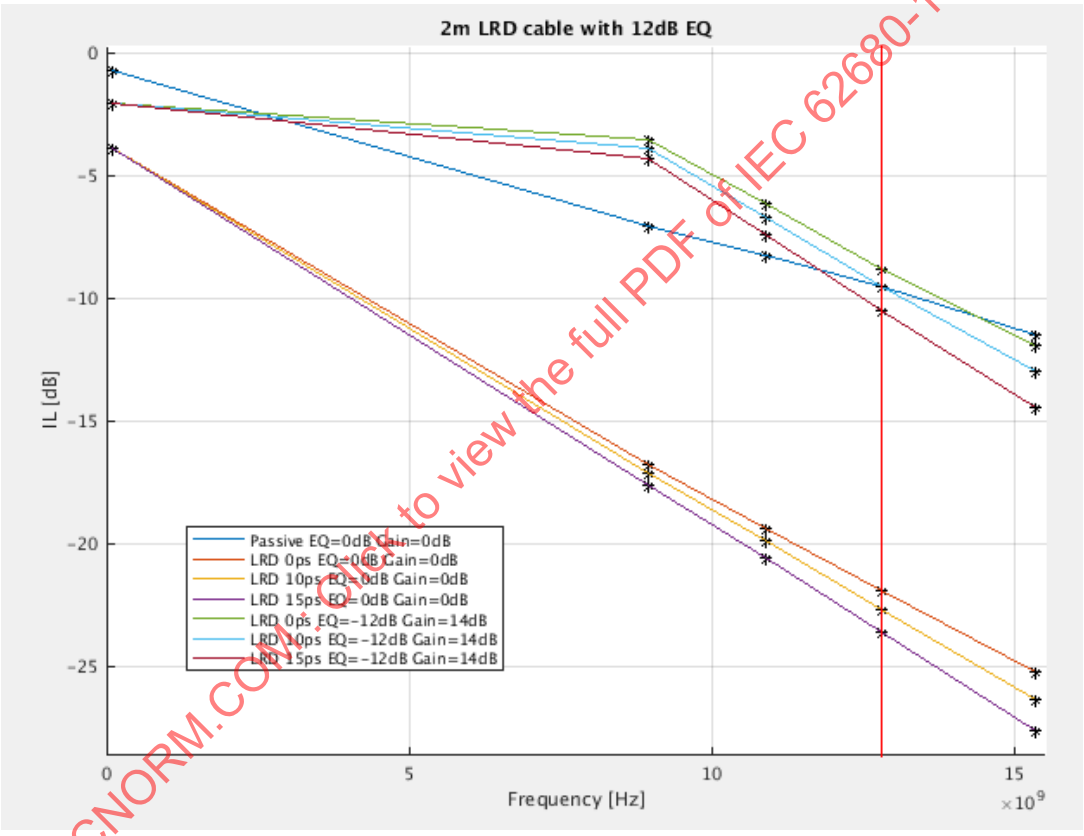
This is a cable system model used for the specification development:



The settings of the NE (near-end, i.e., closer to the TX) and FE (far-end, i.e., closer to the RX) LRDs are as follows:

1. NE EQ setting: $A_{DC} = -7dB$
2. FE EQ setting: $A_{DC} = -5dB$
3. Self-tuning gain enabled in both NE and FE LRDs
4. Raw cable n-p skew is limited to 10 ps

The response of the cable including the LRD's EQ and gain is:



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Partie 1-3: Composants communs – Spécification des câbles et des connecteurs USB Type-C®

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Bus universel en série Spécification des câbles et connecteurs de Type-C

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Version 2.3
Octobre 2023

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Sommaire

AVANT-PROPOS 428
Éditeur de la spécification 447
Contributeurs du groupe de travail de la spécification 447
Sociétés du secteur qui ont apporté leurs commentaires au stade révision de la version initiale 455
Historique des révisions 455
1 Introduction 456
1.1 Objet 456
1.2 Domaine d'application 456
1.3 Documents connexes 457
1.4 Conventions 457
1.4.1 Ordre de priorité 457
1.4.2 Mots-clés 457
1.4.3 Numérotation 458
1.5 Termes et abréviations 458
2 Vue d'ensemble 464
2.1 Introduction 464
2.2 Fiches, embases et câbles USB Type-C 465
2.3 Processus de configuration 466
2.3.1 Détection des branchements/débranchements entre la source et le destinataire 467
2.3.2 Détection de l'orientation de la fiche ou des câbles torsadés 467
2.3.3 Détection de l'alimentation initiale (source-destinataire) et établissement de la relation avec les données (hôte-dispositif) 467
2.3.4 Détection et utilisation du courant VBUS USB Type-C 468
2.3.5 Communications *USB PD* 469
2.3.6 Extensions fonctionnelles 469
2.4 VBUS 469
2.5 VCONN 470
2.6 Hubs 470
3 Mécanique 471
3.1 Vue d'ensemble 471
3.1.1 Connecteurs conformes 471
3.1.2 Ensembles câble-connecteurs conformes 471
3.1.3 Ensembles câble-connecteurs USB Type-C vers existant conformes 472
3.1.4 Ensembles adaptateurs USB Type-C vers existant conformes 473
3.2 Interfaces de couplage des connecteurs USB Type-C 474
3.2.1 Définition de l'interface 474

IECNORM.COM : Click to view the full PDF of IEC 62680-1-3:2024

3.2.2 Schémas de référence 501
3.2.3 Affectation des broches et descriptions 512
3.3 Construction des câbles et affectation des fils 513
3.3.1 Construction des câbles (*informative*) 514
3.3.2 Affectation des fils 516
3.3.3 Calibres de fil et diamètres de câble (*informatifs*) 517
3.4 Ensembles câble-connecteurs USB Type-C normalisés 519
3.4.1 Ensemble câble-connecteurs USB Type-C Complet 519
3.4.2 Ensemble câble-connecteurs *USB 2.0* Type-C 521
3.4.3 Ensemble câble-connecteurs captif USB Type-C 521
3.4.4 Ensemble USB Type-C 522
3.5 Ensembles câble-connecteurs existants 522
3.5.1 Ensemble câble-connecteurs USB Type-C vers *USB 3.1* Standard-A 523
3.5.2 Ensemble câble-connecteurs USB Type-C vers *USB 2.0* Standard-A 525
3.5.3 Ensemble câble-connecteurs USB Type-C vers *USB 3.1* Standard-B 526
3.5.4 Ensemble câble-connecteurs USB Type-C vers *USB 2.0* Standard-B 528
3.5.5 Ensemble câble-connecteurs USB Type-C vers *USB 2.0* Mini-B 529
3.5.6 Ensemble câble-connecteurs USB Type-C vers USB 3.1 Micro-B 530
3.5.7 Ensemble câble-connecteurs USB Type-C vers USB 2.0 Micro-B 531
3.6 Ensembles adaptateurs existants 532
3.6.1 Ensemble adaptateur USB Type-C vers embase *USB 3.1* Standard-A 532
3.6.2 Ensemble adaptateur USB Type-C vers embase *USB 2.0* Micro-B 533
3.7 Caractéristiques électriques 534
3.7.1 Câble brut (*informatif*) 535
3.7.2 Ensembles câble-connecteurs passifs USB Type-C vers USB Type-C 536
3.7.3 Connecteur coplé (*informatif – USB 3.2* Gen2 et *USB4* Gen2) 562
3.7.4 Exigences SI et essais de l'embase (*normatifs – USB4* Gen3/Gen4) 567
3.7.5 Ensembles câble-connecteurs USB Type-C vers USB existant (*normatifs*) 569
3.7.6 Ensembles adaptateurs USB Type-C vers USB existants (*normatifs*) 573
3.7.7 Exigences relatives à l'efficacité de l'écrantage (*normatives*) 576
3.7.8 Exigences électriques en courant continu (*normatives*) 578
3.8 Exigences mécaniques et environnementales (*normatives*) 582
3.8.1 Exigences mécaniques 582
3.8.2 Exigences environnementales 587
3.9 Applications d'accueil (*informatives*) 589
3.10 Notes relatives à la mise en œuvre et guides de conception 590
3.10.1 Gestion de la CEM (*informative*) 590

IECNORM.COM : Click to view the full PDF of IEC 62680-1-3:2024

3.10.2 Espacement physique des connecteurs empilés et adjacents (*informatif*) 594
3.10.3 Remarques sur le couplage des câbles (*informatives*) 594
3.11 Câbles EPR (Extended Power Range) 595
3.11.1 Exigences électriques 595
3.11.2 Exigences d'identification du câble EPR 595
4 Fonctionnel 596
4.1 Récapitulatif des signaux 596
4.2 Description des broches de signal 596
4.2.1 Broches *USB 3.2*/*USB4* 596
4.2.2 Broches *USB 2.0* 597
4.2.3 Broches de signal auxiliaire 597
4.2.4 Broches d'alimentation et de masse 597
4.2.5 Broches de configuration 597
4.3 Utilisation en bande latérale (SBU) 597
4.4 Alimentation et masse 598
4.4.1 Chute de tension ohmique 598
4.4.2 VBUS 599
4.4.3 VCONN 600
4.5 Canal de configuration (CC) 606
4.5.1 Vue d'ensemble de l'architecture 606
4.5.2 Exigences fonctionnelles et comportementales des broches CC 621
4.5.3 Comportement d'interopérabilité des ports USB 663
4.6 Alimentation 687
4.6.1 Exigences relatives à l'alimentation pendant la veille USB 688
4.6.2 Alimentation de la VBUS par câble USB Type-C 689
4.7 Hubs USB 695
4.8 Alimentation et charge 696
4.8.1 DFP comme source d'alimentation 696
4.8.2 Méthodes de charge non USB 699
4.8.3 Hôte destinataire 699
4.8.4 Dispositif d'alimentation 699
4.8.5 Charge d'un système avec une batterie déchargée 700
4.8.6 Chargeurs multiports USB Type-C 700
4.9 Câbles avec marquage électronique 704
4.9.1 Valeurs de paramètres 706
4.9.2 Câbles actifs 706
4.10 Accessoires alimentés par VCONN (VPA) et dispositifs USB alimentés par VCONN (VPD) 707

IECNORM.COM : Click to view the full PDF of IEC 62680-1-3:2024

4.10.1 Accessoires alimentés par VCONN (VPA) 707
4.10.2 Dispositifs alimentés par VCONN (VPD) 707
4.11 Valeurs de paramètres 709
4.11.1 Paramètres de terminaison 709
4.11.2 Paramètres de temporisation 711
4.11.3 Paramètres de tension 714
5 Découverte et mise en service *USB4* 716
5.1 Vue d'ensemble du processus de découverte et de mise en service 716
5.2 Exigences fonctionnelles concernant l'*USB4* 717
5.2.1 Exigences fonctionnelles concernant les hôtes *USB4* 717
5.2.2 Exigences fonctionnelles concernant les dispositifs USB 717
5.2.3 Prise en charge du mode alternatif *USB4* 717
5.3 Exigences d'alimentation *USB4* 718
5.3.1 Exigences d'alimentation de la source 718
5.3.2 Exigences d'alimentation du destinataire 718
5.3.3 Exigences relatives à la gestion de l'alimentation d'un dispositif 719
5.4 Exigences relatives au processus de découverte et de mise en service de l'*USB4* 719
5.4.1 Connexion USB Type-C initiale 719
5.4.2 Contrat d'alimentation USB 720
5.4.3 Processus de découverte et de mise en service de l'USB4 720
5.4.4 Fonctionnement après mise en service de l'*USB4* 726
5.5 Exigences relatives à la connexion des hubs *USB4* 727
5.5.1 Exigences relatives à la connexion initiale des ports d'un hub *USB4* 727
5.5.2 Découverte des capacités de l'hôte et de l'UFP d'un hub *USB4* 727
5.5.3 Exigences relatives à la connexion au DFP d'un hub 728
5.5.4 Exemples de processus de comportement de connexion des ports d'un hub 729
5.5.5 Connexion aux hubs *USB4* en aval 737
5.5.6 Exigences fonctionnelles concernant le repli des hubs *USB4* 737
5.6 Exigences relatives à la connexion des dispositifs *USB4* 737
5.6.1 Mise en correspondance de repli des fonctions périphériques *USB4* vers les types de classes de dispositifs USB 737
5.7 Valeurs de paramètres 739
5.7.1 Paramètres de temporisation 739
6 Câbles actifs 740
6.1 Spécifications générales applicables à tous les câbles actifs 740
6.1.1 Découverte des caractéristiques d'un câble actif 740
6.1.2 Exigences électriques 742

IECNORM.COM : Click to view the full PDF of IEC 62680-1-3:2024

6.1.3 Exigences mécaniques 782
6.2 Spécifications supplémentaires pour les câbles actifs cuivre et optiques hybrides 784
6.2.1 Schéma fonctionnel d'un câble actif 784
6.2.2 Prise en charge du mode asymétrique *USB4* 785
6.2.3 Exigences relatives aux câbles actifs *USB PD* 785
6.2.4 Comportements des câbles actifs en réponse aux événements *USB PD* 785
6.2.5 Exigences d'alimentation des câbles actifs 785
6.3 Spécifications supplémentaires pour les câbles actifs à isolation optique 786
6.3.1 Schémas fonctionnels des câbles OIAC 786
6.3.2 Limitations et exigences générales concernant les câbles OIAC 789
6.3.3 Exigences d'alimentation des câbles OIAC 791
6.3.4 Exigences relatives à l'*USB PD* d'un OIAC 791
6.3.5 Processus et diagrammes d'états de connexion des câbles OIAC 805
6.3.6 Exigences électriques supplémentaires applicables aux câbles OIAC 829
6.3.7 Exigences mécaniques supplémentaires applicables aux câbles OIAC 833
A Mode inhibition de corrosion liquide 834
A.1 Vue d'ensemble 834
A.2 Description 835
A.3 Méthodes de détection de liquide 836
A.3.1 Méthode de mesure des liquides 837
A.3.2 Méthode de mesure par impulsions 837
A.3.3 Méthode de mesure de l'impédance 838
A.4 Broches de détection de liquide dans le connecteur 841
B Mode accessoire de débogage 844
B.1 Vue d'ensemble 844
B.2 Fonctionnel 844
B.2.1 Récapitulatif des signaux 845
B.2.2 Interopérabilité des ports 845
B.2.3 Entrée en mode accessoire de débogage 845
B.2.4 Diagrammes d'états de connexion 846
B.2.5 Comportements d'interopérabilité des ports d'un DTS 855
B.2.6 Détection de l'orientation 865
B.3 Exigences de sécurité/confidentialité 866
C Audio numérique USB Type-C 867
C.1 Vue d'ensemble 867
C.2 Spécifications USB Type-C audio numérique 867
D Considérations relatives à la conception thermique des câbles actifs 869

IECNORM.COM : Click to view the full PDF of IEC 62680-1-3:2024

D.1 Introduction 869
D.2 Modèle 869
D.2.1 Hypothèses 869
D.2.2 Architecture du modèle 870
D.2.3 Sources de chaleur 871
D.2.4 Flux thermique 871
D.3 Câble actif *USB 3.2* à voie unique 873
D.3.1 Considérations relatives à la conception des câbles actifs *USB 3.2* à voie unique 873
D.4 Câbles actifs à double voie 876
D.4.1 Considérations relatives à la conception des câbles actifs *USB 3.2* à double voie 877
D.4.2 Câble actif *USB 3.2* à double voie en configuration à plusieurs ports 879
D.5 Considérations relatives à la conception des hôtes et des dispositifs *USB 3.2* 881
D.5.1 Diffusion thermique ou refroidissement à partir de l'hôte ou du dispositif 881
D.5.2 Contrôle de la température de la carte mère 882
D.5.3 Espacement élargi des ports pour les applications à plusieurs ports 882
D.5.4 Stratégies d'alimentation 882
E Modes alternatifs 883
E.1 Architecture des modes alternatifs 883
E.2 Exigences relatives aux modes alternatifs 883
E.2.1 Réaffectation des broches en mode alternatif 884
E.2.2 Exigences électriques relatives aux modes alternatifs 885
E.3 Valeurs de paramètres 888
E.4 Exemple de mode alternatif – Station d'accueil USB DisplayPort™ 888
E.4.1 Exemple de station d'accueil USB DisplayPort™ 889
E.4.2 Vue d'ensemble fonctionnelle 890
E.4.3 Récapitulatif fonctionnel 891
E.5 Exemple de processus d'entrée dans un mode alternatif avec avertissements de câble 892
E.5.1 Récapitulatif fonctionnel 893
F Découverte de compatibilité et mise en service de Thunderbolt™ 3 895
F.1 Exigences fonctionnelles concernant le mode de compatibilité *TBT3* 895
F.1.1 Exigences d'alimentations compatibles *TBT3* 895
F.1.2 Exigences relatives aux hôtes compatibles *TBT3* 895
F.1.3 Exigences en amont concernant les dispositifs compatibles *TBT3* 895
F.1.4 Exigences en aval concernant les dispositifs compatibles *TBT3* 895
F.1.5 Dispositif autoalimenté compatible *TBT3* sans règles prédéfinies pour les ports en amont 896
F.1.6 Dispositifs compatibles *TBT3* avec câble captif 896
F.2 Processus de découverte et de mise en service *TBT3* 896

IECNORM.COM : Click to view the full PDF of IEC 62680-1-3:2024

F.2.1 Réponses de découverte d'identité d'un câble passif *TBT3* 898
F.2.2 Réponses de découverte d'identité d'un câble actif *TBT3* 901
F.2.3 Réponses de découverte d'identité d'un dispositif *TBT3* 904
F.2.4 Réponses de découverte de SVID *TBT3* 905
F.2.5 Réponses de découverte de mode d'un dispositif *TBT3* 906
F.2.6 Réponses de découverte de mode d'un câble *TBT3* 907
F.2.7 Commande Enter Mode d'un câble *TBT3* 908
F.2.8 Commande Enter Mode d'un dispositif *TBT3* 909
F.2.9 Récapitulatif des différences fonctionnelles entre les câbles *TBT3* 911
G Extraction de la réponse aux impulsions des données échantillonnées et calcul du bruit de non-linéarité 913
H Considérations relatives à la conception *USB PD* haute tension 915
H.1 Éventuels dommages dus à l'arc lors du retrait du câble 915
H.2 Arc lors du retrait du câble USB Type-C 915
H.3 Atténuation des dommages dus à l'arc lors du retrait du câble en raison d'une décharge du destinataire 917
H.3.1 Limitation de la vitesse de décharge du destinataire 918
H.3.2 Retrait de la charge 920
H.3.3 Limitation de la capacité électrique de la source 922
I Lignes directrices de codage *USB PD* pour les types de produits USB Type-C 923
I.1 Définition des types de produits USB Type-C et des codages *USB PD* 923
I.2 Tableaux des lignes directrices de codage *USB PD* 924
I.3 Exemples détaillés 931
I.3.1 Hôte *USB 3.2* – pas de CC – Consommateur d'alimentation: DRP (source ou destinataire) / Non DRD (DFP) 931
I.3.2 Périphérique *USB 3.2* – Fournisseur d'alimentation: DRP (source ou destinataire) / Non DRD (UFP) 932
I.3.3 Hôte *USB4* – Consommateur d'alimentation: DRP (source ou destinataire) / Non DRD (DFP) ... 932
I.3.4 *USB4* Hôte – DC *USB4* – Équivalent partiel ou aucun équivalent USB: DRP (source ou destinataire) / DRD 933
I.3.5 Périphérique *USB4*: UFP (destinataire) 934
I.3.6 Station d'accueil *USB4* (amont) – Fournisseur d'alimentation: DRP (source ou destinataire) / Non DRD (UFP) 935
I.3.7 Hub *USB4* (aval) – DFP (source) 935
J Hypothèses de conception pour la spécification de câble LRD *USB4* Gen4 937

Figures

Figure 2-1 Interface d'une embase USB Type-C (vue de face) 465
Figure 2-2 Interface d'une fiche USB Type-C Complète (vue de face) 465

IECNORM.COM : Click to view the full PDF of IEC 62680-1-3:2024

Figure 3-1 Dimensions d'interface d'une embase USB Type-C 477
Figure 3-2 Schéma de référence des zones de contact d'un ressort CEM externe pour une fiche USB Type-C 481
Figure 3-3 Dimensions d'interface d'une fiche USB Type-C Complète 482
Figure 3-4 Empreinte de référence d'une embase USB Type-C montée à la verticale (*informative*) 486
Figure 3-5 Empreinte de référence d'une embase USB Type-C montée en surface, à angle droit et sur deux rangées (*informative*) 487
Figure 3-6 Empreinte de référence d'une embase USB Type-C hybride montée à angle droit (*informative*) 488
Figure 3-7 Empreinte de référence d'une embase USB Type-C montée en surface, au centre et sur deux rangées (*informative*) 490
Figure 3-8 Empreinte de référence d'une embase USB Type-C hybride montée au centre (*informative*) 491
Figure 3-9 Empreinte de référence d'une embase *USB 2.0* Type-C à insérer montée à angle droit (*informative*) 493
Figure 3-10 Empreinte de référence d'une embase *USB 2.0* Type-C montée à angle droit sur une rangée (*informative*) 494
Figure 3-11 Dimensions d'interface d'une fiche *USB 2.0* Type-C 495
Figure 3-12 Exigences relatives à la pointe du ressort d'écrantage CEM d'une fiche USB Type-C 500
Figure 3-13 Schéma de référence de la plaque médiane de l'embase 501
Figure 3-14 Schéma de référence du verrou latéral 503
Figure 3-15 Représentation du verrou brasé à la masse de la carte d'accès 504
Figure 3-16 Schéma de référence du ressort CEM interne d'une fiche USB Type-C Complète 505
Figure 3-17 Schéma de référence du ressort CEM interne d'une fiche *USB 2.0* Type-C 506
Figure 3-18 Schéma de référence d'une plaque CEM interne 508
Figure 3-19 Schéma de référence d'une embase USB Type-C équipée de ressorts CEM externes 509
Figure 3-20 Conception de référence de la carte d'accès d'une fiche USB Type-C Complète 511
Figure 3-21 Représentation d'une coupe d'un câble USB Type-C Complet; exemple de fil coaxial avec VCONN 514
Figure 3-22 Représentation d'une coupe d'un câble USB Type-C Complet; exemple de fil coaxial sans VCONN 515
Figure 3-23 Ensemble câble-connecteurs USB Type-C Complet normalisé 519
Figure 3-24 Ensemble câble-connecteurs USB Type-C vers *USB 3.1* Standard-A 523
Figure 3-25 Ensemble câble-connecteurs USB Type-C vers *USB 2.0* Standard-A 525
Figure 3-26 Ensemble câble-connecteurs USB Type-C vers *USB 3.1* Standard-B 526
Figure 3-27 Ensemble câble-connecteurs USB Type-C vers *USB 2.0* Standard-B 528
Figure 3-28 Ensemble câble-connecteurs USB Type-C vers *USB 2.0* Mini-B 529
Figure 3-29 Ensemble câble-connecteurs USB Type-C vers USB 3.1 Micro-B 530
Figure 3-30 Ensemble câble-connecteurs USB Type-C vers USB 2.0 Micro-B 531
Figure 3-31 Ensemble adaptateur USB Type-C vers embase *USB 3.1* Standard-A 532
Figure 3-32 Ensemble adaptateur USB Type-C vers embase *USB 2.0* Micro-B 534
Figure 3-33 Représentation des points d'essai pour un ensemble câble-connecteurs couplé 536
Figure 3-34 Exigence concernant la perte d'insertion différentielle recommandée (*USB 3.2* Gen2 et *USB4* Gen2) 537
Figure 3-35 Exigence concernant le facteur d'adaptation différentiel recommandé 538
Figure 3-36 Exigence concernant la diaphonie différentielle recommandée 538
Figure 3-37 Exigence concernant la paradiaphonie et la télédiaphonie différentielles recommandées entre la paire USB D+/D− et les paires TX/RX 539
Figure 3-38 Exigence concernant la perte d'insertion différentielle recommandée (*USB4* Gen3/Gen4) 540
Figure 3-39 Représentation de l'ajustement de la perte d'insertion à la fréquence de Nyquist 541
Figure 3-40 Spectre d'une impulsion en entrée 542
Figure 3-41 Limite IMR en fonction de ILfitatNq 543
Figure 3-42 Limite IRL en fonction de ILfitatNq 545
Figure 3-43 Exigence concernant la conversion du mode différentiel en mode commun 546

IECNORM.COM : Click to view the full PDF of IEC 62680-1-3:2024

Figure 3-44 Limite IMR en fonction de ILfit à 10 GHz (USB4 Gen3/Gen4) 550
Figure 3-45 Définition du port, de la victime et de l'agresseur 551
Figure 3-46 Limite IXT_DP et IXT_USB en fonction de ILfit à 10 GHz (*USB4* Gen3/Gen4) 552
Figure 3-47 Limite IRL en fonction de ILfit à 10 GHz (USB4 Gen3/Gen4) 552
Figure 3-48 Exigence concernant la conversion du mode différentiel en mode commun (*USB4* Gen3/Gen4) 553
Figure 3-49 Ensemble câble-connecteurs dans le système 554
Figure 3-50 Exigence concernant le couplage différentiel entre le fil CC et le fil D+/D– 557
Figure 3-51 Exigence concernant le couplage asymétrique entre le fil CC et le fil D– dans les câbles *USB 2.0* Type-C 557
Figure 3-52 Exigence concernant le couplage asymétrique entre le fil CC et le fil D– dans les câbles USB Type-C Complets 558
Figure 3-53 Exigence concernant le couplage différentiel entre le fil VBUS et le fil D+/D– 559
Figure 3-54 Exigence concernant le couplage asymétrique entre SBU_A et SBU_B 560
Figure 3-55 Exigence concernant le couplage asymétrique entre SBU_A/SBU_B et CC 560
Figure 3-56 Exigence concernant le couplage entre SBU_A et D+/D– en mode différentiel, et entre SBU_B et D+/D– en mode différentiel 561
Figure 3-57 Représentation du connecteur couplé USB Type-C 562
Figure 3-58 Limites d'impédance recommandées d'un connecteur couplé USB Type-C 563
Figure 3-59 Dimensions recommandées des vides de masse pour une embase USB Type-C 564
Figure 3-60 Limites recommandées pour la paradiaphonie et la télédiaphonie différentielles entre la paire D+/D– et les paires TX/RX 566
Figure 3-61 Limites recommandées pour la conversion du mode différentiel en mode commun 567
Figure 3-62 Limite IMR en fonction de ILfitatNq pour un ensemble câble-connecteurs USB Type-C vers existant 572
Figure 3-63 Limite IRL en fonction de ILfitatNq pour un ensemble câble-connecteurs USB Type-C vers existant 572
Figure 3-64 Essai d'efficacité de l'écrantage d'un ensemble câble-connecteurs 576
Figure 3-65 Critères de réussite et d'échec pour l'efficacité de l'écrantage 577
Figure 3-66 Diagramme de mesure de la LLCR 578
Figure 3-67 Point de mesure de la température 580
Figure 3-68 Exemple de configuration de la piste de montage pour l'essai du courant assigné 581
Figure 3-69 Exemple de montage d'essai de continuité sur 4 axes 583
Figure 3-70 Exemple de montage d'essai de résistance à l'arrachement pour les fiches sans surmoulage 586
Figure 3-71 Montage d'essai de continuité/résistance à l'arrachement de référence 586
Figure 3-72 Exemple de point de défaillance mécanique pour l'essai de résistance à l'arrachement 587
Figure 3-73 Essai de résistance à l'arrachement avec un câble dans le montage 587
Figure 3-74 Exemple de collerette pour une embase de câble USB Type-C 589
Figure 3-75 Lignes directrices relatives à la CEM pour les verrous latéraux et la plaque médiane 591
Figure 3-76 Connexions du doigt CEM sur l'enveloppe de la fiche 591
Figure 3-77 Connexions de la plaque CEM sur l'enveloppe de l'embase 592
Figure 3-78 Exemples d'ouvertures de connecteur 593
Figure 3-79 Espacement minimal recommandé entre les connecteurs 594
Figure 3-80 Espace minimal recommandé pour le surmoulage de la fiche 594
Figure 3-81 Surmoulage de la fiche de câble et surface inclinée 595
Figure 4-1 Chute de tension ohmique d'un câble 598
Figure 4-2 Chute de tension ohmique des câbles alimentés 599
Figure 4-3 Modèle logique du routage du bus de données à voie unique sur les ports USB Type-C 607
Figure 4-4 Modèle logique des ports USB Type-C du dispositif à voie unique et connexion directe 608
Figure 4-5 Modèle CC de polarisation/dépolarisation 610
Figure 4-6 Modèle CC de source de courant/dépolarisation 610
Figure 4-7 Modèle fonctionnel des broches CC1 et CC2 d'une source 613

IECNORM.COM : Click to view the full PDF of IEC 62680-1-3:2024

Figure 4-8 Modèle fonctionnel d'une source prenant en charge *USB PD* PR_Swap 614
Figure 4-9 Modèle fonctionnel des broches CC1 et CC2 d'un destinataire 615
Figure 4-10 Modèle fonctionnel d'un destinataire prenant en charge l'*USB PD* PR_Swap et VCONN_Swap 616
Figure 4-11 Modèle fonctionnel des broches CC1 et CC2 d'une DRP 617
Figure 4-12 Diagramme d'états de connexion: Source 622
Figure 4-13 Diagramme d'états de connexion: Destinataire 624
Figure 4-14 Diagramme d'états de connexion: Destinataire avec prise en charge des accessoires 625
Figure 4-15 Diagramme d'états de connexion: DRP 627
Figure 4-16 Diagramme d'états de connexion: DRP avec prise en charge de l'état Try.SRC et des modes accessoires 628
Figure 4-17 Diagramme d'états de connexion: DRP avec prise en charge de l'état Try.SNK et des modes accessoires 630
Figure 4-18 Diagramme d'états de connexion: VPD de charge 632
Figure 4-19 Sous-états Sink Power 657
Figure 4-20 Diagramme d'états de connexion par câble passif avec marqueur électronique 659
Figure 4-21 Diagramme d'états de connexion par câble actif avec marqueur électronique 659
Figure 4-22 Diagramme d'états de gestion de câble Ra 661
Figure 4-23 Modèle fonctionnel d'une source branchée à un destinataire 664
Figure 4-24 Modèle fonctionnel d'une source branchée à une DRP 665
Figure 4-25 Modèle fonctionnel d'une DRP branchée à un destinataire 666
Figure 4-26 Modèle fonctionnel d'une DRP branchée à une DRP – CAS n° 1 668
Figure 4-27 Modèle fonctionnel d'une DRP branchée à une DRP – CAS n° 2 et 3 669
Figure 4-28 Modèle fonctionnel d'une source branchée à une source 672
Figure 4-29 Modèle fonctionnel d'un destinataire branché à un destinataire 673
Figure 4-30 Modèle fonctionnel d'une DRP branchée à un VPD 674
Figure 4-31 Exemple de modèle de DRP-VPD de charge 675
Figure 4-32 Modèle fonctionnel d'une source branchée à un port de dispositif existant 683
Figure 4-33 Modèle fonctionnel d'un port hôte existant branché à un destinataire 684
Figure 4-34 Modèle fonctionnel d'une DRP branchée à un port de dispositif existant 685
Figure 4-35 Modèle fonctionnel d'un port hôte existant branché à une DRP 686
Figure 4-36 Surveillance du courant par le destinataire avec les modèles de broches CC à polarisation/dépolarisation 690
Figure 4-37 Surveillance du courant par le destinataire avec les modèles de broches CC à source de courant/dépolarisation 691
Figure 4-38 *USB PD* sur les broches CC 692
Figure 4-39 Signalisation BMC *USB PD* sur les broches CC 693
Figure 4-40 Sortie d'un câble USB Type-C en tant que fonction de charge USB Type-C non PD 698
Figure 4-41 Sortie d'un câble USB Type-C de chargeur *USB PD* de 0 A à 3 A en tant que fonction de charge 698
Figure 4-42 Sortie d'un câble USB Type-C de chargeur *USB PD* de 3 A à 5 A en tant que fonction de charge 699
Figure 4-43 Câble avec marquage électronique, VCONN étant connectée par le câble 705
Figure 4-44 Câble avec marquage électronique, avec SOP' à chaque extrémité 706
Figure 4-45 Exemple de cas d'utilisation d'un dispositif USB alimenté par VCONN de charge 709
Figure 4-46 Temporisation des DRP 712
Figure 5-1 Modèle du processus de découverte et de mise en service de l'*USB4* 721
Figure 5-2 Alignement du processus de connexion d'un hub *USB4* sur un hôte et un dispositif *USB4* 730
Figure 5-3 Processus de connexion d'un hub *USB4* avec un hôte *USB 3.2*et un dispositif *USB4* 731
Figure 5-4 Alignement du processus de connexion d'un hub *USB4* sur un hôte *USB4* et un dispositif *USB 3.2* 732
Figure 5-5 Processus de connexion d'un hub *USB4* avec un hôte et un dispositif *USB 3.2* 733
Figure 5-6 Processus de connexion d'un hub *USB4* avec un hôte *USB4* et un dispositif en mode alternatif DP 735

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Figure 5-7 Processus de connexion d'un hub *USB4* avec un hôte *USB 3.2* et un dispositif en mode alternatif DP 736
Figure 6-1 Topologies des câbles actifs 743
Figure 6-2 Points d'essai électrique USB SuperSpeed 746
Figure 6-3 Montage d'essai de conformité USB SuperSpeed 747
Figure 6-4 Définition des points de conformité 751
Figure 6-5 Masque de facteur d'adaptation différentiel RX 752
Figure 6-6 Montage d'essai de conformité du câble actif fondé sur le circuit de retemporisation 753
Figure 6-7 Exemple de variation de fréquence de l'émetteur pendant un basculement d'horloge 756
Figure 6-8 Montage d'essai fonctionnel du câble actif 757
Figure 6-9 Montage de conformité du câble actif fondé sur le circuit d'amplification linéaire 758
Figure 6-10 Paramètres de gain spécifiés pour le câble actif du circuit d'amplification linéaire 762
Figure 6-11 Limite OUTPUT_NOISE / ILfitatNq 764
Figure 6-12 Paramètres de gain pour les câbles actifs fondés sur le LRD *USB4* Gen4 767
Figure 6-13 Surveillance de négociation TxFFE sur un câble actif LRD *USB4* 773
Figure 6-14 Diagramme d'états *USB4* par canal (*informatif*) 774
Figure 6-15 Flux de sortie de l'état CL1/CL2 *USB4* Gen4 avec un câble actif LRD 777
Figure 6-16 Transition de l'état symétrique à l'état asymétrique pour l'*USB4* 778
Figure 6-17 Transition de l'état asymétrique à l'état symétrique pour l'*USB4* 780
Figure 6-18 Transfert des messages *USB PD* d'un câble OIAC 797
Figure 6-19 Permutation des rôles de transmission de données de câbles OIAC concluante 800
Figure 6-20 Permutation des rôles de transmission de données de câbles OIAC rejetée 801
Figure 6-21 Permutation des rôles de transmission de données de câbles OIAC en attente 802
Figure 6-22 Permutation des rôles de transmission de données de câbles OIAC rejetée par l'initiateur 803
Figure 6-23 Permutation des rôles de transmission de données de câbles OIAC mise en attente par l'initiateur 804
Figure 6-24 Découverte des câbles OIAC – Phase 1 806
Figure 6-25 Réamorçage des câbles OIAC – Phase 2 808
Figure 6-26 Configuration de la fiche A du câble OIAC en tant que UFP – Phase 3 809
Figure 6-27 Configuration de la fiche A du câble OIAC en tant qu'UFP – Phase 3 810
Figure 6-28 Aucune connexion possible de la fiche A du câble OIAC avec le billboard – Phase 3 811
Figure 6-29 Diagramme d'états de la fiche A d'un câble OIAC – Partie 1 (Phases 1 et 2) 813
Figure 6-30 Diagramme d'états de la fiche A d'un câble OIAC – Partie 2 (Phase 3) 816
Figure 6-31 Diagramme d'états de la fiche B d'un câble OIAC 824
Figure 6-32 Exemple d'utilisation d'un câble OIAC qui exige un adaptateur ou un hub 831
Figure A-1 Exemple de corrosion liquide électrolytique 834
Figure A-2 Inhibition de corrosion dans le modèle CC de polarisation/dépolarisation 835
Figure A-3 Inhibition de corrosion dans le modèle CC de source de courant/dépolarisation 835
Figure A-4 Inhibition de corrosion dans le modèle CC de source de courant/dépolarisation avec une autre approche 836
Figure A-5 Détection de liquide par mesurage de la fuite 837
Figure A-6 Détection de liquide avec la méthode de mesure par impulsions 838
Figure A-7 Exemple de mesurage d'un port sec 839
Figure A-8 Exemple de mesurage d'un port avec de l'eau d'osmose inverse 839
Figure A-9 Exemple de mesurage d'un port avec de l'eau du robinet 840
Figure A-10 Exemple de mesurage d'un port avec de la sueur artificielle 840
Figure A-11 Exemple de mesurage d'un port avec de l'eau de mer 841
Figure A-12 Exemple de localisation des broches/plaques de détection de liquide 842
Figure A-13 Exemple de plaque de détection de liquide le long de toutes les broches de connecteur 842
Figure A-14 Exemples de broches de détection de liquide adjacentes aux broches VBUS/SBU/CC 843
Figure A-15 Exemple de montage en surface du connecteur de détection de liquide 843

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Figure B-1 Comportement par couche du mode accessoire de débogage USB Type-C 844
Figure B-2 Interface de la fiche d'un DTS 845
Figure B-3 Diagramme d'états de connexion: Source DTS 846
Figure B-4 Diagramme d'états de connexion: Destinataire d'un DTS 847
Figure B-5 Diagramme d'états de connexion: DRP d'un DTS 848
Figure B-6 Sous-états TS Sink Power 853
Figure D-1 Modèle de câble actif (port unique, embase à montage supérieur) 870
Figure D-2 Architecture du modèle 870
Figure D-3 Sources de chaleur et voies thermiques 872
Figure D-4 Configuration des connecteurs horizontaux à empilage vertical 3 x 1 (VERT) 874
Figure D-5 Configuration des connecteurs verticaux à empilage horizontal 1 x 3 (HZ90) 874
Figure D-6 Configuration des connecteurs horizontaux à empilage horizontal 1 x 3 (HORZ) 874
Figure D-7 Câble actif *USB 3.2* à voie unique de 3 A en configuration à trois ports 875
Figure D-8 Câble actif *USB 3.2* à voie unique de 5 A en configuration à trois ports 876
Figure D-9 Incidence de la puissance du surmoulage P_O et de la température de limite thermique T_{MB} à une V_{BUS} de 3 A en configuration à port unique 877
Figure D-10 Incidence de la puissance du surmoulage P_O et de la température de limite thermique T_{MB} à une V_{BUS} de 5 A en configuration à port unique 878
Figure D-11 Conception de câbles dongles actifs *USB 3.2* (une extrémité représentée) 879
Figure D-12 Câble actif USB 3.2 à double voie de 3 A en configuration à trois ports 879
Figure D-13 Câble actif USB 3.2 à double voie de 5 A en configuration à trois ports 880
Figure D-14 Exemple: Diffuseur de chaleur supplémentaire sur l'embase de l'hôte ou du dispositif 881
Figure D-15 Exemple: Dissipation thermique sur le châssis de l'hôte ou du dispositif 882
Figure E-1 Broches disponibles pour une reconfiguration dans un câble complet 884
Figure E-2 Broches disponibles pour une reconfiguration dans des applications à connexion directe 884
Figure E-3 Mise en œuvre en mode alternatif avec un câble USB Type-C vers USB Type-C 886
Figure E-4 Mise en œuvre en mode alternatif avec un câble ou un dispositif USB Type-C vers mode alternatif 887
Figure E-5 Exemple de station d'accueil USB DisplayPort 889
Figure E-6 Exemple de processus d'entrée en mode DFP *USB4* 892
Figure F-1 Processus de découverte *TBT3* 897
Figure H-1 Dommages dus à l'arc sur les contacts USB Type-C V_{BUS} 915
Figure H-2 Arc dû à la décharge 916
Figure H-3 Empêcher la formation d'arcs pendant la décharge du destinataire en limitant la vitesse de balayage 918
Figure H-4 Empêcher la formation d'arcs pendant la décharge du destinataire 920

Tableaux

Tableau 2-1 Récapitulatif des options d'alimentation 469
Tableau 3-1 Ensembles câble-connecteurs USB Type-C normalisés 472
Tableau 3-2 Ensembles câble-connecteurs USB Type-C existants 473
Tableau 3-3 Ensembles adaptateurs USB Type-C existants 474
Tableau 3-4 Affectation des broches de l'interface d'une embase USB Type-C 512
Tableau 3-5 Affectation des broches de l'interface d'une embase USB Type-C pour la prise en charge d'*USB 2.0* uniquement 513
Tableau 3-6 Affectation des fils pour un câble USB Type-C normalisé 516
Tableau 3-7 Affectation des fils d'un câble USB Type-C pour les câbles/adaptateurs existants 517
Tableau 3-8 Calibres de fil de référence pour les ensembles câble-connecteurs USB Type-C normalisés 518
Tableau 3-9 Calibres de fil de référence pour les ensembles câble-connecteurs USB Type-C normalisés vers existant 518

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Tableau 3-10 Câblage de l'ensemble câble-connecteurs USB Type-C Complet normalisé 520
Tableau 3-11 Câblage de l'ensemble câble-connecteurs *USB 2.0* Type-C normalisé 521
Tableau 3-12 Câblage de l'ensemble câble-connecteurs USB Type-C vers *USB 3.1* Standard-A 524
Tableau 3-13 Câblage de l'ensemble câble-connecteurs USB Type-C vers *USB 2.0* Standard-A 525
Tableau 3-14 Câblage de l'ensemble câble-connecteurs USB Type-C vers *USB 3.1* Standard-B 526
Tableau 3-15 Câblage de l'ensemble câble-connecteurs USB Type-C vers *USB 2.0* Standard-B 528
Tableau 3-16 Câblage de l'ensemble câble-connecteurs USB Type-C vers *USB 2.0* Mini-B 529
Tableau 3-17 Câblage de l'ensemble câble-connecteurs USB Type-C vers USB 3.1 Micro-B 530
Tableau 3-18 Câblage de l'ensemble câble-connecteurs USB Type-C vers USB 2.0 Micro-B 532
Tableau 3-19 Câblage de l'ensemble adaptateur USB Type-C vers embase *USB 3.1* Standard-A 533
Tableau 3-20 Câblage de l'ensemble adaptateur USB Type-C vers embase *USB 2.0* Micro-B 534
Tableau 3-21 Exemples de perte d'insertion différentielle pour USB TX/RX avec une construction en paire torsadée 535
Tableau 3-22 Exemples de perte d'insertion différentielle pour USB TX/RX avec une construction coaxiale. 536
Tableau 3-23 Paramètres clés du fichier de configuration de la COM 555
Tableau 3-24 Exigences électriques concernant les fils CC et SBU 556
Tableau 3-25 Matrice de couplage des signaux à basse vitesse 556
Tableau 3-26 Inductance mutuelle maximale (M) entre VBUS et les lignes de signaux à basse vitesse 559
Tableau 3-27 Exigences relatives à l'intégrité du signal USB D+/D− pour les ensembles câble-connecteurs passifs USB Type-C vers USB Type-C 561
Tableau 3-28 Caractéristiques recommandées d'intégrité de signal pour des connecteurs couplés USB Type-C (*informatives*) 565
Tableau 3-29 Caractéristiques d'intégrité de signal pour une embase USB Type-C pour *USB4* Gen3 (*normatives*) 568
Tableau 3-30 Exigences relatives à l'intégrité du signal USB D+/D− pour les ensembles câble-connecteurs USB Type-C vers USB existant (*normatives*) 569
Tableau 3-31 Objectifs de conception pour les ensembles câble-connecteurs USB Type-C vers *USB 3.1* Gen2 existant (*informatifs*) 570
Tableau 3-32 Exigences relatives à l'intégrité du signal pour un ensemble câble-connecteurs USB Type-C vers *USB 3.1* Gen2 existant (*normatives*) 571
Tableau 3-33 Exigences relatives à l'intégrité du signal USB D+/D− pour les ensembles adaptateurs USB Type-C vers USB existant (*normatives*) 574
Tableau 3-34 Objectifs de conception pour les ensembles adaptateurs USB Type-C vers *USB 3.1* Standard-A (*informatifs*) 574
Tableau 3-35 Exigences relatives à l'intégrité du signal pour un ensemble adaptateur USB Type-C vers embase *USB 3.1* Standard-A (*normatives*) 575
Tableau 3-36 CCI d'essai du courant assigné 580
Tableau 3-37 Exigence concernant la résistance en courant continu maximale (*normative*) 581
Tableau 3-38 Exigences relatives à la force et au moment 584
Tableau 3-39 Conditions d'essai environnementales 588
Tableau 3-40 Matériaux de référence 588
Tableau 4-1 Liste des signaux utilisés sur les connecteurs USB Type-C 596
Tableau 4-2 Caractéristiques d'une source VBUS 599
Tableau 4-3 Caractéristiques d'un destinataire VBUS 600
Tableau 4-4 Récapitulatif des exigences de tension VCONN du port Source USB Type-C 601
Tableau 4-5 Caractéristiques d'une source VCONN 602
Tableau 4-6 Caractéristiques d'un destinataire VCONN de câble 603
Tableau 4-7 Caractéristiques d'un destinataire VPA (accessoire alimenté par VCONN) 604
Tableau 4-8 Caractéristiques d'un destinataire VPD (dispositif alimenté par VCONN) 605
Tableau 4-9 Interopérabilité d'un port USB Type-C 609
Tableau 4-10 Point de vue de la source 611

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Tableau 4-11 Comportements de la source (hôte) et du destinataire (dispositif) par état 611
Tableau 4-12 Mise en œuvre recommandée de Try.SRC et Try.SNK pour les ports double fonction avec rôles préférentiels 619
Tableau 4-13 Récapitulatif du comportement de permutation des ports *USB PD* 619
Tableau 4-14 Utilisation de la permutation des rôles d'alimentation et de données pour les ports double fonction avec des rôles préférentiels 620
Tableau 4-15 Récapitulatif du modèle comportemental des rôles d'alimentation 620
Tableau 4-16 États des broches CC d'un port source 634
Tableau 4-17 États des broches CC d'un port destinataire 634
Tableau 4-18 États obligatoires et facultatifs 662
Tableau 4-19 Ordre de priorité pour l'utilisation des sources d'alimentation 688
Tableau 4-20 Annonce de courant USB Type-C et équivalent PDP 690
Tableau 4-21 Limite de courant maximal du destinataire lorsqu'il est branché au CTVPD 694
Tableau 4-22 Exemples de courant maximal entre le VPD de charge et le destinataire selon l'impédance sur les broches VBUS et GND 695
Tableau 4-23 Exemples de chargeurs à capacité partagée à 4 ports et de politiques de partage de puissance 702
Tableau 4-24 Temporisation SOP' et SOP" 706
Tableau 4-25 Exigences relatives à l'impédance CC du VPD de charge (RccCON) 708
Tableau 4-26 Exigences relatives au découplage de la VBUS du port de charge du CTVPD 708
Tableau 4-27 Exigences relatives aux terminaisons CC de la source (Rp) 709
Tableau 4-28 Exigences relatives aux terminaisons CC du destinataire (Rd) 710
Tableau 4-29 Exigences relatives aux terminaisons des câbles alimentés 710
Tableau 4-30 Exigences relatives aux terminaisons CC pour les états Disabled, ErrorRecovery et Unpowered Source 710
Tableau 4-31 Exigences relatives aux terminaisons SBU 711
Tableau 4-32 Paramètres de temporisation de la VBUS et de la VCONN 711
Tableau 4-33 Paramètres de temporisation des DRP 712
Tableau 4-34 Paramètres de temporisation des CC 713
Tableau 4-35 Tensions CC côté source – USB par défaut 714
Tableau 4-36 Tensions CC côté source – 1,5 A à 5 V 714
Tableau 4-37 Tensions CC côté source – 3,0 A à 5 V 714
Tableau 4-38 Tension sur les broches CC d'un destinataire – Courant USB Type-C par défaut uniquement 714
Tableau 4-39 Tension sur les broches CC d'un destinataire – Annonces de courant de plusieurs sources 715
Tableau 4-40 Tension de blocage de la broche CC 715
Tableau 5-1 Câbles certifiés lorsqu'un fonctionnement compatible *USB4* est attendu 724
Tableau 5-2 Mise en correspondance de repli des fonctions périphériques USB4 vers les types de classes de dispositifs USB 738
Tableau 5-3 Disponibilité USB Billboard Device Class à l'issue d'un échec de mise en service d'un dispositif *USB4* 739
Tableau 6-1 Récapitulatif de l'identité de câble *USB4* 741
Tableau 6-2 Caractéristiques d'un câble actif 742
Tableau 6-3 Exigences relatives aux SBU des câbles actifs 743
Tableau 6-4 Exigences relatives à la mise sous tension des câbles actifs 745
Tableau 6-5 Délai *USB 3.2* U0 maximal pour un câble OIAC 745
Tableau 6-6 Exigences relatives aux états U de l'*USB 3.2* 746
Tableau 6-7 Oscillation de la source contrainte *USB 3.2* d'un câble actif, TP1 748
Tableau 6-8 Gigue de la source contrainte *USB 3.2* d'un câble actif, TP1 748
Tableau 6-9 Oscillation de l'entrée *USB 3.2* d'un câble actif au niveau du TP2 (*informative*) 749
Tableau 6-10 Oscillation de la sortie *USB 3.2* d'un câble actif au niveau du TP3 (*informative*) 749
Tableau 6-11 Définition des points de conformité 751

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Tableau 6-12 Exigences d'alimentation *USB4* à l'état CL pour les câbles actifs 753
Tableau 6-13 Spécifications de sortie du câble actif *USB4* fondé sur le circuit de retemporisation, appliquées pour toutes les vitesses (au niveau de TP3') 754
Tableau 6-14 Conditions de réception contraintes pour un essai de conformité de câble *USB4* Gen2 et Gen3 (au niveau de TP2) 757
Tableau 6-15 Paramètres de sortie du câble actif fondé sur le circuit d'amplification linéaire 760
Tableau 6-16 Signal d'entrée au niveau de TP2 pour l'essai de conformité 761
Tableau 6-17 Limites ILfitMask d'un câble actif fondé sur le LRD *USB4* Gen4 766
Tableau 6-18 Schéma de câblage d'un câble actif fondé sur le LRD *USB4* Gen4 pour la conformité 768
Tableau 6-19 Surveillance des transactions SBx d'un câble actif *USB4* Gen4 769
Tableau 6-20 Paramètres de temporisation logique d'un câble actif LRD *USB4* 770
Tableau 6-21 Surveillance du registre LRD_Tuning *USB4* 782
Tableau 6-22 Exigences relatives à la température des câbles 783
Tableau 6-23 Gestion des messages *USB PD* d'un OIAC 792
Tableau 6-24 PDO Sink_Capabilities recommandé d'un câble OIAC (SOP) lors de la connexion initiale 793
Tableau 6-25 PDO Sink_Capabilities recommandé d'un câble OIAC (SOP) lors de la connexion active 793
Tableau 6-26 RDO Active Sink recommandé d'un câble OIAC (SOP) 794
Tableau 6-27 Temporisation des messages *USB PD* d'un câble OIAC 798
Tableau 6-28 Capacités des ports et des fiches 805
Tableau 6-29 Exigences relatives aux états U de l'*USB 3.2* 832
Tableau 6-30 Exigences d'alimentation *USB4* à l'état CL pour les câbles OIAC 833
Tableau A-1 Exemples de conditions d'essai de mesure 838
Tableau B-1 Interopérabilité des ports des DTS-TS 845
Tableau B-2 Valeurs du courant de charge Rp/Rp pour la source d'un DTS 853
Tableau B-3 États obligatoires et facultatifs 855
Tableau D-1 Exemples de sources de chaleur et de dissipation thermique (câble de 1,5 W et 5 A) 872
Tableau D-2 Études de cas de conception de câbles actifs *USB 3.2* à port unique avec une température ambiante de 35 °C et une limite thermique de 60 °C (voie unique) 873
Tableau D-3 Études de cas de conception de câbles actifs *USB 3.2* à port unique avec une température ambiante de 35 °C et une limite thermique de 60 °C (double voie) 877
Tableau E-1 Exigences électriques concernant l'USB Safe State 887
Tableau E-2 Disponibilité USB Billboard Device Class à l'issue d'un échec d'entrée en mode alternatif 888
Tableau E-3 Exigences relatives à l'ajout de bruits sur les signaux en mode alternatif 888
Tableau F-1 Réponses de VDO de découverte d'identité d'un câble passif *TBT3* 899
Tableau F-2 VDO d'un câble passif TBT3 pour l'USB PD Révision 2.0, Version 1.3 900
Tableau F-3 VDO d'un câble passif TBT3 pour l'USB PD Révision 3.0, Version 1.2 900
Tableau F-4 Réponses de VDO de découverte d'identité d'un câble actif *TBT3* 901
Tableau F-5 VDO d'un câble actif *TBT3* pour l'*USB PD* Révision 2.0, Version 1.3 902
Tableau F-6 VDO 1 d'un câble actif TBT3 pour l'USB PD Révision 3.0, Version 1.2 902
Tableau F-7 VDO 2 d'un câble actif TBT3 pour l'USB PD Révision 3.0, Version 1.2 903
Tableau F-8 Réponses de VDO de découverte d'identité d'un dispositif *TBT3* 904
Tableau F-9 Réponses de VDO de découverte de SVID *TBT3* 905
Tableau F-10 Réponses de VDO de découverte de mode d'un dispositif *TBT3* 906
Tableau F-11 Réponses de VDO de découverte de mode d'un câble *TBT3* 907
Tableau F-12 Commande Enter Mode d'un câble *TBT3* 908
Tableau F-13 Commande Enter Mode d'un dispositif *TBT3* 909
Tableau F-14 Récapitulatif des différences fonctionnelles entre les câbles *TBT3* 911
Tableau G-1 Paramètres d'extraction de l'impulsion linéaire 914
Tableau I-1 Clarifications pour les exemples de produits USB Type-C 925
Tableau I-2 Lignes directrices relatives au codage *USB PD* pour les exemples de produits 928

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Sociétés du secteur qui ont apporté leurs commentaires au stade révision de la version initiale

Aces	JST Mfg. Co., Ltd.	Pericom
Fairchild Semiconductor	Korea Electric Terminal	Semtech Corporation
Fujitsu Ltd.	Marvell Semiconductor	Silicon Image
Industrial Technology Research Institute (ITRI)	Motorola Mobility LLC	SMK Corporation
Joinsoon Electronics Mfg. Co. Ltd.	PalCONN/PalNova (Palpilot International Corp.)	Toshiba Corporation

Historique des révisions

Version	Date	Description
1.0	11 août 2014	Version initiale.
1.1	3 avril 2015	Réédition papier comprenant l'incorporation de l'ensemble des ECN approuvés à la date de révision, ainsi que les corrections rédactionnelles.
1.2	25 mars 2016	Réédition papier comprenant l'incorporation de l'ensemble des ECN approuvés à la date de révision, ainsi que les corrections rédactionnelles.
1.3	14 juillet 2017	Réédition papier comprenant l'incorporation de l'ensemble des ECN approuvés à la date de révision, ainsi que les corrections rédactionnelles.
1.4	29 mars 2019	Réédition papier comprenant l'incorporation de l'ensemble des ECN approuvés à la date de révision, ainsi que les corrections rédactionnelles.
2.0	Août 2019	Nouvelle version essentiellement destinée à permettre l'activation de la spécification ***USB4*** sur les connecteurs et câbles USB Type-C. Comprend également l'incorporation de l'ensemble des ECN approuvés à la date de révision, ainsi que les corrections rédactionnelles.
2.1	Mai 2021	Nouvelle version essentiellement destinée à l'application de l'Extended Power Range (EPR) et définissant les câbles EPR conjointement avec la Spécification R3.1 V1.0 ***USB Power Delivery***. Comprend également l'incorporation de l'ensemble des ECN approuvés à la date de révision, ainsi que les corrections rédactionnelles.
2.2	Octobre 2022	Nouvelle version essentiellement destinée à permettre l'activation de la spécification ***USB4*** Version 2.0 (80 Gbit/s) sur les connecteurs et câbles USB Type-C. Comprend également l'incorporation de l'ensemble des ECN approuvés à la date de révision, ainsi que les corrections rédactionnelles.
2.3	Octobre 2023	Nouvelle version essentiellement destinée à *déconseiller* le ***Mode accessoire d'adaptateur audio*** et à le *remplacer* par le ***Mode inhibition de corrosion liquide***, et à mettre à jour la définition et les comportements de la ***Capacité partagée des chargeurs multiports***. Comprend également l'incorporation de l'ensemble des ECN approuvés à la date de révision. Note: Cette version a été créée à l'aide d'un nouveau modèle de document qui inclut des ajustements de style et des corrections rédactionnelles.

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1 Introduction

Face au succès continu de l'interface USB, il est devenu nécessaire d'adapter la technologie USB aux nouvelles plateformes et aux nouveaux dispositifs informatiques dont la conception est de plus en plus compacte, fine et légère. Un grand nombre de ces plateformes et dispositifs récents ont atteint un stade auquel les fiches et embases USB actuellement en usage constituent un frein à l'innovation, en particulier en raison de leur taille relativement importante et des contraintes de volume interne des versions Standard-A et Standard-B des connecteurs USB. De plus, avec l'évolution des modèles d'utilisation de ces plateformes, les exigences de convivialité et de robustesse ont également évolué. Or, à l'origine, les connecteurs USB existants n'ont pas été conçus pour répondre à ces nouvelles exigences. La présente spécification établit un nouvel écosystème de connecteurs USB, qui répond aux besoins évolutifs des plateformes et dispositifs tout en conservant tous les avantages fonctionnels de la norme USB, qui constituent le fondement de l'interface d'interconnexion informatique la plus populaire.

1.1 Objet

La présente spécification définit les fiches et embases, ainsi que les câbles USB Type-C®.

La spécification des câbles et connecteurs USB Type-C est guidée par les principes suivants:

- favoriser des critères de forme d'hôtes et dispositifs innovants et agréables, où la taille, la conception industrielle et le style constituent des paramètres importants;
- interagir en toute fluidité avec les solutions d'hôtes et de dispositifs USB silicium actuelles;
- améliorer la facilité d'utilisation pour la connexion des dispositifs USB, en réduisant autant que possible le risque de confusion lors de l'insertion des connecteurs et des câbles.

La spécification des câbles et connecteurs USB Type-C définit des techniques de connexion et de détection des embases, fiches et câbles USB, qui sont compatibles avec les spécifications électriques et fonctionnelles d'interface USB existantes. La présente spécification couvre les aspects suivants, qui sont nécessaires à la production et à l'utilisation de cette nouvelle solution de câble/connecteur USB pour les plateformes et dispositifs récents, et qui interagissent avec les plateformes et dispositifs actuels:

- les embases USB Type-C, notamment la description électromécanique et les exigences de performance;
- les fiches et les ensembles câble-connecteurs USB Type-C, notamment la description électromécanique et les exigences de performance;
- les ensembles câble-connecteurs et les adaptateurs USB Type-C pour la connexion avec les solutions existantes;
- la configuration d'interface et la détection des dispositifs USB Type-C, notamment la prise en charge des solutions de connexion existantes;
- le système ***USB Power Delivery*** optimisé pour les connecteurs USB Type-C.

La spécification des câbles et connecteurs USB Type-C définit un mécanisme normalisé qui prend en charge les ***modes alternatifs***, comme la reconversion du connecteur pour un usage spécifiquement lié au branchement.

1.2 Domaine d'application

La présente spécification complète les spécifications ***USB 2.0***, ***USB 3.2***, ***USB4®*** et ***USB Power Delivery*** existantes. Elle ne s'applique qu'aux éléments exigés pour la mise en œuvre et la prise en charge des fiches et embases, ainsi que des câbles USB Type-C.

Des informations ***normatives*** sont fournies pour assurer l'interopérabilité des composants conçus selon la présente spécification. Lorsqu'elles sont fournies, des exemples de mises en œuvre peuvent être fournis à titre ***informatif***.

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1.3 Documents connexes

USB 2.0 ***Spécification Universal Serial Bus Révision 2.0***
Inclut l'édition intégrale du document.

USB 3.2 ***Spécification Universal Serial Bus Révision 3.2***
Inclut l'édition intégrale du document.
USB 3.1 Legacy Cable and Connector Specification, Révision 1.0

USB4 ***USB4 Specification, Version 2.0, octobre 2022***
(y compris les errata et ECN publiés)

TBT3 *Article 13 du document* ***USB4 Specification, Version 2.0, octobre 2022***

USB PD ***USB Power Delivery Specification, Révision 2.0, Version 1.3, 12 janvier 2017***
USB Power Delivery Specification, Révision 3.2, Version 1.0, octobre 2023
(y compris les errata et ECN publiés)

USB BB ***USB Billboard Device Class Specification, Révision 1.2.2, 29 janvier 2021***

USB BC ***Battery Charging Specification, Révision 1.2, 15 mars 2012***
(y compris les errata et ECN publiés)

DP AM ***DisplayPort™ Alt Mode on USB Type-C Standard, Version 2.1, octobre 2022***

Tous les documents relatifs à l'USB sont disponibles au téléchargement à l'adresse http://www.usb.org/documents.
La spécification ***DisplayPort Alt Mode*** est disponible sur le site Web de VESA (http://www.vesa.org).

1.4 Conventions

1.4.1 Ordre de priorité

En cas de contradiction entre les textes, les figures et les tableaux, l'ordre suivant ***doit*** prévaloir: tableaux, puis figures, puis textes.

1.4.2 Mots-clés

Les mots-clés suivants permettent de différencier les niveaux d'exigences et d'options.

1.4.2.1 Informatif(ve)

Le mot-clé ***Informatif(ve)*** est utilisé pour décrire les informations de la présente spécification qui visent à traiter et clarifier les exigences et fonctionnalités (et non à les rendre obligatoires).

1.4.2.2 Pouvoir/Peut/Peuvent

Les mots-clés ***Pouvoir/Peut/Peuvent*** sont utilisés pour indiquer un choix sans préférence implicite.

1.4.2.3 Peut ne pas/Peuvent ne pas

Les mots-clés ***Peut ne pas/Peuvent ne pas*** ont une signification inverse à ***Pouvoir/Peut/Peuvent***. Ils indiquent la possibilité de ne pas mettre en œuvre une fonction donnée, sans préférence implicite.

1.4.2.4 N/A

Le mot-clé ***N/A*** est utilisé pour indiquer qu'un champ ou une valeur ne s'applique pas, qu'il n'a pas de valeur définie et qu'il ***ne doit pas*** être vérifié ou utilisé par le destinataire.

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1.4.2.5 Normatif(ve)

Le mot-clé ***Normatif(ve)*** est utilisé pour décrire les fonctionnalités obligatoires de la présente spécification.

1.4.2.6 Facultatif(ve) et De manière facultative

Les mots-clés ***Facultatif(ve)*** et ***De manière facultative*** sont utilisés pour décrire les fonctionnalités non obligatoires de la présente spécification. Toutefois, lorsqu'une fonctionnalité ***facultative*** est mise en œuvre, elle ***doit*** respecter la présente spécification (***normative facultative***).

1.4.2.7 Réservé

Le mot-clé ***Réservé*** est utilisé pour indiquer les valeurs réservées d'un bit, d'un octet, d'un mot, d'un champ ou d'un code, qui sont mises de côté pour une normalisation future. Leur utilisation et leur interprétation peuvent être spécifiées par de futurs compléments à la présente spécification; sauf indication contraire, elles ***ne doivent pas*** être utilisées ou modifiées par la mise en œuvre d'un fournisseur. Un bit, un octet, un mot ou un champ réservé ***doit*** être défini sur zéro par l'émetteur et ***doit*** être ignoré par le destinataire. Les valeurs d'un champ ***Réservé ne doivent pas*** être envoyées par l'envoyeur. S'il les reçoit, le destinataire ***doit*** les ignorer.

1.4.2.8 Devoir/Doit/Doivent

Les mots-clés ***Devoir/Doit/Doivent*** indiquent une exigence obligatoire (***normative***). Les concepteurs sont tenus de mettre en œuvre l'ensemble de ces exigences afin d'assurer l'interopérabilité avec les autres dispositifs conformes.

1.4.2.9 Ne doit pas/Ne doivent pas

Les mots-clés ***Ne doit pas/Ne doivent pas*** ont une signification inverse à ***Devoir/Doit/Doivent***, indiquant une opération non conforme.

1.4.2.10 Il convient de/que

Le mot-clé ***Il convient de/que*** est utilisé pour indiquer la latitude concernant un choix avec alternative préférentielle. Il équivaut à l'expression "Il est recommandé de/que".

1.4.2.11 Il convient de ne pas

Le mot-clé ***Il convient de ne pas*** a une signification inverse à ***Il convient de/que***. Il équivaut à l'expression "Il est recommandé de ne pas...".

1.4.3 Numérotation

Les nombres immédiatement suivis de la lettre "b" en minuscule (01b, par exemple) sont des valeurs binaires. Les nombres immédiatement suivis de la lettre "B" en majuscule sont des valeurs exprimées en octets. Les nombres immédiatement suivis de la lettre "h" en minuscule (3Ah, par exemple) sont des valeurs hexadécimales. Les nombres qui ne sont pas immédiatement suivis des lettres "b", "B" ou "h" sont des valeurs décimales.

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1.5 Termes et abréviations

Terme	Description
Mode accessoire	Reconfiguration du connecteur en fonction de la présence de ***Rd***/***Rd*** respectivement sur le CC1/CC2.

Terme	Description
Câble actif	Les câbles actifs sont des câbles USB Type-C Complets qui intègrent des répéteurs dans le chemin de données ***USB 3.2***. Il est attendu que tous les câbles actifs, quelle que soit leur longueur, respectent la présente spécification, l'Annexe E de la spécification ***USB 3.2*** et le CTS de câble actif ***USB 3.2***. Les câbles actifs ***peuvent*** incorporer des répéteurs sur les deux extrémités du câble, sur une extrémité ou n'importe où dans le câble. Voir l'Article 6.
Mode alternatif	Opération définie par un fournisseur ou un organisme de normalisation, associée à un SVID attribué par ***USB-IF***. L'entrée en ***mode alternatif*** et la sortie de ce mode sont contrôlées par les commandes Enter Mode et Exit Mode des VDM dont la structure est définie par l'***USB PD***. Voir l'Annexe E.
Adaptateur de mode alternatif (AMA, *Alternate Mode Adapter*)	Dispositif ***USB PD*** qui prend en charge les ***modes alternatifs*** et joue le rôle d'UFP.
Mode accessoire d'adaptateur audio	Mode accessoire défini en fonction de la présence de ***Ra***/***Ra*** respectivement sur le CC1/CC2. Ce mode est ***déconseillé*** et remplacé par le ***mode inhibition de corrosion liquide***.
BMC (Biphase Mark Coding)	Codage de marques biphase utilisé pour la communication ***USB PD*** par le biais du fil CC.
Port de câble partenaire	DRP, source ou destinataire USB Type-C connecté à la fiche de câble.
Câble captif	Câble terminé à une extrémité par une fiche USB Type-C et dont l'extrémité opposée est composée d'un moyen de connexion spécifique au fournisseur (câblée ou amovible personnalisée).
CC (canal de configuration)	Canal de configuration (CC) utilisé dans la découverte, la configuration et la gestion des connexions par le biais d'un câble USB Type-C. Voir 4.5.
VPD de charge (***CTVPD***, *Charge-Through VPD*)	Dispositif USB alimenté par VCONN dont la technologie permet de transmettre l'alimentation et la communication CC d'un port vers un autre, sans aucun reparamétrage de réglementation. Voir 4.10.2.
Voie de configuration	La voie de configuration ***USB 3.2*** est utilisée pour établir et gérer le fonctionnement d'USB SuperSpeed à double voie. La voie de configuration est spécifiquement le signal différentiel SuperSpeed USB TX1/RX1 dans le câble/la fiche.
Mode accessoire de débogage (DAM, *Debug Accessory Mode*)	Mode accessoire défini en fonction de la présence de ***Rd***/***Rd*** ou de ***Rp***/***Rp*** respectivement sur le CC1/CC2. Voir l'Annexe B.
Système de débogage et d'essai (DTS, *Debug and Test System*)	Système matériel et logiciel combiné qui fournit à un développeur de système une visibilité et un contrôle sur le débogage, lorsqu'il est connecté à un ***système cible*** en ***mode accessoire de débogage***.
VBUS par défaut	Tension VBUS définie par les spécifications ***USB 2.0*** et ***USB 3.2***. Note: Lorsqu'elle est mentionnée, une tension VBUS de 5 V porte la même signification.

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Terme	Description
DFP (Downstream Facing Port)	Port orienté en aval, spécifiquement associé au flux de données dans une connexion USB. Il s'agit généralement des ports placés sur un hôte ou sur un hub, auxquels les dispositifs sont connectés. Dans un premier temps, le DFP alimente VBUS et VCONN, et prend en charge les données. Un DFP destiné uniquement à la charge n'alimente que VBUS.
Dispositif à connexion directe	Dispositif équipé d'un câble captif ou d'une simple fiche USB Type-C (par exemple, une clé USB).
DRD (Dual-Role Data - données double fonction)	Acronyme utilisé dans la présente spécification pour se référer à un port USB qui peut fonctionner comme DFP (hôte) ou UFP (dispositif). Le rôle joué initialement par le port est déterminé par la fonction d'alimentation du port lors du branchement. Un port source prend le rôle de données d'un DFP et un port destinataire prend le rôle de données d'un UFP. Le rôle de données du port ***peut*** être modifié dynamiquement avec la technique de permutation des rôles de transmission de données (Data Role Swap) de l'***USB PD***.
DRP (Dual-Role Power - alimentation double fonction)	Acronyme utilisé dans la présente spécification pour se référer à un port USB qui peut fonctionner comme source ou destinataire. Le rôle joué par le port ***peut*** être fixe (source ou destinataire) ou ***peut*** alterner entre ces deux états. Lors de son fonctionnement initial en tant que source, le port prend également le rôle de données d'un DFP. Lorsqu'il fonctionne en tant que destinataire, il prend aussi le rôle de données d'un UFP. Le rôle d'alimentation du port ***peut*** être modifié de manière dynamique avec la technique de permutation des rôles d'alimentation (Power Role Swap) de l'***USB PD***.
DR_Swap	Permutation des rôles de transmission de données (Data Role Swap) de l'***USB PD***.
Double voie (x2)	Le fonctionnement à double voie est défini comme la signalisation simultanée sur les deux ensembles de paires différentielles d'émission et de réception USB (TX1/RX1 et TX2/RX2 dans le câble/la fiche).
Câble avec marquage électronique	Câble USB Type-C qui utilise l'***USB PD*** pour fournir les caractéristiques du câble. Voir 4.9.
Marqueur électronique	Élément d'un câble avec marquage électronique qui renvoie des informations sur le câble en réponse à une commande de ***découverte d'identité*** de l'***USB PD***.
Câble actif optique hybride	Câble utilisant une ligne de transmission optique intermédiaire pour le chemin de signalisation à grande vitesse (TX/RX) tout en conservant une solution à conducteur métallique pour le reste des interfaces définies, par exemple CC, ***USB 2.0***, SBU, etc.
Initiateur	Port qui initie un message défini par le fournisseur (VDM, *Vendor Defined Message*). Il ne dépend pas du rôle PD du port (par exemple, fournisseur, consommateur, fournisseur/consommateur ou consommateur/fournisseur). Dans la plupart des cas, l'initiateur est un hôte.
Température interne	En référence à un câble actif, température mesurée à l'intérieur d'une fiche. Il ne s'agit pas de la température externe. Il existe une relation entre la température interne et la température externe de la fiche, mais cette relation dépend de la conception.
Mode inhibition de corrosion liquide	Mode défini en fonction de la présence de ***Ra***/***Ra*** respectivement sur le CC1/CC2. Voir l'Annexe A.
Fiche locale	Fiche de câble associée.

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Terme	Description
Câble actif à isolation optique (OIAC, *Optically Isolated Active Cable*)	Câble qui utilise une ligne de transmission optique intermédiaire pour l'ensemble des signaux. Ce câble ne comporte aucun conducteur métallique et est isolé électriquement entre les deux fiches. Ce câble dispose d'une fiche USB Type-C à chaque extrémité, dont une fiche de câble prend en charge SOP' et l'autre prend en charge SOP".
Câble passif	Câble qui ne comporte aucun composant électronique pour conditionner les signaux de chemin de données. Un câble passif ***peut*** ou ***peut ne pas*** comporter un marquage électronique.
Port partenaire	Se rapporte à un port (dispositif ou hôte) auquel un autre port est branché.
Batterie d'alimentation	Dispositif équipé d'une batterie, dont la fonction principale est de charger ou d'étendre la durée de fonctionnement d'autres dispositifs USB Type-C.
Mode alimentation électrique	Mode dans lequel les ports partenaires sont indiqués dans un contrat d'alimentation ***USB PD*** (Explicite ou Implicite).
Dispositif destinataire d'alimentation (PSD, *Power Sinking Device*)	Destinataire qui puise du courant, mais n'a pas d'autre fonction de communication USB ou ***mode alternatif***; par exemple, un éclairage alimenté par USB.
Câble alimenté	Câble dont la fiche comporte des composants électroniques et qui exige que la tension VCONN soit indiquée par la présence de ***Ra*** entre la broche VCONN et la masse.
PR_Swap	Permutation des rôles d'alimentation ***USB PD***.
Circuit d'amplification	Un circuit d'amplification désigne un composant analogique qui fonctionne sur le signal sans le retemporiser. Il ***peut*** inclure l'égalisation, l'amplification et l'émetteur. Un circuit d'amplification ne comprend pas de circuit de récupération des données d'horloge (CDR, *Clock-Data Recovery*). Les circuits d'amplification ne relèvent pas du domaine d'application du présent document.
Capacité partagée restante	Puissance restante disponible pour un groupe de ports à capacité partagée après l'attribution de la puissance à un ou plusieurs de ses ports.
Fiche distante	Dans le contexte des fiches OIAC, une fiche de câble distante est la fiche située à l'autre extrémité du câble actif à isolation optique.
Répéteur	Un répéteur désigne tout composant actif qui agit sur un signal afin d'augmenter la longueur physique et/ou la perte d'interconnexion sur laquelle le signal peut être transmis avec succès. La catégorie des répéteurs englobe les circuits de retemporisation et les circuits d'amplification.
Répondeur	Port qui répond à l'initiateur d'un message défini par le fournisseur (VDM, *Vendor Defined Message*). Il ne dépend pas du rôle ***USB PD*** du port (par exemple, fournisseur, consommateur, fournisseur/consommateur ou consommateur/fournisseur). Dans la plupart des cas, le répondeur est un dispositif.
Circuit de retemporisation	Un circuit de retemporisation désigne un composant qui contient un circuit de récupération des données d'horloge (CDR) qui "retemporise" le signal. Un circuit de retemporisation verrouille le signal dans un élément de mémoire synchrone avant de le retransmettre. Il est utilisé pour étendre la longueur physique du système sans accumuler de gigue haute fréquence en créant des domaines d'horloge séparés de part et d'autre du circuit de retemporisation. Les circuits de retemporisation sont définis dans l'Annexe E de la spécification ***USB 3.2*** et dans la spécification ***USB4***.

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Terme	Description
SBU (Sideband Use)	Utilisation en bande latérale.
Puissance disponible du port partagé	Puissance disponible, jusqu'à la PDP du port, sur un port non branché d'un groupe de ports à capacité partagée. Cette puissance représente ce qui est disponible pour chaque port du groupe lorsqu'un destinataire est branché en tenant compte de la puissance déjà allouée aux ports où sont connectés les destinataires. Cette puissance est d'au moins 7,5 W, initialement fournie sous la forme d'un courant USB Type-C à 1,5 A.
Câble actif court (SAC, *Short Active Cable*)	Câble avec une fiche USB Type-C à chaque extrémité dont au moins l'une d'entre elles est une fiche de câble qui prend en charge SOP'. Câble jusqu'à 5 m de longueur.
SID (Standard ID)	Un identifiant normalisé est une valeur unique à 16 bits, attribuée par l'***USB-IF*** pour identifier une norme industrielle.
Voie unique (x1)	Le fonctionnement ***USB 3.2*** à voie unique est défini comme la signalisation sur un seul ensemble de paires différentielles d'émission et de réception USB SuperSpeed (TX1/RX1 dans le câble/la fiche).
Destinataire	Port marqué par ***Rd*** sur le CC qui, lorsqu'il est branché, consomme l'alimentation de VBUS. Dans la plupart des cas, il s'agit d'un dispositif.
Température externe	En référence à un câble actif, température du surmoulage d'une fiche.
Source	Port marqué par ***Rp*** sur le CC qui, lorsqu'il est branché, fournit de l'alimentation par VBUS. Dans la plupart des cas, il s'agit d'un hôte ou d'un hub DFP.
SVID	Référence générale à un SID ou à un VID. Utilisé par les VDM structurés ***USB PD*** lors d'une demande de SID et de VID auprès d'un dispositif.
Système cible (TS, *Target System*)	Système en cours de débogage en ***mode accessoire de débogage***.
Capacité totale partagée	Puissance totale disponible pour un groupe de ports à capacité partagée. Il s'agit de la puissance globale disponible lorsqu'aucun des ports du groupe n'est connecté aux destinataires.
Type-A	Référence générale à l'ensemble des versions des fiches et embases USB "A".
Type-B	Référence générale à l'ensemble des versions des fiches et embases USB "B".
Fiche Type-C	Fiche USB conforme aux exigences électriques et mécaniques définies dans la présente spécification.
Port Type-C	Port USB associé à une embase USB Type-C. Cela inclut la signalisation USB, la logique CC, les multiplexeurs et d'autres logiques associées.
Embase Type-C	Embase USB conforme aux exigences électriques et mécaniques définies dans la présente spécification.
UFP (Upstream Facing Port)	Port orienté en amont, spécifiquement associé au flux de données dans une connexion USB. Ce port se trouve sur un dispositif ou un hub et se connecte à un hôte ou au DFP d'un hub. À l'état initial, l'UFP reçoit la tension VBUS et prend en charge les données.
Câble ***USB 2.0*** Type-C	Câble USB Type-C vers Type-C qui prend uniquement en charge l'exploitation des données ***USB 2.0***. Ce câble n'inclut pas les fils ***USB 3.2*** ou SBU.

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Terme	Description
Fiche ***USB 2.0*** Type-C	Fiche USB Type-C spécifiquement conçu pour mettre en œuvre le câble ***USB 2.0*** Type-C.
Câble USB Type-C Complet	Câble USB Type-C vers Type-C qui prend en charge l'exploitation des données ***USB 2.0***, ***USB 3.2*** et ***USB4***. Ce câble comprend les fils SBU et est un câble avec marquage électronique.
Fiche USB Type-C Complète	Fiche USB Type-C, spécifiquement conçu pour mettre en œuvre le câble USB Type-C Complet.
Hub ***USB4***	Un hub ***USB4*** est utilisé pour l'extension de port USB. Il comprend uniquement les ports USB en amont et en aval. Il ne comprend aucune capacité supplémentaire qui expose d'autres types de connecteurs ou d'autres fonctions, à l'exception de celles définies en 5.2.3 (prise en charge des ***modes alternatifs***).
Station d'accueil ***USB4***	Une station d'accueil ***USB4*** associe un hub ***USB4*** (qui comprend au moins un port USB Type-C exposé en aval) avec des capacités supplémentaires qui exposent d'autres types de connecteurs et/ou incluent d'autres fonctions visibles par l'utilisateur comme le stockage, la mise en réseau, etc. Les exemples de fonctions qui ne s'interprètent pas comme visibles par l'utilisateur englobent la mise à jour de microprogramme et l'authentification de dispositif.
État de sécurité USB	État USB Safe State défini par la spécification ***USB PD***.
Accessoire alimenté par ***VCONN*** (***VPA***)	Accessoire alimenté par la tension VCONN pour fonctionner en ***mode alternatif***. Les ***VPA*** ne peuvent pas appliquer la technique de charge décrite pour les ***VPD***. Ils doivent, en lieu et place, négocier le déclenchement de l'***USB Power Delivery*** avec l'hôte connecté et la source afin d'assurer une fonctionnalité similaire. Voir 4.10.1.
Dispositif USB alimenté par VCONN (***VPD***)	Dispositif USB à connexion directe ou à câble captif qui peut être alimenté exclusivement par VCONN ou VBUS. Les ***VPD peuvent***, ***de manière facultative***, prendre en charge la capacité de charge par ***VPD***. Voir 4.10.2.
VCONN_Swap	Permutation de VCONN ***USB PD***
VDM (Vendor Defined Message)	Message défini par le fournisseur, défini par la spécification ***USB PD***.
VID	Un identifiant de fournisseur (Vendor ID) est une valeur unique à 16 bits attribuée par l'***USB-IF*** pour identifier un fournisseur.
vSafe0V	Tension VBUS de "0 V" définie par la spécification ***USB PD***.
vSafe5V	Tension VBUS de "5 V" définie par la spécification ***USB PD***.
x1	Voir Voie unique.
x2	Voir Double voie.

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2 Vue d'ensemble

2.1 Introduction

Les fiches et embases ainsi que le câble USB Type-C® offrent une alternative plus petite, plus fine et plus robuste aux interconnexions USB existantes (câbles et connecteurs Standard et Micro-SB). Cette solution est prévue pour une utilisation sur des plateformes très fines (des ordinateurs portables ultrafins aux mobiles multifonctions), sur lesquelles les embases Standard A et Micro-AB existantes sont jugées trop imposantes, difficilement utilisables ou pas suffisamment robustes.

Les principales améliorations sont les suivantes:

- l'embase USB Type-C peut être utilisée sur des plateformes très fines, compte tenu de la hauteur totale du dispositif après montage, qui est inférieure à 3 mm;
- la fiche USB Type-C est plus facile à utiliser, puisqu'il est enfichable face vers le haut ou face vers le bas;
- le câble USB Type-C est plus facile à utiliser, puisqu'il est enfichable dans le dispositif et l'hôte dans les deux sens.

L'interconnexion USB Type-C ne fait plus la distinction physique entre les connecteurs de type A ou de type B d'un câble, tandis que l'interface USB maintient cette relation logique entre l'hôte et le dispositif. La détermination de cette relation entre hôte et dispositif est réalisée par le biais d'un canal de configuration (CC) connecté par le câble. Le canal de configuration permet également de configurer et de gérer l'alimentation et les modes alternatif et accessoire.

À l'aide du canal de configuration, l'interconnexion USB Type-C définit une solution simplifiée pour la charge et l'alimentation électrique, avec une tension VBUS de 5 V, qui vient compléter la spécification ***USB 3.2***. Les fonctionnalités plus avancées d'alimentation électrique et de charge de batterie au moyen de l'interconnexion USB Type-C reposent sur la spécification ***USB Power Delivery***. Autre amélioration concernant la mise en œuvre du produit, l'interconnexion USB Type-C permet au protocole de communication ***USB PD***, auparavant communiqué par VBUS, d'être distribué sur le canal de configuration USB Type-C.

Il est prévu que la conception même des fiches et embases, ainsi que celle du câble USB Type-C, prennent en charge les futures extensions fonctionnelles USB. À ce titre, une attention particulière a été accordée aux performances de gradation des fréquences, à la disposition des broches et aux mécanismes de configuration lors du développement de cette solution. La définition des futures extensions fonctionnelles USB ne relève pas du domaine d'application de la présente spécification; elle sera fournie dans les futures éditions de la spécification USB de base, c'est-à-dire ultérieures à la spécification ***USB4*** existante.

La Figure 2-1 représente le plan complet des signaux fonctionnels pour l'embase USB Type-C Complète. Tous les signaux représentés ne sont pas exigés sur toutes les plateformes ou tous les dispositifs. Comme cela est indiqué, la liste des signaux de l'embase alimente de manière fonctionnelle les bus de données ***USB 2.0*** (D+ et D−), et ***USB 3.2*** ou ***USB4*** (paires TX et RX), l'alimentation USB (VBUS), la masse (GND), les signaux du canal de configuration (CC1 et CC2) et deux broches de signaux d'utilisation en bande latérale (SBU). Cet agencement, qui comprend plusieurs emplacements pour les signaux de bus de données USB, facilite la capacité à mettre les signaux USB en correspondance de manière fonctionnelle, quelle que soit l'orientation de la fiche dans l'embase. Les broches de signal sont étiquetées à titre de référence. Pour l'embase ***USB 2.0*** Type-C, ni les signaux ***USB 3.2*** ni les signaux ***USB4*** ne sont mis en œuvre.

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Figure 2-1 Interface d'une embase USB Type-C (vue de face)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	VBUS	CC1	D+	D−	SBU1	VBUS	RX2−	RX2+	GND
GND	RX1+	RX1−	VBUS	SBU2	D−	D+	CC2	VBUS	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

La Figure 2-2 représente le plan complet des signaux fonctionnels pour la fiche USB Type-C. Une seule broche CC est connectée par le biais du câble pour établir l'orientation du signal; l'autre broche CC est refonctionnalisée comme VCONN pour alimenter les composants électroniques de la fiche SB Type-C. De plus, un seul ensemble de fils ***USB 2.0*** D+/D− est mis en œuvre dans un câble USB Type-C. Pour les câbles USB Type-C qui prennent uniquement en charge la fonctionnalité ***USB 2.0***, les signaux TX/RX et SBU ne sont pas mis en œuvre. Seuls neuf contacts sont mis en œuvre pour prendre en charge les broches CC, VBUS et GND dans la fiche USB Type-C d'alimentation uniquement (destinée uniquement aux applications de destinataire USB Type-C).

Figure 2-2 Interface d'une fiche USB Type-C Complète (vue de face)

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

2.2 Fiches, embases et câbles USB Type-C

Les câbles et les connecteurs, notamment les câbles et adaptateurs USB Type-C vers USB, sont définis de manière explicite par la présente spécification. Il s'agit des seuls connecteurs et câbles autorisés par les termes de la licence de la présente spécification. Tous les câbles et connecteurs sous licence doivent satisfaire aux exigences de conformité et de certification établies et gérées par l'***USB-IF***.

Les fiches et embases USB Type-C suivantes sont définies:

- embase USB Type-C Complète pour les plateformes et dispositifs ***USB 2.0***, ***USB 3.2*** et ***USB4*** Complets;
- embase ***USB 2.0*** Type-C pour les plateformes et dispositifs ***USB 2.0***;
- fiche USB Type-C Complète;
- fiche ***USB 2.0*** Type-C;
- fiche USB Type-C d'alimentation uniquement.

Les câbles USB Type-C suivants sont définis:

- câble USB Type-C Complet avec fiche USB Type-C Complète à chaque extrémité pour les applications ***USB 3.2***, ***USB4*** Complètes;
- câble ***USB 2.0*** Type-C avec fiche ***USB 2.0*** Type-C aux deux extrémités pour les applications ***USB 2.0***;
- câble captif équipé soit d'une fiche USB Type-C Complète, soit d'une fiche ***USB 2.0*** Type-C à une extrémité;
- câbles actifs définis à l'Article 6.

L'ensemble des fiches, embases et câbles USB Type-C définis (hors OIAC) prennent en charge les applications de charge par USB, y compris la mise en œuvre ***facultative*** spécifique USB Type-C de la spécification ***USB Power Delivery*** (voir 4.6.2.4).

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Tous les câbles USB Type-C Complets ont un marquage électronique. Les câbles ***USB 2.0*** Type-C ***peuvent*** avoir un marquage électronique. Voir 4.9 pour les exigences relatives aux câbles avec marquage électronique.

Les câbles et adaptateurs USB Type-C vers USB suivants sont définis:

- câble ***USB 3.2*** Type-C vers hôte existant avec une fiche USB Type-C Complète à une extrémité et une fiche ***USB 3.1*** Standard-A à l'autre extrémité – ce câble prend en charge l'utilisation d'un dispositif USB Type-C avec un port USB existant;
- câble ***USB 2.0*** Type-C vers hôte existant avec une fiche ***USB 2.0*** Type-C à une extrémité et une fiche ***USB 2.0*** Standard-A à l'autre extrémité – ce câble prend en charge l'utilisation d'un dispositif USB Type-C avec un hôte ***USB 2.0*** existant (notamment pour les applications mobiles de synchronisation et de charge);
- câble ***USB 3.2*** Type-C vers dispositif existant avec une fiche USB Type-C Complète à une extrémité et une fiche ***USB 3.1*** Standard-B à l'autre extrémité – ce câble prend en charge l'utilisation de hubs et dispositifs ***USB 3.1*** existants avec un hôte USB Type-C;
- câble ***USB 2.0*** Type-C vers dispositif existant avec une fiche ***USB 2.0*** Type-C à une extrémité et une fiche ***USB 2.0*** Standard-B à l'autre extrémité – ce câble prend en charge l'utilisation de hubs et dispositifs ***USB 2.0*** existants avec un hôte USB Type-C;
- câble ***USB 2.0*** Type-C vers mini-dispositif existant avec une fiche ***USB 2.0*** Type-C à une extrémité et une fiche ***USB 2.0*** Mini-B à l'autre extrémité – ce câble prend en charge l'utilisation de dispositifs existants avec un hôte ***USB 2.0*** Type-C;
- câble ***USB 3.2*** Type-C vers microdispositif existant avec une fiche USB Type-C Complète à une extrémité et une fiche ***USB 3.1*** Micro-B à l'autre extrémité – ce câble prend en charge l'utilisation de hubs et de dispositifs ***USB 3.1*** existants avec un hôte USB Type C;
- câble ***USB 2.0*** Type-C vers microdispositif existant avec une fiche ***USB 2.0*** Type-C à une extrémité et une fiche ***USB 2.0*** Micro-B à l'autre extrémité – ce câble prend en charge l'utilisation de hubs et de dispositifs ***USB 2.0*** existants avec un hôte USB Type-C;
- adaptateur ***USB 3.2*** Type-C vers connecteur Standard-A existant avec une fiche USB Type-C Complète à une extrémité et une embase ***USB 3.1*** Standard-A à l'autre extrémité – cet adaptateur prend en charge l'utilisation d'un dispositif de type "clés USB" existantes ou d'un dispositif USB ThinCard existant avec un hôte ***USB 3.2*** Type-C;
- adaptateur ***USB 2.0*** Type-C vers connecteur Micro-B existant avec une fiche ***USB 2.0*** Type-C à une extrémité et une embase ***USB 2.0*** Micro-B à l'autre extrémité – cet adaptateur prend en charge la charge d'un dispositif mobile USB Type-C avec des chargeurs existants USB Micro-B, avec un câble captif ou conjointement avec un câble ***USB 2.0*** Standard-A vers Micro-B existant.

Les adaptateurs pour embases USB Type-C vers des connecteurs USB existants ne sont explicitement ni définis ni admis. Ces adaptateurs permettent de nombreux câblages non valides et potentiellement dangereux par les utilisateurs.

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2.3 Processus de configuration

Les solutions de fiches, embases et câbles USB Type-C intègrent un processus de configuration qui permet de détecter une connexion entre un port orienté en aval et un port orienté en amont (source-destinataire), dans le cadre de la gestion de la tension VBUS et la détermination des relations entre l'hôte et le dispositif connecté.

Le processus de configuration de port USB Type-C permet de réaliser les tâches suivantes:

- détection des branchements/débranchements entre la source et le destinataire;
- détection de l'orientation de la fiche ou des câbles torsadés;
- détection de l'alimentation initiale (source-destinataire) et établissement de la relation avec les données (hôte-dispositif);

- détection de l'exigence relative à la VCONN;
- détection et utilisation du courant VBUS USB Type-C;
- communication ***USB PD***; et
- découverte et configuration des extensions fonctionnelles.

À ce titre, deux broches sont utilisées sur l'embase USB Type-C: CC1 et CC2. Dans un câble USB Type-C normalisé, une seule position de broche CC pour chaque connecteur du câble est connectée par le biais du câble.

2.3.1 Détection des branchements/débranchements entre la source et le destinataire

Initialement, la liaison source-destinataire est détectée par un port hôte ou hub (source) lorsque l'une des broches CC de son embase USB Type-C détecte une résistance spécifiée à la GND. Par la suite, la fin de liaison source-destinataire est détectée lorsque la broche CC qui a été branchée à son embase USB Type-C n'est plus reliée à la GND.

L'alimentation n'est pas appliquée à l'embase hôte ou hub USB Type-C (VBUS ou VCONN), tant que la source ne détecte pas la présence d'un port de dispositif (destinataire) branché. Lorsqu'un branchement source-destinataire est détecté, il est prévu que la source alimente l'embase et poursuive son fonctionnement USB normal avec le dispositif branché. Lorsqu'une fin de liaison source-destinataire est détectée, le port qui fournit la tension VBUS coupe l'alimentation.

2.3.2 Détection de l'orientation de la fiche ou des câbles torsadés

La fiche USB Type-C peut être insérée dans une embase dans les deux sens. De fait, les broches CC permettent la détection de l'orientation de la fiche afin de déterminer l'ordre des voies des paires de signaux de données USB TX/RX qui sont connectées de manière fonctionnelle par le câble, et identifient la voie de configuration en fonctionnement à double voie, lorsque celui-ci est pris en charge. Ceci permet d'établir, si nécessaire, le routage des signaux au sein d'un hôte ou d'un dispositif pour assurer la connexion.

2.3.3 Détection de l'alimentation initiale (source-destinataire) et établissement de la relation avec les données (hôte-dispositif)

Contrairement aux fiches et embases USB Type-A et USB Type-B existants, les caractéristiques mécaniques des fiches et embases USB Type-C n'établissent pas en elles-mêmes la relation entre les hôtes USB et les ports de dispositifs. Les broches CC sur l'embase servent également à établir des relations d'alimentation initiale (source-destinataire) et de données (hôte-dispositif) avant le processus d'énumération USB normal.

Dans le but de définir la manière dont les broches CC sont utilisées pour établir la relation d'alimentation initiale, les modes de comportement suivants sont définis pour l'alimentation du port:

1. source uniquement – dans ce mode, le port se comporte exclusivement comme une source;
2. destinataire uniquement – dans ce mode, le port se comporte exclusivement comme un destinataire;
3. alimentation double fonction (DRP) – dans ce mode, le port peut se comporter comme une source ou comme un destinataire.

Par ailleurs, lorsqu'un port prend en charge l'exploitation des données USB, les modes de comportement suivants des données d'un port sont définis:

1. DFP uniquement – dans ce mode, le port se comporte exclusivement comme un DFP;
2. UFP uniquement – dans ce mode, le port se comporte exclusivement comme un UFP;
3. données double fonction (DRD) – dans ce mode, le port peut se comporter comme un DFP ou comme un UFP.

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Le comportement des ports DFP uniquement et UFP uniquement est mis en correspondance avec les comportements types des ports respectivement USB hôte et dispositif, mais ***peuvent ne pas*** nécessairement établir une communication avec les données USB. Lorsque le port d'un hôte est branché à un port de dispositif, le comportement du point de vue de l'utilisateur suit le modèle classique de l'hôte USB vers le port du dispositif. Toutefois, la technique du connecteur USB Type-C n'empêche pas les connexions physiques entre hôtes ou entre dispositifs. Dans ce cas, la connexion entre hôtes ou entre dispositifs établie est certes sécurisée, mais n'est pas fonctionnelle.

Lors de la connexion initiale, la source alimente en tension BUS et se comporte comme un DFP, tandis que le destinataire consomme de la tension BUS et se comporte comme un UFP. Lorsqu'elle est prise en charge par les deux ports, l'***USB PD peut*** ensuite être utilisée pour permuter les rôles d'alimentation et de données des ports de manière indépendante.

Un port est une DRP lorsqu'il prend en charge une double fonction, c'est-à-dire lorsqu'il peut basculer vers le mode de connexion approprié selon qu'il est branché à un port Source uniquement ou Destinataire uniquement. Dans le cas particulier d'une DRP branchée à une autre DRP, un protocole d'initialisation des broches CC permet d'établir la relation initiale entre l'hôte et le dispositif. Sans l'intervention de la permutation de rôles, la détermination du DFP ou de l'UFP est aléatoire du point de vue de l'utilisateur.

Deux ensembles indépendants de mécanismes sont définis pour permettre à une DRP USB Type-C d'effectuer une permutation fonctionnelle des rôles entre l'alimentation et les données. Lorsque l'***USB PD*** est prise en charge, la permutation entre le rôle d'alimentation et le rôle de données est réalisée après le processus de connexion initiale. Pour les mises en œuvre ne prenant pas en charge PD, la permutation des rôles alimentation/données peut, ***de manière facultative***, être traitée dans le cadre du processus de connexion initiale. Dans le but d'améliorer l'expérience utilisateur lors de la connexion de dispositifs de types différents, des matériels ***peuvent*** être développés avec intégration d'un rôle préférentiel DFP ou UFP, de sorte que la détermination du DFP/UFP soit prévisible dès la connexion. Pour plus d'informations sur les mécanismes de permutation disponibles, voir 4.5.1.4.

Outre la permutation de rôles, une DRP USB Type-C ***peut*** également proposer une fonctionnalité utile: exposer une pile CDC/réseau (de préférence TCP/IP) lorsqu'il fonctionne en tant qu'hôte, ou exposer une interface CDC/réseau lorsqu'il fonctionne en tant que dispositif.

Les hubs USB possèdent deux types de ports: un UFP connecté à un DFP (hôte ou autre hub) qui fonctionne initialement comme un destinataire, ainsi qu'un ou plusieurs DFP pour la connexion d'autres dispositifs qui fonctionnent initialement en tant que sources.

2.3.4 Détection et utilisation du courant VBUS USB Type-C

Avec la technique du connecteur USB Type-C, une source (port hôte ou hub en aval) ***peut*** appliquer un courant source plus élevé sur la VBUS afin de charger plus rapidement les dispositifs mobiles ou les dispositifs de puissance supérieure. Tous les ports USB hôte et hub annoncent, par le biais des broches CC, le niveau de courant actuellement disponible. Le port du dispositif USB doit gérer sa charge pour s'aligner sur l'intensité de courant fournie par l'hôte ou le hub. Il doit notamment réduire dynamiquement la charge si le port hôte ou hub annonce un niveau plus faible par le biais des broches CC.

Trois annonces d'intensité de courant à une tension VBUS de 5 V sont définies par le ***courant USB Type-C***:

- le ***courant USB Type-C*** à la valeur par défaut correspond à la valeur configurée pour une valeur de courant de fonctionnement sous tension élevée et définie par une spécification USB (500 mA pour les ports ***USB 2.0***; 900 mA/1 500 mA pour les ports ***USB 3.2*** respectivement à voie unique/double voie);
- le ***courant USB Type-C*** de 1,5 A; et
- le ***courant USB Type-C*** de 3,0 A.

Il existe une distinction fonctionnelle évidente entre l'annonce du ***courant USB Type-C*** à la valeur par défaut et le ***courant USB Type-C*** de 1,5 A ou 3,0 A.

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- Le ***courant USB Type-C*** à la valeur par défaut est prévu pour que l'hôte fonctionne et fournisse l'alimentation du bus à un dispositif connecté, où l'hôte gère la consommation de courant du dispositif pour les états de faible puissance, de haute puissance et de veille définis dans les spécifications USB de base.
- Le ***courant USB Type-C*** de 1,5 A ou 3,0 A est essentiellement destiné aux applications de charge. Le destinataire peut varier son appel de courant jusqu'à la limite annoncée. Il est admis de fournir un ***courant USB Type-C*** de 1,5 A ou 3,0 A dans le cas d'un hôte qui fournit l'alimentation du bus à un dispositif. Il est nécessaire que l'hôte prenne pour hypothèse que le dispositif puise continuellement le courant à la limite proposée.

Les intensités supérieures de ***courant USB Type-C*** qui peuvent être déclarées permettent aux hôtes et aux dispositifs qui ne mettent pas en œuvre l'***USB PD*** d'utiliser un courant de charge supérieur.

2.3.5 Communications *USB PD*

USB Power Delivery est une fonctionnalité intégrée aux matériels (hôtes, hubs et dispositifs). Les communications ***USB PD*** sont utilisées pour:

- établir des contrats d'alimentation qui permettent de fournir des valeurs de tension et de courant supérieures aux spécifications de bus de données USB existantes;
- modifier le port qui alimente la tension VBUS;
- modifier le port qui alimente la tension VCONN;
- permuter les rôles DFP et UFP; et
- communiquer par l'intermédiaire de câbles.

Les communications BMC ***USB PD*** sont établies sur le fil CC du câble USB Type-C.

2.3.6 Extensions fonctionnelles

Les extensions fonctionnelles, y compris l'***USB4*** et les ***modes alternatifs*** (voir l'Annexe E) sont établies par le biais d'un canal de communications sur le CC, selon les méthodes définies dans la spécification ***USB Power Delivery***.

2.4 VBUS

VBUS fournit un chemin qui permet de déclencher l'alimentation entre un hôte et un dispositif, ou entre un chargeur USB et un hôte/dispositif. Une capacité d'alimentation simplifiée sous tension élevée est définie pour les hôtes et les chargeurs qui prennent en charge, ***de manière facultative***, des intensités de courant supérieures aux spécifications ***USB 2.0***, ***USB 3.2*** et ***USB4***. La spécification ***USB Power Delivery*** est prise en charge.

Le Tableau 2-1 récapitule les options d'alimentation disponibles depuis le dispositif équipé du connecteur USB Type-C. Tous les ports hôte ou hub ne permettent pas au dispositif d'accéder à toutes les options. Seules les deux premières options répertoriées correspondent aux obligations des spécifications USB de base et constituent le fondement du ***courant USB Type-C*** au niveau de puissance USB par défaut.

Tableau 2-1 Récapitulatif des options d'alimentation

Mode de fonctionnement	Tension	Courant	Notes
USB 2.0	5 V	Voir ***USB 2.0***	
USB 3.2	5 V	Voir ***USB 3.2***	
USB4	5 V	1,5 A	Voir 5.3.
USB BC 1.2	5 V	1,5 A[1]	Charge existante

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Courant USB Type-C de 1,5 A	5 V	1,5 A	Prend en charge les dispositifs d'alimentation supérieure
Courant USB Type-C de 3,0 A	5 V	3 A	Prend en charge les dispositifs d'alimentation supérieure
USB PD	Paramétrable jusqu'à 48 V	Paramétrable jusqu'à 5 A	Commande directionnelle et gestion du niveau d'alimentation
Note 1: Lorsque la spécification ***USB BC 1.2*** permet de concevoir un fournisseur d'alimentation qui prend en charge un niveau d'alimentation compris entre 0,5 A et 1,5 A, la spécification USB Type-C exige qu'un port source prenant en charge l'***USB BC 1.2*** soit capable de fournir un courant d'au moins 1,5 A et d'annoncer un ***courant USB Type-C*** de 1,5 A en plus de prendre en charge la terminaison du fournisseur d'alimentation ***USB BC 1.2***.			

L'embase USB Type-C est spécifiée pour une capacité électrique de 5 A, alors que le courant assigné des ensembles câble-connecteurs USB Type-C normalisés est de 3 A. Une valeur assignée plus élevée pour l'embase permet aux systèmes de fournir davantage d'alimentation, par le biais de solutions d'accueil directement branchées, ou avec des chargeurs adaptés avec des câbles captifs lors de la mise en œuvre de l'***USB PD***. Par ailleurs, il est admis que les ensembles câble-connecteurs USB Type-C conçus pour l'***USB PD*** et dûment identifiés par un marquage électronique, prennent en charge jusqu'à 5 A.

Les ensembles câble-connecteurs USB Type-C conçus pour le fonctionnement ***USB PD*** Extended Power Range (EPR) doivent porter un marquage électronique indiquant la compatibilité EPR. Ces câbles doivent comporter un marquage électronique pour 5 A et 50 V et inclure le bit de conformité au mode EPR.

2.5 VCONN

Après avoir établi la connexion entre l'hôte et le dispositif, la broche CC (CC1 ou CC2) de l'embase qui n'est pas connectée par le fil CC au sein du câble normalisé est refonctionnalisée pour alimenter VCONN et donc les circuits de la fiche nécessaires à la mise en œuvre des câbles avec marquage électronique (voir 4.9), des ***accessoires alimentés par VCONN*** et des ***dispositifs USB alimentés par VCONN***. À l'origine, la source alimente VCONN et la source de VCONN ***peut*** être permutée au moyen du mécanisme ***VCONN_Swap*** de l'***USB PD***.

Dès que VCONN est disponible, tous les câbles avec marquage électronique l'utilisent comme seule source d'alimentation. Si VCONN est appliqué après VBUS, tant que VCONN n'est pas disponible, le câble ***peut*** rester non alimenté ou ***peut*** puiser la puissance dans VBUS.

Sur le plan fonctionnel, VCONN diffère de VBUS dans le sens où il est isolé de l'autre extrémité du câble. VCONN est indépendant de VBUS et, contrairement à VBUS qui peut utiliser l'***USB PD*** pour prendre en charge des tensions plus élevées, la tension VCONN reste dans la plage comprise entre 3,0 V et 5,5 V.

2.6 Hubs

Les hubs USB mis en œuvre avec des embases USB Type-C doivent identifier clairement le port orienté en amont. Cette exigence est nécessaire, car un utilisateur ne peut plus savoir quel port d'un hub est orienté en amont et quels ports sont orientés en aval en fonction du type des embases visibles. En d'autres termes, USB Type-B est le port orienté en amont et USB Type-A est un port orienté en aval.

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3 Mécanique

3.1 Vue d'ensemble

Le présent article définit les connecteurs et les ensembles filaires câble-connecteurs USB Type-C. Les câbles qui incluent les éléments actifs dans le chemin de données sont définis à l'Article 6 (Câbles actifs).

3.1.1 Connecteurs conformes

La spécification USB Type-C définit les connecteurs normalisés suivants:

- embase USB Type-C Complète;
- embase ***USB 2.0*** Type-C;
- fiche USB Type-C Complète;
- fiche ***USB 2.0*** Type-C; et
- fiche USB Type-C d'alimentation uniquement.

3.1.2 Ensembles câble-connecteurs conformes

Le Tableau 3-1 récapitule les ensembles câble-connecteurs USB Type-C normalisés, ainsi que les principales caractéristiques distinctives. Tous les câbles USB Type-C Complets ***doivent*** prendre en charge l'émission de signaux indépendante et simultanée sur les deux bus de données ***USB 3.2*** et ***USB4*** (paires TX et RX). Les longueurs de câble répertoriées dans le tableau sont ***données à titre informatif*** et représentent les longueurs fonctionnelles, en se fondant sur les exigences de performance des câbles. Pour l'***USB Power Delivery***, chaque ensemble câble-connecteurs est identifié comme étant uniquement utilisable pour le fonctionnement ***USB PD*** Standard Power Range (SPR) ou pour ***USB PD*** SPR et ***USB PD*** Extended Power Range (EPR). Les câbles ***USB PD*** SPR 5 A existants ont été déconseillés et remplacés par des câbles ***USB PD*** EPR. Tous les câbles, qu'ils soient complets et/ou assignés à un courant supérieur à 3 A, sont des câbles avec marquage électronique.

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Tableau 3-1 Ensembles câble-connecteurs USB Type-C normalisés

Réf. du câble	Fiche 1	Fiche 2	Version USB	Longueur du câble[2]	Courant assigné	USB Power Delivery	Câble USB Type-C avec marquage électronique
CC2-3	C	C	***USB 2.0***	≤ 4 m	3 A	Pris en charge (SPR uniquement)	***Facultatif***
CC2-5[1]					5 A		***Exigé***
CC2-5E					5 A	Pris en charge (SPR et EPR)	***Exigé***
CC3G1-3	C	C	***USB 3.2*** Gen1 et ***USB4*** Gen2	≤ 2 m	3 A	Pris en charge (SPR uniquement)	***Exigé***
CC3G1-5[1]					5 A		
CC3G1-5E					5 A	Pris en charge (SPR et EPR)	***Exigé***
CC3G2-3	C	C	***USB 3.2*** Gen2 et ***USB4*** Gen2	≤ 1 m	3 A	Pris en charge (SPR uniquement)	***Exigé***
CC3G2-5[1]					5 A		
CC3G2-5E					5 A	Pris en charge (SPR et EPR)	***Exigé***
CC4G3-3	C	C	***USB4*** Gen3 et ***USB4*** Gen4[3]	≤ 0,8 m	3 A	Pris en charge (SPR uniquement)	***Exigé***
CC4G3-5[1]					5 A		
CC4G3-5E					5 A	Pris en charge (SPR et EPR)	***Exigé***

Notes:
1. Ces câbles sont déconseillés. Il est préférentiel que tous les câbles 5 A soient des versions compatibles avec EPR.
2. Les longueurs de câble répertoriées dans le tableau sont données à titre ***informatif*** et représentent les longueurs fonctionnelles, en se fondant sur les exigences de performance des câbles.
3. Les câbles passifs ***USB4*** Gen4 sont équivalents du point de vue électrique aux câbles passifs ***USB4*** Gen3. En ce qui concerne les câbles actifs ***USB4*** Gen4, voir l'Article 6 pour les exigences électriques relatives aux câbles ***USB4*** Gen3 et Gen4.

Les produits USB Type-C peuvent disposer d'un câble captif. Voir 3.4.3.

3.1.3 Ensembles câble-connecteurs USB Type-C vers existant conformes

Le Tableau 3-2 récapitule les ensembles câble-connecteurs USB Type-C existants, ainsi que les principales caractéristiques distinctives. Les longueurs de câble répertoriées dans le tableau sont ***données à titre informatif*** et représentent les longueurs fonctionnelles, en se fondant sur les exigences de performance des câbles. Tous les ensembles câble-connecteurs USB Type-C vers existant sont uniquement et spécifiquement définis pour l'***USB 2.0*** et l'***USB 3.2***, car il n'y a pas de câble USB Type-C vers existant qui s'applique exclusivement à l'***USB4***.

Pour les ensembles câble-connecteurs USB Type-C existants qui intègrent la terminaison ***Rp***, la valeur de cette terminaison doit être spécifiée au réglage par défaut du ***courant USB Type-C***, y compris lorsque les ensembles câble-connecteurs ont une valeur assignée de 3 A. Il est prévu que la terminaison ***Rp*** de ces câbles représente le courant maximal d'un port hôte USB existant conforme, et non le courant assigné du câble en lui-même. Dans la mesure où de nombreux chargeurs non normalisés ne se limitent pas aux niveaux par défaut établis par les spécifications ***USB 2.0*** et ***USB 3.1***, le courant assigné du câble est intentionnellement réglé sur un niveau plus élevé.

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Tableau 3-2 Ensembles câble-connecteurs USB Type-C existants

Réf. du câble	Fiche 1[3]	Fiche 2[3]	Version USB	Longueur du câble[2]	Courant assigné
AC2-3	***USB 2.0*** Standard-A	Câble ***USB 2.0*** Type-C[1]	***USB 2.0***	≤ 4 m	3 A
AC3G1-3	***USB 3.1*** Standard-A	Câble USB Type-C[1] Complet	***USB 3.1*** Gen1	≤ 2 m	3 A
AC3G2-3	***USB 3.1*** Standard-A	Câble USB Type-C[1] Complet	***USB 3.1*** Gen2	≤ 1 m	3 A
CB2-3	Câble ***USB 2.0*** Type-C[2]	***USB 2.0*** Standard-B	***USB 2.0***	≤ 4 m	3 A
CB3G2-3	Câble USB Type-C[2] Complet	***USB 3.1*** Standard-B	***USB 3.1*** Gen2	≤ 1 m	3 A
CmB2	Câble ***USB 2.0*** Type-C[2]	***USB 2.0*** Mini-B	***USB 2.0***	≤ 4 m	500 mA
CμB2-3	Câble ***USB 2.0*** Type-C[2]	***USB 2.0*** Micro-B	***USB 2.0***	≤ 2 m	3 A
CμB3G1-3	Câble USB Type-C[2] Complet	***USB 3.1*** Micro-B	***USB 3.1*** Gen1	≤ 2 m	3 A
CμB3G2-3	Câble USB Type-C[2] Complet	***USB 3.1*** Micro-B	***USB 3.1*** Gen2	≤ 1 m	3 A

Notes:

1. Les fiches USB Type-C associées à l'extrémité "B" d'un câble d'adaptateur existant doivent intégrer une terminaison ***Rp*** (56 kΩ ± 5 %) dans l'ensemble de fiches (voir 4.5.3.2.2).
2. Les fiches USB Type-C associées à l'extrémité "A" d'un câble d'adaptateur existant doivent intégrer une terminaison ***Rd*** (5,1 kΩ ± 20 %) dans l'ensemble de fiches (voir 4.5.3.2.1).
3. Pour plus d'informations sur la résistance après branchement et l'échauffement exigés pour les fiches existantes, voir 3.7.5.3.

3.1.4 Ensembles adaptateurs USB Type-C vers existant conformes

Le Tableau 3-3 récapitule les ensembles adaptateurs USB Type-C existants, ainsi que les principales caractéristiques distinctives. Les longueurs de câble répertoriées dans le tableau sont ***données à titre informatif*** et représentent les longueurs fonctionnelles, en se fondant sur les exigences de performance des câbles. Tous les ensembles adaptateurs USB Type-C vers existant sont uniquement et spécifiquement définis pour l'***USB 2.0*** et l'***USB 3.2***, car il n'existe pas d'adaptateur USB Type-C vers existant qui s'applique exclusivement à l'***USB4***.

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Tableau 3-3 Ensembles adaptateurs USB Type-C existants

Réf. du câble	Fiche	Embase[3]	Version USB	Longueur du câble	Courant assigné
CμBR2-3	Câble ***USB 2.0*** Type-C[1]	***USB 2.0*** Micro-B	***USB 2.0***	≤ 0,15 m	3 A
CAR3G1-3	Câble USB Type-C[2] Complet	***USB 3.1*** Standard-A	***USB 3.1*** Gen1	≤ 0,15 m	3 A

Notes:

1. Les fiches USB Type-C associées à l'extrémité "B" d'un adaptateur existant doivent intégrer une terminaison ***Rp*** (56 kΩ ± 5 %) dans l'ensemble de fiches (voir 4.5.3.2.2).
2. Les fiches USB Type-C associées à l'extrémité "A" d'un adaptateur existant doivent intégrer une terminaison ***Rd*** (5,1 kΩ ± 20 %) dans l'ensemble de fiches (voir 4.5.3.2.1).
3. Pour plus d'informations sur la résistance après branchement et l'échauffement exigés pour les embases existantes, voir 3.7.5.3.

3.2 Interfaces de couplage des connecteurs USB Type-C

Le présent paragraphe définit les interfaces de couplage des connecteurs, notamment les dessins d'interface des connecteurs, l'affectation des broches et leurs descriptions. Toutes les dimensions mentionnées dans les figures sont données en millimètres.

3.2.1 Définition de l'interface

La Figure 3-1 et la Figure 3-3 représentent respectivement les dimensions d'interface d'une embase USB Type-C et d'une fiche USB Type-C Complète.

La
Figure 3-11 représente les dimensions d'interface d'une fiche ***USB 2.0*** Type-C. Les dimensions qui régissent l'interopérabilité du couplage sont spécifiées. Toutes les dimensions référencées sont fournies à titre indicatif uniquement et ne constituent pas des exigences strictes.

Les principales fonctionnalités, options de configuration et domaines de conception qu'il est nécessaire de prendre en compte sont les suivants:

1. La Figure 3-1 représente une embase montée à la verticale. D'autres types de montages de CCI (carte de circuit imprimé), comme le montage à angle droit et le montage central, sont admis.
2. Une plaque médiane est exigée à l'intérieur de la languette de l'embase, entre les signaux supérieur et inférieur, afin de gérer la diaphonie dans les applications complètes. La plaque médiane ***doit*** être reliée à la masse de la CCI en au moins deux points de mise à la masse. La plaque médiane ***doit*** être conçue de sorte que les broches de la fiche A4, A5, A6, A7, A8, A9 et B4, B5, B6, B7, B8, B9 ne court-circuitent pas à la masse pendant le processus de couplage du connecteur avec une mise en œuvre d'enveloppe de l'embase de 6,2 mm. Si l'embase comporte une enveloppe courte ou ne comporte pas d'enveloppe, le fabricant du connecteur ***doit*** fournir un montage d'enveloppe de longueur effective pour les essais de conformité. Le 3.2.2.1 fournit un schéma de référence de la plaque médiane.
3. Le maintien de l'ensemble câble-connecteurs au sein de l'embase est assuré par un verrou latéral dans la fiche installé sur les côtés de la languette de l'embase. Ce verrou latéral est exigé pour l'ensemble des fiches, à l'exception des fiches sans fil utilisées pour les stations d'accueil. Il ***doit*** être relié à la masse à l'intérieur de la fiche. Un schéma de référence pour le verrou latéral est fourni au 3.2.2.2, avec son diagramme de mise à la masse. Les applications d'accueil ***peuvent ne pas*** comporter de verrou latéral et nécessitent une attention particulière à la compatibilité électromagnétique (CEM).
4. Des ressorts d'écrantage CEM sont exigés à l'intérieur de la fiche de câble. Les ressorts d'écrantage ***doivent*** être connectés à l'enveloppe de la fiche. La pointe du ressort d'écrantage CEM de la fiche USB Type-C Complète, ou de la fiche ***USB 2.0*** Type-C, ***ne doit pas*** être visible par l'ouverture du boîtier de la fiche USB Type-C non couplée (voir la Figure 3-12). Le 3.2.2.3 contient des schémas de référence du ressort CEM.

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5. Il n'est pas admis de court-circuiter le ressort de signal ou d'alimentation par contact sur l'enveloppe métallique de la fiche. ***Il convient que*** le ressort, lorsqu'il est fléchi, ne soit ***pas*** en contact avec l'enveloppe de la fiche. Il est recommandé d'utiliser une couche d'isolation (par exemple, ruban en Kapton apposé sur l'enveloppe du connecteur) pour empêcher tout court-circuit accidentel dû à la déformation de l'enveloppe du connecteur.
6. L'embase USB Type-C ***doit*** fournir un chemin de retour à la masse CEM par le biais de l'une des options suivantes:
    - un système de points de contact spécifiques sur l'enveloppe externe de l'embase (par exemple, doigts de ressort ou doigts de ressort et saillies);
    - des plaques CEM internes; ou
    - une combinaison de points de contact sur l'enveloppe externe de l'embase et de plaques CEM internes.

    Si des points de contact sont utilisés sur l'embase, ils ***doivent*** être en contact avec la fiche couplée à l'intérieur des zones de contact définies à la Figure 3-2. Au moins quatre points de contact distincts sont exigés. Des points de contact supplémentaires sont admis. Pour accéder au schéma de référence de l'enveloppe externe de l'embase, voir 3.2.2.4. Le schéma de référence inclut quatre doigts de ressort utilisés comme points de contact. Les autres configurations ***peuvent*** inclure des doigts de ressort côté contact A et des saillies (par exemple, des encoches) côté contact B, ou inversement. Des doigts de ressort sont exigés sur un côté au moins, afin que l'enveloppe de la fiche soit ajustée par pression sur le côté opposé. Des saillies supplémentaires ***peuvent*** être utilisées; toutefois, si elles se trouvent sur des faces opposées de l'enveloppe de l'embase, la distance minimale entre les saillies ***doit*** être supérieure aux dimensions maximales définies pour l'enveloppe de la fiche.

    Si des plaques CEM internes sont présentes dans l'embase, elles ***doivent*** satisfaire aux exigences définies à la Figure 3-1. Les plaques d'écrantage ***doivent*** être connectées à l'enveloppe de l'embase. En l'absence d'enveloppe de l'embase, celui-ci ***doit*** comporter un moyen de relier la plaque d'écrantage à la masse. Pour accéder au schéma de référence de la plaque d'écrantage et de la connexion à la masse, voir 3.2.2.3.
7. La présente spécification établit la longueur de l'enveloppe de l'embase USB Type C à 6,20 mm, à titre de dimension de référence. L'embase USB Type-C, dont la longueur d'enveloppe est de 6,20 mm ± 0,20 mm, est conçue pour assurer un couplage mécanique et électrique correct de la fiche à l'embase (par exemple, fiche correctement encastrée dans l'embase, languette de l'embase protégée lors de l'insertion/du retrait). Au niveau du système, ***il convient*** d'intégrer l'embase USB Type-C de sorte que la longueur effective de son enveloppe intégrée à la machine physique soit de 6,20 mm ± 0,20 mm.
8. L'interface de couplage du connecteur USB Type-C est définie de sorte que la connexion électrique ***puisse*** être établie sans l'enveloppe de l'embase. Pour éviter un mauvais alignement de la fiche lors de son insertion dans ou de son retrait de l'embase, ***il convient que*** le boîtier soit équipé d'outils pour guider la fiche lors de son insertion et de son retrait, en présence d'une enveloppe d'embase modifiée. Si la dimension spécifiée pour l'enveloppe de l'embase USB Type-C a été modifiée, la dimension recommandée pour l'entrée de la languette de l'embase au point d'entrée de la fiche est alors de 1,5 mm au minimum lors du montage dans le système.

    La présente spécification admet les configurations d'embase comprenant une enveloppe conductrice, une enveloppe non conductrice ou aucune enveloppe. Les exigences suivantes s'appliquent aux dimensions de contact de l'embase représentées en COUPE A-A et en COUPE ALTERNATIVE A-A à la Figure 3-1:

    - Si l'enveloppe de l'embase est conductrice, les dimensions de contact de l'embase représentées en COUPE A-A ou en COUPE ALTERNATIVE A-A à la Figure 3-1 ***doivent*** être utilisées.

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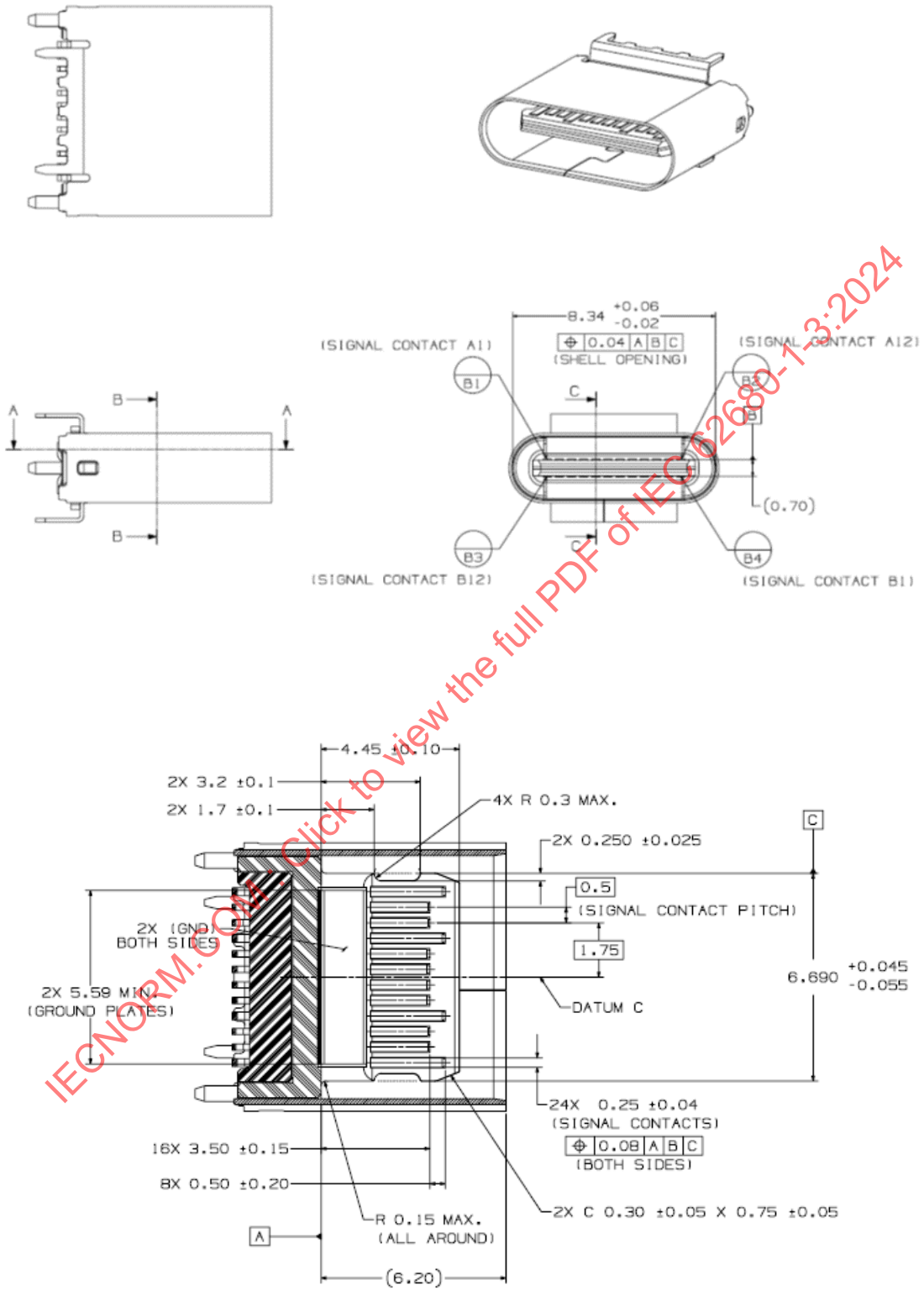
- Si l'enveloppe de l'embase n'est pas conductrice, les dimensions de contact de l'embase représentées en COUPE ALTERNATIVE A-A à la Figure 3-1 ***doivent*** être utilisées. Les dimensions de contact représentées en COUPE A-A ne sont pas admises.
- Si l'embase ne comporte aucune enveloppe, les dimensions de contact de l'embase représentées en COUPE A-A ou en COUPE ALTERNATIVE A-A à la Figure 3-1 ***doivent*** être utilisées. Si l'embase ne comporte aucune enveloppe et qu'elle est utilisée dans une mise en œuvre qui ne fournit pas d'enveloppe conductrice, ***il convient*** alors d'utiliser une embase dont les dimensions de contact sont représentées en COUPE ALTERNATIVE A-A à la Figure 3-1.

Note: Si le produit qui intègre une embase USB Type-C prend en charge le fonctionnement ***USB PD*** Extended Power Range (EPR), ***il convient*** de choisir minutieusement les dimensions de contact de la COUPE A-A par rapport à la COUPE ALTERNATIVE A-A. Les sources et destinataires compatibles ***USB PD*** EPR doivent être conçus pour résister à un éventuel arc électrique lorsqu'ils sont débranchés lorsque la puissance est fournie sur le connecteur, et une différence de longueur plus importante entre les broches CC et VBUS ***peut*** s'avérer avantageuse lors de la mise en œuvre des circuits de détection destinés à faciliter l'atténuation des dommages dus à un éventuel arc. Pour plus d'informations, voir H.3.2.

9. Une carte d'accès (une CCI, par exemple) ***peut*** être utilisée dans la fiche USB Type-C pour gérer les terminaisons de fils et les performances électriques. Le 3.2.2.5 fournit les lignes directrices et un exemple de schéma d'une carte d'accès.
10. La présence spécification ne définit pas les empreintes normalisées. La Figure 3-4 représente un exemple d'empreinte de montage en surface (SMT, *Surface Mount*) pour l'embase verticale représentée à la Figure 3-1. Des empreintes de référence supplémentaires et des configurations de montage sont représentées à la Figure 3-5, la Figure 3-6, la Figure 3-7, la Figure 3-8, la Figure 3-9 et la Figure 3-10.
11. L'enveloppe de l'embase ***doit*** être reliée au plan de masse de la CCI.
12. Toutes les broches VBUS ***doivent*** être connectées ensemble dans la fiche USB Type-C.
13. Toutes les broches de retour à la masse ***doivent*** être connectées ensemble dans la fiche USB Type-C.
14. Toutes les broches VBUS ***doivent*** être connectées ensemble au niveau de l'embase USB Type-C lorsqu'elle est à l'état monté (par exemple, toutes les broches VBUS connectées en bus ensemble dans la CCI).
15. Toutes les broches de retour à la masse ***doivent*** être connectées ensemble au niveau de l'embase USB Type-C lorsqu'elle est à l'état monté (par exemple, toutes les broches de retour à la masse connectées en bus ensemble dans la CCI).
16. La fiche USB Type-C d'alimentation uniquement est une version vide de la fiche USB Type-C Complète ou ***USB 2.0***. Les dimensions d'interface ***doivent*** être conformes à la Figure 3-3 ou à la Figure 3-11. Les contacts des broches CC, VBUS et GND (à savoir A1, A4, A5, A9, A12, B1, B4, B9 et B12) ***doivent*** être présents. La présence physique de contacts dans les 15 autres points de contact est ***facultative***. La fiche USB Type-C d'alimentation uniquement ne ***doit*** être utilisée que sur une application à câble captif qui n'est pas un chargeur. La mise en œuvre de la communication ***Rd*** ou CC sur la broche A5 est exigée dans l'application.

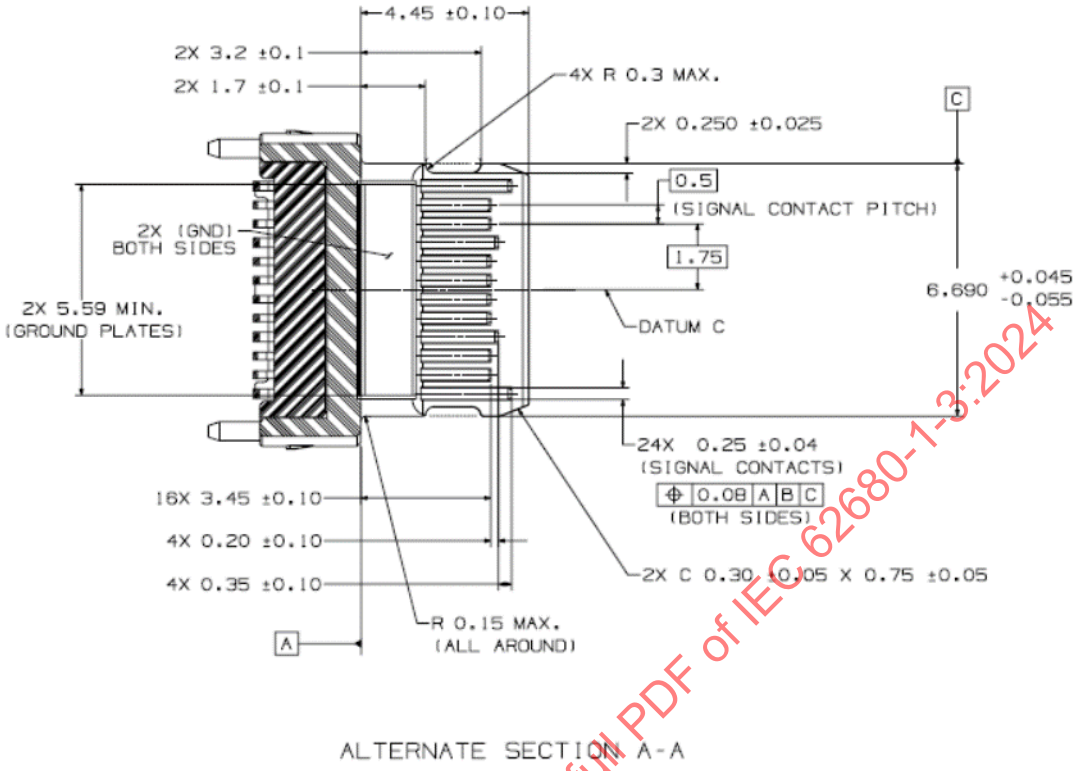
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Figure 3-1 Dimensions d'interface d'une embase USB Type-C

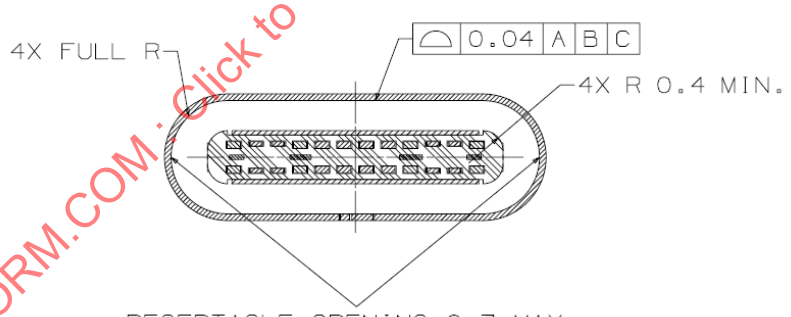


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Figure 3-1 Dimensions d'interface d'une embase USB Type-C (suite)



ALTERNATE SECTION A-A

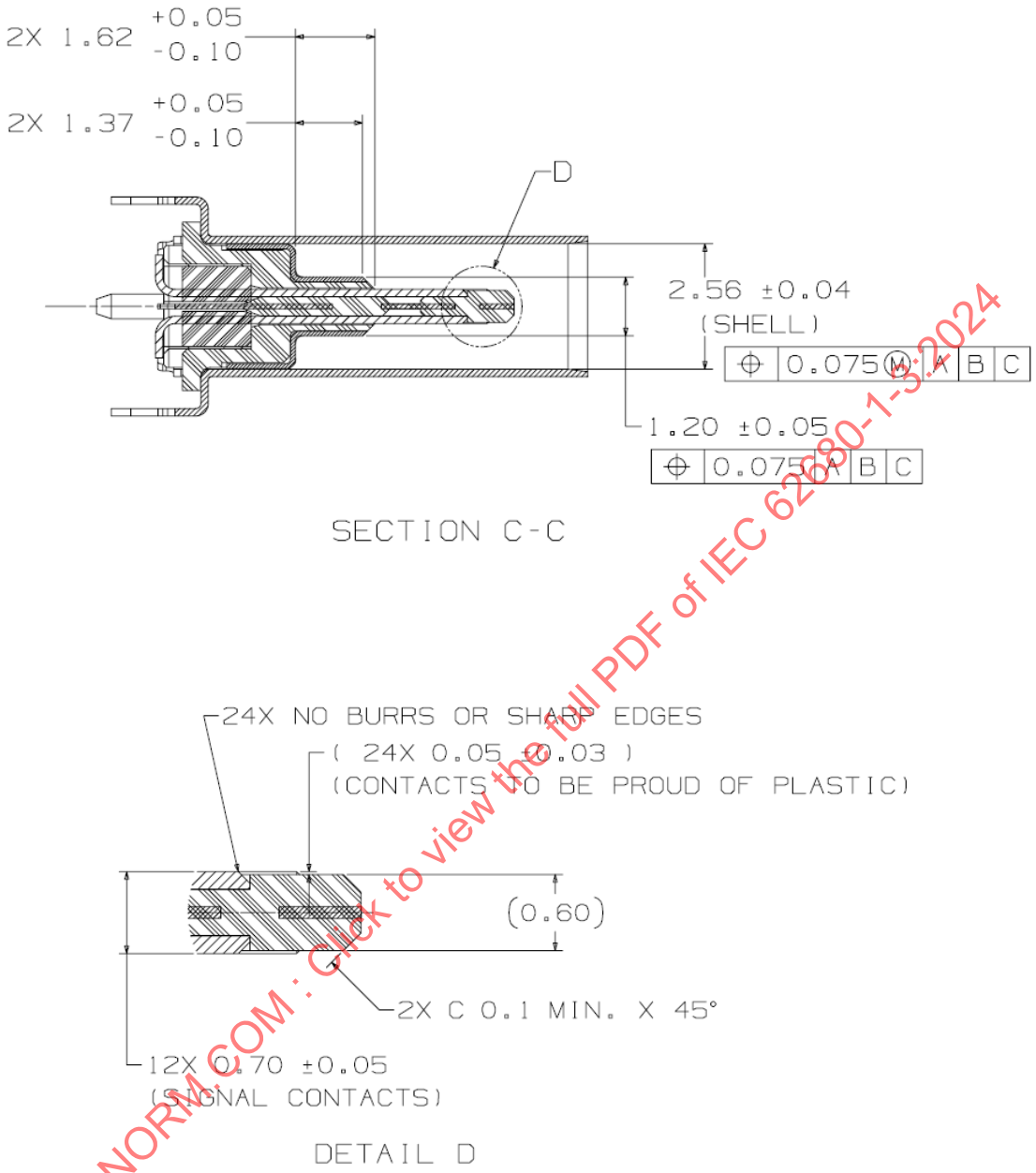


RECEPTACLE OPENING 0.7 MAX.
FLAT SIDES ALLOWED

SECTION B-B

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Figure 3-1 Dimensions d'interface d'une embase USB Type-C (suite)



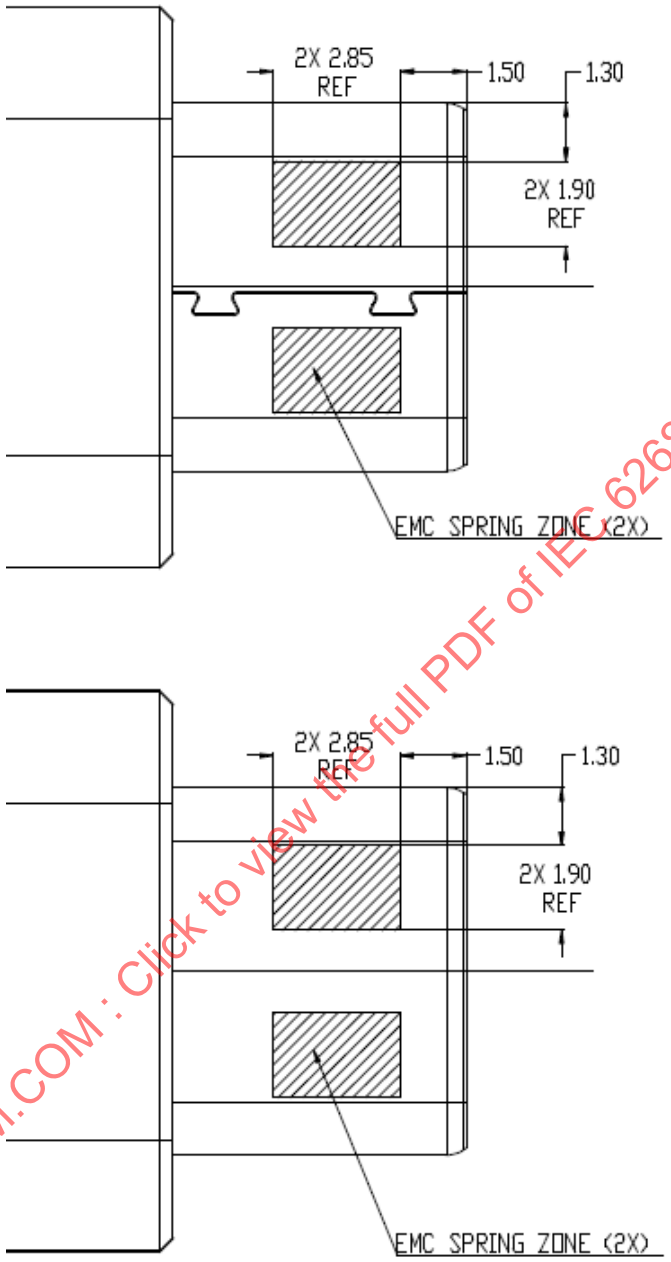
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Anglais	Français
Section A-A	Coupe A-A
Signal contact	Contact de signal
Sell opening	Ouverture de l'enveloppe
Signal contact pitch	Pas du contact de signal
Both sides	Des deux côtés
Ground plates	Plans de masse

Anglais	Français
Datum C	Plan de référence C
All around	Tout autour
Alternate section A-A	Coupe alternative A-A
4X FULL	4X FULL
Receptacle opening 0.7 max.	Ouverture de l'embase 0,7 au maximum
Flat sides allowed	Côtés plats admis
Section C-C	Coupe C-C
Shell	Enveloppe
No burrs or sharp edges	Aucune bavure ni arête vive
Contacts to be proud of plastic	Contacts dont la conception doit être en plastique
Signal contacts	Contacts de signal
Detail D	Élément D

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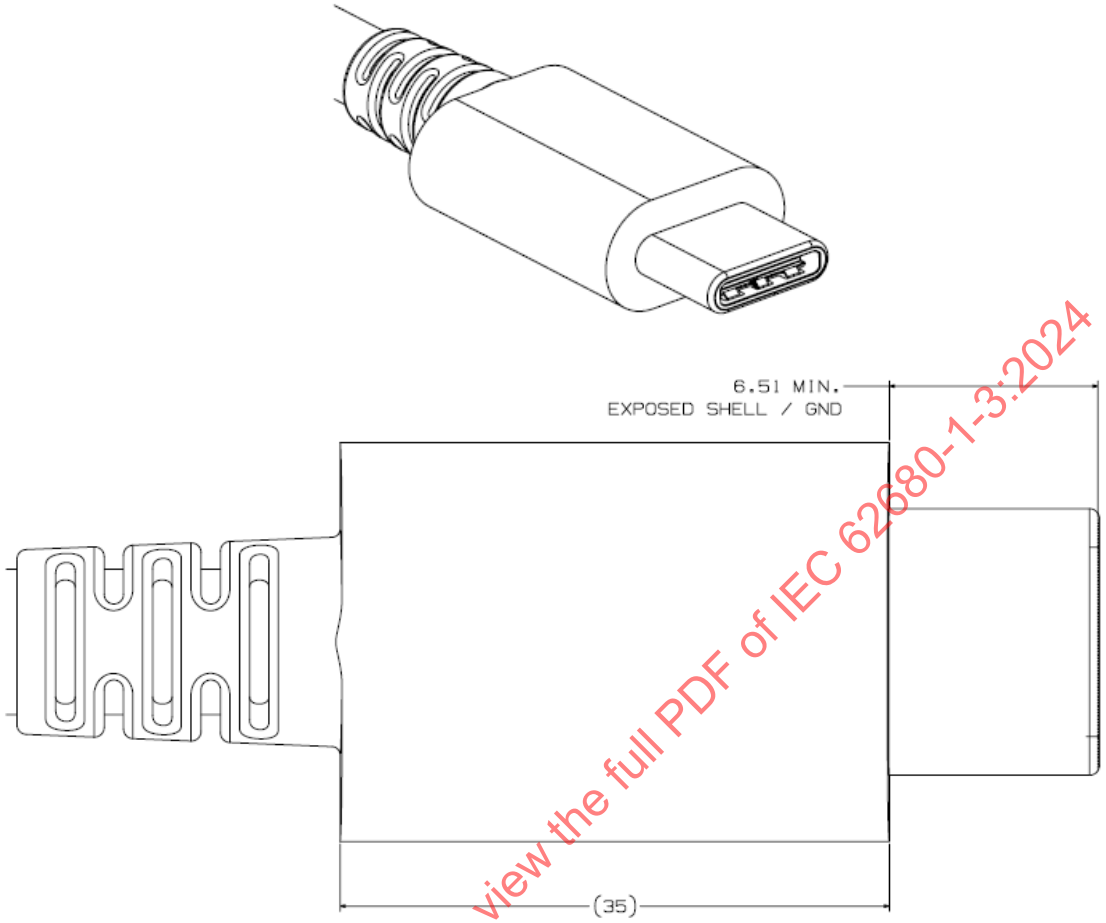
Figure 3-2 Schéma de référence des zones de contact d'un ressort CEM externe pour une fiche USB Type-C



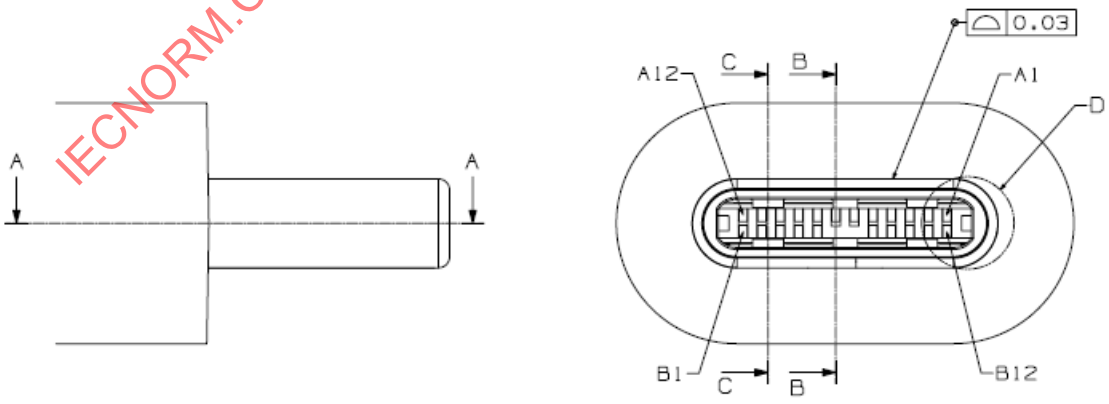
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Anglais	Français
EMC spring zone (2x)	Zone de ressort CEM (x2)

Figure 3-3 Dimensions d'interface d'une fiche USB Type-C Complète

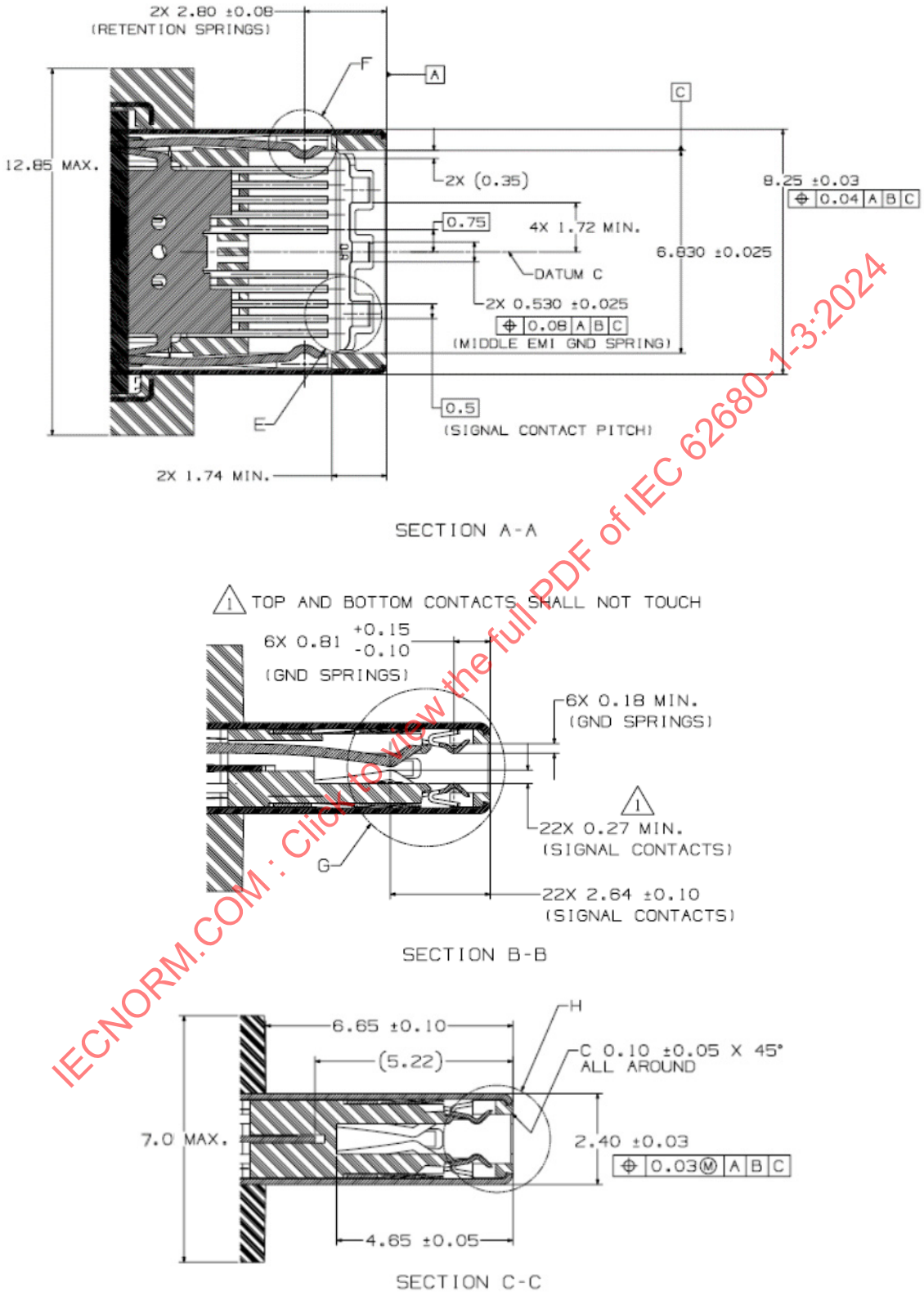


Anglais	Français
Exposed shell/GND	Enveloppe/GND exposées



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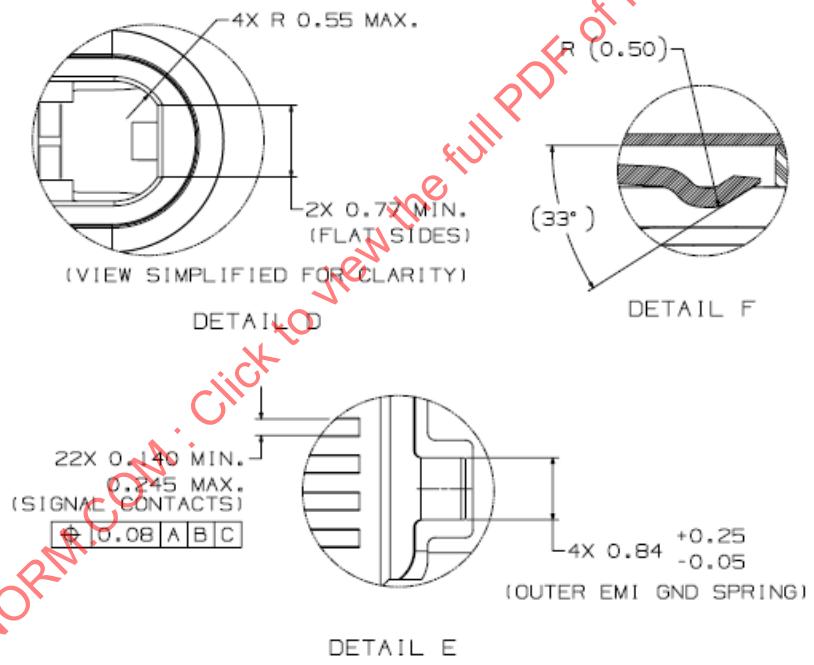
Figure 3-3 Dimensions d'interface d'une fiche USB Type-C Complète (suite)



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Anglais	Français
Retention springs	Ressorts de maintien
Datum C	Plan de référence C
Middle EMI GND spring	Ressort GND EMI central
Signal contact pitch	Pas du contact de signal
Section A-A	Coupe A-A
Top and bottom contacts shall not touch	Les contacts supérieurs et inférieurs ne doivent pas se toucher
GND springs	Ressorts GND
Signal contacts	Contacts de signal
Section B-B	Coupe B-B
All around	Tout autour
Section C-C	Coupe C-C

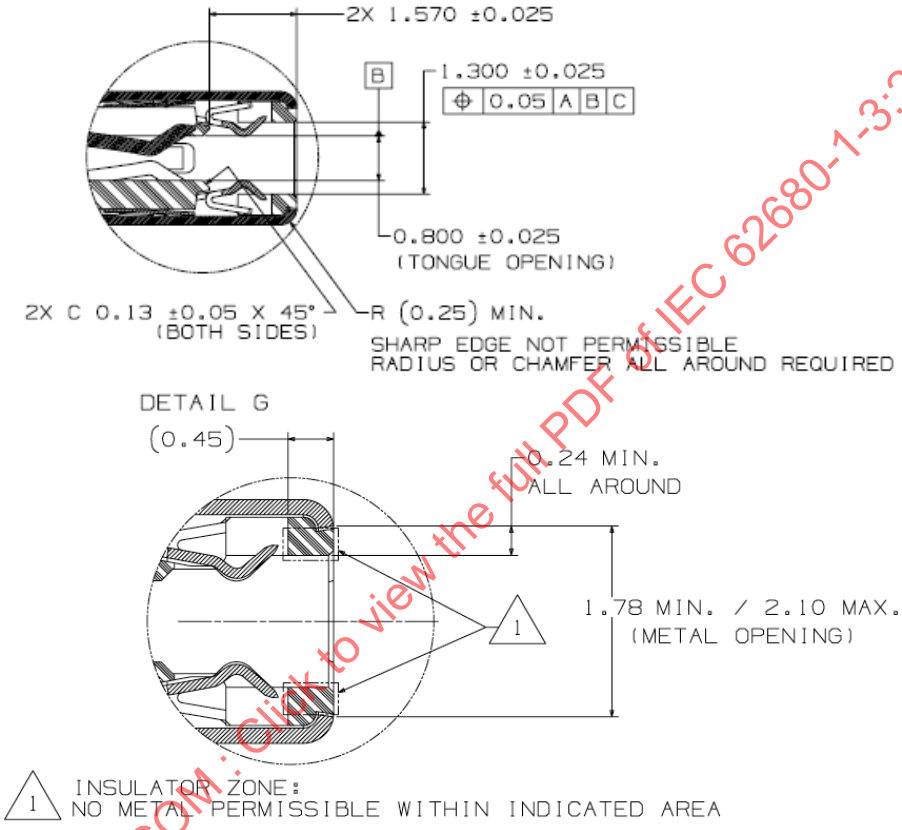
Figure 3-3 Dimensions d'interface d'une fiche USB Type-C Complète (suite)



Anglais	Français
Flat sides	Côtés plats
View simplified for clarity	Vue simplifiée pour une meilleure lisibilité
Detail	Élément
Signal contacts	Contacts de signal
Outer EMI GND spring	Ressort GND EMI extérieur
Tongue opening	Ouverture de la languette
Both sides	Des deux côtés

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Anglais	Français
Sharp edge not permissible	Arêtes vives non admises
Radius or chamfer all around required	Fraisage ou chanfrein exigé tout autour
All around	Tout autour
Metal opening	Ouverture métallique
Insulator zone	Zone d'isolation
No metal permissible within indicated area	Aucun métal admis dans la zone indiquée

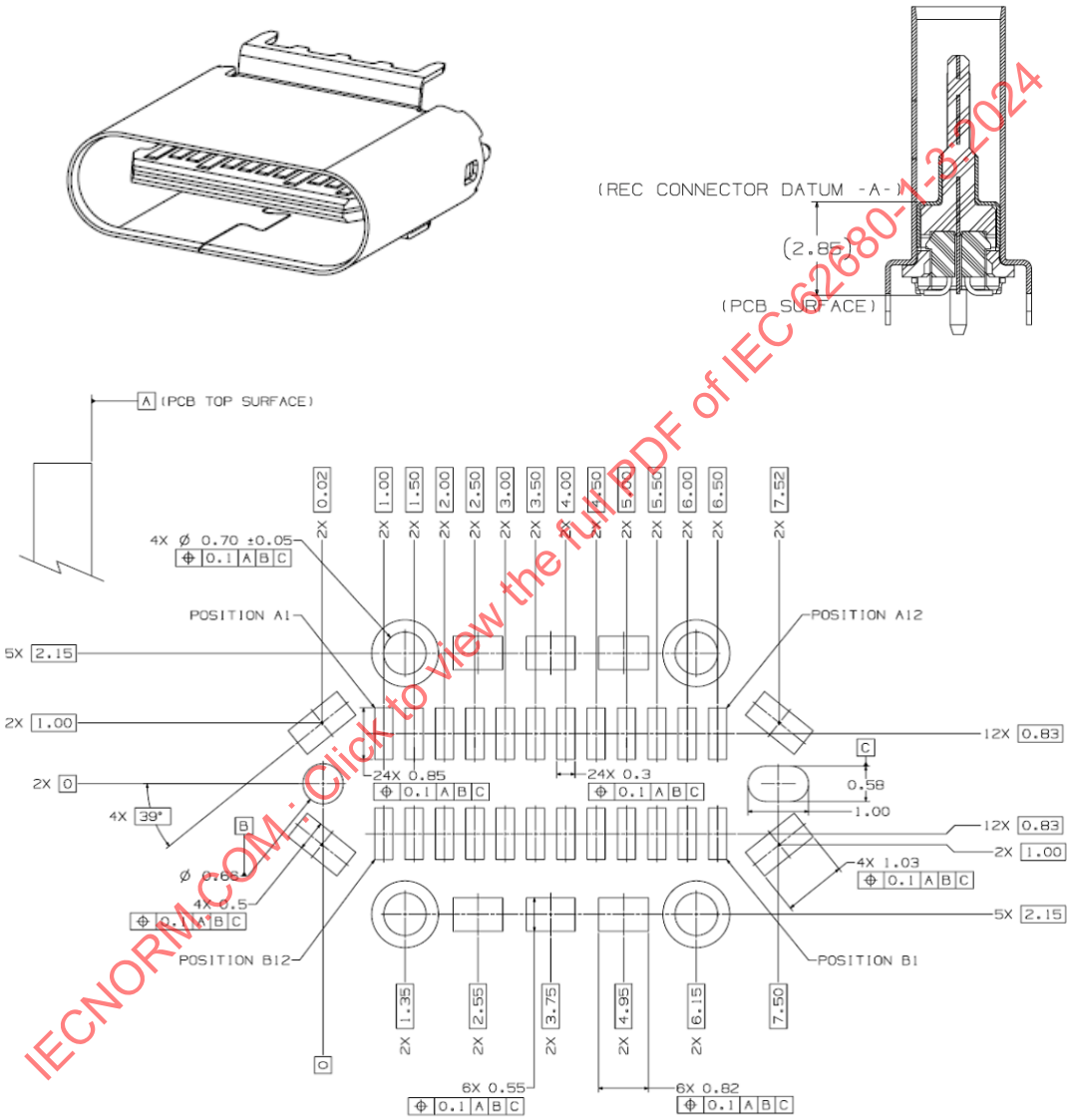


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Anglais	Français
Flat sides	Côtés plats
View simplified for clarity	Vue simplifiée pour une meilleure lisibilité
Detail	Élément
Signal contacts	Contacts de signal
Outer EMI GND spring	Ressort GND EMI extérieur
Tongue opening	Ouverture de la languette
Both sides	Des deux côtés
Sharp edge not permissible	Arêtes vives non admises
Radius or chamfer all around required	Fraisage ou chanfrein exigé tout autour
All around	Tout autour

Anglais	Français
Metal opening	Ouverture métallique
Insulator zone	Zone d'isolation
No metal permissible within indicated area	Aucun métal admis dans la zone indiquée

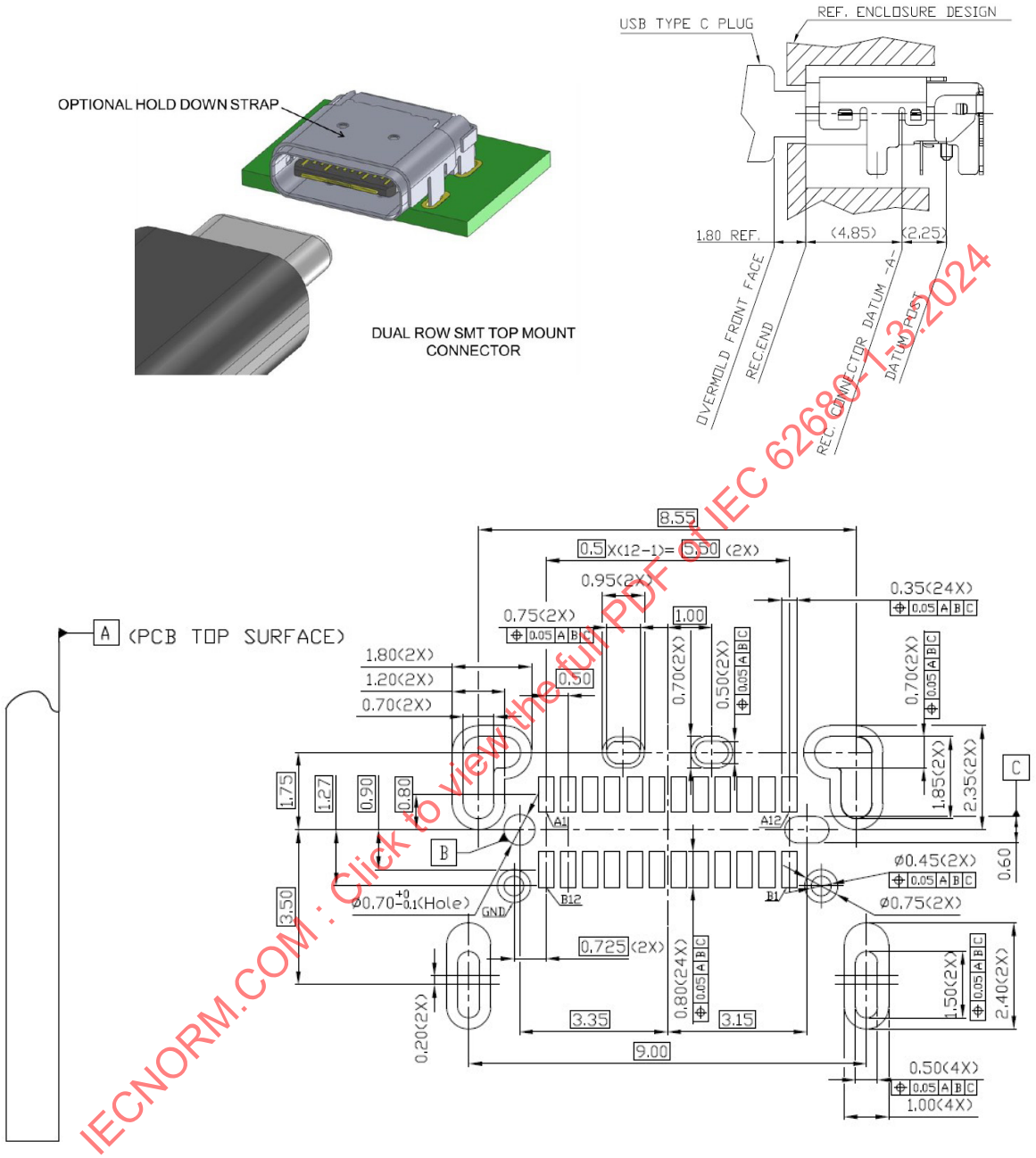
Figure 3-4 Empreinte de référence d'une embase USB Type-C montée à la verticale (*informative*)



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Anglais	Français
Rec connector datum -A-	Embase réf -A-
PCB surface	Surface de la CCI
PCB top surface	Surface supérieure de la CCI

Figure 3-5 Empreinte de référence d'une embase USB Type-C montée en surface, à angle droit et sur deux rangées (*informative*)

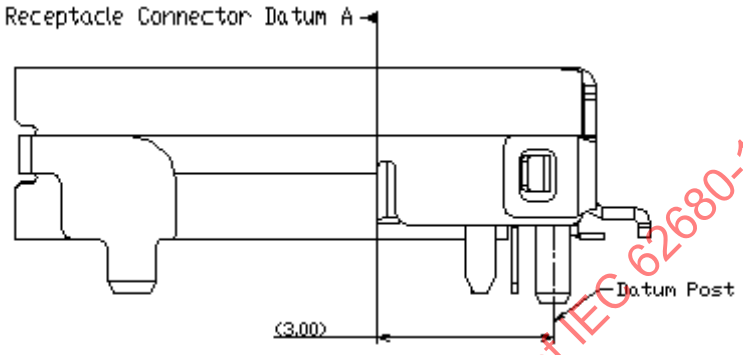


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Anglais	Français
Optional hold down strap	Bride de maintien facultative
Dual row SMT top mount connector	Connecteur SMT pour montage supérieur en double anneau
USB Type C plug	Fiche USB Type-C
Ref. Enclosure design	Réf conception de l'enveloppe
Overmold front face	Face avant du surmoulage
Rec. end	Terminaison de l'embase

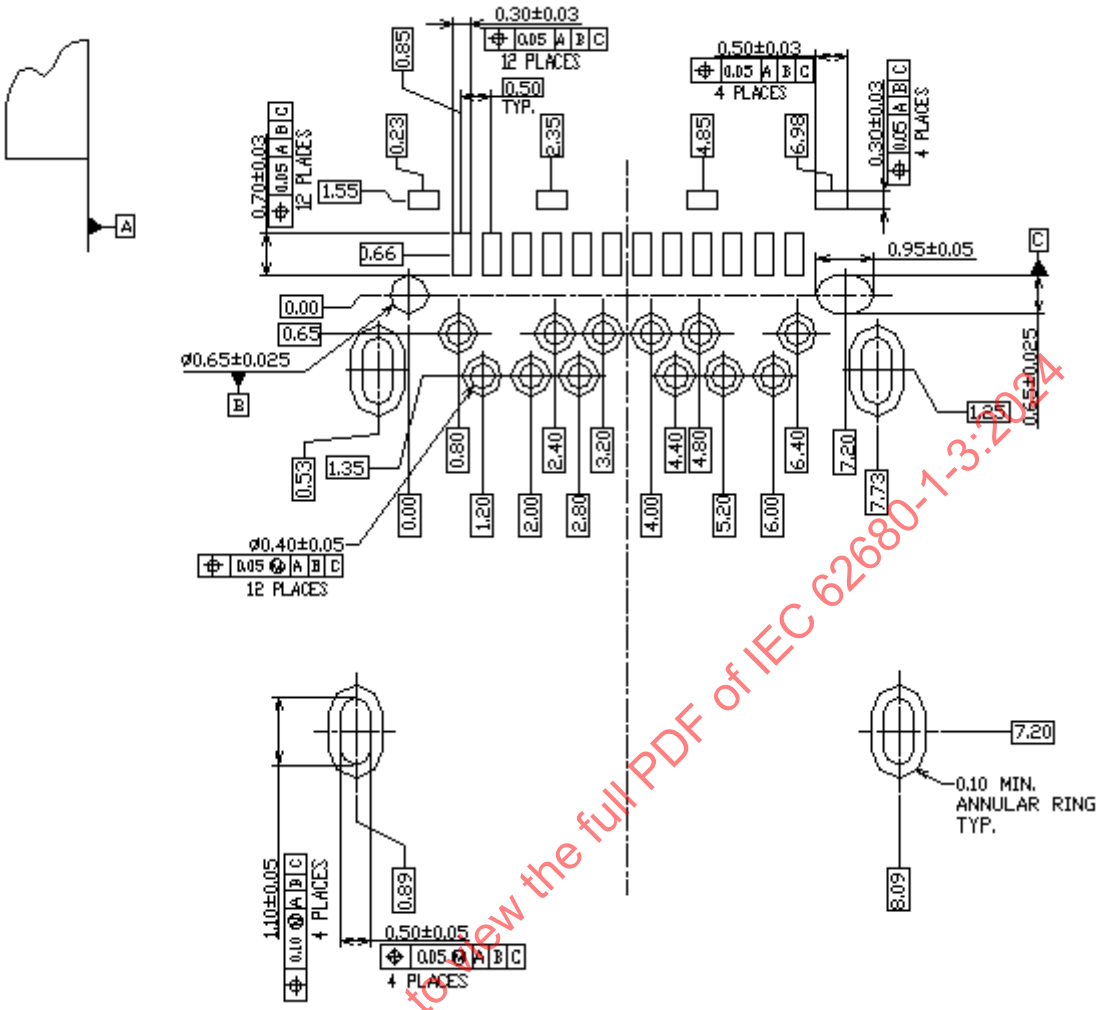
Anglais	Français
Rec. Connector datum -A-	Embase réf -A-
Datum post	Réf support
PCB top surface	Surface supérieure de la CCI
Hole	Trou

Figure 3-6 Empreinte de référence d'une embase USB Type-C hybride montée à angle droit (*informative*)



Anglais	Français
Receptacle connector datum A	Embase réf A
Datum post	Réf support

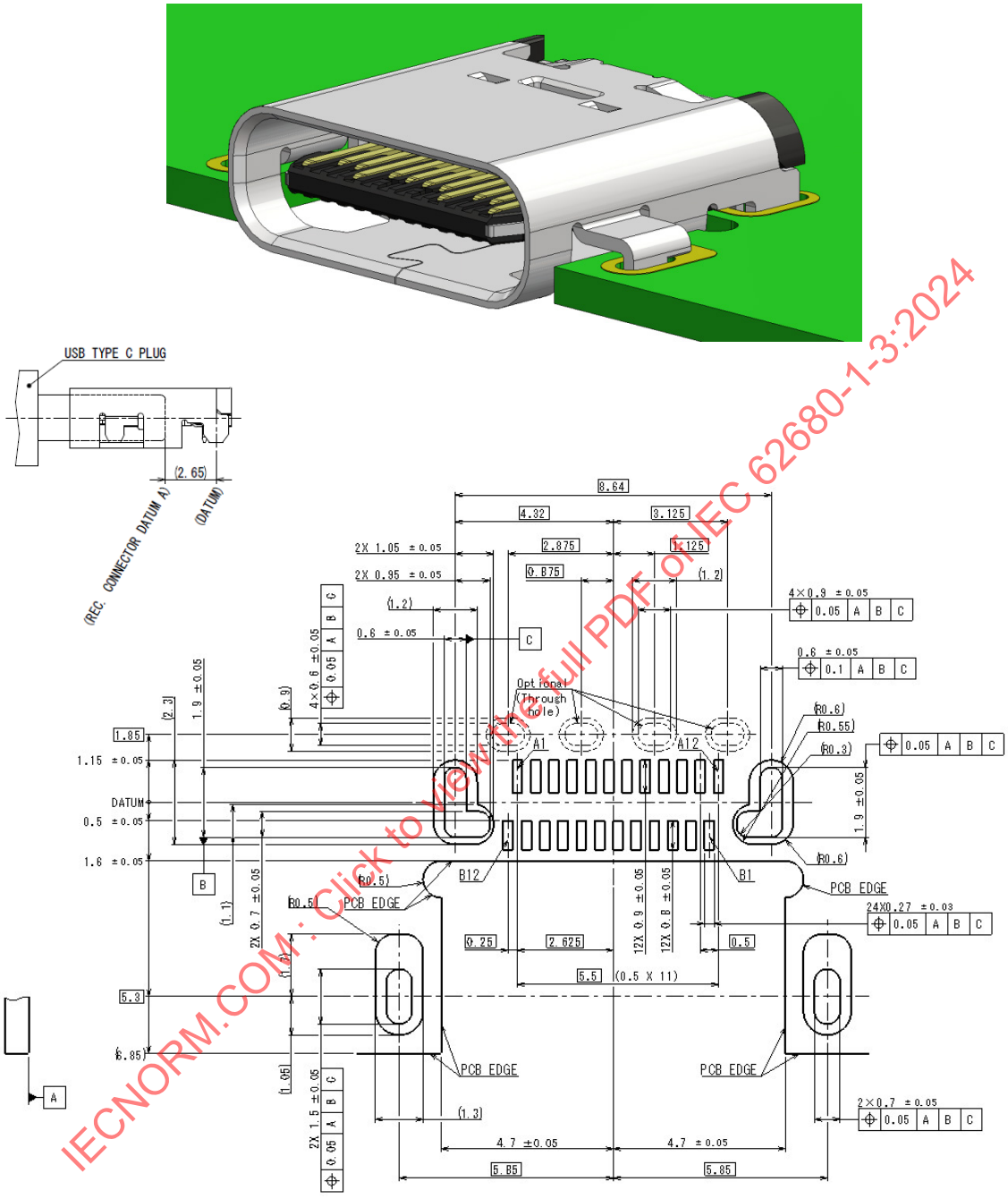
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Anglais	Français
Receptacle connector datum A	Embase réf A
Datum post	Réf support
Places	Emplacements
0.10 min. Annular ring typ.	Bague annulaire type 0,10 min

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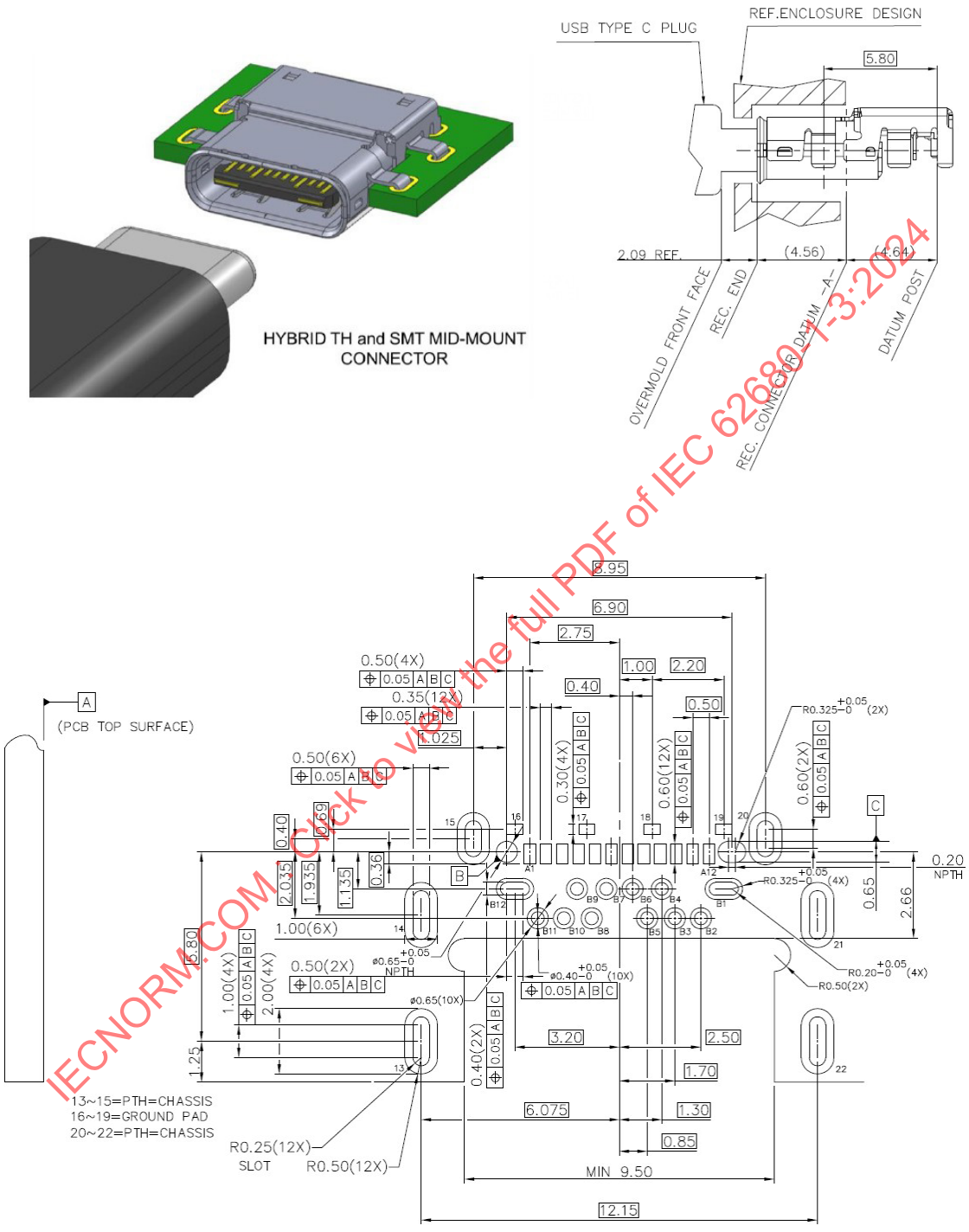
Figure 3-7 Empreinte de référence d'une embase USB Type-C montée en surface, au centre et sur deux rangées (*informative*)



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Anglais	Français
USB Type C plug	Fiche USB Type-C
Rec. Connector datum A	Embase réf A
Datum	Plan de référence
Optional (through hole)	Facultatif (trou métallisé)
PCB edge	Arête de la CCI

Figure 3-8 Empreinte de référence d'une embase USB Type-C hybride montée au centre (*informative*)



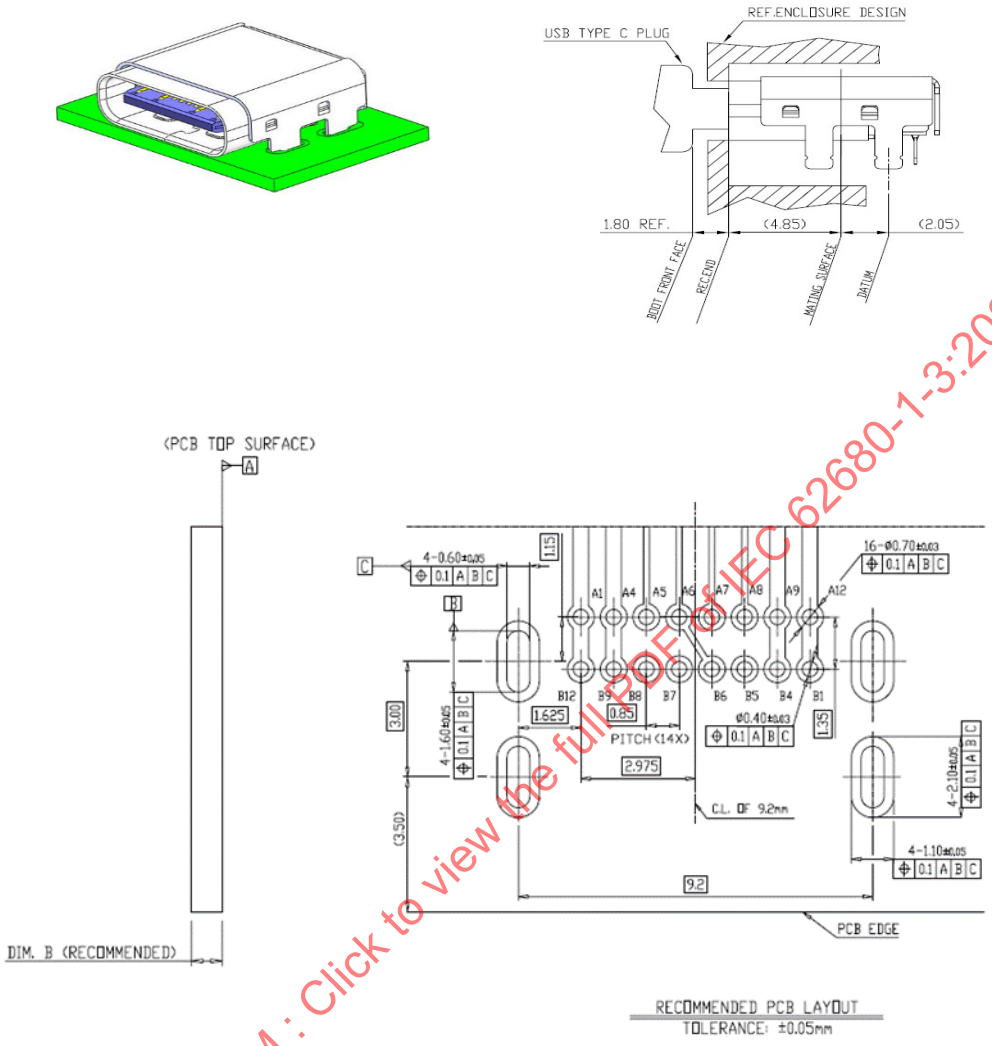
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Anglais	Français
Hybrid TH and SMT mid-mount connector	Connecteur TH hybride et connecteur SMT pour montage central
USB Type C plug	Fiche USB Type-C

Anglais	Français
Ref. Enclosure design	Réf conception de l'enveloppe
Overmold front face	Face avant du surmoulage
Rec. End	Terminaison de l'embase
Rec. Connector datum -A-	Embase réf -A-
Datum post	Réf support
PCB top surface	Surface supérieure de la CCI
PTH = chassis	Trou métallisé = châssis
Ground pad	Coussin de masse
Slot	Logement

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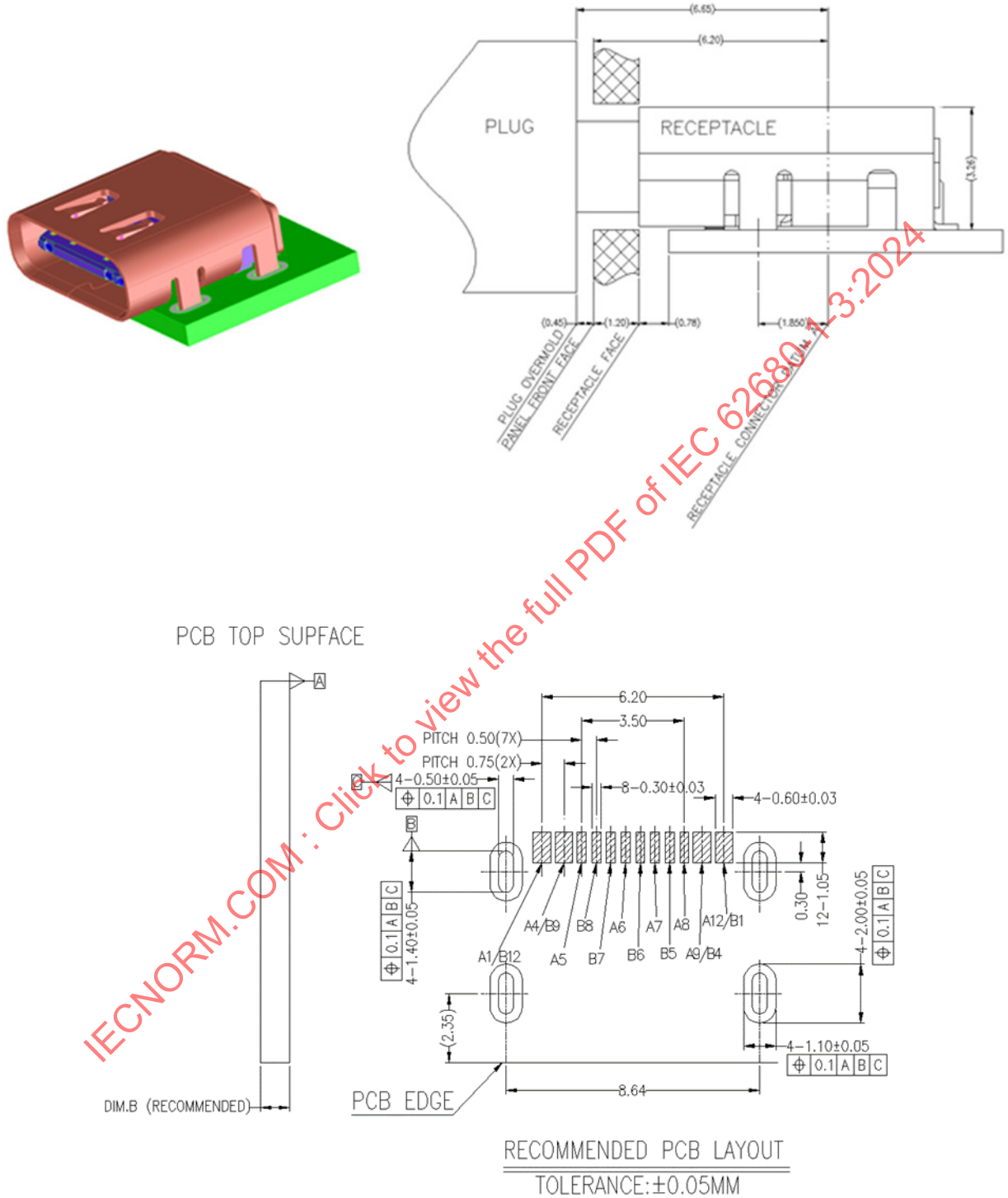
Figure 3-9 Empreinte de référence d'une embase *USB 2.0* Type-C à insérer montée à angle droit (*informative*)



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Anglais	Français
USB Type C plug	Fiche USB Type-C
Ref enclosure design	Réf conception de l'enveloppe
Boot front face	Face avant d'amorçage
Rec. End	Terminaison de l'embase
Mating surface	Surface de couplage
Datum	Plan de référence
PCB top surface	Surface supérieure de la CCI
Dim. B (recommended)	Dim. B (recommandée)
Recommended PCB layout	Montage de CCI recommandé
Tolerance	Tolérance

Figure 3-10 Empreinte de référence d'une embase *USB 2.0* Type-C montée à angle droit sur une rangée (*informative*)



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Anglais	Français
Plug	Fiche
Receptacle	Embase

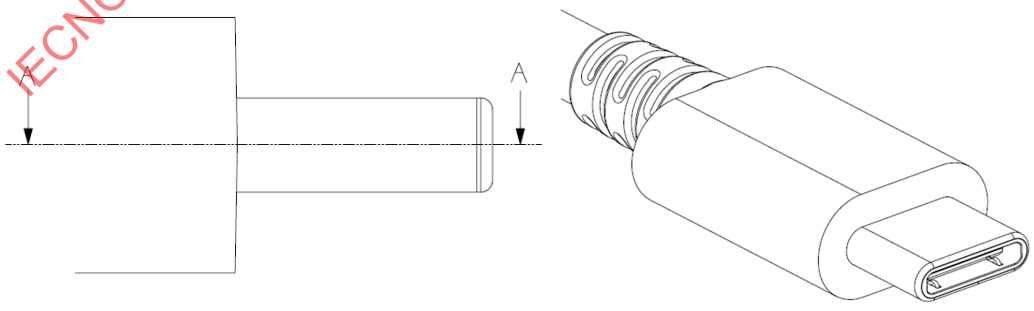
Anglais	Français
Plug overmold	Surmoulage de la fiche
Panel front face	Face avant du panneau
Receptacle face	Face de l'embase
Receptacle connector datum -A-	Embase réf -A-
PCB top surface	Surface supérieure de la CCI
Pitch	Pas
Dim.B (recommended)	Dim. B (recommandée)
PCB edge	Arête de la CCI
Recommended PCB layout	Montage de CCI recommandé
Tolerance	Tolérance

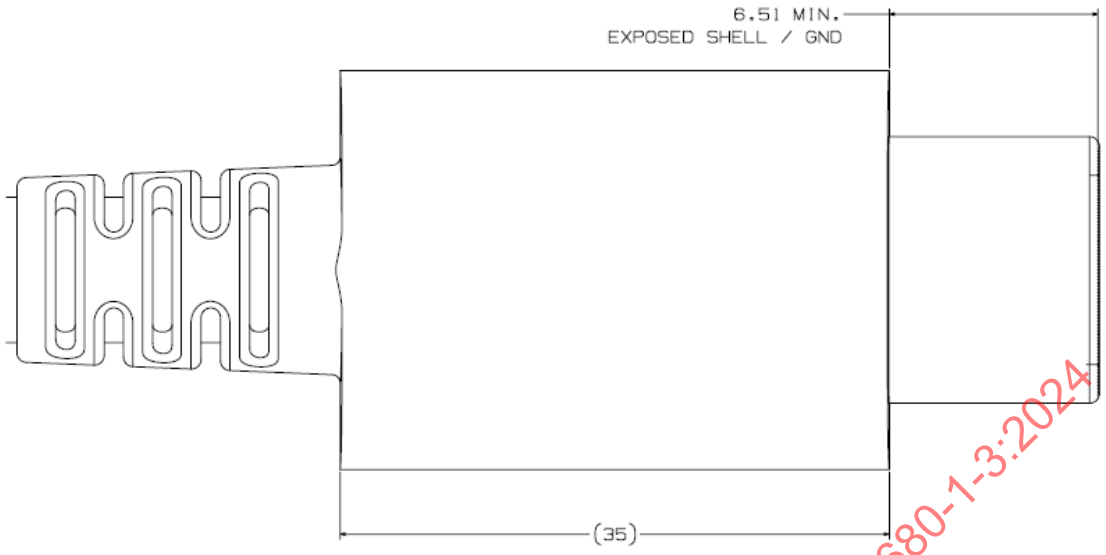
La présente spécification exige que tous les contacts soient présents dans l'interface de couplage de l'embase USB Type-C Complète et que tous les contacts, à l'exception des signaux ***USB 3.2*** ou ***USB4*** (c'est-à-dire A2, A3, A10, A11, B2, B3, B10 et B11) soient présents dans l'interface de couplage de l'embase ***USB 2.0*** Type-C; elle permet toutefois à la fiche d'inclure uniquement les contacts exigés pour la fonctionnalité ***USB PD*** et ***USB 2.0*** des applications qui ne prennent en charge que l'***USB 2.0***. La fiche ***USB 2.0*** Type-C est représentée à la Figure 3-11. Les simplifications de conception suivantes ne ***peuvent*** être appliquées que si l'***USB 2.0*** est pris en charge:

- Seuls les contacts nécessaires à la prise en charge de l'***USB PD*** et de l'***USB 2.0*** sont exigés pour la fiche. Tous les autres emplacements de broche ***peuvent*** être vidés. Voir le Tableau 3-5.
- Contrairement à la fiche USB Type-C Complète, les ressorts CEM internes ***peuvent*** être formés à partir de la même bande que les contacts de signal, d'alimentation et de masse. Les ressorts CEM internes sont en contact avec la surface interne de l'enveloppe de la fiche et sont couplés avec les plaques CEM de l'embase lorsque la fiche est insérée dans l'embase. Sinon, la fiche ***USB 2.0*** Type-C ***peut*** utiliser la même configuration de ressort CEM que celle définie pour la fiche USB Type-C Complète. Les quatre emplacements du ressort CEM pour la fiche ***USB 2.0*** Type-C sont définis à la Figure 3-11. La configuration alternative qui utilise les six emplacements de ressort est définie à la Figure 3-1. Pour plus de précisions, se référer aussi aux schémas de référence en 3.2.2.3.
- Une carte d'accès ***peut ne pas*** être nécessaire à l'intérieur de la fiche si les fils sont directement branchés aux broches de contact.

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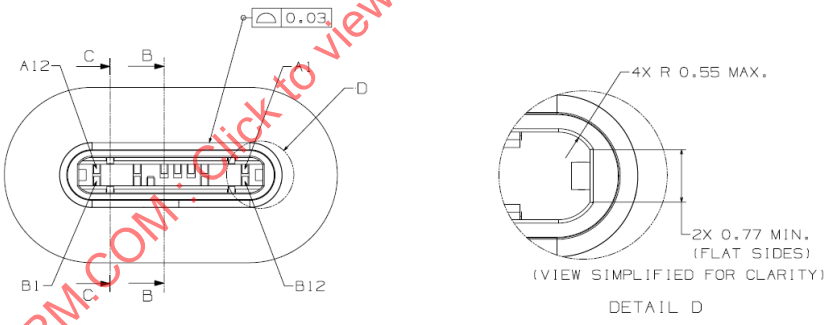
Figure 3-11 Dimensions d'interface d'une fiche *USB 2.0* Type-C



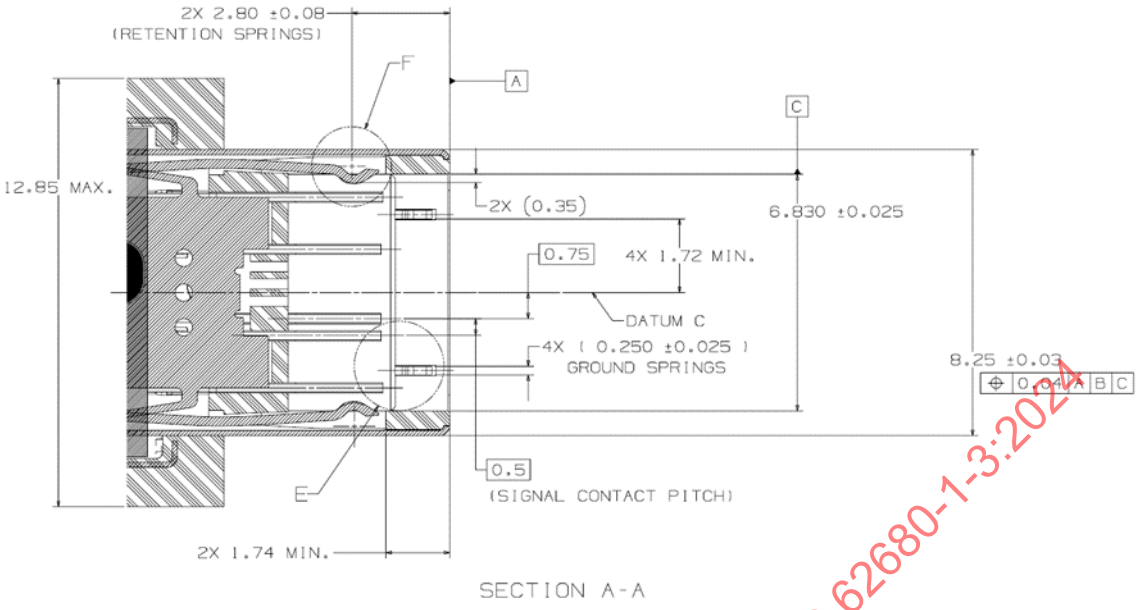


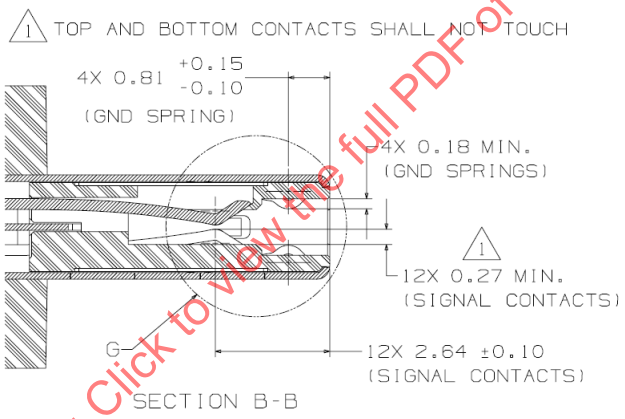
Anglais	Français
Exposed shell/GND	Enveloppe/GND exposées

Figure 3-11 Dimensions d'interface d'une fiche *USB 2.0* Type-C (suite)



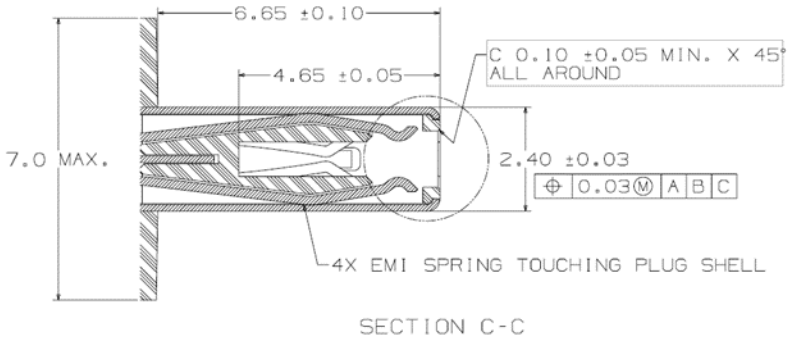
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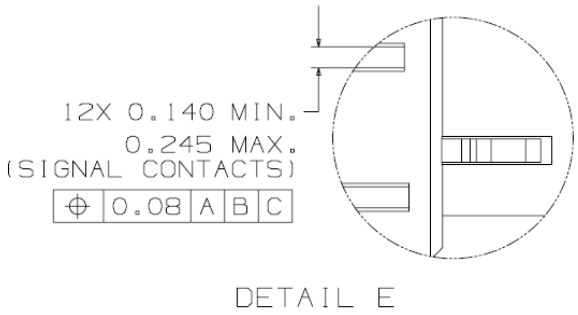




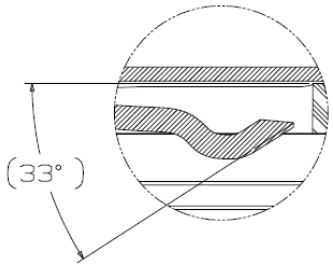
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Figure 3-11 Dimensions d'interface d'une fiche *USB 2.0* Type-C (suite)





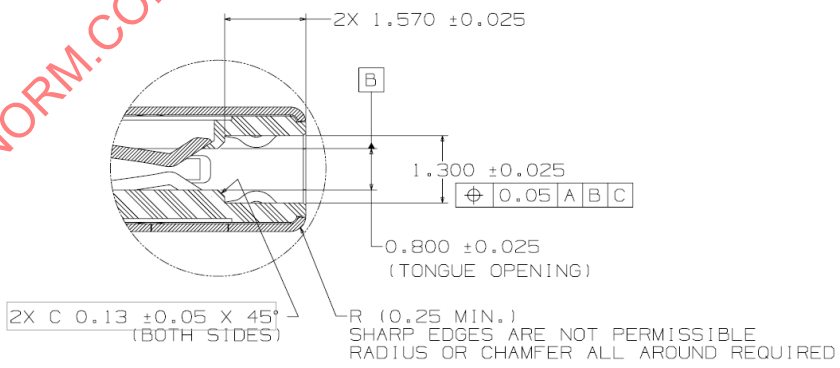
DETAIL E



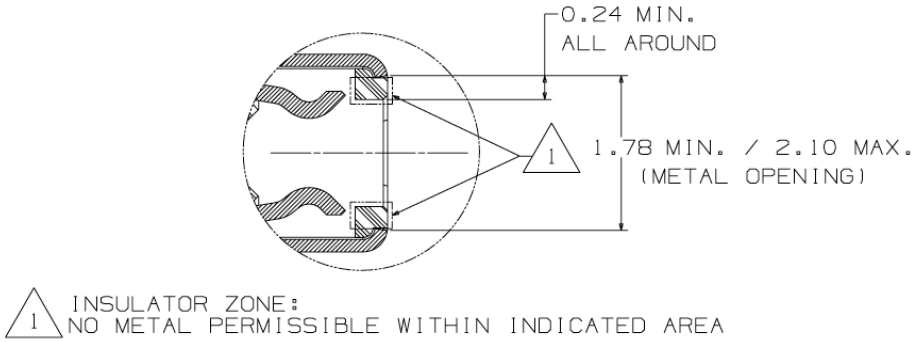
DETAIL F

Anglais	Français
Flat sides	Côtés plats
View simplified for clarity	Vue simplifiée pour une meilleure lisibilité
Detail D	Élément D
Retention springs	Ressorts de maintien
Ground springs	Ressorts GND
Signal contact pitch	Pas du contact de signal
Section A-A	Coupe A-A
Top and bottom contacts shall not touch	Les contacts supérieurs et inférieurs ne doivent pas se toucher
GND spring	Ressort GND
GND springs	Ressorts GND
Signal contacts	Contacts de signal
Section B-B	Coupe B-B
EMI spring touching plug shell	Ressort EMI en contact avec l'enveloppe de la fiche
All around	Tout autour
Section C-C	Coupe C-C

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DETAIL G

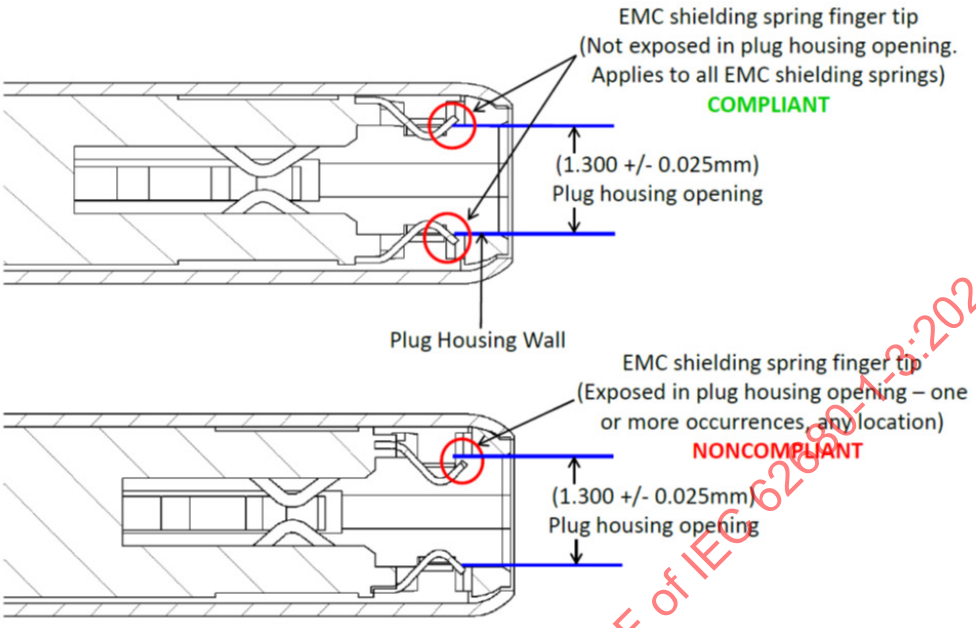


DETAIL H

Anglais	Français
Signal contacts	Contacts de signal
Detail E	Élément E
Detail F	Élément F
Tongue opening	Ouverture de la languette
Both sides	Des deux côtés
Detail G	Élément G
Sharp edges are not permissible	Arêtes vives non admises
Radius or chamfer all around required	Fraisage ou chanfrein exigé tout autour
All around	Tout autour
Metal opening	Ouverture métallique
Insulator zone	Zone d'isolation
No metal permissible within indicated area	Aucun métal admis dans la zone indiquée

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Figure 3-12 Exigences relatives à la pointe du ressort d'écrantage CEM d'une fiche USB Type-C



Anglais	Français
EMC shielding spring finger tip (not exposed in plug housing opening. Applies to all EMC shielding springs)	Pointe du ressort d'écrantage CEM (non exposée par l'ouverture du boîtier de la fiche – s'applique à tous les ressorts d'écrantage CEM)
Compliant	Conforme
Plug housing opening	Ouverture du boîtier de la fiche
Plug Housing Wall	Paroi du boîtier de la fiche
EMC shielding spring finger tip (Exposed in plug housing opening – one or more occurrences, any location)	Pointe du ressort d'écrantage CEM (exposée par l'ouverture du boîtier de la fiche – une ou plusieurs occurrences, n'importe quel emplacement)
Noncompliant	Non conforme

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3.2.2 Schémas de référence

Le présent paragraphe fournit des schémas de référence pour certaines caractéristiques essentielles du connecteur USB Type-C. Les schémas de référence sont fournis à des fins d'exemple de conception admise. Ils ne sont pas ***normatifs***.

3.2.2.1 Plaque médiane de l'embase (*informative*)

Les signaux situés entre la partie supérieure et la partie inférieure de la languette de l'embase sont isolés par une plaque médiane à l'intérieur de la languette.

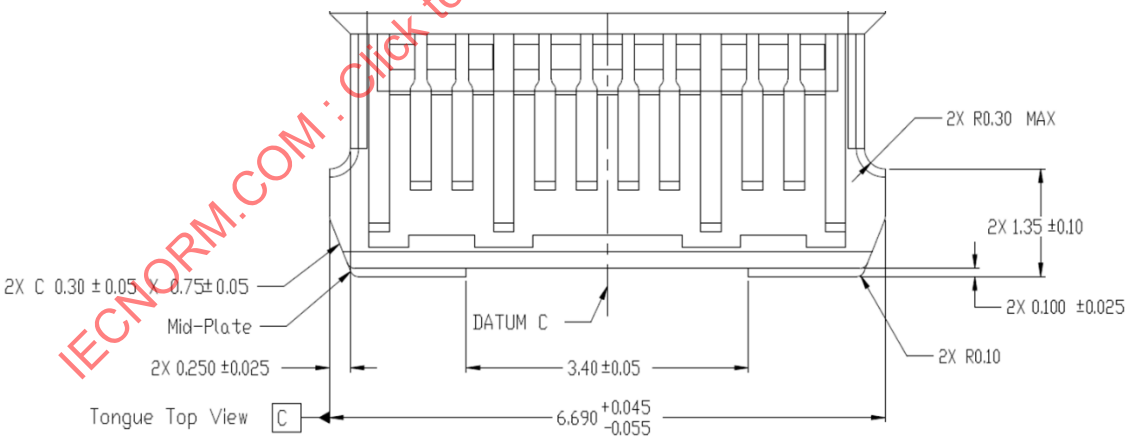
La

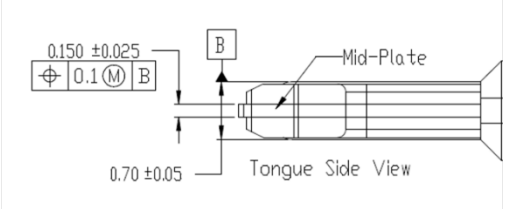
Figure 3-13 représente un schéma de référence de la plaque médiane. Il est important de prêter attention aux caractéristiques suivantes de la plaque médiane:

- ***Il convient de*** contrôler avec exactitude la distance entre les contacts de signal et la plaque médiane, car la variation de cette distance ***peut*** avoir une incidence significative sur l'impédance du connecteur.
- Dans ce schéma, la plaque médiane dépasse légèrement de la surface avant de la languette. Cela permet de protéger la surface avant de la languette contre tout dommage provoqué par une mauvaise insertion de petits objets dans l'embase.
- La plaque médiane doit être reliée directement à la masse de la CCI en au moins deux points de mise à la masse.
- Les côtés de la plaque médiane sont couplés avec le verrou latéral de la fiche, ce qui permet de réduire la CEM par un raccordement à la masse. Des finitions de surface adéquates sont nécessaires sur les surfaces où se trouvent le verrou latéral et les connexions de la plaque médiane.

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Figure 3-13 Schéma de référence de la plaque médiane de l'embase





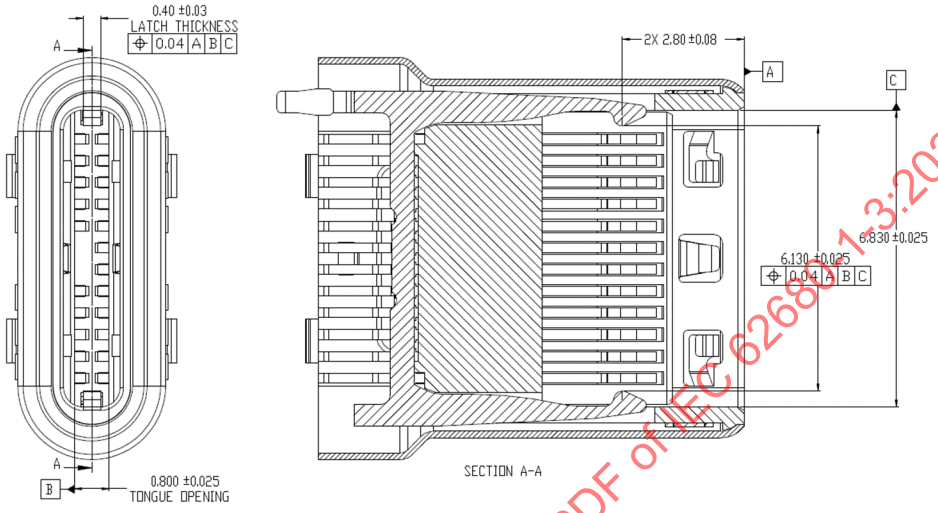
Anglais	Français
Mid-Plate	Plaque médiane
Tongue Top View	Vue supérieure de la languette
Datum C	Plan de référence C
Tongue Side View	Vue latérale de la languette

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3.2.2.2 Verrou latéral (*informatif*)

Les verrous latéraux (verrous de maintien) se situent à l'intérieur de la fiche. La Figure 3-14 représente un schéma de référence d'un verrou latéral. ***Il convient*** que le verrou latéral de la fiche soit en contact avec la plaque médiane de l'embase, afin de fournir un chemin de retour à la masse supplémentaire.

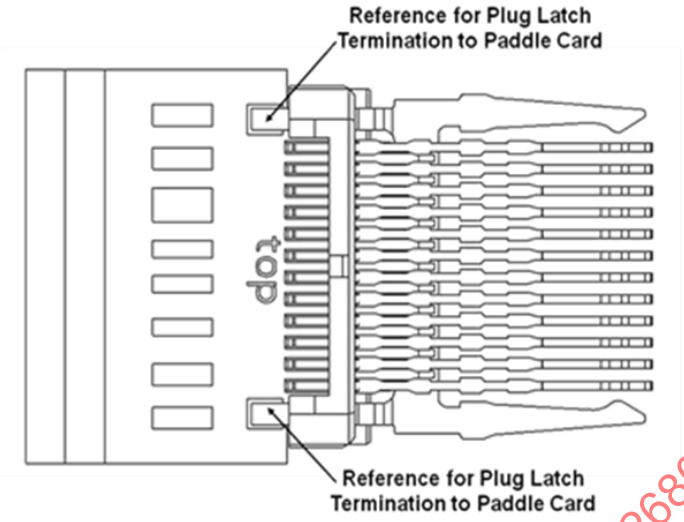
Figure 3-14 Schéma de référence du verrou latéral



Anglais	Français
Latch thickness	Épaisseur du verrou
Tongue opening	Ouverture de la languette
Section A-A	Coupe A-A

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Figure 3-15 Représentation du verrou brasé à la masse de la carte d'accès



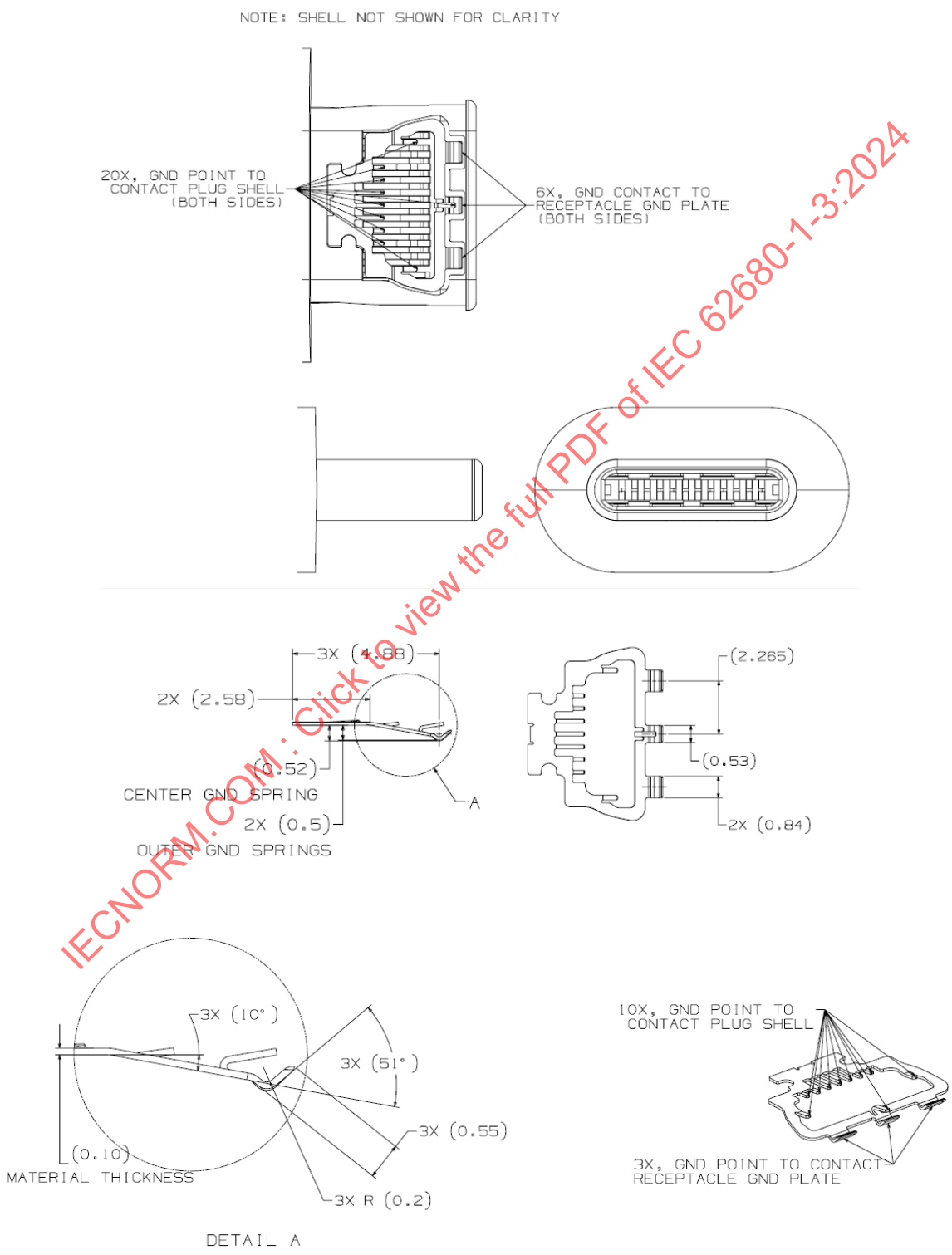
Anglais	Français
Reference for Plug Latch Termination to Paddle Card	Référence pour la terminaison du verrou de connecteur vers la carte d'accès

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3.2.2.3 Ressorts et plaques CEM internes (*informatifs*)

La Figure 3-16 est un schéma de référence du ressort CEM interne, situé à l'intérieur de la fiche USB Type-C Complète. La Figure 3-17 est un schéma de référence du ressort CEM interne situé à l'intérieur de la fiche ***USB 2.0*** Type-C.

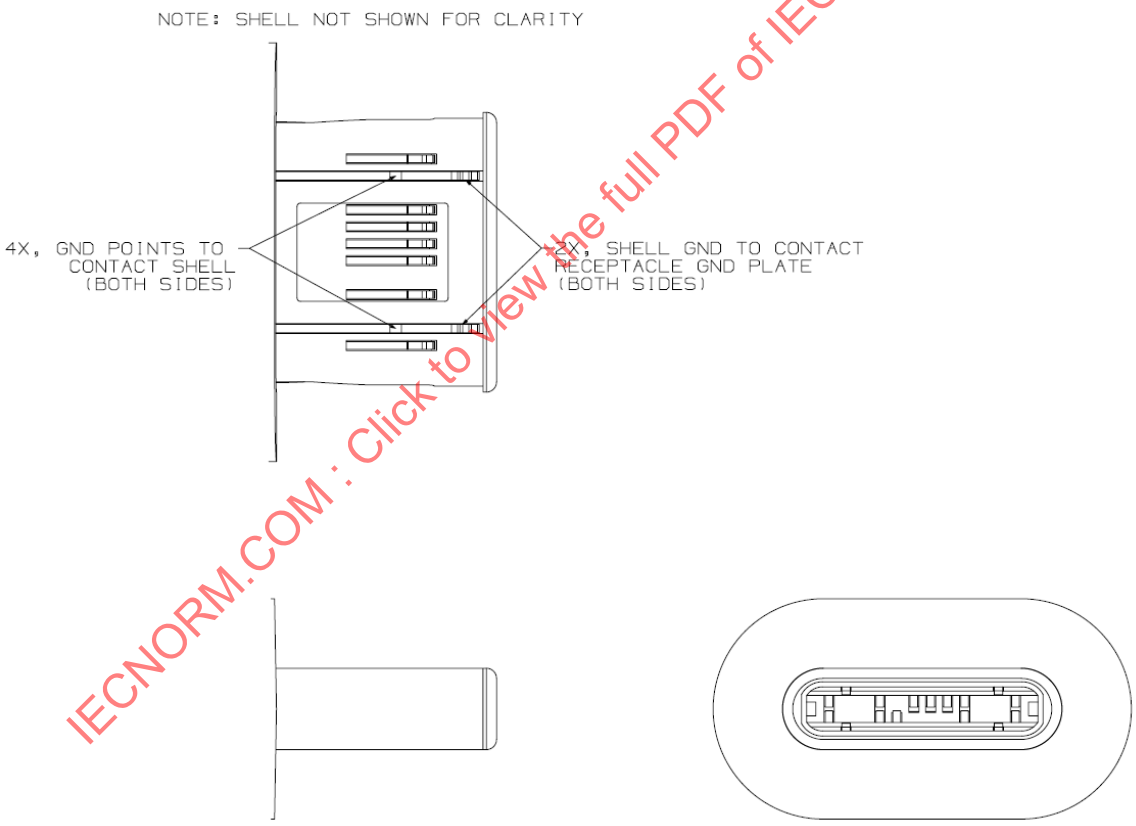
Figure 3-16 Schéma de référence du ressort CEM interne d'une fiche USB Type-C Complète



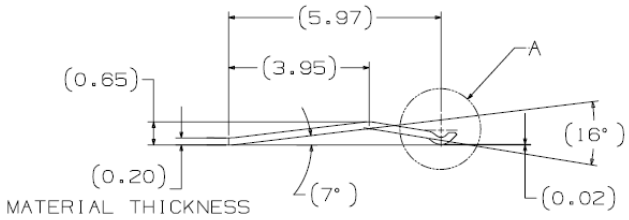
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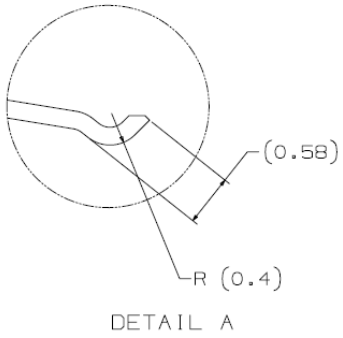
Anglais	Français
Note: shell no shown for clarity	Note: enveloppe non représentée pour une meilleure lisibilité
20x, GND point to contact plug shell (both sides)	20x, contact GND vers contact de l'enveloppe de la fiche (des deux côtés)
6x, GND contact to receptacle GND plate (both sides)	6x, contact GND vers plan de masse de l'embase (des deux côtés)
Center GND springs	Ressorts GND centraux
Outer GND springs	Ressorts GND extérieurs
Material thickness	Épaisseur du matériau
Detail A	Élément A
10x, GND point to contact plug shell	10x, contact GND vers contact de l'enveloppe de la fiche
3x, GND point to contact receptacle GND plate	3x, contact GND vers contact du plan de masse de l'embase

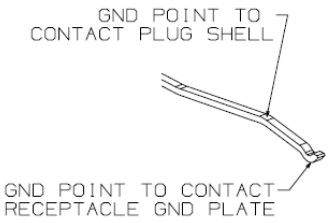
Figure 3-17 Schéma de référence du ressort CEM interne d'une fiche *USB 2.0* Type-C

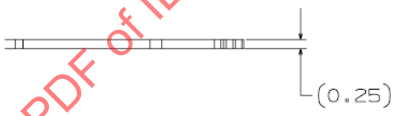


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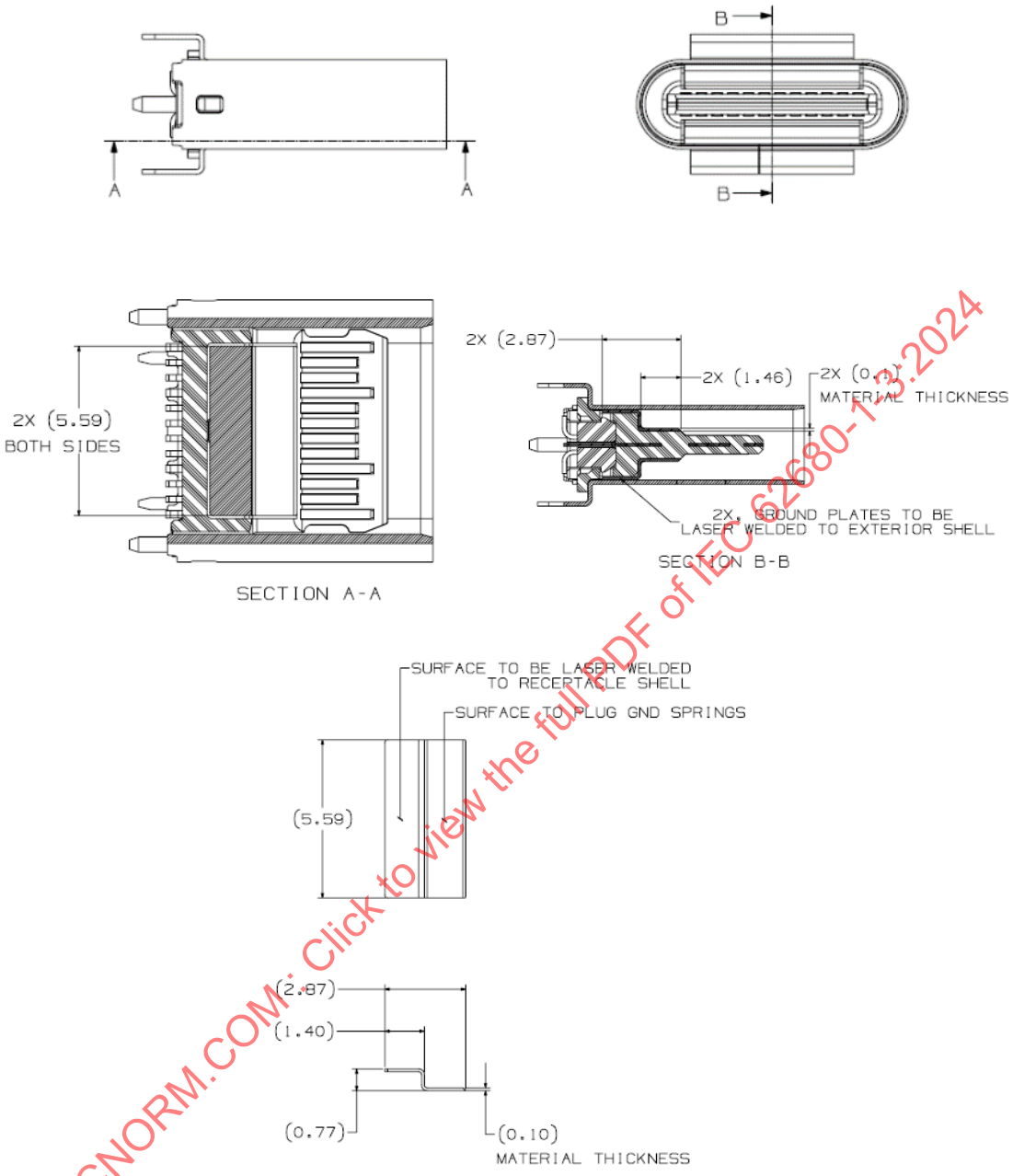
Anglais	Français
Note: shell no shown for clarity	Note: enveloppe non représentée pour une meilleure lisibilité
4x, GND point to contact shell (both sides)	4x, contact GND vers contact de l'enveloppe (des deux côtés)
2x, shell GND to contact receptacle GND plate (both sides)	2x, GND de l'enveloppe vers contact du plan de masse de l'embase (des deux côtés)
Material thickness	Épaisseur du matériau
GND point to contact plug shell	Contact GND vers contact de l'enveloppe de la fiche
GND point to contact receptacle GND plate	Contact GND vers contact du plan de masse de l'embase
Detail A	Élément A

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Il est essentiel que le ressort CEM interne soit en contact avec l'enveloppe de la fiche au plus près possible de l'interface de couplage du ressort CEM, afin de réduire le plus possible la longueur du chemin de retour.

La plaque CEM interne (à savoir le plan de masse) représentée à la Figure 3-18 se trouve à l'intérieur de l'embase. Elle est couplée avec le ressort CEM dans la fiche. Pour assurer un retour à la masse efficace, ***il convient que*** les plaques CEM comportent plusieurs connexions à l'enveloppe de l'embase.

Figure 3-18 Schéma de référence d'une plaque CEM interne



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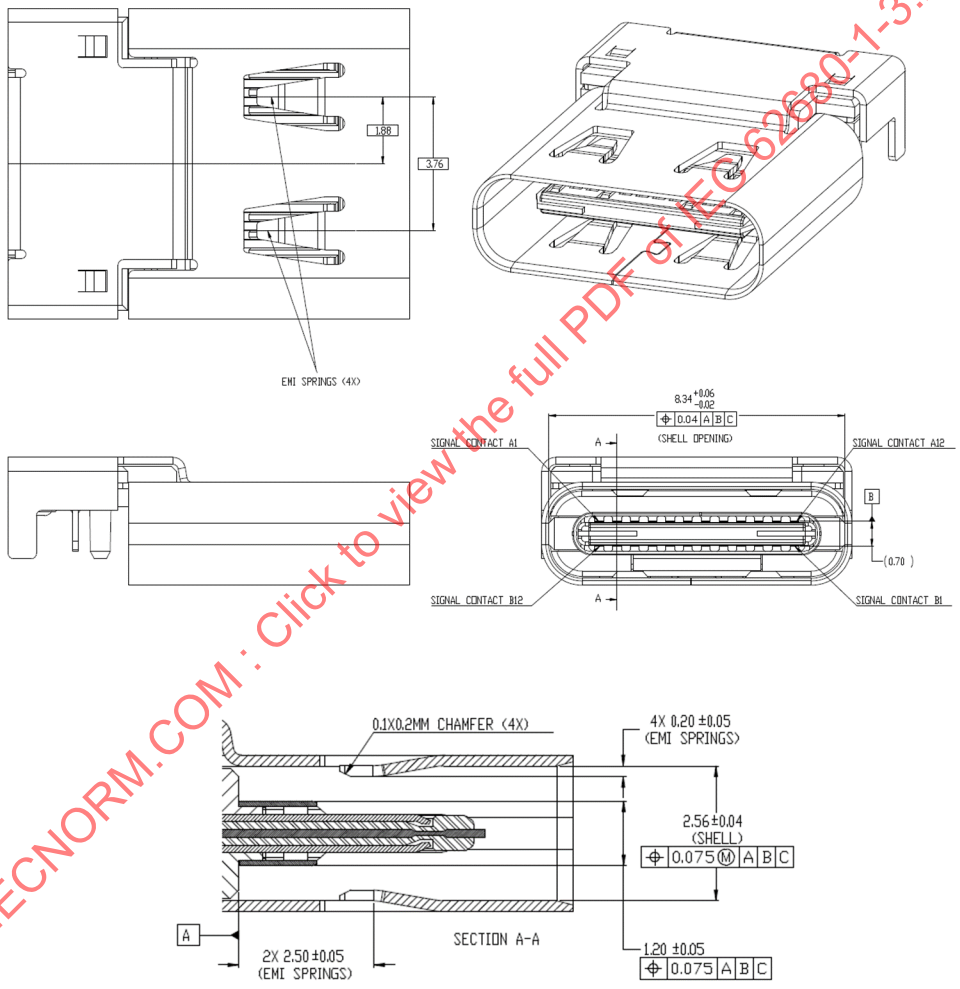
Anglais	Français
Both sides	Des deux côtés
Section A-A	Coupe A-A
Material thickness	Épaisseur du matériau
2x, ground plates to be laser welded to exterior shell	2x, plans de masse à souder par laser à l'enveloppe externe
Section B-B	Coupe B-B
Surface to be laser welded to receptacle shell	Surface à souder par laser à l'enveloppe de l'embase

Anglais	Français
Surface to plug GND springs	Ressorts GND entre la surface et la fiche

3.2.2.4 Ressorts CEM externes facultatifs d'une embase (*informatifs*)

Certaines applications ***peuvent*** utiliser des embases équipées de ressorts CEM qui sont en contact avec la partie externe de l'enveloppe de la fiche. La Figure 3-19 représente un schéma de référence d'une embase équipée de ressorts CEM externes. Les zones de contact du ressort CEM à l'état complètement couplé sont ***normatives*** et définies en 3.2.1.

Figure 3-19 Schéma de référence d'une embase USB Type-C équipée de ressorts CEM externes



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Anglais	Français
EMI springs	Ressorts EMI
Signal contact A1	Contact de signal A1
Signal contact B12	Contact de signal B12
Signal contact B1	Contact de signal B1

Anglais	Français
Signal contact A12	Contact de signal A12
Shell opening	Ouverture de l'enveloppe
Chamfer (x4)	Chanfrein (x4)
Section A-A	Coupe A-A
(Shell)	(enveloppe)

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3.2.2.5 Carte d'accès d'une fiche USB Type-C Complète (*informative*)

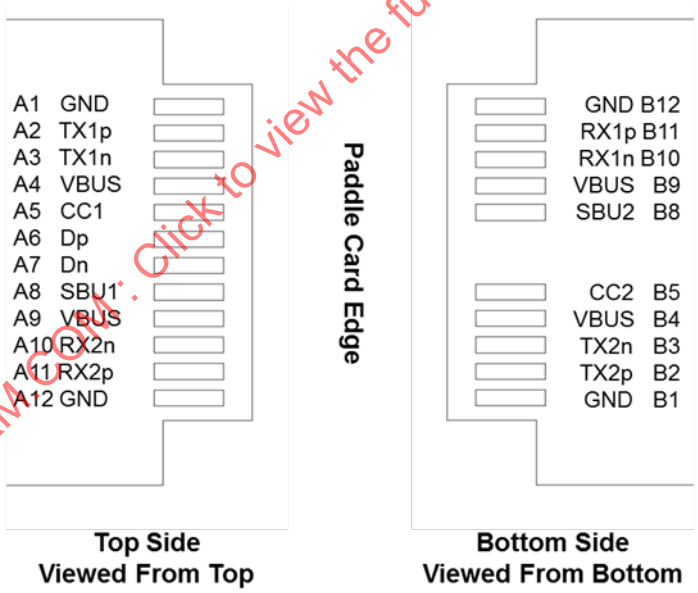
L'utilisation d'une carte d'accès est prévue dans la fiche USB Type-C Complète.

Figure 3-20 représente l'affectation des broches de la carte d'accès et l'emplacement de connexion du ressort de contact d'une fiche USB Type-C Complète. Les lignes directrices suivantes s'appliquent à la conception de la carte d'accès:

- ***il convient que*** la carte d'accès utilise un matériau de substrat hautes performances. ***Il convient*** d'appliquer une tolérance inférieure ou égale à ± 10 % sur l'épaisseur recommandée de la carte d'accès;
- ***il convient que*** les pistes USB RX soient aussi courtes que possible et possèdent une impédance caractéristique différentielle nominale de 85 Ω;
- ***il convient que*** le raccordement filaire possède deux paires différentielles à grande vitesse d'un côté et deux autres paires différentielles à grande vitesse de l'autre côté, aussi éloignées que possible l'une de l'autre, dans les limites admises en pratique;
- il est recommandé de choisir un guide d'ondes coplanaire (CPWG, *Coplanar Waveguide*) mis à la masse en tant que méthode de ligne de transmission;
- ***il convient de*** réduire le plus possible l'emploi de liaisons;
- ***il convient de*** connecter en bus les broches VBUS ensemble sur la carte d'accès;
- ***il convient de*** connecter en bus les broches GND ensemble sur la carte d'accès.

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Figure 3-20 Conception de référence de la carte d'accès d'une fiche USB Type-C Complète



Anglais	Français
Paddle Card Edge	Arête de la carte d'accès
Top Side Viewed From Top	Vue latérale de dessus
Bottom Side Viewed From Bottom	Vue latérale de dessous

3.2.3 Affectation des broches et descriptions

L'utilisation et l'affectation des 24 broches de l'interface de l'embase USB Type-C sont définies dans le Tableau 3-4.

Tableau 3-4 Affectation des broches de l'interface d'une embase USB Type-C

Broche	Nom du signal	Description	Séquence de couplage	Broche	Nom du signal	Description	Séquence de couplage
A1	GND	Retour à la masse	En premier	B12	GND	Retour à la masse	En premier
A2	TXp1	Moitié positive de la première paire différentielle TX	En second	B11	RXp1	Moitié positive de la première paire différentielle RX	En second
A3	TXn1	Moitié négative de la première paire différentielle TX	En second	B10	RXn1	Moitié négative de la première paire différentielle RX	En second
A4	VBUS	Alimentation de bus	En premier	B9	VBUS	Alimentation de bus	En premier
A5	CC1	Canal de configuration	En second	B8	SBU2	Utilisation en bande latérale (SBU)	En second
A6	Dp1	Moitié positive de la paire différentielle ***USB 2.0*** – Position 1	En second	B7	Dn2	Moitié négative de la paire différentielle ***USB 2.0*** – Position 2	En second
A7	Dn1	Moitié négative de la paire différentielle ***USB 2.0*** – Position 1	En second	B6	Dp2	Moitié positive de la paire différentielle ***USB 2.0*** – Position 2	En second
A8	SBU1	Utilisation en bande latérale (SBU)	En second	B5	CC2	Canal de configuration	En second
A9	VBUS	Alimentation de bus	En premier	B4	VBUS	Alimentation de bus	En premier
A10	RXn2	Moitié négative de la seconde paire différentielle RX	En second	B3	TXn2	Moitié négative de la seconde paire différentielle TX	En second
A11	RXp2	Moitié positive de la seconde paire différentielle RX	En second	B2	TXp2	Moitié positive de la seconde paire différentielle TX	En second
A12	GND	Retour à la masse	En premier	B1	GND	Retour à la masse	En premier

Notes:

1. Il ***convient*** que les contacts B6 et B7 ***ne*** soient ***pas*** présents dans la fiche USB Type-C. La face latérale de l'embase ***doit*** prendre en charge la paire différentielle ***USB 2.0*** présente sur Dp1/Dn1 ou Dp2/Dn2. L'orientation de la fiche détermine la paire active. Dans une mise en œuvre, Dp1 et Dp2 ***peuvent*** être court-circuités sur l'hôte/le dispositif aussi près de l'embase que possible, afin de réduire le plus possible la longueur de broche; Dn1 et Dn2 ***peuvent*** également être court-circuités. Il ***convient*** que la longueur maximale de court-circuit de la piste ne dépasse ***pas*** 3,5 mm.
2. Toutes les broches VBUS ***doivent*** être connectées ensemble à l'intérieur de la fiche USB Type-C et ***doivent*** être connectées au niveau de l'embase USB Type-C, lorsque cette dernière est à l'état monté (par exemple, toutes les broches VBUS connectées en bus ensemble sur la carte à circuits imprimés).
3. Toutes les broches de retour à la masse ***doivent*** être connectées ensemble à l'intérieur de la fiche USB Type-C et au niveau de l'embase USB Type-C, lorsque cette dernière est à l'état monté (par exemple, toutes les broches de retour à la masse connectées en bus ensemble sur la carte à circuits imprimés).
4. Si les dimensions de contact représentées en COUPE ALTERNATIVE A-A à la Figure 3-1 sont utilisées, les contacts VBUS (A4, A9, B4 et B9) sont couplés alors dans un deuxième temps, puis les contacts de signal (A2, A3, A5, A6, A7, A8, A10, A11, B2, B3, B5, B6, B7, B8, B10 et B11) en troisième position.

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L'utilisation et l'affectation des signaux nécessaires pour la prise en charge de l'***USB 2.0*** uniquement avec l'interface de couplage USB Type-C sont définies dans le Tableau 3-5.

Tableau 3-5 Affectation des broches de l'interface d'une embase USB Type-C pour la prise en charge d'*USB 2.0* uniquement

Broche	Nom du signal	Description	Séquence de couplage	Broche	Nom du signal	Description	Séquence de couplage
A1	GND	Retour à la masse	En premier	B12	GND	Retour à la masse	En premier
A2				B11			
A3				B10			
A4	VBUS	Alimentation de bus	En premier	B9	VBUS	Alimentation de bus	En premier
A5	CC1	Canal de configuration	En second	B8	SBU2	Utilisation en bande latérale (SBU)	En second
A6	Dp1	Moitié positive de la paire différentielle ***USB 2.0*** – Position 1	En second	B7	Dn2	Moitié négative de la paire différentielle ***USB 2.0*** – Position 2	En second
A7	Dn1	Moitié négative de la paire différentielle ***USB 2.0*** – Position 1	En second	B6	Dp2	Moitié positive de la paire différentielle ***USB 2.0*** – Position 2	En second
A8	SBU1	Utilisation en bande latérale (SBU)	En second	B5	CC2	Canal de configuration	En second
A9	VBUS	Alimentation de bus	En premier	B4	VBUS	Alimentation de bus	En premier
A10				B3			
A11				B2			
A12	GND	Retour à la masse	En premier	B1	GND	Retour à la masse	En premier

Notes:

1. Les emplacements de contact inutilisés ***doivent*** être isolés électriquement des contacts d'alimentation, de masse ou de signal (à savoir non connectés).
2. Il ***convient*** que les contacts B6 et B7 ***ne*** soient ***pas*** présents dans la fiche USB Type-C. La face latérale de l'embase ***doit*** prendre en charge la paire différentielle ***USB 2.0*** présente sur Dp1/Dn1 ou Dp2/Dn2. L'orientation de la fiche détermine la paire active. Dans une mise en œuvre, Dp1 et Dp2 ***peuvent*** être court-circuités sur l'hôte/le dispositif aussi près de l'embase que possible, afin de réduire le plus possible la longueur de broche; Dn1 et Dn2 ***peuvent*** également être court-circuités. Il ***convient*** que la longueur maximale de court-circuit de la piste ne dépasse ***pas*** 3,5 mm.
3. Les contacts A8 et B8 (SBU1 et SBU2) ***ne doivent pas*** être connectés, sauf si cela est exigé dans un but précis.
4. Toutes les broches VBUS ***doivent*** être connectées ensemble à l'intérieur de la fiche USB Type-C et ***doivent*** être connectées au niveau de l'embase USB Type-C, lorsque cette dernière est à l'état monté (par exemple, toutes les broches VBUS connectées en bus ensemble sur la carte à circuits imprimés).
5. Toutes les broches de retour à la masse ***doivent*** être connectées ensemble à l'intérieur de la fiche USB Type-C et au niveau de l'embase USB Type-C, lorsque cette dernière est à l'état monté (par exemple, toutes les broches de retour à la masse connectées en bus ensemble sur la carte à circuits imprimés).
6. Si les dimensions de contact représentées en COUPE ALTERNATIVE A-A de la Figure 3-1 sont utilisées, les contacts VBUS (A4, A9, B4 et B9) sont couplés alors dans un deuxième temps, puis les contacts de signal (A5, A6, A7, A8, B5, B6, B7 et B8) en troisième position.

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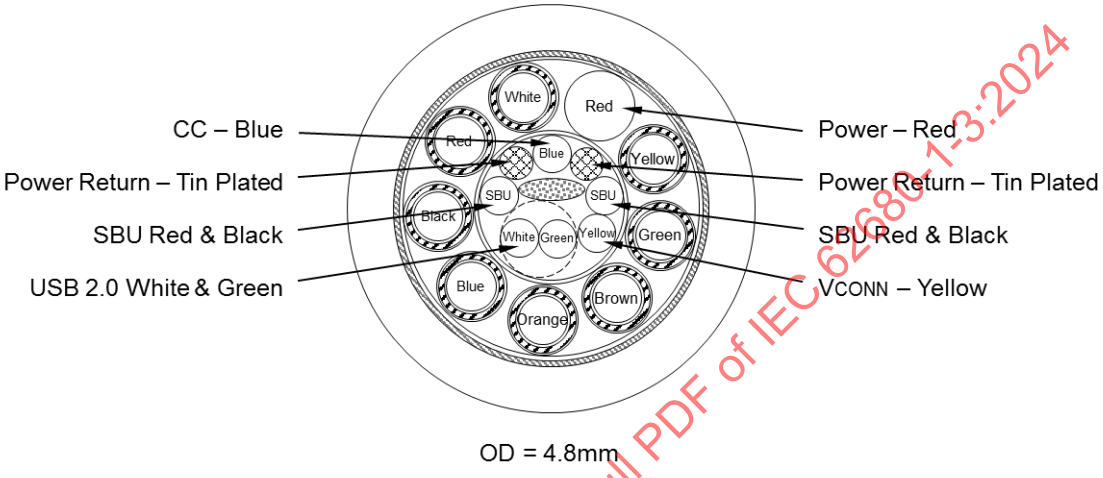
3.3 Construction des câbles et affectation des fils

Le présent paragraphe traite des câbles USB Type-C, notamment de leur construction, de l'affectation des fils et des calibres de fil.

3.3.1 Construction des câbles (*informative*)

La Figure 3-21 représente un exemple de coupe d'un câble USB Type-C Complet, avec des fils microcoaxiaux pour les paires TX/RX. Il existe quatre groupes de fils: USB D+/D− (généralement des paires torsadées non écrantées (UTP)), paires de signaux TX/RX (fils coaxiaux, fils coaxiaux doubles ou paires torsadées écrantées), fils de signal en bande latérale et fils d'alimentation et de masse. Dans cet exemple, le fil VCONN ***facultatif*** est représenté, alors que dans la Figure 3-22, le fil VCONN n'apparaît pas: cela dépend de l'approche de mise en œuvre choisie pour les câbles avec marquage électronique (voir 4.9).

Figure 3-21 Représentation d'une coupe d'un câble USB Type-C Complet; exemple de fil coaxial avec VCONN

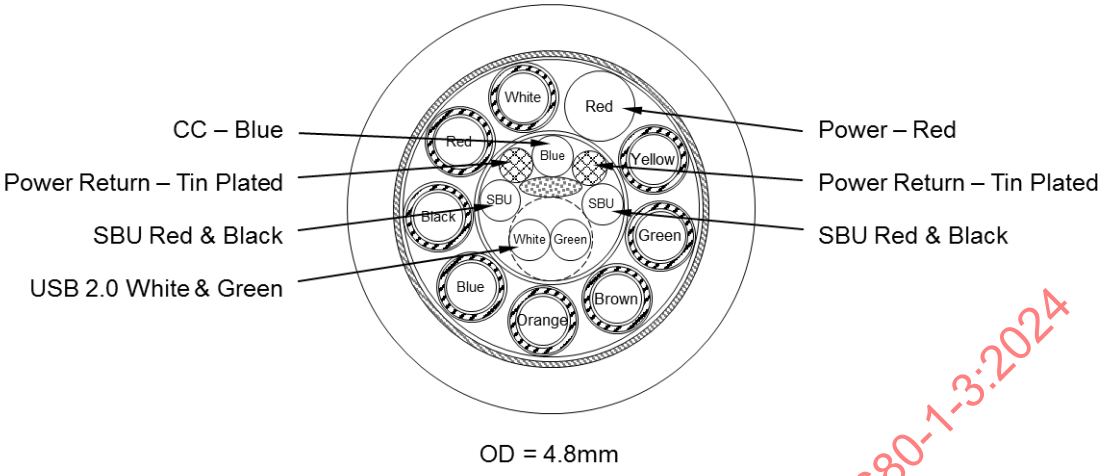


Anglais	Français
CC – Blue	CC – bleu
Power – Red	Alimentation – rouge
Power Return – Tin Plated	Retour d'alimentation – plaqué étain
SBU Red & Black	SBU rouge et noir
USB 2.0 White & Green	USB 2.0 blanc et vert
VCONN – Yellow	VCONN – jaune
OD = 4.8 mm	Diamètre extérieur = 4,8 mm

Les fils coaxiaux sont des paires TX/RX; ces paires spécifiques ne sont pas définies dans le câble.

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Figure 3-22 Représentation d'une coupe d'un câble USB Type-C Complet; exemple de fil coaxial sans VCONN



Anglais	Français
CC – Blue	CC – bleu
Power – Red	Alimentation – rouge
Power Return – Tin Plated	Retour d'alimentation – plaqué étain
SBU Red & Black	SBU rouge et noir
USB 2.0 White & Green	USB 2.0 blanc et vert
OD = 4.8 mm	Diamètre extérieur = 4,8 mm

Les fils coaxiaux sont des paires TX/RX; ces paires spécifiques ne sont pas définies dans le câble.

Il est prévu que la paire de signaux USB D+/D– transmette les signaux ***USB 2.0*** à basse vitesse, à vitesse intégrale et à grande vitesse, alors que les paires de signaux TX/RX sont utilisées pour transmettre les signaux ***USB 3.2*** ou ***USB4***. L'écrantage est nécessaire pour les paires différentielles TX/RX afin d'assurer l'intégrité des signaux et les performances CEM.

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3.3.2 Affectation des fils

Le Tableau 3-6 décrit l'ensemble complet des fils possibles nécessaires à la production des ensembles câble-connecteurs USB Type-C normalisés. Pour certains ensembles câble-connecteurs, tous ces fils ne sont pas utilisés. Par exemple, un câble USB Type-C qui ne fournit que la fonctionnalité ***USB 2.0*** n'inclut pas les fils 6 à 15.

Tableau 3-6 Affectation des fils pour un câble USB Type-C normalisé

Numéro de fil	Nom du signal	Description
1	GND_PWRrt1	Masse pour le retour à l'alimentation
2	PWR_VBUS1	Alimentation de la VBUS
3	CC	Canal de configuration
4	UTP_Dp	Paire torsadée non écrantée, positive
5	UTP_Dn	Paire torsadée non écrantée, négative
6	SDPp1	Paire différentielle écrantée n° 1, positive
7	SDPn1	Paire différentielle écrantée n° 1, négative
8	SDPp2	Paire différentielle écrantée n° 2, positive
9	SDPn2	Paire différentielle écrantée n° 2, négative
10	SDPp3	Paire différentielle écrantée n° 3, positive
11	SDPn3	Paire différentielle écrantée n° 3, négative
12	SDPp4	Paire différentielle écrantée n° 4, positive
13	SDPn4	Paire différentielle écrantée n° 4, négative
14	SBU_A	Utilisation en bande latérale
15	SBU_B	Utilisation en bande latérale
16	GND_PWRrt2	Masse pour le retour à l'alimentation (***facultative***)
17	PWR_VBUS2	Alimentation de la VBUS (***facultative***)
18	PWR_VCONN	Alimentation de VCONN (***facultative***, voir 4.9)
Tresse	Blindage	Tresse externe du câble

Note:

1. Ce tableau prend pour hypothèse que l'ensemble des SDP utilisent des fils coaxiaux et qu'il n'existe pas de fil de continuité. Le retour à la masse du signal passe par l'écrantage des fils coaxiaux. Si des paires coaxiales doubles ou torsadées écrantées sont utilisées, des fils de continuité sont alors nécessaires.

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Le Tableau 3-7 décrit l'ensemble complet des fils possibles nécessaires à la production des ensembles câble-connecteurs USB Type-C vers existant. Pour certains ensembles câble-connecteurs, tous ces fils ne sont pas nécessaires. Par exemple, un câble USB Type-C vers ***USB 2.0*** Standard-B n'inclut pas les fils 5 à 10.

Tableau 3-7 Affectation des fils d'un câble USB Type-C pour les câbles/adaptateurs existants

Numéro de fil	Nom du signal	Description
1	GND_PWRrt1	Masse pour le retour à l'alimentation
2	PWR_VBUS1	Alimentation de la VBUS
3	UTP_Dp	Paire torsadée non écrantée, positive
4	UTP_Dn	Paire torsadée non écrantée, négative
5	SDPp1	Paire différentielle écrantée n° 1, positive
6	SDPn1	Paire différentielle écrantée n° 1, négative
7	SDP1_Drain	Fil de continuité pour SDPp1 et SDPn1
8	SDPp2	Paire différentielle écrantée n° 2, positive
9	SDPn2	Paire différentielle écrantée n° 2, négative
10	SDP2_Drain	Fil de continuité pour SDPp2 et SDPn2
Tresse	Blindage	Tresse externe du câble

Note:
1. Ce tableau prend pour hypothèse qu'une paire torsadée écrantée est utilisée pour l'ensemble des SDP et qu'il existe des fils de continuité. Si des fils coaxiaux sont utilisés, aucun fil de continuité n'est alors nécessaire, et le retour à la masse du signal passe par l'écrantage des fils coaxiaux.

3.3.3 Calibres de fil et diamètres de câble (*informatifs*)

La présente spécification ne spécifie pas le calibre des fils. Le Tableau 3-8 et le Tableau 3-9 répertorient les calibres de fil classiques à titre de référence uniquement. Un fil de grand calibre entraîne moins de perte, mais au détriment du diamètre de câble et de la souplesse. Plusieurs fils ***peuvent*** être utilisés pour un seul fil, comme pour VBUS ou le fil de masse par exemple. Il est recommandé d'utiliser les plus petits calibres de fil possible qui satisfont aux exigences électriques et mécaniques des ensembles câble-connecteurs.

Pour optimiser la souplesse du câble, ***il convient de*** câbler l'ensemble des fils et ***il convient de*** réduire le plus possible le diamètre externe du câble. Un diamètre externe de câble USB Type-C Complet classique ***peut*** être compris entre 4 mm et 6 mm, alors qu'un diamètre externe de câble ***USB 2.0*** Type-C classique peut être compris entre 2 mm et 4 mm. Un diamètre externe classique de câble USB Type-C vers ***USB 3.1*** existant ***peut*** être compris entre 3 mm et 5 mm.

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Tableau 3-8 Calibres de fil de référence pour les ensembles câble-connecteurs USB Type-C normalisés

Numéro de fil	Nom du signal	Calibre de fil (AWG)
1	GND_PWRrt1	20-28
2	PWR_VBUS1	20-28
3	CC	32-34
4	UTP_Dp	28 à 34
5	UTP_Dn	28 à 34
6	SDPp1	26 à 34
7	SDPn1	26 à 34
8	SDPp2	26 à 34
9	SDPn2	26 à 34
10	SDPp3	26 à 34
11	SDPn3	26 à 34
12	SDPp4	26 à 34
13	SDPn4	26 à 34
14	SBU_A	32-34
15	SBU_B	32-34
16	GND_PWRrt2	20-28
17	PWR_VBUS2	20-28
18	PWR_VCONN	32-34

Tableau 3-9 Calibres de fil de référence pour les ensembles câble-connecteurs USB Type-C normalisés vers existant

Numéro de fil	Nom du signal	Calibre de fil (AWG)
1	GND_PWRrt1	20-28
2	PWR_VBUS1	20-28
3	UTP_Dp	28 à 34
4	UTP_Dn	28 à 34
5	SDPp1	26 à 34
6	SDPn1	26 à 34
7	SDP1_Drain	28 à 34
8	SDPp2	26 à 34
9	SDPn2	26 à 34
10	SDP2_Drain	28 à 34

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3.4 Ensembles câble-connecteurs USB Type-C normalisés

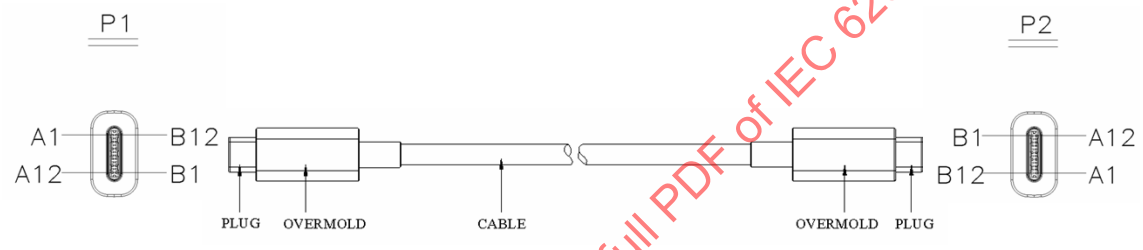
Deux ensembles câble-connecteurs USB Type-C normalisés sont définis et admis par la présente spécification. De plus, les câbles captifs sont admis (voir 3.4.3). L'écrantage (tresse) est exigé pour entourer l'ensemble des fils dans le câble USB Type-C. L'écran ***doit*** être branché aux enveloppes en métal de la fiche. ***Il convient de*** connecter physiquement l'écran à l'enveloppe en métal de la fiche sous un angle qui approche autant que possible les 360°, afin de contrôler la CEM.

Note: Jusqu'à la version 1.4 de la présente spécification, les signaux TX et RX utilisés étaient nommés SSTX et SSRX. Avec l'adoption de l'***USB4***, ces signaux ont été renommés afin qu'ils puissent s'appliquer de façon générique à la signalisation USB SuperSpeed comme à la signalisation ***USB4***. Il est prévu que les noms des signaux TX et RX soient un synonyme des noms SSTX et SSRX d'origine pour les mises en œuvre antérieures à la version 2.0 de la présente spécification.

3.4.1 Ensemble câble-connecteurs USB Type-C Complet

La Figure 3-23 représente un ensemble câble-connecteurs USB Type-C Complet normalisé.

Figure 3-23 Ensemble câble-connecteurs USB Type-C Complet normalisé



Anglais	Français
Plug	Fiche
Overmold	Surmoulage
Cable	Câble

Le Tableau 3-10 définit les connexions filaires de l'ensemble câble-connecteurs USB Type-C Complet normalisé.

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Tableau 3-10 Câblage de l'ensemble câble-connecteurs USB Type-C Complet normalisé

Fiche USB Type-C n° 1		Fil		Fiche USB Type-C n° 2	
Broche	**Nom du signal**	**Numéro de fil**	**Nom du signal**	**Broche**	**Nom du signal**
A1, B1, A12, B12	GND	1 [16]	GND_PWRrt1 [GND_PWRrt2]	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2 [17]	PWR_VBUS1 [PWR_VBUS2]	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (voir 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
A2	TXp1	6	SDPp1	B11	RXp1
A3	TXn1	7	SDPn1	B10	RXn1
B11	RXp1	8	SDPp2	A2	TXp1
B10	RXn1	9	SDPn2	A3	TXn1
B2	TXp2	10	SDPp3	A11	RXp2
B3	TXn2	11	SDPn3	A10	RXn2
A11	RXp2	12	SDPp4	B2	TXp2
A10	RXn2	13	SDPn4	B3	TXn2
A8	SBU1	14	SBU_A	B8	SBU2
B8	SBU2	15	SBU_B	A8	SBU1
Enveloppe	Blindage	Écrantage externe	Blindage	Enveloppe	Blindage

Notes:

1. Ce tableau prend pour hypothèse que l'ensemble des SDP utilisent des fils coaxiaux et qu'il n'existe pas de fil de continuité. L'écrantage des fils coaxiaux est connecté aux broches de masse. Si une paire torsadée écrantée est utilisée, des fils de continuité sont alors nécessaires et ***doivent*** être connectés aux broches GND.
2. La broche B5 (VCONN) de la fiche USB Type-C ***doit*** être utilisée dans les versions marquées électroniquement de ce câble. Voir 4.9.
3. Il ***convient*** que les contacts B6 et B7 ***ne*** soient ***pas*** présents dans la fiche USB Type-C.
4. Toutes les broches VBUS ***doivent*** être connectées ensemble dans la fiche USB Type-C. Un condensateur de découplage de 10 nF (tension assignée minimale recommandée de 30 V, 63 V si compatible EPR) est exigé pour la broche VBUS à chaque extrémité du câble complet. Il ***convient*** de placer le condensateur de découplage aussi près que possible de la plaque d'alimentation.
5. Toutes les broches GND ***doivent*** être connectées ensemble dans la fiche USB Type-C.
6. L'écran et la broche GND ***doivent*** être connectés dans la fiche USB Type-C aux deux extrémités de l'ensemble câble-connecteurs.

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3.4.1.1 Identification et certification du câble

Tous les ensembles câble-connecteurs USB Type-C Complets ***doivent*** comporter un marquage électronique et inclure des informations dans le marqueur électronique comme cela est défini dans la spécification ***USB PD***.

Il convient que tous les ensembles câble-connecteurs USB Type-C Complets soient certifiés et identifiés de manière visible par des icônes d'identification de câble certifiées, comme cela défini par l'***USB-IF***. Cela permet aux utilisateurs finaux d'être en mesure de confirmer visuellement les capacités fonctionnelles du câble en ce qui concerne la puissance assignée du câble, soit 60 W soit 240 W, et en ce qui concerne les performances de transmission de données du câble, par exemple 5 Gbit/s, 20 Gbit/s ou plus.

3.4.2 Ensemble câble-connecteurs *USB 2.0* Type-C

Un ensemble câble-connecteurs ***USB 2.0*** Type-C normalisé possède le même facteur de forme que celui représenté à la Figure 3-23.

Le Tableau 3-11 définit les connexions filaires de l'ensemble câble-connecteurs ***USB 2.0*** Type-C normalisé.

Tableau 3-11 Câblage de l'ensemble câble-connecteurs *USB 2.0* Type-C normalisé

Fiche USB Type-C n° 1		Fil		Fiche USB Type-C n° 2	
Broche	**Nom du signal**	**Numéro de fil**	**Nom du signal**	**Broche**	**Nom du signal**
A1, B1, A12, B12	GND	1 [16]	GND_PWRrt1 [GND_PWRrt2]	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2 [17]	PWR_VBUS1 [PWR_VBUS2]	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (voir 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
Enveloppe	Blindage	Écrantage externe	Blindage	Enveloppe	Blindage

Notes:

1. La broche B5 (VCONN) de la fiche USB Type-C ***doit*** être utilisée dans les versions marquées électroniquement de ce câble. Voir 4.9.
2. Il ***convient*** que les contacts B6 et B7 ***ne*** soient ***pas*** présents dans la fiche USB Type-C.
3. Toutes les broches VBUS ***doivent*** être connectées ensemble dans la fiche USB Type-C. Aucun condensateur de découplage n'est exigé pour la broche VBUS du câble ***USB 2.0*** Type-C.
4. Toutes les broches GND ***doivent*** être connectées ensemble dans la fiche USB Type-C.
5. Toutes les broches de la fiche USB Type-C qui ne sont pas répertoriées dans ce tableau ***doivent*** être ouvertes (non connectées).
6. L'écran et la broche GND ***doivent*** être connectés dans la fiche USB Type-C aux deux extrémités de l'ensemble câble-connecteurs.

3.4.2.1 Identification et certification du câble

Tous les ensembles câble-connecteurs câbles ***USB 2.0*** Type-C d'une puissance assignée supérieure à 3 A ***doivent*** comporter un marquage électronique et inclure des informations dans le marqueur électronique comme cela est défini dans la spécification ***USB PD***.

Il convient que tous les ensembles câble-connecteurs ***USB 2.0*** Type-C soient certifiés et identifiés de manière visible par des icônes d'identification de câble certifiées, comme cela est défini par l'***USB-IF***. Cela permet aux utilisateurs finaux d'être en mesure de confirmer visuellement les capacités fonctionnelles du câble en ce qui concerne la puissance assignée du câble, soit 60 W soit 240 W.

3.4.3 Ensemble câble-connecteurs captif USB Type-C

Un ensemble câble-connecteurs captif est un ensemble câble-connecteurs terminé à une extrémité par une fiche USB Type-C et qui comporte un moyen de connexion spécifique au fournisseur (câblé ou amovible personnalisé) à l'extrémité opposée. L'ensemble câble-connecteurs qui est câblé n'est pas détachable du dispositif.

Le câblage des ensembles câble-connecteurs captifs USB Type-C utilise les mêmes affectations de câbles que les ensembles câble-connecteurs normalisés (voir le Tableau 3-10 et le Tableau 3-11), à l'exception du branchement câblé côté dispositif qui remplace l'extrémité de la fiche USB Type-C n° 2.

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Le fil CC d'un câble captif ***doit*** être raccordé et avoir un comportement adapté à la fonction du produit pour lequel il est captif (par exemple, hôte ou dispositif).

Un dispositif (destinataire, UFP ou DRP) avec un ensemble câble-connecteurs captif ***doit*** répondre aux enquêtes d'identité de câble SOP' lorsque le dispositif reçoit une tension supérieure au courant de 3 A ou prend en charge l'opération ***USB4***. Le marqueur électronique peut se trouver physiquement dans le câble captif ou dans le dispositif contenant le câble.

La présente spécification ne définit pas la manière dont le branchement matériel est physiquement établi côté dispositif.

3.4.4 Ensemble USB Type-C

Un ensemble USB est un ensemble qui comporte une fiche USB Type-C qui est son interface USB principale. D'un point de vue fonctionnel, cet ensemble ne contient pas d'ensembles câble-connecteurs.

Un dispositif USB (destinataire, UFP ou DRP) ***doit*** répondre aux enquêtes d'identité de câble SOP' lorsqu'il reçoit une tension supérieure au courant de 3 A ou prend en charge l'opération ***USB4***.

3.5 Ensembles câble-connecteurs existants

Pour assurer l'interopérabilité entre les produits USB Type-C et les produits USB existants, les ensembles câble-connecteurs existants normalisés suivants sont définis. Seuls les câbles définis dans la présente spécification sont admis.

Les ensembles câble-connecteurs existants qui assurent l'alimentation d'un connecteur USB Type-C (par exemple, un ensemble câble-fiche USB Type-C vers USB Standard-A et un ensemble adaptateur-fiche USB Type-C vers embase USB Micro-B) doivent utiliser la résistance ***Rp*** de ***courant USB Type-C*** par défaut (56 kΩ). La valeur de ***Rp*** est utilisée pour informer le destinataire de la quantité de courant qui peut être fournie par la source. Étant donné que l'ensemble câble-connecteurs existant ne comprend pas la capacité de la source à laquelle il est connecté, il est uniquement admis d'annoncer le ***courant USB Type-C*** par défaut défini par les spécifications ***USB 2.0***, ***USB 3.1*** et ***USB BC 1.2***. Aucune autre valeur ***Rp*** n'est admise, car cela ***peut*** entraîner un destinataire USB Type-C à surcharger une alimentation existante.

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3.5.1 Ensemble câble-connecteurs USB Type-C vers *USB 3.1* Standard-A

La Figure 3-24 représente un ensemble câble-connecteurs USB Type-C vers ***USB 3.1*** Standard-A.

Figure 3-24 Ensemble câble-connecteurs USB Type-C vers *USB 3.1* Standard-A



Anglais	Français
Plug	Fiche
Overmold	Surmoulage
Cable	Câble
Pin	Broche

Le Tableau 3-12 définit les connexions filaires de l'ensemble câble-connecteurs USB Type-C vers ***USB 3.1*** Standard-A.

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Tableau 3-12 Câblage de l'ensemble câble-connecteurs USB Type-C vers *USB 3.1* Standard-A

Fiche USB Type-C		Fil		Fiche *USB 3.1* Standard-A	
Broche	**Nom du signal**	**Numéro de fil**	**Nom du signal**	**Broche**	**Nom du signal**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	Voir la Note 2			
B5	VCONN				
A6	Dp1	4	UTP_Dp	3	D+
A7	Dn1	5	UTP_Dn	2	D–
A2	TXp1	6	SDPp1	6	StdA_SSRX+
A3	TXn1	7	SDPn1	5	StdA_SSRX–
B11	RXp1	8	SDPp2	9	StdA_SSTX+
B10	RXn1	9	SDPn2	8	StdA_SSTX–
Enveloppe	Blindage	Écrantage externe	Blindage	Enveloppe	Blindage

Notes:

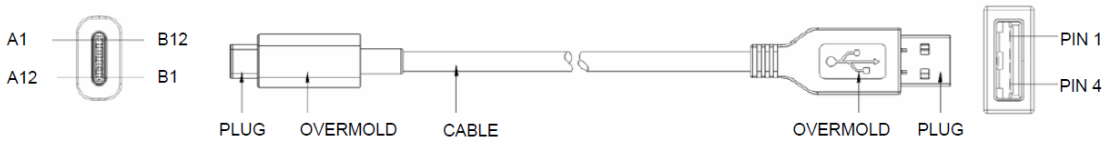
1. Ce tableau prend pour hypothèse qu'une paire torsadée écrantée est utilisée pour l'ensemble des SDP et qu'il existe des fils de continuité. Si des fils coaxiaux sont utilisés, aucun fil de continuité n'est présent et l'écrantage des fils coaxiaux est connecté aux broches de masse.
2. La broche A5 (CC) de la fiche USB Type-C ***doit*** être connectée à VBUS par une résistance ***Rp*** (56 kΩ ± 5 %). Pour obtenir une description fonctionnelle et la valeur de ***Rp***, voir 4.5.3.2.2 et le Tableau 4-27.
3. Il ***convient*** que les contacts B6 et B7 ***ne*** soient ***pas*** présents dans la fiche USB Type-C.
4. Toutes les broches VBUS ***doivent*** être connectées ensemble dans la fiche USB Type-C. Un condensateur de découplage est exigé entre les broches VBUS et de masse du côté fiche USB Type-C du câble. Le condensateur de découplage ***doit*** être de 10 nF ± 20 % dans les câbles qui intègrent une fiche USB Standard-A. Le condensateur de découplage ***doit*** être placé aussi près que possible de la plaque d'alimentation.
5. Toutes les broches de retour à la masse ***doivent*** être connectées ensemble dans la fiche USB Type-C.
6. L'écran et la broche GND ***doivent*** être connectés dans les fiches USB Type-C et ***USB 3.1*** Standard-A aux deux extrémités de l'ensemble câble-connecteurs.
7. Toutes les broches de la fiche USB Type-C qui ne sont pas répertoriées dans ce tableau ***doivent*** être ouvertes (non connectées).

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3.5.2 Ensemble câble-connecteurs USB Type-C vers *USB 2.0* Standard-A

La Figure 3-25 représente un ensemble câble-connecteurs USB Type-C vers ***USB 2.0*** Standard-A.

Figure 3-25 Ensemble câble-connecteurs USB Type-C vers *USB 2.0* Standard-A



Anglais	Français
Plug	Fiche
Overmold	Surmoulage
Cable	Câble
Pin	Broche

Le Tableau 3-13 définit les connexions filaires de l'ensemble câble-connecteurs USB Type-C vers ***USB 2.0*** Standard-A.

Tableau 3-13 Câblage de l'ensemble câble-connecteurs USB Type-C vers *USB 2.0* Standard-A

Fiche USB Type-C		Fil		Fiche *USB 2.0* Standard-A	
Broche	**Nom du signal**	**Numéro de fil**	**Nom du signal**	**Broche**	**Nom du signal**
A1, B1, A12, B12	GND	1	GND_PWRrt1	4	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	Voir la Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
Enveloppe	Blindage	Écrantage externe	Blindage	Enveloppe	Blindage

Notes:

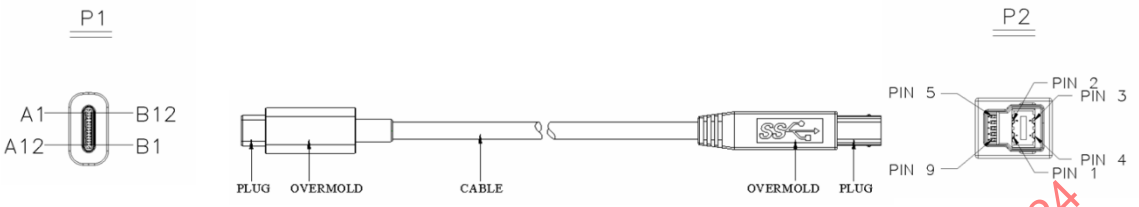
1. La broche A5 (CC) de la fiche USB Type-C ***doit*** être connectée à VBUS par une résistance ***Rp*** (56 kΩ ± 5 %). Pour obtenir une description fonctionnelle et la valeur de ***Rp***, voir 4.5.3.2.2 et le Tableau 4-27.
2. Il ***convient*** que les contacts B6 et B7 ***ne*** soient ***pas*** présents dans la fiche USB Type-C.
3. Toutes les broches VBUS ***doivent*** être connectées ensemble dans la fiche USB Type-C. Aucun condensateur de découplage n'est exigé pour les broches VBUS de ce câble.
4. Toutes les broches de retour à la masse ***doivent*** être connectées ensemble dans la fiche USB Type-C.
5. L'écran et la broche GND ***doivent*** être connectés dans les fiches USB Type-C et ***USB 2.0*** Standard-A aux deux extrémités de l'ensemble câble-connecteurs.
6. Toutes les broches de la fiche USB Type-C qui ne sont pas répertoriées dans ce tableau ***doivent*** être ouvertes (non connectées).

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3.5.3 Ensemble câble-connecteurs USB Type-C vers *USB 3.1* Standard-B

La Figure 3-26 représente un ensemble câble-connecteurs USB Type-C vers ***USB 3.1*** Standard-B.

Figure 3-26 Ensemble câble-connecteurs USB Type-C vers *USB 3.1* Standard-B



Anglais	Français
Plug	Fiche
Overmold	Surmoulage
Cable	Câble
Pin	Broche

Le Tableau 3-14 définit les connexions filaires de l'ensemble câble-connecteurs USB Type-C vers ***USB 3.1*** Standard-B.

Tableau 3-14 Câblage de l'ensemble câble-connecteurs USB Type-C vers *USB 3.1* Standard-B

Fiche USB Type-C		Fil		Fiche *USB 3.1* Standard-B	
Broche	**Nom du signal**	**Numéro de fil**	**Nom du signal**	**Broche**	**Nom du signal**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	Voir la Note 1			
B5	VCONN				
A6	Dp1	4	UTP_Dp	3	D+
A7	Dn1	5	UTP_Dn	2	D–
A2	TXp1	6	SDPp1	9	StdB_SSRX+
A3	TXn1	7	SDPn1	8	StdB_SSRX–
B11	RXp1	8	SDPp2	6	StdB_SSTX+
B10	RXn1	9	SDPn2	5	StdB_SSTX–
Enveloppe	Blindage	Écrantage externe	Blindage	Enveloppe	Blindage

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Notes:

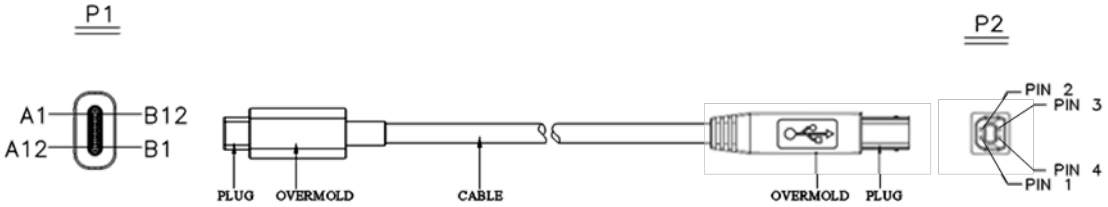
1. La broche A5 (CC) de la fiche USB Type-C ***doit*** être connectée à la broche GND par une résistance ***Rd*** (5,1 kΩ ± 20 %). Pour obtenir une description fonctionnelle et la valeur de ***Rd***, voir 4.5.3.2.1 et le Tableau 4-28.
2. Ce tableau prend pour hypothèse qu'une paire torsadée écrantée est utilisée pour l'ensemble des SDP et qu'il existe des fils de continuité. Si des fils coaxiaux sont utilisés, aucun fil de continuité n'est présent et l'écrantage des fils coaxiaux est connecté aux broches de masse.
3. Il ***convient*** que les contacts B6 et B7 ***ne*** soient ***pas*** présents dans la fiche USB Type-C.
4. Toutes les broches VBUS ***doivent*** être connectées ensemble dans la fiche USB Type-C. Un condensateur de découplage est exigé entre les broches VBUS et de masse du côté fiche USB Type-C du câble. Le condensateur de découplage ***doit*** être de 10 nF ± 20 % dans les câbles qui intègrent une fiche USB Standard-B. Le condensateur de découplage ***doit*** être placé aussi près que possible de la plaque d'alimentation.
5. Toutes les broches de retour à la masse ***doivent*** être connectées ensemble dans la fiche USB Type-C.
6. L'écran et la broche GND ***doivent*** être connectés dans les fiches USB Type-C et ***USB 3.1*** Standard-B aux deux extrémités de l'ensemble câble-connecteurs.
7. Toutes les broches de la fiche USB Type-C qui ne sont pas répertoriées dans ce tableau ***doivent*** être ouvertes (non connectées).

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3.5.4 Ensemble câble-connecteurs USB Type-C vers *USB 2.0* Standard-B

La Figure 3-27 représente un ensemble câble-connecteurs USB Type-C vers ***USB 2.0*** Standard-B.

Figure 3-27 Ensemble câble-connecteurs USB Type-C vers *USB 2.0* Standard-B



Anglais	Français
Plug	Fiche
Overmold	Surmoulage
Cable	Câble
Pin	Broche

Le Tableau 3-15 définit les connexions filaires de l'ensemble câble-connecteurs USB Type-C vers ***USB 2.0*** Standard-B.

Tableau 3-15 Câblage de l'ensemble câble-connecteurs USB Type-C vers *USB 2.0* Standard-B

Fiche USB Type-C		Fil		Fiche *USB 2.0* Standard-B	
Broche	**Nom du signal**	**Numéro de fil**	**Nom du signal**	**Broche**	**Nom du signal**
A1, B1, A12, B12	GND	1	GND_PWRrt1	4	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	Voir la Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
Enveloppe	Blindage	Écrantage externe	Blindage	Enveloppe	Blindage

Notes:

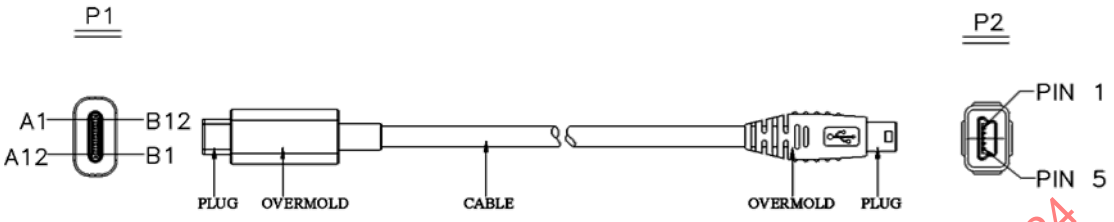
1. La broche A5 (CC) de la fiche USB Type-C ***doit*** être connectée à la broche GND par une résistance ***Rd*** (5,1 kΩ ± 20 %). Pour obtenir une description fonctionnelle et la valeur de ***Rd***, voir 4.5.3.2.1 et le Tableau 4-28.
2. Il ***convient*** que les contacts B6 et B7 ***ne*** soient ***pas*** présents dans la fiche USB Type-C.
3. Toutes les broches VBUS ***doivent*** être connectées ensemble dans la fiche USB Type-C. Aucun condensateur de découplage n'est exigé pour les broches VBUS de ce câble.
4. Toutes les broches de retour à la masse ***doivent*** être connectées ensemble dans la fiche USB Type-C.
5. L'écran et la broche GND ***doivent*** être connectés dans les fiches USB Type-C et ***USB 2.0*** Standard-B aux deux extrémités de l'ensemble câble-connecteurs.
6. Toutes les broches de la fiche USB Type-C qui ne sont pas répertoriées dans ce tableau ***doivent*** être ouvertes (non connectées).

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3.5.5 Ensemble câble-connecteurs USB Type-C vers *USB 2.0* Mini-B

La Figure 3-28 représente un ensemble câble-connecteurs USB Type-C vers ***USB 2.0*** Mini-B.

Figure 3-28 Ensemble câble-connecteurs USB Type-C vers *USB 2.0* Mini-B



Anglais	Français
Plug	Fiche
Overmold	Surmoulage
Cable	Câble
Pin	Broche

Le Tableau 3-16 définit les connexions filaires de l'ensemble câble-connecteurs USB Type-C vers ***USB 2.0*** Mini-B.

Tableau 3-16 Câblage de l'ensemble câble-connecteurs USB Type-C vers *USB 2.0* Mini-B

Fiche USB Type-C		Fil		Fiche *USB 2.0* Mini-B	
Broche	**Nom du signal**	**Numéro de fil**	**Nom du signal**	**Broche**	**Nom du signal**
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	Voir la Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
				4	ID
Enveloppe	Blindage	Écrantage externe	Blindage	Enveloppe	Blindage

Notes:

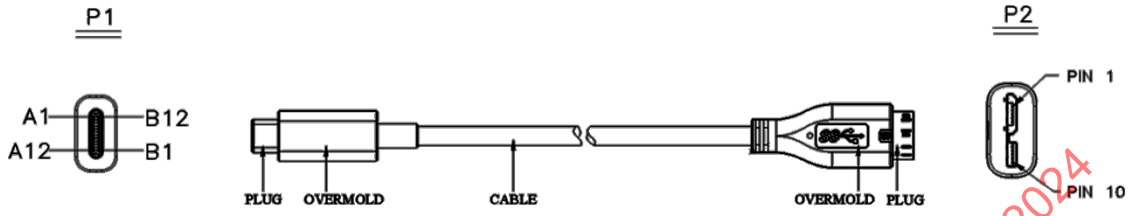
1. La broche A5 (CC) de la fiche USB Type-C ***doit*** être connectée à la broche GND par une résistance ***Rd*** (5,1 kΩ ± 20 %). Pour obtenir une description fonctionnelle et la valeur de ***Rd***, voir 4.5.3.2.1 et le Tableau 4-28.
2. Il ***convient*** que les contacts B6 et B7 ***ne*** soient ***pas*** présents dans la fiche USB Type-C.
3. Toutes les broches VBUS ***doivent*** être connectées ensemble dans la fiche USB Type-C. Aucun condensateur de découplage n'est exigé pour les broches VBUS de ce câble.
4. Toutes les broches de retour à la masse ***doivent*** être connectées ensemble dans la fiche USB Type-C.
5. La broche 4 (ID) de la fiche ***USB 2.0*** Mini-B ***doit*** être terminée, comme cela est défini dans la spécification applicable au type de câble.
6. L'écran et la broche GND ***doivent*** être connectés dans les fiches USB Type-C et ***USB 2.0*** Mini-B aux deux extrémités de l'ensemble câble-connecteurs.
7. Toutes les broches de la fiche USB Type-C qui ne sont pas répertoriées dans ce tableau ***doivent*** être ouvertes (non connectées).

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3.5.6 Ensemble câble-connecteurs USB Type-C vers USB 3.1 Micro-B

La Figure 3-29 représente un ensemble câble-connecteurs USB Type-C vers USB 3.1 Micro-B.

Figure 3-29 Ensemble câble-connecteurs USB Type-C vers USB 3.1 Micro-B



Anglais	Français
Plug	Fiche
Overmold	Surmoulage
Cable	Câble
Pin	Broche

Le Tableau 3-17 définit les connexions filaires de l'ensemble câble-connecteurs USB Type-C vers USB 3.1 Micro-B.

Tableau 3-17 Câblage de l'ensemble câble-connecteurs USB Type-C vers USB 3.1 Micro-B

Fiche USB Type-C		Fil		Fiche *USB 3.1* Micro-B	
Broche	**Nom du signal**	**Numéro de fil**	**Nom du signal**	**Broche**	**Nom du signal**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	5 8	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	Voir la Note 1			
B5	VCONN				
A6	Dp1	4	UTP_Dp	3	D+
A7	Dn1	5	UTP_Dn	2	D–
A2	TXp1	6	SDPp1	10	MicB_SSRX+
A3	TXn1	7	SDPn1	9	MicB_SSRX–
B11	RXp1	8	SDPp2	7	MicB_SSTX+
B10	RXn1	9	SDPn2	6	MicB_SSTX–
				4	ID
Enveloppe	Blindage	Écrantage externe	Blindage	Enveloppe	Blindage

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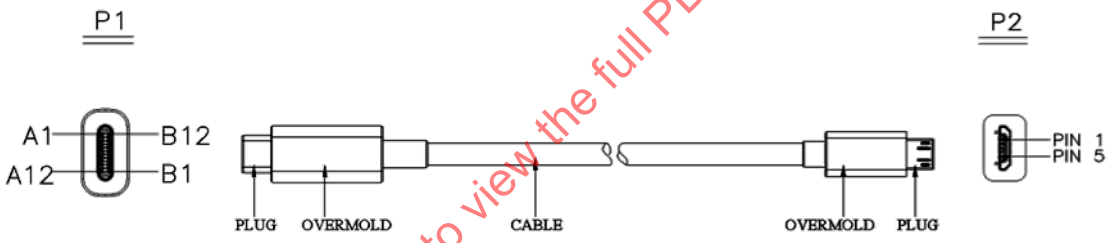
Notes:

1. La broche A5 (CC) de la fiche USB Type-C ***doit*** être connectée à la broche GND par une résistance ***Rd*** (5,1 kΩ ± 20 %). Pour obtenir une description fonctionnelle et la valeur de ***Rd***, voir 4.5.3.2.1 et le Tableau 4-28.
2. Ce tableau prend pour hypothèse qu'une paire torsadée écrantée est utilisée pour l'ensemble des SDP et qu'il existe des fils de continuité. Si des fils coaxiaux sont utilisés, aucun fil de continuité n'est présent et l'écrantage des fils coaxiaux est connecté aux broches de masse.
3. Il ***convient*** que les contacts B6 et B7 ***ne*** soient ***pas*** présents dans la fiche USB Type-C.
4. Toutes les broches VBUS ***doivent*** être connectées ensemble dans la fiche USB Type-C. Un condensateur de découplage est exigé entre les broches VBUS et de masse du côté fiche USB Type-C du câble. Le condensateur de découplage ***doit*** être de 10 nF ± 20 % dans les câbles qui intègrent une fiche USB Mini-B. Le condensateur de découplage ***doit*** être placé aussi près que possible de la plaque d'alimentation.
5. Toutes les broches de retour à la masse ***doivent*** être connectées ensemble dans la fiche USB Type-C.
6. La broche 4 (ID) de la fiche ***USB 3.1*** Micro-B ***doit*** être terminée comme cela est défini dans la spécification applicable au type de câble.
7. L'écrantage et la broche GND ***doivent*** être connectés dans les fiches USB Type-C et ***USB 3.1*** Micro-B aux deux extrémités de l'ensemble câble-connecteurs.
8. Toutes les broches de la fiche USB Type-C qui ne sont pas répertoriées dans ce tableau ***doivent*** être ouvertes (non connectées).

3.5.7 Ensemble câble-connecteurs USB Type-C vers USB 2.0 Micro-B

La Figure 3-30 représente un ensemble câble-connecteurs USB Type-C vers USB 2.0 Micro-B.

Figure 3-30 Ensemble câble-connecteurs USB Type-C vers USB 2.0 Micro-B



Anglais	Français
Plug	Fiche
Overmold	Surmoulage
Cable	Câble
Pin	Broche

Le Tableau 3-18 définit les connexions filaires de l'ensemble câble-connecteurs USB Type-C vers USB 2.0 Micro-B.

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Tableau 3-18 Câblage de l'ensemble câble-connecteurs USB Type-C vers USB 2.0 Micro-B

Fiche USB Type-C		Fil		Fiche *USB 2.0* Micro-B	
Broche	**Nom du signal**	**Numéro de fil**	**Nom du signal**	**Broche**	**Nom du signal**
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	Voir la Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
				4	ID
Enveloppe	Blindage	Écrantage externe	Blindage	Enveloppe	Blindage

Notes:

1. La broche A5 (CC) de la fiche USB Type-C ***doit*** être connectée à la broche GND par une résistance ***Rd*** (5,1 kΩ ± 20 %). Pour obtenir une description fonctionnelle et la valeur de ***Rd***, voir 4.5.3.2.1 et le Tableau 4-28.
2. Il ***convient*** que les contacts B6 et B7 ***ne*** soient ***pas*** présents dans la fiche USB Type-C.
3. Toutes les broches VBUS ***doivent*** être connectées ensemble dans la fiche USB Type-C. Aucun condensateur de découplage n'est exigé pour les broches VBUS de ce câble.
4. Toutes les broches de retour à la masse ***doivent*** être connectées ensemble dans la fiche USB Type-C.
5. La broche 4 (ID) de la fiche ***USB 2.0*** Micro-B ***doit*** être terminée comme cela est défini dans la spécification applicable au type de câble.
6. L'écrantage et la broche GND ***doivent*** être connectés dans les fiches USB Type-C et ***USB 2.0*** Micro-B aux deux extrémités de l'ensemble câble-connecteurs.
7. Toutes les broches de la fiche USB Type-C qui ne sont pas répertoriées dans ce tableau ***doivent*** être ouvertes (non connectées).

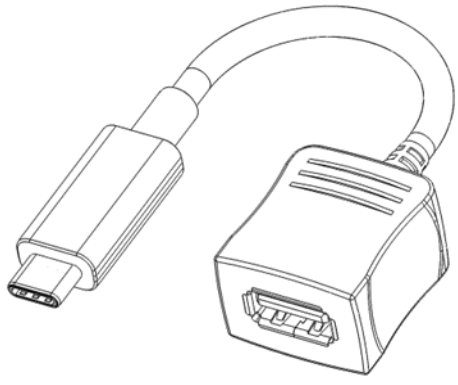
3.6 Ensembles adaptateurs existants

Pour assurer l'interopérabilité entre les produits USB Type-C et les produits USB existants, les ensembles adaptateurs existants normalisés suivants sont définis. Seuls les ensembles adaptateurs définis dans la présente spécification sont admis.

3.6.1 Ensemble adaptateur USB Type-C vers embase *USB 3.1* Standard-A

La Figure 3-31 représente un ensemble adaptateur USB Type-C vers embase ***USB 3.1*** Standard-A. Cet ensemble câble-connecteurs est défini pour une connexion directe à un dispositif USB (par exemple., une clé USB). La fonctionnalité système permettant d'utiliser cet ensemble adaptateur avec un autre ensemble câble-connecteurs USB n'est pas garantie.

Figure 3-31 Ensemble adaptateur USB Type-C vers embase *USB 3.1* Standard-A



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Le Tableau 3-19 définit les connexions filaires de l'ensemble adaptateur USB Type-C vers embase ***USB 3.1*** Standard-A.

Tableau 3-19 Câblage de l'ensemble adaptateur USB Type-C vers embase *USB 3.1* Standard-A

Fiche USB Type-C		Fil (facultatif – Voir la Note 7)		Embase *USB 3.1* Standard-A	
Broche	**Nom du signal**	**Numéro de fil**	**Nom du signal**	**Broche**	**Nom du signal**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	Voir la Note 1			
B5	VCONN				
A6	Dp1	4	UTP_Dp	3	D+
A7	Dn1	5	UTP_Dn	2	D–
A2	TXp1	6	SDPp1	9	StdB_SSTX+
A3	TXn1	7	SDPn1	8	StdB_SSTX–
B11	RXp1	8	SDPp2	6	StdB_SSRX+
B10	RXn1	9	SDPn2	5	StdB_SSRX–
Enveloppe	Blindage	Écrantage externe	Blindage	Enveloppe	Blindage

Notes:

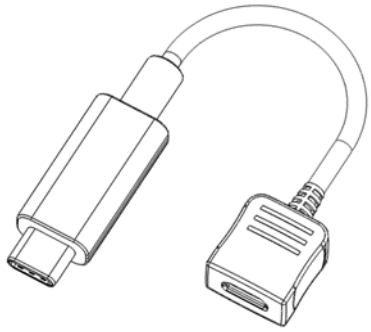
1. La broche A5 (CC) de la fiche USB Type-C ***doit*** être connectée à la broche GND par une résistance ***Rd*** (5,1 kΩ ± 20 %). Pour obtenir une description fonctionnelle et la valeur de ***Rd***, voir 4.5.3.2.1 et le Tableau 4-28.
2. Ce tableau prend pour hypothèse qu'une paire torsadée écrantée est utilisée pour l'ensemble des SDP et qu'il existe des fils de continuité. Si des fils coaxiaux sont utilisés, aucun fil de continuité n'est présent et l'écrantage des fils coaxiaux est connecté aux broches de masse.
3. Il ***convient*** que les contacts B6 et B7 ***ne*** soient ***pas*** présents dans la fiche USB Type-C.
4. Toutes les broches VBUS ***doivent*** être connectées ensemble dans la fiche USB Type-C. Un condensateur de découplage de 10 nF est exigé pour la broche VBUS à l'extrémité de la fiche USB Type-C du câble. Il ***convient*** de placer le condensateur de découplage aussi près que possible de la plaque d'alimentation. Aucun condensateur de découplage n'est exigé pour la broche VBUS dans l'embase Standard-A.
5. L'écran et la broche GND ***doivent*** être connectés dans la fiche USB Type-C et l'embase ***USB 3.1*** Standard-A aux deux extrémités de l'ensemble adaptateur.
6. Toutes les broches de la fiche USB Type-C qui ne sont pas répertoriées dans ce tableau ***doivent*** être ouvertes (non connectées).
7. Cet ensemble adaptateur ***peut*** ou ***peut ne pas*** comporter de câble entre la fiche USB Type-C et l'embase ***USB 3.1*** Standard-A. Les informations relatives aux fils sont fournies ici lorsqu'un câble fait partie de l'ensemble.

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3.6.2 Ensemble adaptateur USB Type-C vers embase *USB 2.0* Micro-B

La Figure 3-32 représente un ensemble adaptateur USB Type-C vers embase ***USB 2.0*** Micro-B.

Figure 3-32 Ensemble adaptateur USB Type-C vers embase *USB 2.0* Micro-B



Le Tableau 3-20 définit les connexions filaires de l'ensemble adaptateur USB Type-C vers embase ***USB 2.0*** Micro-B.

Tableau 3-20 Câblage de l'ensemble adaptateur USB Type-C vers embase *USB 2.0* Micro-B

Fiche USB Type-C		Fil (facultatif – Voir la Note 6)		Embase *USB 2.0* Micro-B	
Broche	**Nom du signal**	**Numéro de fil**	**Nom du signal**	**Broche**	**Nom du signal**
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	Voir la Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
				4	ID
Enveloppe	Blindage	Écrantage externe	Blindage	Enveloppe	Blindage

Notes:

1. La broche A5 (CC) de la fiche USB Type-C ***doit*** être connectée à VBUS par une résistance ***Rp*** (56 kΩ ± 5 %). Pour obtenir une description fonctionnelle et la valeur de ***Rp***, voir 4.5.3.2.2 et le Tableau 4-27.
2. Il ***convient*** que les contacts B6 et B7 ***ne*** soient ***pas*** présents dans la fiche USB Type-C.
3. Toutes les broches VBUS ***doivent*** être connectées ensemble dans la fiche USB Type-C. Aucun condensateur de découplage n'est exigé pour les broches VBUS à l'extrémité de l'embase Micro-B de ce câble.
4. L'écran et la broche GND ***doivent*** être connectés dans la fiche USB Type-C et l'embase ***USB 2.0*** Micro-B aux deux extrémités de l'ensemble adaptateur.
5. Toutes les broches de la fiche USB Type-C qui ne sont pas répertoriées dans ce tableau ***doivent*** être ouvertes (non connectées).
6. Cet ensemble adaptateur ***peut*** ou ***peut ne pas*** comporter de câble entre la fiche USB Type-C et l'embase ***USB 2.0*** Micro-B. Les informations relatives aux fils sont fournies ici lorsqu'un câble fait partie de l'ensemble.

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3.7 Caractéristiques électriques

Le présent paragraphe définit les exigences électriques des ensembles câble-connecteurs, des connecteurs et des câbles bruts USB Type-C, y compris les exigences relatives à l'intégrité du signal, à l'efficacité de l'écrantage et au courant continu. Le 3.11.1 définit les exigences complémentaires relatives à la définition du signal fonctionnel, à la découverte de la configuration de l'hôte ou du dispositif et à l'alimentation électrique.

Sauf spécification contraire, l'ensemble des mesurages est réalisé à une température de 15 °C à 35 °C, une humidité relative de 25 % à 85 %, et une pression atmosphérique de 86 kPa à 106 kPa. Tous les paramètres S sont normalisés avec une impédance différentielle de 85 Ω.

3.7.1 Câble brut (*informatif*)

Les objectifs de performance électrique des câbles bruts sont donnés à titre ***informatif*** pour aider les fabricants d'ensembles câble-connecteurs à gérer l'approvisionnement en câbles bruts. Ces objectifs ne relèvent pas des exigences de conformité de l'USB Type-C. À titre ***normatif***, il est exigé est que l'ensemble câble-connecteurs soit conforme aux caractéristiques de performance spécifiées en 3.7.2 et 3.7.5.3.

Il est recommandé que l'impédance caractéristique différentielle soit de 90 Ω ± 5 Ω pour les paires différentielles écrantées. Il est recommandé que l'impédance caractéristique asymétrique soit de 45 Ω ± 3 Ω pour les fils coaxiaux. ***Il convient*** d'évaluer l'impédance avec un temps de montée de 200 ps (10 % à 90 %). Un temps de montée supérieur n'est pas nécessaire pour un câble brut, car il fait ressortir les irrégularités du montage d'essai du câble.

3.7.1.1 Obliquité dans les paires (*informative*)

Il est recommandé que l'obliquité dans les paires d'une paire différentielle soit inférieure à 10 ps/m. ***Il convient de*** la mesurer avec une transmission dans le domaine temporel (TDT, *Time Domain Transmission*) en mode différentiel qui utilise un temps de montée de 200 ps (10 % à 90 %) et un croisement à 50 % de la tension d'entrée.

3.7.1.2 Perte d'insertion différentielle (*informative*)

L'affaiblissement du câble dépend des calibres de fil, du placage et des matériaux diélectriques. Le Tableau 3-21 et le Tableau 3-22 contiennent des exemples de perte d'insertion différentielle.

Tableau 3-21 Exemples de perte d'insertion différentielle pour USB TX/RX avec une construction en paire torsadée

Fréquence	34AWG	32AWG	30AWG	28AWG
0,625 GHz	−1,8 dB/m	−1,4 dB/m	−1,2 dB/m	−1,0 dB/m
1,25 GHz	−2,5 dB/m	−2,0 dB/m	−1,7 dB/m	−1,4 dB/m
2,50 GHz	−3,7 dB/m	−2,9 dB/m	−2,5 dB/m	−2,1 dB/m
5,00 GHz	−5,5 dB/m	−4,5 dB/m	−3,9 dB/m	−3,1 dB/m
7,50 GHz	−7,0 dB/m	−5,9 dB/m	−5,0 dB/m	−4,1 dB/m
10,00 GHz	−8,4 dB/m	−7,2 dB/m	−6,1 dB/m	−4,8 dB/m
12,50 GHz	−9,5 dB/m	−8,2 dB/m	−7,3 dB/m	−5,5 dB/m
15,00 GHz	−11,0 dB/m	−9,5 dB/m	−8,7 dB/m	−6,5 dB/m

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Tableau 3-22 Exemples de perte d'insertion différentielle pour USB TX/RX avec une construction coaxiale

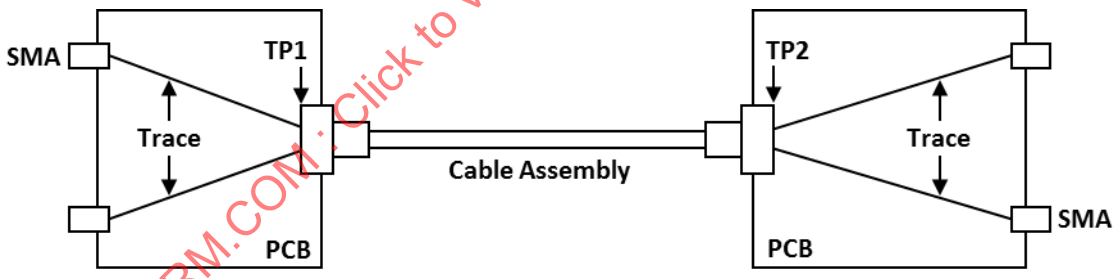
Fréquence	34AWG	32AWG	30AWG	28AWG
0,625 GHz	−1,8 dB/m	−1,5 dB/m	−1,2 dB/m	−1,0 dB/m
1,25 GHz	−2,8 dB/m	−2,2 dB/m	−1,8 dB/m	−1,3 dB/m
2,50 GHz	−4,2 dB/m	−3,4 dB/m	−2,7 dB/m	−1,9 dB/m
5,00 GHz	−6,1 dB/m	−4,9 dB/m	−4,0 dB/m	−3,1 dB/m
7,50 GHz	−7,6 dB/m	−6,5 dB/m	−5,2 dB/m	−4,2 dB/m
10,0 GHz	−8,8 dB/m	−7,6 dB/m	−6,1 dB/m	−4,9 dB/m
12,5 GHz	−9,9 dB/m	−8,6 dB/m	−7,1 dB/m	−5,7 dB/m
15,0 GHz	−12,1 dB/m	−10,9 dB/m	−9,0 dB/m	−6,5 dB/m

3.7.2 Ensembles câble-connecteurs passifs USB Type-C vers USB Type-C

Un ensemble câble-connecteurs USB Type-C vers Type-C ***doit*** être soumis à l'essai au moyen d'un montage d'essai avec la languette de l'embase fabriquée dans le montage d'essai. Ceci est représenté à la Figure 3-33. Les embases USB Type-C ne sont pas incluses dans le montage d'essai. ***Il convient que*** les hôtes et les dispositifs tiennent compte de la dégradation de signal supplémentaire induite par l'embase.

Les exigences s'appliquent à l'intégralité du chemin du signal de l'ensemble câble-connecteurs couplé aux languettes de CCI du montage, sans inclure les pistes CCI d'entrée. Comme cela est représenté à la Figure 3-33, le mesurage est réalisé entre le point d'essai 1 (TP1) et le point d'essai 2 (TP2). Pour obtenir une description d'un montage d'essai normalisé, se référer à la documentation disponible sur la page Cables and Connectors du site web de l'***USB-IF***.

Figure 3-33 Représentation des points d'essai pour un ensemble câble-connecteurs couplé



Anglais	Français
Cable Assembly	Ensemble câble-connecteurs
Trace	Piste

Les exigences relatives aux ensembles câble-connecteurs se divisent en exigences ***informatives*** et ***normatives***. Les exigences ***informatives*** sont destinées aux fabricants d'ensembles câble-connecteurs en tant qu'objectifs de conception. Les exigences ***normatives*** constituent les critères de réussite et d'échec à la conformité des ensembles câble-connecteurs.

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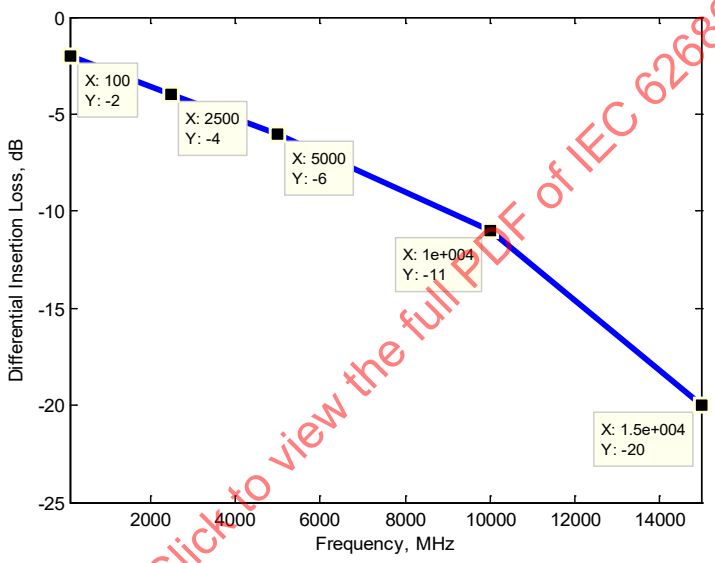
3.7.2.1 Caractéristiques recommandées pour les ensembles câble-connecteurs passifs TX/RX (*USB 3.2* Gen2 et *USB4* Gen2)

Les caractéristiques électriques recommandées définies dans le présent paragraphe sont des lignes directrices de conception ***informatives***. Les ensembles câble-connecteurs qui ne satisfont pas à ces caractéristiques électriques recommandées ***peuvent*** toutefois satisfaire aux essais de certification USB. De même, les ensembles câble-connecteurs conformes à ces caractéristiques électriques recommandées ***peuvent*** satisfaire ou ***peuvent ne pas*** satisfaire aux essais de certification USB.

3.7.2.1.1 Perte d'insertion différentielle (*Informative – USB 3.2* Gen2 et *USB4* Gen2)

La Figure 3-34 représente la limite de la perte d'insertion différentielle pour un ensemble câble-connecteurs ***USB 3.2*** Gen2 ou ***USB4*** Gen2 Type-C, définie par les valeurs maximales suivantes: (100 MHz, −2 dB), (2,5 GHz, −4 dB), (5,0 GHz, −6 dB), (10 GHz, −11 dB) et (15 GHz, −20 dB).

Figure 3-34 Exigence concernant la perte d'insertion différentielle recommandée (*USB 3.2* Gen2 et *USB4* Gen2)



Anglais	Français
Differential Insertion Loss	Perte d'insertion différentielle
Frequency	Fréquence

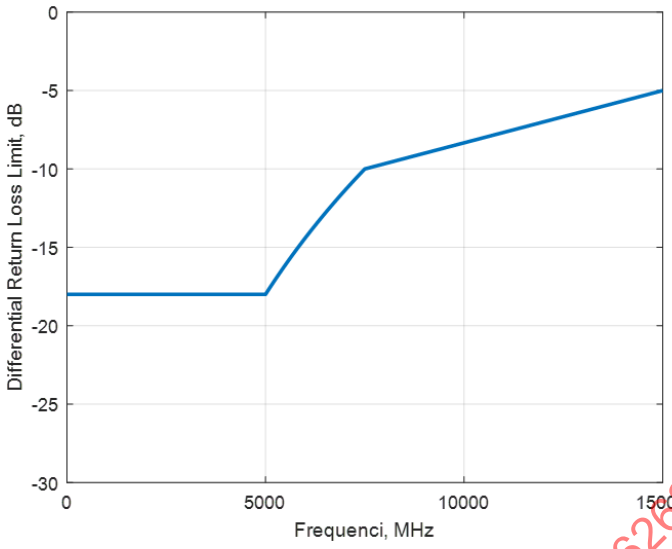
3.7.2.1.2 Facteur d'adaptation différentiel (*informatif – USB 3.2* Gen2 et *USB4* Gen2)

La Figure 3-35 représente la limite du facteur d'adaptation différentiel, définie par l'équation suivante:

$$Masque\ RL = \begin{cases} -18\ dB,\ f < 5\ Ghz \\ -18 + 45.43 \times \log_{10}\left(\frac{f}{5}\right)\ dB\ ,\ 5\ Ghz < f\ \leq 7.5\ Ghz \\ -15 + \frac{2}{3} \times f\ dB,\ 7.5\ Ghz < f \leq 15\ Ghz \end{cases}$$

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Figure 3-35 Exigence concernant le facteur d'adaptation différentiel recommandé

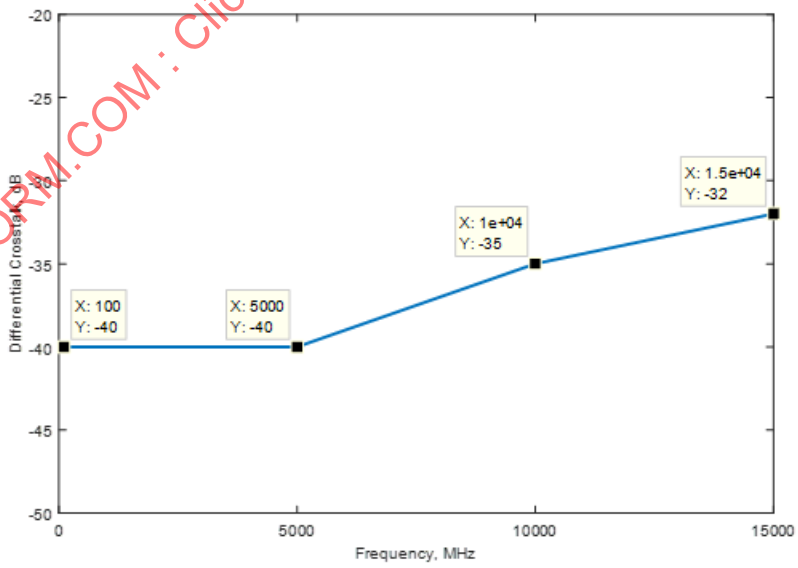


Anglais	Français
Differential Return Loss Limit	Limite du facteur d'adaptation différentiel
Frequency	Fréquence

3.7.2.1.3 Paradiaphonie et télédiaphonie différentielles entre les paires TX/RX (*informatives – USB 3.2* Gen2 et *USB4* Gen2)

La paradiaphonie (DDNEXT) et la télédiaphonie (DDFEXT) sont spécifiées, comme cela est représenté à la Figure 3-36. Les limites de DDNEXT/DDFEXT sont définies par les valeurs maximales suivantes: (100 MHz, −40 dB), (5 GHz, −40 dB), (10 GHz, −35 dB) et (15 GHz, −32 dB).

Figure 3-36 Exigence concernant la diaphonie différentielle recommandée



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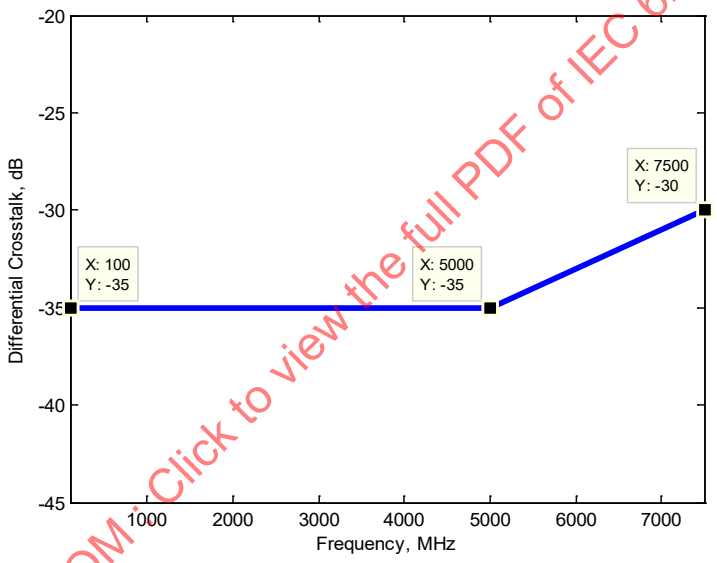
Anglais	Français
Differential Crosstalk	Diaphonie différentielle
Frequency	Fréquence

3.7.2.1.4 Diaphonie différentielle entre les paires USB D+/D− et TX/RX (*informative – USB 3.2* Gen2 et *USB4* Gen2)

Il convient de gérer la paradiaphonie et la télédiaphonie différentielles entre la paire USB D+/D− et les paires TX/RX afin qu'elle ne dépasse pas les limites représentées à la Figure 3-37. ***Il convient*** d'interpréter la paire USB D+/D− et les paires TX/RX dans le contexte d'un agresseur et d'une victime. ***Il convient*** également de prendre en compte le fait que la fréquence maximale de la paire D+/D− pour des essais similaires est de

1,2 GHz (voir le Tableau 3-31), mais dans ce cas, la diaphonie sur la paire D+/D− est étendue à 7,5 GHz. Les limites sont définies par les points suivants: (100 MHz, −35 dB), (5 GHz, −35 dB) et (7,5 GHz, −30 dB).

Figure 3-37 Exigence concernant la paradiaphonie et la télédiaphonie différentielles recommandées entre la paire USB D+/D− et les paires TX/RX



Anglais	Français
Differential Crosstalk	Diaphonie différentielle
Frequency	Fréquence

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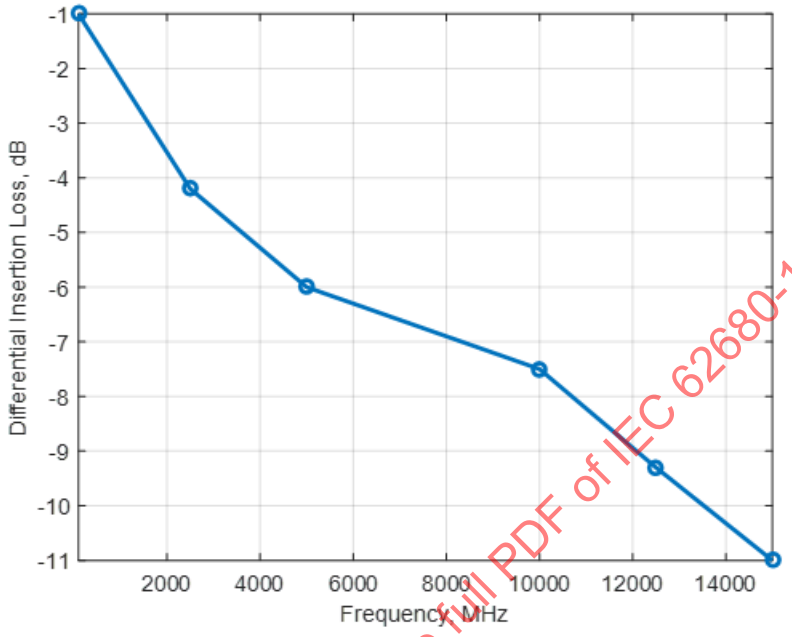
3.7.2.2 Caractéristiques recommandées pour les ensembles câble-connecteurs passifs TX/RX (*USB4* Gen3/Gen4)

Note: Bien que les caractéristiques recommandées du présent paragraphe soient définies en ***USB4*** Gen3, elles s'appliquent également aux ensembles câble-connecteurs passifs ***USB4*** Gen4 car ils sont électriquement équivalents aux ensembles câble-connecteurs passifs ***USB4*** Gen3.

3.7.2.2.1 Perte d'insertion différentielle (*informative – USB4* Gen3/Gen4)

La Figure 3-38 représente la limite de la perte d'insertion différentielle recommandée pour un ensemble câble-connecteurs ***USB4*** Gen3 Type-C, définie par les valeurs maximales suivantes: (100 MHz, −1 dB), (2,5 GHz, −4,2 dB), (5,0 GHz, −6 dB), (10 GHz, −7,5 dB), (12 GHz, −9,3 dB) et (15 GHz, −11 dB).

Figure 3-38 Exigence concernant la perte d'insertion différentielle recommandée (*USB4* Gen3/Gen4)



Anglais	Français
Differential Insertion Loss	Perte d'insertion différentielle
Frequency	Fréquence

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3.7.2.2.2 Facteur d'adaptation différentiel (*informatif – USB4* Gen3/Gen4)

Le masque du facteur d'adaptation différentiel ***informatif*** est identique à celui du 3.7.2.1.2.

3.7.2.2.3 Paradiaphonie et télédiaphonie différentielles entre les paires TX/RX (*informatives – USB4* Gen3/Gen4)

La paradiaphonie (DDNEXT) et la télédiaphonie (DDFEXT) recommandées sont définies au 3.7.2.1.3. Pour réduire le plus possible la diaphonie, il est important d'optimiser la conception de la carte d'accès et de la terminaison des fils à l'intérieur de la fiche de câble.

3.7.2.2.4 Diaphonie différentielle entre la paire USB D+/D− et les paires TX/RX (*informative – USB4* Gen3/Gen4)

La paradiaphonie et la télédiaphonie ***informatives*** entre la paire USB D+/D− et les paires TX/RX sont identiques à celles du 3.7.2.1.4.

3.7.2.3 Exigences *normatives* relatives à l'ensemble câble-connecteurs passif TX/RX pour *USB 3.2* Gen2 et *USB4* Gen2

Les paramètres intégrés sont utilisés pour la conformité de l'ensemble câble-connecteurs (sauf pour la perte d'insertion et la conversion du mode différentiel en mode commun) afin d'éviter un potentiel rejet d'un ensemble câble-connecteurs opérationnel qui ***peut*** ne pas être conforme à la spécification traditionnelle des paramètres S à certaines fréquences.

3.7.2.3.1 Ajustement de la perte d'insertion différentielle aux fréquences de Nyquist (*normatif – USB 3.2* Gen2 et *USB4* Gen2)

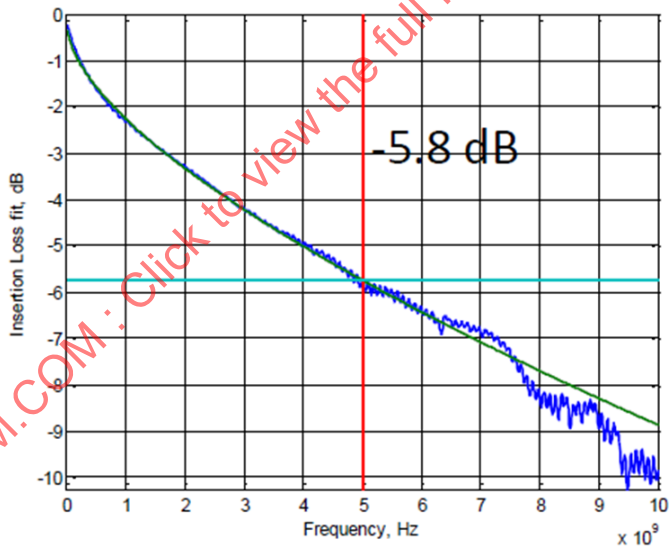
L'ajustement de la perte d'insertion à la fréquence de Nyquist mesure l'affaiblissement de l'ensemble câble-connecteurs. Pour obtenir l'ajustement de la perte d'insertion à la fréquence de Nyquist, la perte d'insertion différentielle mesurée pour l'ensemble câble-connecteurs est ajustée avec une fonction de lissage. Un algorithme et un outil d'ajustement normalisés ***doivent*** être utilisés pour extraire l'ajustement de la perte d'insertion aux fréquences de Nyquist. L'équation d'ajustement est définie comme suit:

$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3}$$

où f est la fréquence, et a, b, c et d sont les coefficients d'ajustement.

La Figure 3-39 représente un exemple de perte d'insertion, mesurée pour un ensemble câble-connecteurs, puis ajustée avec une fonction de lissage. L'ajustement de la perte d'insertion à la fréquence de Nyquist de l'USB SuperSpeed Gen2 (5,0 GHz) est de −5,8 dB.

Figure 3-39 Représentation de l'ajustement de la perte d'insertion à la fréquence de Nyquist



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Anglais	Français
Insertion Loss fit	Ajustement de la perte d'insertion
Frequency	Fréquence

L'ajustement de la perte d'insertion à la fréquence de Nyquist (ILfitatNq) ***doit*** satisfaire aux exigences suivantes:

- ≥ −4 dB à 2,5 GHz,

- ≥ –6 dB à 5 GHz, et
- ≥ –11 dB à 10 GHz.

Les fréquences de Nyquist sont respectivement de 2,5 GHz, 5,0 GHz et 10 GHz pour les débits de données USB SuperSpeed Gen1, USB SuperSpeed Gen2 et ***USB4*** Gen3.

3.7.2.3.2 Multiréflexion intégrée (*normative – USB 3.2* Gen2 et *USB4* Gen2)

L'écart de la perte d'insertion (ILD) est défini comme suit

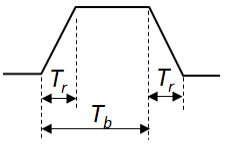
$$ILD(f) = IL(f) - ILfit(f)$$

Il mesure l'ondulation de la perte d'insertion, provoquée par les multiples réflexions à l'intérieur de l'ensemble câble-connecteurs (couplé au montage). L'intégration de *ILD(f)* est appelée "multiréflexion intégrée" (IMR, *Integrated Multi-Reflection*):

$$IMR = dB\left(\sqrt{\frac{\int_0^{fmax}|ILD(f)|^2|Vin(f)|^2df}{\int_0^{fmax}|Vin(f)|^2df}}\right)$$

où f_{max} = 12,5 GHz et *Vin(f)* est le spectre d'une impulsion trapézoïdale en entrée, défini à la Figure 3-40.

Figure 3-40 Spectre d'une impulsion en entrée



$$|V_{in}(f)| = \left|\frac{\sin(\pi f T_r)}{\pi f T_r} \cdot \frac{\sin(\pi f T_b)}{\pi f T_b}\right|$$

T_b=Unit interval=100 ps
T_r=0 to 100% rise time = 0.4T_b

Anglais	Français
Unit interval	Intervalle unitaire
0 to 100% rise time	0 % à 100 % du temps de montée

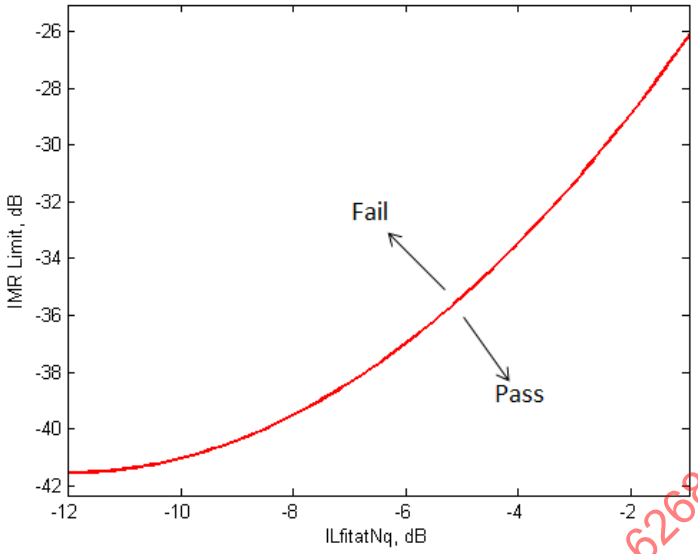
L'IMR dépend de ILfitatNq. Une valeur plus élevée d'IMR ***peut*** être tolérée lorsque ILfitatNq diminue. La limite IMR est spécifiée en fonction de ILfitatNq:

$$IMR \leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 23.392$$

Elle est représentée à la Figure 3-41.

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Figure 3-41 Limite IMR en fonction de ILfitatNq



Anglais	Français
IMR Limit	Limite d'IMR
Fail	Incorrecte
Pass	Correcte

3.7.2.3.3 Diaphonie intégrée entre les paires TX/RX (*normative – USB 3.2* Gen2 et *USB4* Gen2)

La diaphonie intégrée entre l'ensemble des paires TX/RX est calculée avec les équations suivantes:

$$INEXT = dB\left(\sqrt{\frac{\int_0^{f_{max}}(|Vin(f)|^2(|NEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2\,|NEXTd(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2 df}}\right)$$

$$IFEXT = dB\left(\sqrt{\frac{\int_0^{f_{max}}(|Vin(f)|^2(|FEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2\,|FEXTd(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2 df}}\right)$$

où *NEXT(f)*, *FEXT(f)* et *C2D(f)* correspondent respectivement à la paradiaphonie et à la télédiaphonie mesurées entre les paires TX/RX, et à la conversion du mode commun en mode différentiel. Le facteur de 0,1252 repose sur l'hypothèse que l'amplitude du mode commun correspond à 12,5 % de l'amplitude différentielle. *NEXTd(f)* et *FEXTd(f)* correspondent respectivement à la paradiaphonie et à la télédiaphonie entre la paire D+/D− et les paires TX/RX. *Vdd(f)* est le spectre d'impulsion en entrée, évalué au moyen de l'équation représentée à la Figure 3-40 avec Tb = 2,08 ns.

L'intégration ***doit*** être effectuée pour chaque NEXT et FEXT entre toutes les paires différentielles. Les valeurs les plus élevées pour INEXT et IFEXT ***doivent*** satisfaire aux exigences suivantes:

- INEXT ≤ −40 dB à 12,5 GHz, pour TX1 à RX1, TX2 à RX2, TX1 à RX2, TX2 à RX1, TX1 à TX2 et RX1 à RX2,
- IFEXT ≤ −40 dB à 12,5 GHz, pour TX1 à RX1, TX2 à RX2, TX1 à RX2, TX2 à RX1, TX1 à TX2 et RX1 à RX2.

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La diaphonie entre ports (TX1 à RX2, TX2 à RX1, TX1 à TX2 et RX1 à RX2) est spécifiée pour prendre en charge les utilisations où les quatre paires transmettent ou reçoivent des signaux simultanément, par exemple en fonctionnement USB SuperSpeed à double voie.

3.7.2.3.4 Diaphonie intégrée entre les paires TX/RX et la paire USB D+/D− (*normative – USB 3.2* Gen2 et *USB4* Gen2)

La diaphonie entre les paires TX/RX et la paire ***USB 2.0*** D+/D− ***doit*** être contrôlée pour assurer la robustesse de la liaison ***USB 2.0***. Étant donné que les ensembles câble-connecteurs USB Type-C vers USB Type-C complets ***peuvent*** prendre en charge l'utilisation d'***USB 3.2***, d'***USB4*** ou d'un ***mode alternatif*** (par exemple, ***DisplayPort***), la diaphonie entre les quatre paires différentielles à grande vitesse et la paire D+/D− ***peut*** être une paradiaphonie, une télédiaphonie ou une combinaison des deux. La diaphonie intégrée avec D+/D− est calculée avec les équations suivantes:

$$\text{IDDXT_1NEXT + FEXT } = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2(|NEXT1(f)|^2 + |FEXT(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2df}}\right)$$

où:

NEXT = paradiaphonie entre la paire TX et D+/D−,

FEXT = télédiaphonie entre la paire RX et D+/D−, et

f_{max} = 1,2 GHz.

$$\text{IDDXT_2NEXT } = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2(|NEXT1(f)|^2 + |NEXT2(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2df}}\right)$$

où:

NEXT1 = paradiaphonie entre la paire TX et D+/D−,

NEXT2 = paradiaphonie entre la paire RX (RX fonctionnant en mode TX) et D+/D−, et

f_{max} = 1,2 GHz.

L'intégration ***doit*** être effectuée pour NEXT + FEXT et 2NEXT sur D+/D− à partir des deux paires différentielles situées en A2, A3, B10 et B11 (voir la Figure 2-2) et pour NEXT + FEXT et 2NEXT sur D+/D− à partir des deux paires différentielles situées en B2, B3, A10 et A11 (voir la Figure 2-2). Les mesurages sont réalisés dans deux ensembles afin de réduire le plus possible le nombre de ports exigés pour chaque mesurage. La diaphonie différentielle intégrée sur D+/D− ***doit*** satisfaire aux exigences suivantes:

- IDDXT_1NEXT + FEXT ≤ −34,5 dB; et
- IDDXT_2NEXT ≤ −33 dB.

3.7.2.3.5 Facteur d'adaptation intégré (*normatif – USB 3.2* Gen2 et *USB4* Gen2)

Le facteur d'adaptation intégré (IRL, *Integrated Return Loss*) gère la réflexion entre l'ensemble câble-connecteurs et le reste du système (hôte et dispositif). Il est défini comme suit:

$$IRL = dB\left(\sqrt{\frac{\int_0^{fmax}|Vin(f)|^2|SDD21(f)|^2(|SDD11(f)|^2 + |SDD22(f)|^2)df}{\int_0^{fmax}|Vin(f)|^2df}}\right)$$

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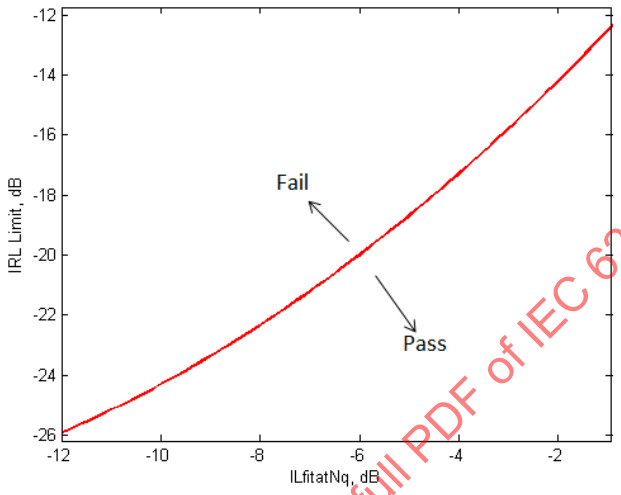
où *SDD21(f)* est la perte d'insertion différentielle mesurée pour l'ensemble câble-connecteurs, *SDD11(f)* et *SDD22(f)* sont les facteurs d'adaptation mesurés pour l'ensemble câble-connecteur côté gauche et côté droit, respectivement, d'une paire différentielle.

L'IRL dépend également fortement de ILfitatNq, et sa limite est spécifiée en fonction de ILfitatNq:

$$IRL \leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 10.784.$$

Elle est représentée à la Figure 3-42.

Figure 3-42 Limite IRL en fonction de ILfitatNq



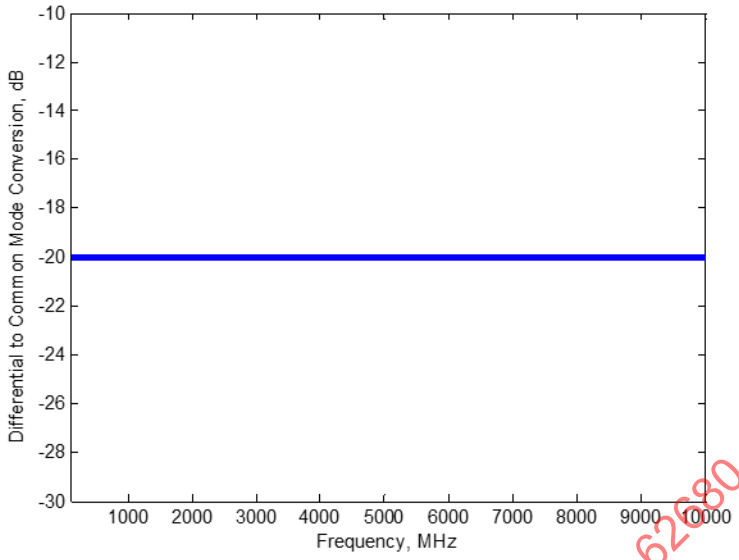
Anglais	Français
IRL Limit	Limite d'IRL
Fail	Incorrecte
Pass	Correcte

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3.7.2.3.6 Conversion du mode différentiel en mode commun (*normative – USB 3.2* Gen2 et *USB4* Gen2)

La conversion du mode différentiel en mode commun permet de contrôler l'injection de bruit en mode commun, de l'ensemble câble-connecteurs dans l'hôte ou le dispositif. La Figure 3-43 représente l'exigence concernant la conversion du mode différentiel en mode commun (SCD12/SCD21). Un ensemble câble-connecteurs couplé satisfait à l'essai si sa conversion SCD12/SCD21 est inférieure ou égale à −20 dB, de 100 MHz à 10 GHz.

Figure 3-43 Exigence concernant la conversion du mode différentiel en mode commun



Anglais	Français
Differential to Comm on Mode Conversion	Conversion du mode différentiel en mode commun
Frequency	Fréquence

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3.7.2.4 Exigences *normatives* relatives à l'ensemble câble-connecteurs passif TX/RX pour *USB 3.2* Gen1 et *USB4* Gen2

3.7.2.4.1 Ajustement de la perte d'insertion différentielle aux fréquences de Nyquist (*normatif – USB 3.2* Gen1 et *USB4* Gen2)

Les exigences relatives aux paramètres S intégrés pour ***USB 3.2*** Gen1 et ***USB4*** Gen2 suivent la même méthodologie que celle définie en 3.7.2.3. Les paramètres sont réglés de façon à convenir au débit de données ***USB4*** Gen2. Sauf spécification contraire, les paramètres suivants ***doivent*** être utilisés pour calculer l'ajustement de la perte d'insertion et les paramètres intégrés:

- l'intervalle unitaire T_b est défini sur 100 ps, ce qui reflète le débit de données ***USB4*** Gen2;
- le temps de montée T_r reste de 0,4 * T_b;
- la fréquence d'intégration ou d'ajustement maximale f_{max} est augmentée à 12,5 GHz;
- l'équation d'ajustement est définie comme suit:

$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3}$$

où f est la fréquence, et a, b, c et d sont les coefficients d'ajustement.

L'ajustement de la perte d'insertion à la fréquence de Nyquist (ILfitatNq) ***doit*** satisfaire aux exigences suivantes:

- ≥ −7,0 dB à 2,5 GHz, et
- > −11,5 dB à 5 GHz.

3.7.2.4.2 Multiréflexion intégrée (*normative – USB 3.2* Gen1 et *USB4* Gen2)

L'écart de la perte d'insertion (ILD) est défini comme suit:

$$ILD(f) = IL(f) - ILfit(f)$$

Il mesure l'ondulation de la perte d'insertion, provoquée par les multiples réflexions à l'intérieur de l'ensemble câble-connecteurs (couplé au montage). L'intégration de ILD(f) est appelée "multiréflexion intégrée" (IMR):

$$IMR = dB\left(\sqrt{\frac{\int_0^{fmax}|ILD(f)|^2|Vin(f)|^2df}{\int_0^{fmax}|Vin(f)|^2df}}\right)$$

où f_{max} = 12,5 GHz et *Vin(f)* est le spectre d'une impulsion trapézoïdale en entrée.

Pour les ensembles câble-connecteurs ***USB 3.2*** Gen1 et ***USB4*** Gen2, la limite IMR est spécifiée comme suit:

$$IMR \leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 24.792$$

3.7.2.4.3 Diaphonie intégrée entre les paires TX/RX (*normative – USB 3.2* Gen1 et *USB4* Gen2)

La diaphonie intégrée entre l'ensemble des paires TX/RX est calculée avec les équations suivantes:

$$INEXT = dB\left(\sqrt{\frac{\int_0^{fmax}(|Vin(f)|^2(|NEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2\ |NEXTd(f)|^2)df}{\int_0^{fmax}|Vin(f)|^2df}}\right)$$

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$$IFEXT = dB\left(\sqrt{\frac{\int_0^{fmax}(|Vin(f)|^2(|FEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2\,|FEXTd(f)|^2)df}{\int_0^{fmax}|Vin(f)|^2 df}}\right)$$

où *NEXT(f)*, *FEXT(f)* et *C2D(f)* correspondent respectivement à la paradiaphonie et à la télédiaphonie mesurées entre les paires TX/RX, et à la conversion du mode commun en mode différentiel. Le facteur de 0,1252 repose sur l'hypothèse que l'amplitude du mode commun correspond à 12,5 % de l'amplitude différentielle. *NEXTd(f)* et *FEXTd(f)* correspondent respectivement à la paradiaphonie et à la télédiaphonie entre la paire D+/D− et les paires TX/RX. *Vdd(f)* est le spectre d'impulsion en entrée Tb = 2,08 ns.

Les valeurs les plus élevées pour INEXT et IFEXT ***doivent*** satisfaire aux exigences suivantes:

- INEXT ≤ −40 dB à 12,5 GHz, pour TX1 à RX1, TX2 à RX2, TX1 à RX2, TX2 à RX1, TX1 à TX2 et RX1 à RX2,
- IFEXT ≤ −40 dB à 12,5 GHz, pour TX1 à RX1, TX2 à RX2, TX1 à RX2, TX2 à RX1, TX1 à TX2 et RX1 à RX2.

La diaphonie entre ports (TX1 à RX2, TX2 à RX1, TX1 à TX2 et RX1 à RX2) est spécifiée pour prendre en charge les utilisations où les quatre paires grande vitesse transmettent ou reçoivent des signaux simultanément (par exemple, en fonctionnement USB à double voie).

3.7.2.4.4 Diaphonie intégrée entre les paires TX/RX et la paire USB D+/D− (*normative – USB 3.2* Gen1 et *USB4* Gen2)

La diaphonie entre les paires TX/RX et la paire ***USB 2.0*** D+/D− ***doit*** être contrôlée pour assurer la robustesse de la liaison ***USB 2.0***. Étant donné que les ensembles câble-connecteurs USB Type-C vers USB Type-C complets ***peuvent*** prendre en charge l'utilisation d'***USB 3.2***, d'***USB4*** ou d'un ***mode alternatif*** (par exemple, ***DisplayPort***), la diaphonie entre les quatre paires différentielles à grande vitesse et la paire D+/D− ***peut*** être une paradiaphonie, une télédiaphonie ou une combinaison des deux. La diaphonie intégrée avec D+/D− est calculée avec les équations suivantes:

$$\text{IDDXT_1NEXT + FEXT } = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2(|NEXT1(f)|^2 + \ |FEXT(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2 df}}\right)$$

où:

NEXT = paradiaphonie entre la paire TX et D+/D−,

FEXT = télédiaphonie entre la paire RX et D+/D−, et

f_{max} = 1,2 GHz.

$$\text{IDDXT}_{\text{2NEXT}} = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2(|NEXT1(f)|^2 + \ |NEXT2(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2 df}}\right)$$

où:

NEXT1 = paradiaphonie entre la paire TX et D+/D−,

NEXT2 = paradiaphonie entre la paire RX (RX fonctionnant en mode TX) et D+/D−, et

f_{max} = 1,2 GHz.

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L'intégration ***doit*** être effectuée pour NEXT + FEXT et 2NEXT sur D+/D− à partir des deux paires différentielles situées en A2, A3, B10 et B11 (voir la Figure 2-2) et pour NEXT + FEXT et 2NEXT sur D+/D− à partir des deux paires différentielles situées en B2, B3, A10 et A11 (voir la Figure 2-2). Les mesurages sont réalisés dans deux ensembles afin de réduire le plus possible le nombre de ports exigés pour chaque mesurage.

La diaphonie différentielle intégrée sur D+/D− ***doit*** satisfaire aux exigences suivantes:

- IDDXT_1NEXT + FEXT ≤ −34,5 dB;
- IDDXT_2NEXT ≤ −33 dB.

3.7.2.4.5 Facteur d'adaptation intégré (*normatif – USB 3.2* Gen1 et *USB4* Gen2)

Le facteur d'adaptation intégré (IRL, *Integrated Return Loss*) gère la réflexion entre l'ensemble câble-connecteurs et le reste du système (hôte et dispositif). Il est défini comme suit:

$$IRL = dB\left(\sqrt{\frac{\int_0^{fmax}|Vin(f)|^2|SDD21(f)|^2(|SDD11(f)|^2 + |SDD22(f)|^2)df}{\int_0^{fmax}|Vin(f)|^2df}}\right)$$

où *SDD21(f)* est la perte d'insertion différentielle mesurée pour l'ensemble câble-connecteurs, *SDD11(f)* et *SDD22(f)* sont les facteurs d'adaptation mesurés pour l'ensemble câble-connecteur côté gauche et côté droit, respectivement, d'une paire différentielle.

Pour les ensembles câble-connecteurs ***USB 3.2*** Gen1 et ***USB4*** Gen2, la limite IRL est spécifiée comme suit:

$$IRL \leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 9.784$$

3.7.2.4.6 Conversion du mode différentiel en mode commun (*normative – USB 3.2* Gen1 et *USB4* Gen2)

La conversion du mode différentiel en mode commun permet de contrôler l'injection de bruit en mode commun, de l'ensemble câble-connecteurs dans l'hôte ou le dispositif. Un ensemble câble-connecteurs couplé satisfait à l'essai si sa conversion SCD12/SCD21 est inférieure ou égale à −17 dB, de 100 MHz à 10 GHz.

3.7.2.5 Exigences *normatives* relatives à l'ensemble câble-connecteurs passif TX/RX pour l'*USB4* Gen3/Gen4

Note: Même si les exigences ***normatives*** de cette section sont définies par rapport à ***USB4*** Gen3, elles s'appliquent également aux ensembles câble-connecteurs passifs ***USB4*** Gen4 car ils sont électriquement équivalents aux ensembles câble-connecteurs passifs ***USB4*** Gen3.

Les exigences relatives aux paramètres S intégrés pour ***USB4*** Gen3 suivent la même méthodologie que celle définie en 3.7.2.3. Les paramètres sont réglés de façon à convenir au débit de données ***USB4*** Gen3. Sauf spécification contraire, les paramètres suivants ***doivent*** être utilisés pour calculer l'ajustement de la perte d'insertion et les paramètres intégrés:

- l'intervalle unitaire T_b est défini sur 50 ps, ce qui reflète le débit de données ***USB4*** Gen3;
- le temps de montée T_r reste de 0,4 * T_b;
- la fréquence d'intégration ou d'ajustement maximale f_{max} est augmentée à 20 GHz;
- un terme f-au-carré est ajouté à l'équation d'ajustement de la perte d'insertion afin d'améliorer la qualité de l'ajustement:

$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3} + e * \sqrt{f^4}$$

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L'***USB4*** Gen3 applique une marge de fonctionnement de canal (COM, *Channel Operating Margin*) au niveau du système pour l'ensemble câble-connecteurs. Les descriptions sont fournies au 3.7.2.5.7.

3.7.2.5.1 Ajustement de la perte d'insertion aux fréquences de Nyquist (*normatif – USB4* Gen3/Gen4)

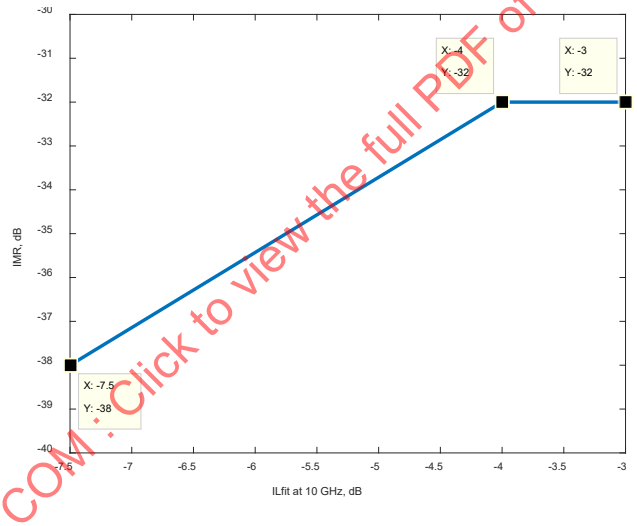
L'ajustement de la perte d'insertion à la fréquence de Nyquist (ILfitatNq) ***doit*** satisfaire aux exigences suivantes:

- ≥ −1 dB à 100 MHz;
- ≥ −4,2 dB à 2,5 GHz;
- ≥ −6 dB à 5 GHz;
- ≥ −7,5 dB à 10 GHz;
- ≥ −9,3 dB à 12,5 GHz; et
- ≥ −11 dB à 15 GHz.

3.7.2.5.2 Multiréflexion intégrée (*normative – USB4* Gen3/Gen4)

La limite IMR est représentée à la Figure 3-44.

Figure 3-44 Limite IMR en fonction de ILfit à 10 GHz (USB4 Gen3/Gen4)



Anglais	Français
at 10 GHz	à 10 GHz

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3.7.2.5.3 Diaphonie intégrée entre les paires TX/RX (*normative – USB4* Gen3/Gen4)

La diaphonie intégrée à l'intérieur d'un port pour TX1 à RX1 et TX2 à RX2 est recommandée pour satisfaire aux exigences ***informatives*** suivantes:

- INEXT ≤ −43 dB; et
- IFEXT ≤ −43 dB.

L'exigence ***informative*** recommandée pour la diaphonie port à port intégrée pour TX1 à RX2, TX2 à RX1, TX1 à TX2 et RX1 à RX2 est définie comme suit:

- INEXT_p2p ≤ −50 dB; et
- IFEXT_p2p ≤ −50 dB.

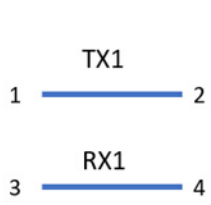
La diaphonie totale est définie pour le ***mode alternatif DP***, le fonctionnement ***USB4*** symétrique et le fonctionnement ***USB4*** asymétrique. En ***mode alternatif DP***, l'ensemble de la diaphonie est FEXT, alors qu'en mode ***USB4***, FEXT et NEXT existent. La diaphonie totale est définie par l'équation ci-dessous:

$$\text{IXTi_DP ou IXTi_USB ou IXTi_ASYM } = dB\left(\sqrt{\frac{\int_0^{f_{max}} |Vin(f)|^2 \sum_j |SDDij|^2 df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

où les victimes *i* = 1 à 8 et les agresseurs *j* sont définis à la Figure 3-45.

Figure 3-45 Définition du port, de la victime et de l'agresseur

IXT_DP

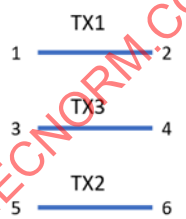


i	j		
1	4	6	8
2	3	5	7
3	2	6	8
4	1	5	7
5	2	4	8
6	1	3	7
7	2	4	6
8	1	3	5

IXT_USB

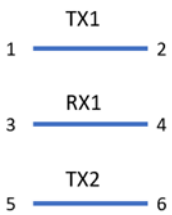
i	j		
1	3	7	6
2	4	8	5
3	1	5	8
4	2	6	7
5	3	7	2
6	4	8	1
7	1	5	4
8	2	6	3

IXT_ASYM_1



i	j		
1	4	6	7
2	3	5	8
3	2	6	7
4	1	5	8
5	2	4	7
6	1	3	8
7	1	3	5
8	2	4	6

IXT_ASYM_2

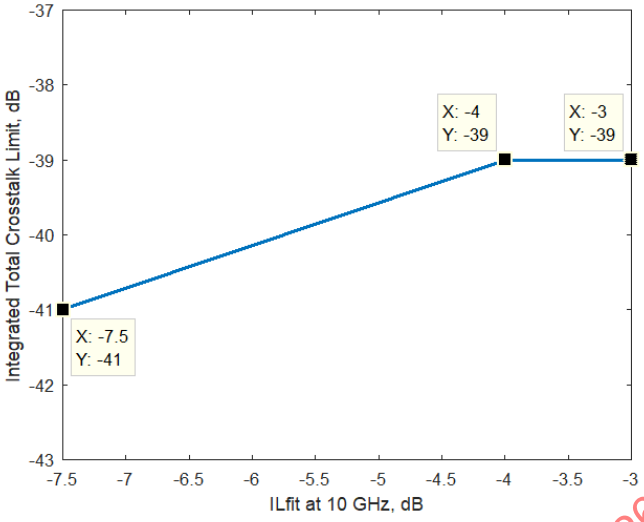


i	j		
1	3	6	8
2	4	5	7
3	1	5	7
4	2	6	8
5	2	3	8
6	1	4	7
7	2	3	6
8	1	4	5

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La diaphonie totale pour le ***mode alternatif DP***, le fonctionnement ***USB4*** symétrique et le fonctionnement ***USB4*** asymétrique ***doit*** être contrôlée. Sa limite ***normative*** est définie à la Figure 3-46.

Figure 3-46 Limite IXT_DP et IXT_USB en fonction de ILfit à 10 GHz (*USB4* Gen3/Gen4)



Anglais	Français
Integrated total crosstalk limit	Limite de diaphonie totale intégrée
at 10 GHz	à 10 GHz

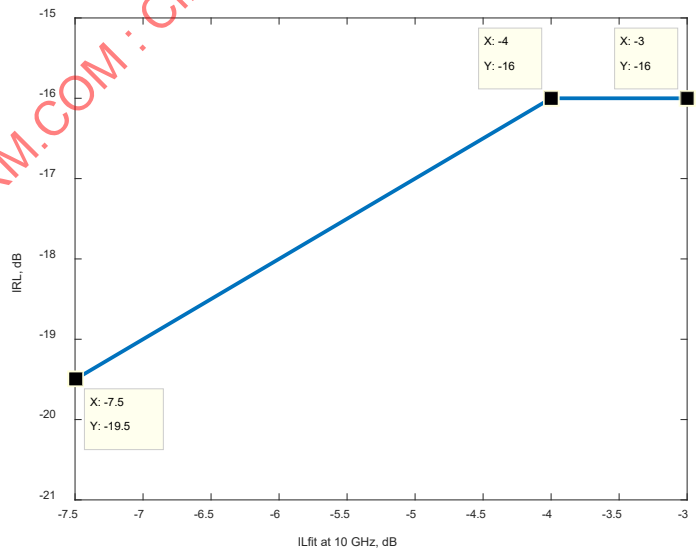
3.7.2.5.4 Diaphonie intégrée entre les paires TX/RX et la paire D+/D– (*normative – USB4* Gen3/Gen4)

Les exigences relatives à la diaphonie intégrée entre les paires TX/RX et la paire ***USB 2.0*** D+/D– sont définies en 3.7.2.3.4.

3.7.2.5.5 Facteur d'adaptation intégré (*normatif – USB4* Gen3/Gen4)

La limite IRL est représentée à la Figure 3-47.

Figure 3-47 Limite IRL en fonction de ILfit à 10 GHz (USB4 Gen3/Gen4)



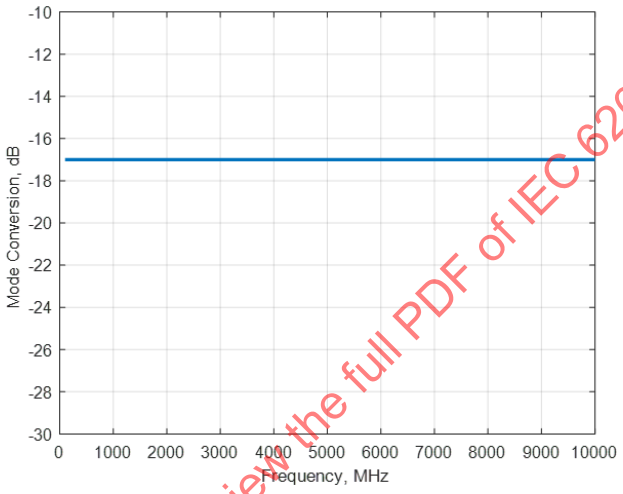
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Anglais	Français
at 10 GHz	à 10 GHz

3.7.2.5.6 Conversion du mode différentiel en mode commun (*normative – USB4* Gen3/Gen4)

La Figure 3-48 représente l'exigence concernant la conversion du mode différentiel en mode commun (SCD12/SCD21). Un ensemble câble-connecteurs couplé satisfait à l'essai si sa conversion SCD12/SCD21 est inférieure ou égale à –17 dB, de 100 MHz à 10 GHz. Noter que – 17 dB est la limite la plus défavorable; aucun câble ***USB4*** Gen3/Gen4 Type-C ne peut la dépasser.

Figure 3-48 Exigence concernant la conversion du mode différentiel en mode commun (*USB4* Gen3/Gen4)



Anglais	Français
Mode Conversion	Conversion du mode
Frequency	Fréquence

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3.7.2.5.7 Exigence concernant la COM (*normative – USB4* Gen3/Gen4)

La marge de fonctionnement de canal (COM) est un facteur de mérite destiné à mesurer la qualité électrique du canal. La description technique de la COM peut être consultée dans la norme IEEE 802.3bj™-2014, 93a.

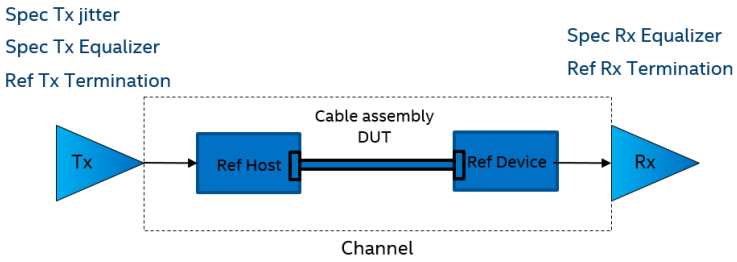
La COM est essentiellement le rapport signal-bruit du canal:

$$COM = 20log10(\frac{A}{N})$$

où A est l'amplitude de signal et N est le bruit combiné au taux d'erreur binaire (BER, *Bit-Error-Ratio*), qui inclut les sources de bruit provenant de l'ISI (interférence intersymbole), la diaphonie, la gigue de l'émetteur, etc.

Pour calculer la COM, les hôtes/dispositifs de référence, qui représentent les hôtes/dispositifs les plus défavorables, ***doivent*** être définis et les valeurs TX et RX de référence ***doivent*** être utilisées. Comme cela est représenté à la Figure 3-49, les paramètres S mesurés pour l'ensemble câble-connecteurs sont mis en cascade avec les modèles de l'hôte de référence et du dispositif de référence pour former le canal complet. Le chargement des matrices et l'égalisation TX et RX sont ensuite appliqués au canal pour calculer la COM.

Figure 3-49 Ensemble câble-connecteurs dans le système



Anglais	Français
Spec Tx jitter	Gigue Tx spé
Spec Tx Equalizer	Équaliseur Tx spé
Ref Tx Termination	Terminaison Tx réf
Ref Host	Hôte de réf
Cable assembly	Ensemble câble-connecteurs
Ref device	Dispositif de réf
Channel	Canal
Spec Rx Equalizer	Équaliseur RX spé
Ref Rx Termination	Terminaison Rx réf

Le Tableau 3-23 définit les paramètres clés du fichier de configuration de la COM. Il utilise les notations COM normalisées. Noter que tous les paramètres d'égalisation TX et RX suivent la spécification ***USB4***.

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Tableau 3-23 Paramètres clés du fichier de configuration de la COM

Paramètre	Réglage	Unité	Informations
f_b	20	GBd	Débit de données ***USB4*** Gen3
C_d	[0 0]	nF	Chargement capacitif TX et RX. Il est défini sur zéro, car le chargement des matrices est traité comme une partie du canal
R_d	[42,5 42,5]	Ohm	Résistance des terminaisons TX et RX
ffe_preset	Tableau 3-4 de la spécification ***USB4***		Préréglages d'égalisation TX
g_DC	[–9:1:0]	dB	Gain DC de CTLE
f_p1	5	GHz	Pôle 1 de CTLE
f_p2	10	GHz	Pôle 2 de CTLE
f_z	3,55	GHz	CTLE zéro
A_v	0,4	V	Oscillation du signal
A_fe	0,4	V	Oscillation de l'agresseur FEXT
A_ne	0,6	V	Oscillation de l'agresseur NEXT
N_b	1		Nombre de marques DFE
b_max(1)	0,7		Liaison DFE, rapport du curseur
Sigma_RJ	0,01	UI	Gigue aléatoire TX, valeur efficace.
A_DD	0,085	UI	Gigue déterministe TX, moyenne à crête
DER_0	1e-12		Taux d'erreur binaire brut cible
eta_0	3,3e-8	V^2/GHz	Densité spectrale du bruit d'un côté
SNR_TX	40	dB	Rapport signal-bruit TX
Seuil COM	3	dB	Critère de réussite/échec

Pour faciliter le calcul de la COM de l'ensemble câble-connecteurs, les garanties suivantes sont fournies et peuvent être obtenues sur le site web de l'***USB-IF***:

- modèles des paramètres S de l'hôte/dispositif de référence;
- modèles des paramètres S de chargement des matrices TX et RX de référence;
- fichier de configuration de la COM;
- outil de calcul de la COM.

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3.7.2.6 Exigences relatives au signal à basse vitesse (*normatives*)

Le présent paragraphe spécifie les exigences électriques concernant les fils CC et SBU, ainsi que le couplage des fils CC, USB D+/D–, VBUS et SBU.

Les fils CC et SBU ***peuvent*** être écrantés ou non, et leurs propriétés ***doivent*** être conformes au Tableau 3-24.

Tableau 3-24 Exigences électriques concernant les fils CC et SBU

Nom	Description	Min.	Max.	Unités
zCable_CC	Impédance caractéristique du câble sur le fil CC	32	93	Ω
rCable_CC	Résistance en courant continu sur le fil CC dans le câble		15	Ω
tCableDelay_CC	Délai de propagation sur le fil CC dans le câble		26	ns
cCablePlug_CC	Capacité du câble pour chaque fiche sur le fil CC		25	pF
zCable_SBU	Impédance caractéristique du câble sur les fils SBU	32	53	Ω
tCableDelay_SBU	Délai de propagation sur les fils SBU dans le câble		26	ns
rCable_SBU	Résistance en courant continu des fils SBU dans le câble		5	Ω
Perte d'insertion SBU SE	Perte d'insertion asymétrique SBU dans le câble		2,0 @ 0,5 MHz 4,0 @ 1 MHz 9,0 @ 10 MHz 10,7 @ 25 MHz 11,9 @ 50 MHz 13,0 @ 100 MHz	dB

Le couplage ou la diaphonie (paradiaphonie et télédiaphonie) ***doivent*** être contrôlés pour les signaux à basse vitesse. Le Tableau 3-25 décrit la matrice des couplages spécifiés.

Tableau 3-25 Matrice de couplage des signaux à basse vitesse

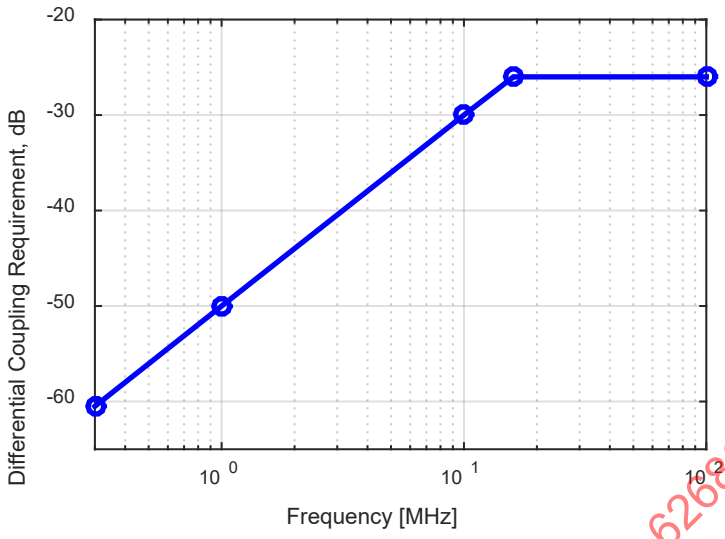
Matrice de couplage	D– (SE)	D+/D– (DF)	VBUS	SBU_B/SBU_A (SE)
CC	FF, CT	FF, CT	FF, CT, CTVPD	FF
D+/D– (DF)	***N/A***	***N/A***	FF, CT	FF
SBU_A/SBU_B	***N/A***	FF	FF	FF
DF: Différentiel; FF: Câble complet; CT: Câble de charge (fonction ***USB 2.0*** incluse); ***CTVPD***: ***Dispositif USB de charge alimenté par VCONN***.				

3.7.2.6.1 CC vers USB D+/D– (*normatif*)

Le couplage différentiel entre le fil CC et le fil D+/D– ***doit*** être au-dessous de la limite représentée à la Figure 3-50. La limite est définie avec les valeurs maximales suivantes: (0,3 MHz, −60,5 dB), (1 MHz, −50 dB), (10 MHz, −30 dB), (16 MHz, −26 dB) et (100 MHz, −26 dB).

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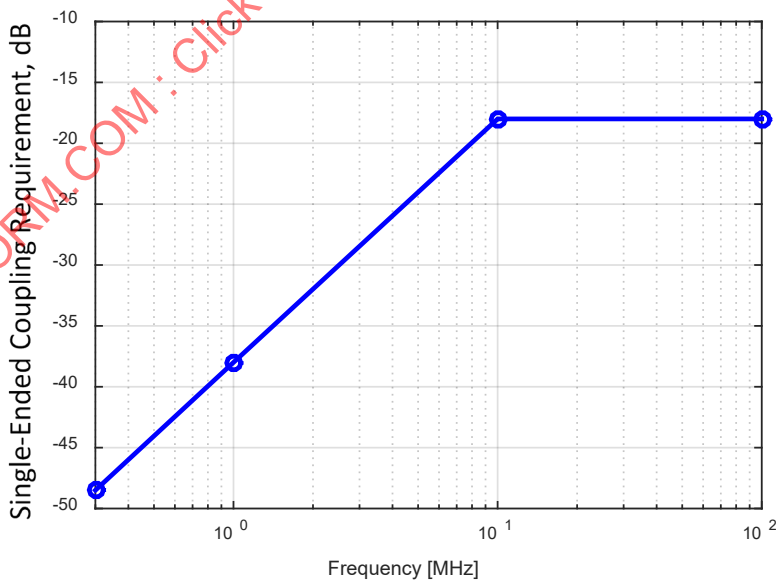
Figure 3-50 Exigence concernant le couplage différentiel entre le fil CC et le fil D+/D–



Anglais	Français
Differential Coupling Requirement	Exigence de couplage différentiel
Frequency	Fréquence

Pour les câbles ***USB 2.0*** Type-C, le couplage asymétrique entre le fil CC et le fil D– ***doit*** être au-dessous de la limite représentée à la Figure 3-51. La limite est définie avec les valeurs maximales suivantes: (0,3 MHz, −48,5 dB), (1 MHz, −38 dB), (10 MHz, −18 dB) et (100 MHz, −18 dB).

Figure 3-51 Exigence concernant le couplage asymétrique entre le fil CC et le fil D– dans les câbles *USB 2.0* Type-C



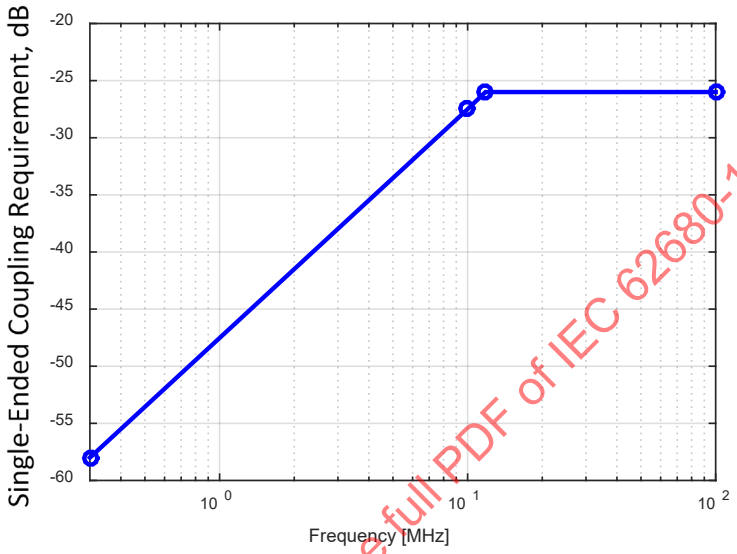
Anglais	Français
Single-Ended Coupling requirement	Exigence de couplage par une seule extrémité

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Frequency	Fréquence

Pour les câbles USB- Type-C Complets, le couplage asymétrique entre le fil CC et le fil D– ***doit*** être au-dessous de la limite représentée à la Figure 3-52. La limite est définie avec les valeurs maximales suivantes: (0,3 MHz, −58 dB), (10 MHz, −27,5 dB), (11,8 MHz, −26 dB) et (100 MHz, −26 dB).

Figure 3-52 Exigence concernant le couplage asymétrique entre le fil CC et le fil D– dans les câbles USB Type-C Complets



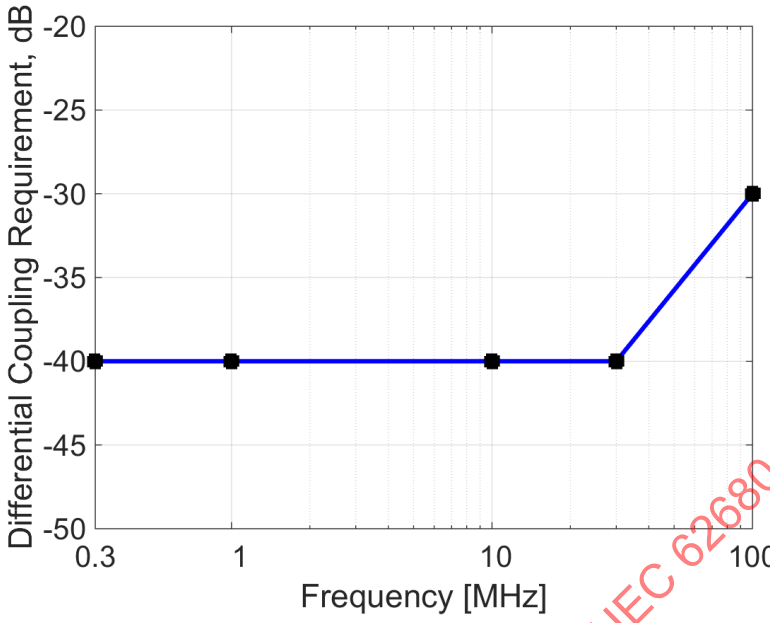
Anglais	Français
Single-Ended Coupling requirement	Exigence de couplage par une seule extrémité
Frequency	Fréquence

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3.7.2.6.2 Couplage VBUS avec SBU_A/SBU_B, CC et USB D+/D– (*normatif*)

Le couplage différentiel entre VBUS et USB D+/D– ***doit*** être au-dessous de la limite représentée à la Figure 3-53. La limite est définie avec les valeurs maximales suivantes: (0,3 MHz, −40 dB), (1 MHz, −40 dB), (30 MHz, −40 dB) et (100 MHz, −30 dB).

Figure 3-53 Exigence concernant le couplage différentiel entre le fil VBUS et le fil D+/D–



Anglais	Français
Single-Ended Coupling requirement	Exigence de couplage par une seule extrémité
Frequency	Fréquence

L'inductance maximale de la boucle VBUS ***doit*** être de 900 nH et l'inductance mutuelle maximale (M) entre VBUS et les lignes de signaux à basse vitesse (CC, SBU_A, SBU_B, D+, D–) ***doit*** être telle qu'elle est spécifiée dans le Tableau 3-26 pour limiter le couplage inductif du bruit VBUS sur les lignes de signaux à basse vitesse. Pour les câbles complets, la capacité de dérivation VBUS ***doit*** être comprise entre 8 nF et 500 nF; les valeurs comprises dans cette plage ont une efficacité équivalente pour la dérivation du chemin retour à grande vitesse.

Tableau 3-26 Inductance mutuelle maximale (M) entre VBUS et les lignes de signaux à basse vitesse

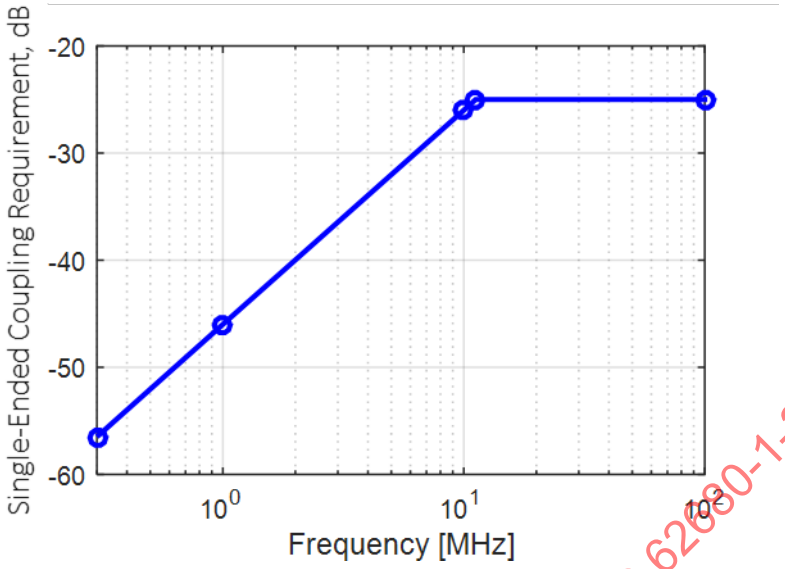
Fil à basse vitesse	Inductance mutuelle maximale (nH)
CC (canal de configuration)	350
SBU_A/SBU_B	330
D+/D–	330

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3.7.2.6.3 Couplage entre SBU_A et SBU_B (*normatif*)

Le couplage asymétrique entre SBU_A et SBU_B ***doit*** être au-dessous de la limite représentée à la Figure 3-54. La limite est définie avec les valeurs maximales suivantes: (0,3 MHz, –56,5 dB), (1 MHz, –46 dB), (10 MHz, –26 dB), (11,2 MHz, –25 dB) et (100 MHz, –25 dB).

Figure 3-54 Exigence concernant le couplage asymétrique entre SBU_A et SBU_B



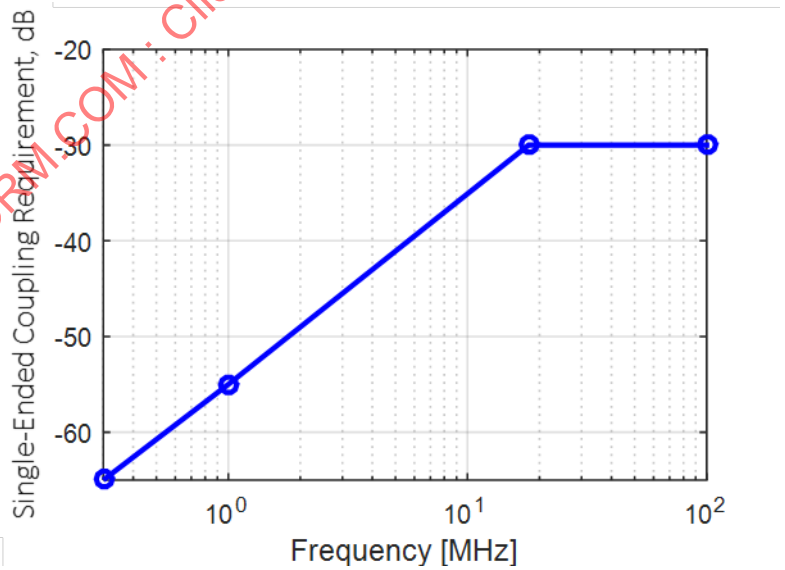
Anglais	Français
Single-Ended Coupling requirement	Exigence de couplage par une seule extrémité
Frequency	Fréquence

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3.7.2.6.4 Couplage entre SBU_A/SBU_B et CC (*normatif*)

Le couplage asymétrique entre SBU_A et CC, et entre SBU_B et CC, ***doit*** être au-dessous de la limite représentée à la Figure 3-55. La limite est définie avec les valeurs maximales suivantes: (0,3 MHz, −65 dB), (1 MHz, −55 dB), (18 MHz, −30 dB) et (100 MHz, −30 dB).

Figure 3-55 Exigence concernant le couplage asymétrique entre SBU_A/SBU_B et CC

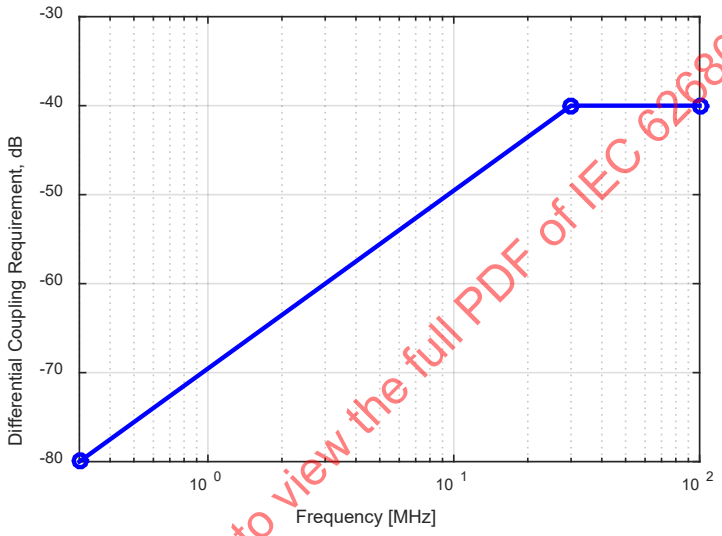


Anglais	Français
Single-Ended Coupling requirement	Exigence de couplage par une seule extrémité
Frequency	Fréquence

3.7.2.6.5 Couplage entre SBU_A/SBU_B et USB D+/D− (*normatif*)

Le couplage entre SBU_A et D+/D− en mode différentiel, et entre SBU_B et D+/D− en mode différentiel, ***doit*** être au-dessous de la limite représentée à la Figure 3-56. La limite est définie avec les valeurs maximales suivantes: (0,3 MHz, −80 dB), (30 MHz, −40 dB) et (100 MHz, −40 dB).

Figure 3-56 Exigence concernant le couplage entre SBU_A et D+/D− en mode différentiel, et entre SBU_B et D+/D− en mode différentiel



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Anglais	Français
Differential Coupling Requirement	Exigence de couplage différentiel
Frequency	Fréquence

3.7.2.7 Exigences relatives au signal USB D+/D− (*normatives*)

Les lignes USB D+/D− de l'ensemble câble-connecteurs passif USB Type-C vers USB Type-C ***doivent*** satisfaire aux exigences définies dans le Tableau 3-27.

Tableau 3-27 Exigences relatives à l'intégrité du signal USB D+/D− pour les ensembles câble-connecteurs passifs USB Type-C vers USB Type-C

Éléments	Descriptions et procédures	Exigences
Impédance différentielle	EIA 364-108 Cet essai permet d'assurer que l'impédance des lignes D+/D− de l'ensemble câble-connecteurs est correcte. Pour l'ensemble câble-connecteurs complet.	75 Ω au minimum et 105 Ω au maximum. Temps de montée: 400 ps (20 % à 80 %).

Éléments	Descriptions et procédures	Exigences
Temps de propagation	EIA 364-103 L'objectif de cet essai est de vérifier la propagation de bout en bout des lignes D+/D– de l'ensemble câble-connecteurs.	26 ns au maximum. Temps de montée: 400 ps (20 % à 80 %).
Obliquité dans les paires	EIA 364-103 Cet essai permet d'assurer que les signaux des lignes D+ et D– de l'ensemble câble-connecteurs atteignent le récepteur en même temps.	100 ps au maximum. Temps de montée: 400 ps (20 % à 80 %).
Affaiblissement des paires D+/D–	EIA 364-101 Cet essai permet d'assurer que la paire D+/D– d'un ensemble câble-connecteurs est capable de fournir une puissance de signal adéquate au récepteur afin de maintenir un taux d'erreur faible.	≥ –1,52 dB @ 50 MHz ≥ –2,03 dB @ 100 MHz ≥ –2,91 dB @ 200 MHz ≥ –4,35 dB @ 400 MHz
Résistance en courant continu D+ ou D–	Cet essai permet d'assurer que la plage de résistances en courant continu du fil D+/D– est correcte afin de prévoir le niveau d'EOP et de régler le niveau de déconnexion de l'***USB 2.0***.	3,5 Ω au maximum.

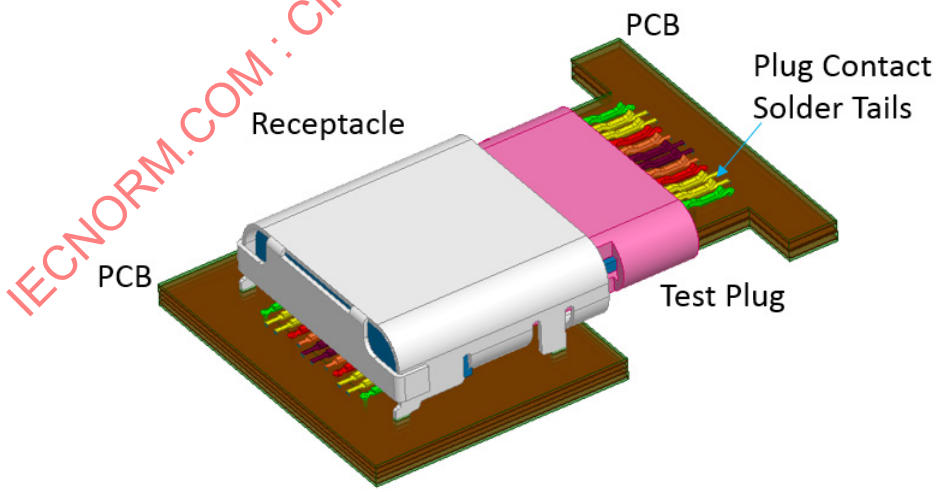
3.7.2.8 Tolérance sur tension continue VBUS (*normative*)

Un ensemble câble-connecteurs USB Type-C vers USB Type-C ***doit*** tolérer une tension continue VBUS de 21 V au courant assigné de câble (c'est-à-dire 3 A ou 5 A) appliquée pendant une heure comme condition préalable à l'essai portant sur les caractéristiques électriques de l'ensemble câble-connecteurs.

3.7.3 Connecteur couplé (*informatif – USB 3.2* Gen2 et *USB4* Gen2)

Le connecteur couplé défini dans la présente spécification USB Type-C se compose d'une embase montée sur une CCI (représentatif du mode d'utilisation de l'embase dans un matériel) et d'une fiche d'essai, elle-même montée sur une CCI (carte d'accès) sans câble. Ceci est représenté à la Figure 3-57. Noter que la fiche d'essai est également utilisée lors de l'essai portant sur les paires TX/RX hôte/dispositif.

Figure 3-57 Représentation du connecteur couplé USB Type-C



Anglais	Français
Receptacle	Embase
Test Plug	Fiche d'essai

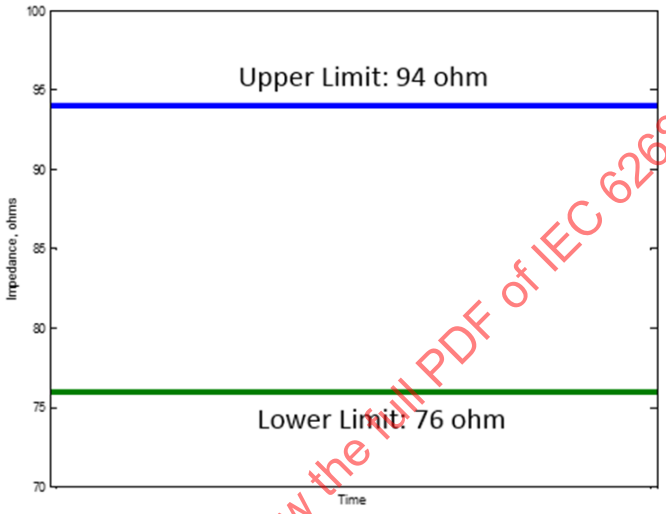
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Anglais	Français
Plug Contact Solder Tails	Connexions brasées de la fiche

3.7.3.1 Impédance différentielle (*informative*)

L'impédance cible du connecteur couplé est spécifiée pour réduire le plus possible la réflexion émise par le connecteur. ***Il convient que*** l'impédance différentielle d'un connecteur couplé soit de 85 Ω ± 9 Ω pour un temps de montée de 40 ps (20 % à 80 %). ***Il convient que*** le profil d'impédance d'un connecteur couplé se situe dans les limites représentées à la Figure 3-58.

Figure 3-58 Limites d'impédance recommandées d'un connecteur couplé USB Type-C

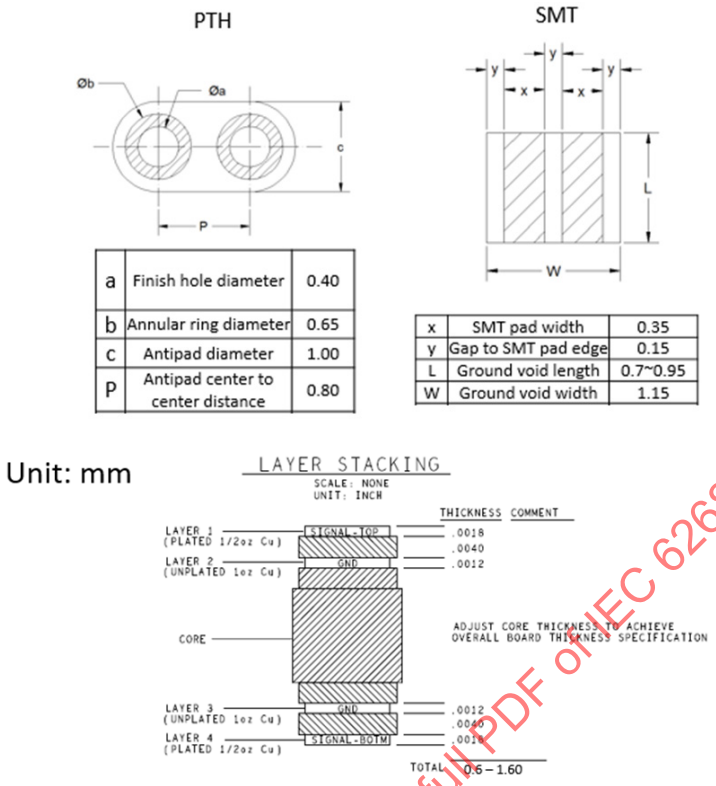


Anglais	Français
Impedance, ohms	Impédance, Ω
Upper Limit: 94 ohm	Limite supérieure: 94 Ω
Lower Limit: 76 ohm	Limite inférieure: 76 Ω
Time	Temps

Il convient de modéliser, au moyen de la solution 3D Field Solver, l'empilage de la CCI, la géométrie des fils et celle des pastilles de brasure afin d'optimiser les performances électriques. Des exemples de vides de masse sous les plaques de signal, reposant sur la géométrie des plaques, le type de montage et l'empilage des CCI sont représentés à la Figure 3-59.

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Figure 3-59 Dimensions recommandées des vides de masse pour une embase USB Type-C



Anglais	Français
PTH	Trou métallisé
SMT	Montage en surface
Finish hole diameter	Diamètre final du trou
Annular ring diameter	Diamètre de la bague annulaire
Antipad diameter	Diamètre de la contrepastille
Antipad center to center distance	Distance centre-à-centre de la pastille
SMT pad width	Largeur de la pastille SMT
Gap to SMT pat edge	Écart avec l'arête de la pastille SMT
Ground void length	Longueur du vide GND
Ground void width	Largeur du vide GND
Layer stacking	Composition des couches
Scale: none	Échelle: aucune
Unit: MM	Unité: MM
Unit: inch	Unité: pouce
Layer 1 (plated 1/2$_{oz\ cu}$)	Couche 1 (plaqué, 1/2$_{once\ de\ cu}$)
Layer 2 (unplated 1$_{oz\ cu}$)	Couche 2 (non plaqué, 1$_{once\ de\ cu}$)
Core	Conducteur
Layer 3 (unplated 1$_{oz\ cu}$)	Couche 3 (non plaqué, 1$_{once\ de\ cu}$)

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Anglais	Français
Layer 4 (plated 1/2 $_{oz\ cu}$)	Couche 4 (plaqué, 1/2$_{once\ de\ cu}$)
Signal - top	Signal - haut
Signal - botm	Signal - bas
Thickness	Épaisseur
Comment	Commentaire
Adjust core thickness to achieve overall board thickness specification	Modifier l'épaisseur du conducteur pour respecter la spécification relative à l'épaisseur totale des parois

3.7.3.2 Caractéristiques recommandées d'intégrité de signal et de paramètre S différentiel pour des connecteurs couplés

Les caractéristiques recommandées d'intégrité de signal pour une paire de connecteurs couplés USB Type-C sont répertoriées dans le Tableau 3-28.

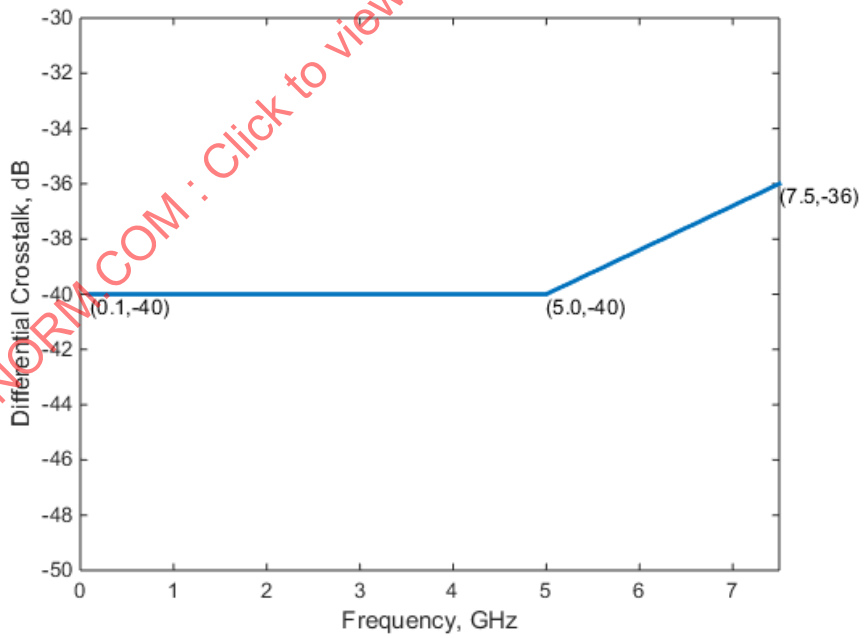
Tableau 3-28 Caractéristiques recommandées d'intégrité de signal pour des connecteurs couplés USB Type-C (*informatives*)

Éléments	Descriptions et procédures	Exigences
Ajustement de la perte d'insertion différentielle aux fréquences de Nyquist (ILfitatNq)	ILfitatNq est évalué aux fréquences de Nyquist TX/RX Gen 1, Gen 2 et Gen 3.	≥ −0,6 dB à 2,5 GHz ≥ −0,8 dB à 5,0 GHz ≥ −1,0 dB à 10 GHz
Multiréflexion différentielle intégrée (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −40 dB ≤ −39 dB (avec fmax = 20 GHz et Vin(f) défini avec Tb (UI) = 50 ps; ***USB4*** Gen3)
Paradiaphonie différentielle intégrée sur TX/RX (INEXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + 0.125^2 \cdot \lvert C2D(f)\rvert^2)df + \int_0^{f_{max}}\lvert Vdd(f)\rvert^2\ \lvert NEXTd(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ où: *NEXT* = NEXT entre les paires TX/RX *NEXTd* = NEXT entre les paires TX/RX et la paire D+/D−	≤ −44 dB
Télédiaphonie différentielle intégrée sur TX/RX (IFEXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2 + 0.125^2 \cdot \lvert C2D(f)\rvert^2)df + \int_0^{f_{max}}\lvert Vdd(f)\rvert^2\ \lvert FEXTd(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ où: *FEXT* = FEXT entre les paires TX/RX *FEXTd* = FEXT entre les paires TX/RX et la paire D+/D−	≤ −44 dB

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Éléments	Descriptions et procédures	Exigences
Diaphonie différentielle de TX/RX sur D+/D−	Paradiaphonie et télédiaphonie différentielles des paires TX/RX sur la paire D+/D− dans les connecteurs couplés.	Voir la Figure 3-60
Diaphonie différentielle de D+/D− sur TX/RX	Paradiaphonie et télédiaphonie différentielles de la paire D+/D− sur les paires TX/RX dans les connecteurs couplés.	Voir la Figure 3-60
Facteur d'adaptation intégré (IRL)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −18 dB
Conversion du mode différentiel en mode commun (SCD12 et SCD21)	La conversion du mode différentiel en mode commun permet de contrôler l'injection de bruit en mode commun, de l'ensemble câble-connecteurs dans l'hôte ou le dispositif. Plage de fréquences: 100 MHz ~ 10,0 GHz	Voir la Figure 3-61
Note: *fmax* = 12,5 GHz (sauf spécification contraire); *Vin(f)* est défini à la Figure 3-40 avec Tb (UI) = 100 ps (sauf spécification contraire); *Vdd(f)* est également défini à la Figure 3-40 avec Tb (UI) = 2,08 ns. *C2D(f)* = paradiaphonie et télédiaphonie respectivement mesurées entre les paires TX/RX, et conversion du mode commun en mode différentiel. Le facteur de $0{,}125^2$ repose sur l'hypothèse que l'amplitude du mode commun correspond à 12,5 % de l'amplitude différentielle.		

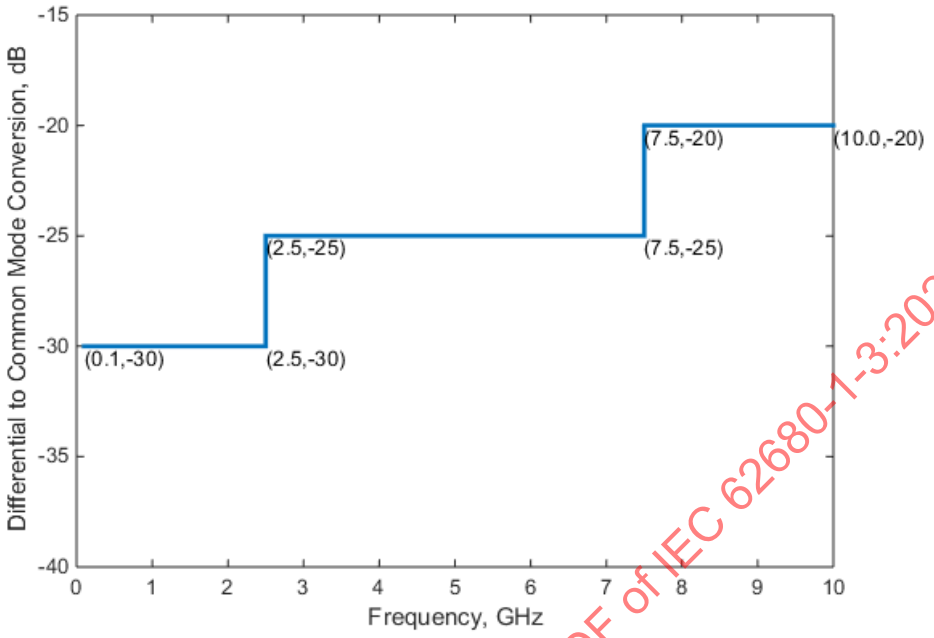
Figure 3-60 Limites recommandées pour la paradiaphonie et la télédiaphonie différentielles entre la paire D+/D− et les paires TX/RX



Anglais	Français
Differential Crosstalk	Diaphonie différentielle
Frequency	Fréquence

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Figure 3-61 Limites recommandées pour la conversion du mode différentiel en mode commun



Anglais	Français
Differential to Comm on Mode Conversion	Conversion du mode différentiel en mode commun
Frequency	Fréquence

3.7.4 Exigences SI et essais de l'embase (*normatifs – USB4* Gen3/Gen4)

Note: Même si les exigences ***normatives*** de cette section sont définies par rapport à ***USB4*** Gen3, elles s'appliquent également aux ensembles câble-connecteurs passifs ***USB4*** Gen4 car ils sont électriquement équivalents aux ensembles câble-connecteurs passifs ***USB4*** Gen3.

Les exigences relatives à l'embase USB Type-C pour ***USB4*** Gen3 sont ***normatives*** et répertoriées dans le Tableau 3-29. Sauf spécification contraire, les éléments à spécifier sont identiques à ceux définis en 3.7.3 et les paramètres utilisés pour calculer les paramètres intégrés sont les mêmes que ceux définis en 3.7.2.4 pour l'ensemble câble-connecteurs ***USB4*** Gen3.

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Tableau 3-29 Caractéristiques d'intégrité de signal pour une embase USB Type-C pour *USB4* Gen3 (*normatives*)

Éléments	Descriptions et procédures	Exigences
Ajustement de la perte d'insertion différentielle aux fréquences de Nyquist (ILfitatNq)	IlfitatNq est évalué à certaines fréquences.	≥ −0,6 dB à 2,5 GHz ≥ −0,8 dB à 5,0 GHz ≥ −1,0 dB à 10 GHz ≥ −1,25 dB à 12,5 GHz ≥ −1,5 dB à 15 GHz
Paradiaphonie différentielle intégrée sur TX/RX (INEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ où: *NEXT* = NEXT entre TX1et RX1, et TX2 et RX2.	≤ −43 dB
Télédiaphonie différentielle intégrée sur TX/RX (IFEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ où: *FEXT* = FEXT entre TX1 et RX1, et TX2 et RX2.	≤ −43 dB
Diaphonie différentielle de TX/RX sur D+/D− Diaphonie différentielle de D+/D− sur TX/RX	Paradiaphonie et télédiaphonie différentielles des paires TX/RX sur la paire D+/D− dans les connecteurs couplés, et paradiaphonie et télédiaphonie différentielles de la paire D+/D− sur les paires TX/RX dans les connecteurs couplés. $dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2+\lvert NEXT(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ où: *FEXT* = télédiaphonie entre les paires TX/RX et la paire D+/D− *NEXT* = paradiaphonie entre les paires TX/RX et la paire D+/D− *fmax* = 1,2 GHz	≤ −50 dB
Facteur d'adaptation intégré (IRL)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −15 dB
Conversion du mode différentiel en mode commun (SCD12 et SCD21)	La conversion du mode différentiel en mode commun permet de contrôler l'injection de bruit en mode commun, de l'ensemble câble-connecteurs dans l'hôte ou le dispositif. Plage de fréquences: 100 MHz ~ 10,0 GHz	≤ −20 dB
Note: *fmax* = 20 GHz (sauf spécification contraire); *Vin(f)* est défini avec Tb (UI) = 50 ps.		

Les exigences définies dans le présent paragraphe ne s'appliquent pas à la fiche USB Type-C, comme les limites du Tableau 3-29 des caractéristiques électriques du montage d'essai qui contient une fiche USB Type-C spécifiquement choisie pour soumettre à l'essai l'embase USB Type-C. La fiche USB Type-C ne présente pas un ensemble d'exigences définies au niveau du connecteur couplé, compte tenu des compromis qui permettent d'atteindre des performances acceptables au niveau de l'ensemble câble-connecteurs fini.

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3.7.5 Ensembles câble-connecteurs USB Type-C vers USB existant (*normatifs*)

Les ensembles câble-connecteurs USB Type-C vers existant ***peuvent*** prendre en charge l'***USB 2.0*** uniquement ou l'***USB 3.1***.

3.7.5.1 Ensembles câble-connecteurs *USB 2.0* uniquement (*normatifs*)

Les ensembles câble-connecteurs ***USB 2.0*** uniquement Type-C vers existant incluent:

- Fiche USB Type-C vers fiche ***USB 2.0*** Standard-A
- Fiche USB Type-C vers fiche ***USB 2.0*** Standard-B
- Fiche USB Type-C vers fiche ***USB 2.0*** Micro-B
- Fiche USB Type-C vers fiche ***USB 2.0*** Mini-B

Les exigences relatives à l'intégrité du signal USB D+/D− sont spécifiées dans le Tableau 3-30.

Tableau 3-30 Exigences relatives à l'intégrité du signal USB D+/D− pour les ensembles câble-connecteurs USB Type-C vers USB existant (*normatives*)

Éléments	Descriptions et procédures	Exigences
Impédance différentielle	EIA 364-108 Cet essai permet d'assurer que l'impédance des lignes D+/D− de l'ensemble câble-connecteurs est correcte. Pour l'ensemble câble-connecteurs complet.	75 Ω au minimum et 105 Ω au maximum. Temps de montée: 400 ps (20 % à 80 %).
Temps de propagation	EIA 364-103 L'objectif de cet essai est de vérifier la propagation de bout en bout des lignes D+/D− de l'ensemble câble-connecteurs.	10 ns maximum pour un ensemble câble-connecteurs USB Type-C vers Micro-B; 20 ns maximum pour tous les autres ensembles câble-connecteurs USB Type-C vers USB existant. Temps de montée: 400 ps (20 % à 80 %).
Obliquité dans les paires	EIA 364-103 Cet essai permet d'assurer que les signaux des lignes D+ et D− de l'ensemble câble-connecteurs atteignent le récepteur en même temps.	100 ps au maximum. Temps de montée: 400 ps (20 % à 80 %).
Affaiblissement des paires D+/D−	EIA 364-101 Cet essai permet d'assurer que les signaux des lignes D+ et D− de l'ensemble câble-connecteurs atteignent le récepteur en même temps.	≥ −1,52 dB @ 50 MHz ≥ −2,03 dB @ 100 MHz ≥ −2,91 dB @ 200 MHz ≥ −4,35 dB @ 400 MHz
Résistance en courant continu D+ ou D−	Cet essai permet d'assurer que la plage de résistances en courant continu du fil D+/D− est correcte afin de prévoir le niveau d'EOP et de régler le niveau de déconnexion de l'***USB 2.0***.	3,5 Ω au maximum.

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3.7.5.2 Ensembles câble-connecteurs *USB 3.1* Gen2 (*normatifs*)

Les ensembles câble-connecteurs USB Type-C vers ***USB 3.1*** Gen2 existant incluent:

- Fiche USB Type-C vers fiche ***USB 3.1*** Standard-A

- Fiche USB Type-C vers fiche ***USB 3.1*** Standard-B
- Fiche USB Type-C vers fiche ***USB 3.1*** Micro-B

Les objectifs de conception ***informatifs*** pour ces câbles sont donnés dans le Tableau 3-31.

Tableau 3-31 Objectifs de conception pour les ensembles câble-connecteurs USB Type-C vers *USB 3.1* Gen2 existant (*informatifs*)

Éléments	Objectifs de conception
Impédance différentielle	76 Ω au minimum et 96 Ω au maximum. Temps de montée: 40 ps (20 % à 80 %).
Perte d'insertion différentielle	≥ −2 dB à 100 MHz ≥ −4 dB à 2,5 GHz, sauf pour l'ensemble câble-fiche USB Type-C vers fiche ***USB 3.1*** Standard-A, dont les valeurs sont les suivantes: ≥ −3,5 dB à 2,5 GHz Au maximum −6,0 dB à 5 GHz
NEXT différentielle entre les paires SuperSpeed	≤ −34 dB à 5 GHz
NEXT et FEXT différentielles entre les paires D+/D− et SuperSpeed	≤ −30 dB à 5 GHz

Les exigences ***normatives*** incluent la signalisation USB D+/D− spécifiée dans le Tableau 3-30 et les paramètres USB SuperSpeed spécifiés dans le Tableau 3-32.

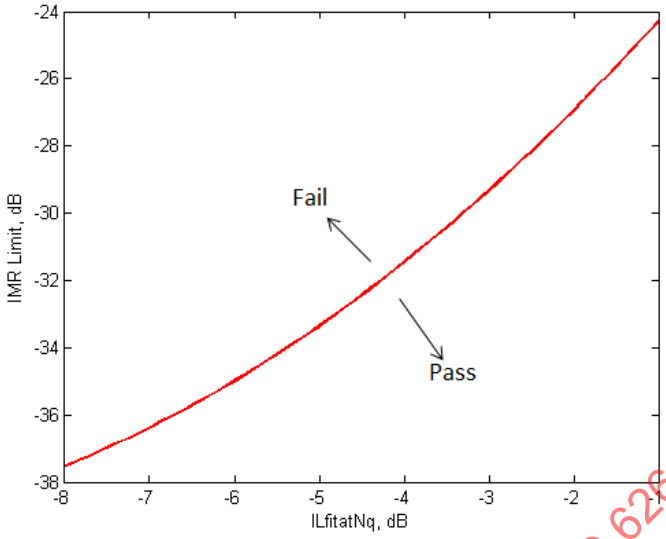
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Tableau 3-32 Exigences relatives à l'intégrité du signal pour un ensemble câble-connecteurs USB Type-C vers *USB 3.1* Gen2 existant (*normatives*)

Éléments	Descriptions et procédures	Exigences
Ajustement de la perte d'insertion différentielle aux fréquences de Nyquist (ILfitatNq)	ILfitatNq est évalué aux fréquences de Nyquist SuperSpeed Gen 1 et Gen 2.	≥ −4 dB à 2,5 GHz, sauf pour l'ensemble câble-fiche USB Type-C vers fiche ***USB 3.1*** Standard-A, dont les valeurs sont les suivantes: ≥ −3,5 dB à 2,5 GHz ≥ −6,0 dB à 5,0 GHz
Multiréflexion différentielle intégrée (IMR)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	$\leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 21.392$ Voir la Figure 3-62.
Diaphonie différentielle intégrée sur SuperSpeed (ISSXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}(\lvert Vin(f)\rvert^2\lvert NEXTs(f)\rvert^2 + \lvert Vdd(f)\rvert^2\lvert NEXTd(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ où: *NEXTs* = NEXT entre les paires SuperSpeed *NEXTd* = NEXT entre les paires D+/D− et SuperSpeed *Vdd(f)* = spectre d'une impulsion en entrée sur la paire D+/D−, évalué au moyen de l'équation représentée à la Figure 3-40 avec Tb (UI) = 2.08 ns.	≤ −38 dB
Diaphonie différentielle intégrée sur D+/D- (IDDXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + \lvert FEXT(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ où: *NEXT* = paradiaphonie entre SuperSpeed et D+/D− *FEXT* = télédiaphonie entre SuperSpeed et D+/D− *fmax* = 1,2 GHz	≤ −28,5 dB
Facteur d'adaptation intégré (IRL)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2 + \lvert SDD22(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	$\leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 9.784$ Voir la Figure 3-63.
Conversion du mode différentiel en mode commun (SCD12 et SCD21)	La conversion du mode différentiel en mode commun permet de contrôler l'injection de bruit en mode commun, de l'ensemble câble-connecteurs dans l'hôte ou le dispositif. Plage de fréquences: 100 MHz ~ 10,0 GHz	≤ −20 dB
Note: *fmax* = 10 GHz (sauf spécification contraire); *Vin(f)* est défini à la Figure 3-40 avec Tb (UI) = 100 ps; et *Vdd(f)* est également défini à la Figure 3-40 avec Tb (UI) = 2,08 ns.		

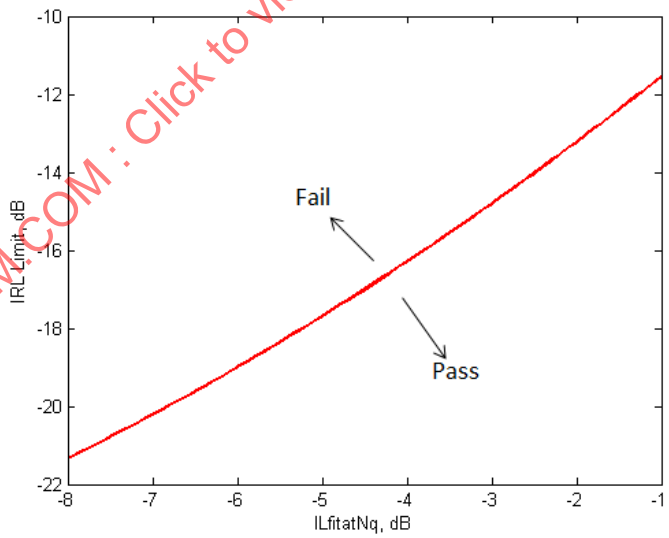
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Figure 3-62 Limite IMR en fonction de ILfitatNq pour un ensemble câble-connecteurs USB Type-C vers existant



Anglais	Français
IMR Limit	Limite d'IMR
Fail	Incorrecte
Pass	Correcte

Figure 3-63 Limite IRL en fonction de ILfitatNq pour un ensemble câble-connecteurs USB Type-C vers existant



Anglais	Français
IRL Limit	Limite d'IRL
Fail	Incorrecte
Pass	Correcte

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3.7.5.3 Fiches USB existantes conformes utilisées dans les ensembles câble-connecteurs USB Type-C vers USB existant

Les exigences suivantes viennent s'ajouter aux exigences existantes pour les connecteurs existants, lorsqu'ils sont utilisés dans les ensembles câble-connecteurs USB Type-C vers existant conformes.

3.7.5.3.1 Exigences relatives aux matériaux de contact pour les ensembles câble-connecteurs USB Type-C vers USB Micro-B

Pour les ensembles câble-connecteurs USB Type-C vers USB Micro-B, modifier le matériau de contact dans le connecteur USB Micro-B pour obtenir la résistance de contact à faible niveau suivante (EIA 364-23B):

- 20 mΩ (valeur maximale) initiaux pour les contacts VBUS et GND; et
- variation maximale (delta) de +10 mΩ après l'application de contraintes environnementales.

3.7.5.3.2 Courant assigné des contacts pour les paires couplées de connecteurs USB Standard-A, USB Standard-B et USB Micro-B (EIA 364-70, Méthode 2)

Lorsqu'un courant de 3 A est appliqué à la broche VBUS et à sa broche GND correspondante (à savoir aux broches 1 et 4 dans un connecteur USB Standard-A ou USB Standard-B, ou aux broches 1 et 5 dans un connecteur USB Micro-B), le delta de température ***ne doit pas*** être supérieur à +30 °C, quel que soit le point des connecteurs en essai, lorsque le mesurage est réalisé à une température ambiante de 25 °C.

3.7.6 Ensembles adaptateurs USB Type-C vers USB existants (*normatifs*)

Seuls les ensembles adaptateurs existants normalisés suivants sont définis:

- fiche ***USB 2.0*** Type-C vers embase ***USB 2.0*** Micro-B; et
- fiche USB Type-C Complète vers embase ***USB 3.1*** Standard-A.

3.7.6.1 Ensemble adaptateur-fiche *USB 2.0* Type-C vers embase *USB 2.0* Micro-B

Cet ensemble adaptateur ne prend en charge que la signalisation ***USB 2.0***. Sa longueur totale ***ne doit pas*** dépasser 150 mm, d'une extrémité à l'autre. Le Tableau 3-33 définit les exigences électriques.

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Tableau 3-33 Exigences relatives à l'intégrité du signal USB D+/D− pour les ensembles adaptateurs USB Type-C vers USB existant (*normatives*)

Éléments	Descriptions et procédures	Exigences
Impédance différentielle	EIA 364-108 Cet essai permet d'assurer que l'impédance des lignes D+/D− de l'ensemble adaptateur est correcte. Pour l'ensemble adaptateur complet.	75 Ω au minimum et 105 Ω au maximum. Temps de montée: 400 ps (20 % à 80 %).
Obliquité dans les paires	EIA 364-103 Cet essai permet d'assurer que les signaux des lignes D+ et D− de l'ensemble adaptateur atteignent le récepteur en même temps.	20 ps au maximum. Temps de montée: 400 ps (20 % à 80 %).
Perte d'insertion différentielle	EIA 364-101 Cet essai permet d'assurer que la paire D+/D− d'un ensemble adaptateur peut fournir l'alimentation de signal adéquate au récepteur.	−0,7 dB au maximum à 400 MHz
Résistance en courant continu D+ ou D−	Cet essai permet d'assurer que la plage de résistances en courant continu du fil D+/D− est correcte afin de prévoir le niveau d'EOP et de régler le niveau de déconnexion de l'***USB 2.0***.	2,5 Ω au maximum.

3.7.6.2 Ensemble adaptateur-fiche USB Type-C Complet vers embase *USB 3.1* Standard-A

L'ensemble adaptateur-fiche USB Type-C Complet vers embase ***USB 3.1*** Standard–A est prévu pour une utilisation avec un dispositif à connexion directe (par exemple, une clé USB). Le fonctionnement d'un système n'est pas garanti lors de l'utilisation d'un ensemble adaptateur avec un ensemble câble-connecteurs USB normalisé.

Pour réduire le plus possible l'incidence de l'ensemble adaptateur sur l'intégrité du signal système, ***il convient que*** l'ensemble adaptateur remplisse les objectifs de conception ***informatifs*** donnés dans le Tableau 3-34.

Tableau 3-34 Objectifs de conception pour les ensembles adaptateurs USB Type-C vers *USB 3.1* Standard-A (*informatifs*)

Éléments	Objectifs de conception
Facteur d'adaptation différentiel	≤ −15 dB à 5 GHz Normalisé avec 85 Ω.
Perte d'insertion différentielle	≥ −2,4 dB à 2,5 GHz, ≥ −3,5 dB à 5 GHz
NEXT différentielle entre les paires SuperSpeed	≤ −40 dB à 2,5 GHz ≤ −34 dB à 5 GHz
NEXT et FEXT différentielles entre les paires D+/D− et SuperSpeed	≤ −30 dB à 2,5 GHz

Les exigences ***normatives*** relatives à l'ensemble adaptateur sont définies dans le Tableau 3-33 et dans le Tableau 3-35. La longueur totale de l'ensemble adaptateur est limitée à 150 mm au maximum.

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Tableau 3-35 Exigences relatives à l'intégrité du signal pour un ensemble adaptateur USB Type-C vers embase *USB 3.1* Standard-A (*normatives*)

Éléments	Descriptions et procédures	Exigences
Ajustement de la perte d'insertion différentielle à la fréquence de Nyquist (ILfitatNq)	ILfitatNq est évalué à la fréquence de Nyquist SuperSpeed Gen 1.	≥ −2,4 dB à 2,5 GHz ≥ −3,5 dB à 5 GHz
Multiréflexion différentielle intégrée (IMR)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −38 dB, Tb = 200 ps ≤ −27 dB, Tb = 100 ps
Diaphonie différentielle intégrée sur SuperSpeed (ISSXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}(\lvert Vin(f)\rvert^2\lvert NEXTs(f)\rvert^2 + \lvert Vdd(f)\rvert^2\lvert NEXTd(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ où: *NEXTs* = NEXT entre les paires SuperSpeed *NEXTd* = NEXT entre les paires D+/D− et SuperSpeed *Vdd(f)* = spectre d'une impulsion en entrée sur la paire D+/D−, évalué au moyen de l'équation représentée à la Figure 3-40 avec Tb (UI) = 2.08 ns.	≤ −37 dB
Diaphonie différentielle intégrée sur D+/D- (IDDXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + \lvert FEXT(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ où: *NEXT* = paradiaphonie entre SuperSpeed et D+/D− *FEXT* = télédiaphonie entre SuperSpeed et D+/D− *fmax* = 1,2 GHz	≤ −30 dB
Facteur d'adaptation intégré (IRL)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2 + \lvert SDD22(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −14,5 dB, Tb = 200 ps ≤ −12,0 dB, Tb = 100 ps
Mode différentiel en mode commun	Conversion du mode différentiel en mode commun (SCD12, SCD21)	≤ −15 dB
Note: *fmax* = 7,5 GHz; *Vin(f)* est défini à la Figure 3-40 avec Tb (UI) = 200 ps; et *Vdd(f)* est également spécifié à la Figure 3-40 avec Tb (UI) = 2,08 ns.		

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3.7.6.3 Embases USB existantes conformes utilisées dans les ensembles adaptateur USB Type-C vers USB existant

3.7.6.3.1 Exigences relatives aux matériaux de contact

Pour consulter les exigences relatives aux matériaux de contact qui s'appliquent aux embases USB Standard-A et USB Micro-B existantes utilisées dans les ensembles adaptateurs USB Type-C vers existant, voir 3.7.5.3.1.

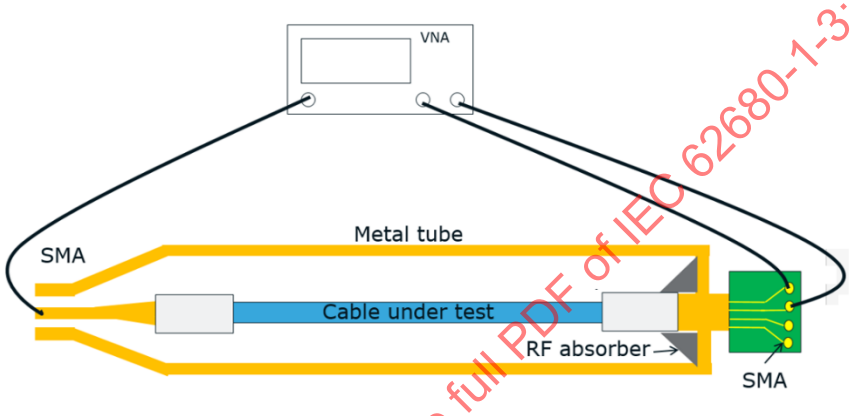
3.7.6.3.2 Courant assigné de contact

Pour consulter les exigences relatives aux courants assignés des contacts qui s'appliquent aux embases USB Standard-A et USB Micro-B existantes utilisées dans les ensembles adaptateurs USB Type-C vers existant, voir 3.7.5.3.2.

3.7.7 Exigences relatives à l'efficacité de l'écrantage (*normatives*)

L'essai d'efficacité de l'écrantage (SE) de l'ensemble de câbles mesure le niveau des perturbations électromagnétiques (EMI) et radioélectriques (RFI) émises par l'ensemble câble-connecteurs. Pour réaliser le mesurage, l'ensemble câble-connecteurs ***doit*** être installé dans le montage d'essai SE du câble, comme cela est représenté à la Figure 3-64. Les facteurs de couplage entre le câble et le montage se caractérisent par un analyseur de réseau vectoriel (VNA).

Figure 3-64 Essai d'efficacité de l'écrantage d'un ensemble câble-connecteurs

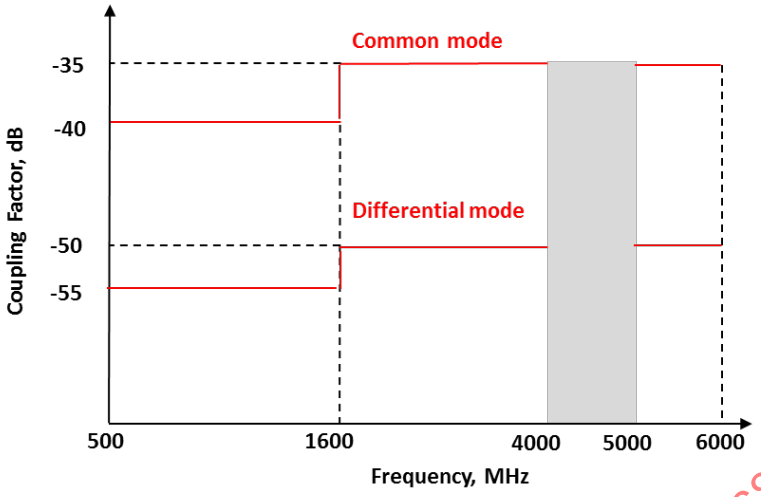


Anglais	Français
Metal Tube	Tube métallique
Cable under test	Câble en essai
RF Absorber	Absorbeur RF

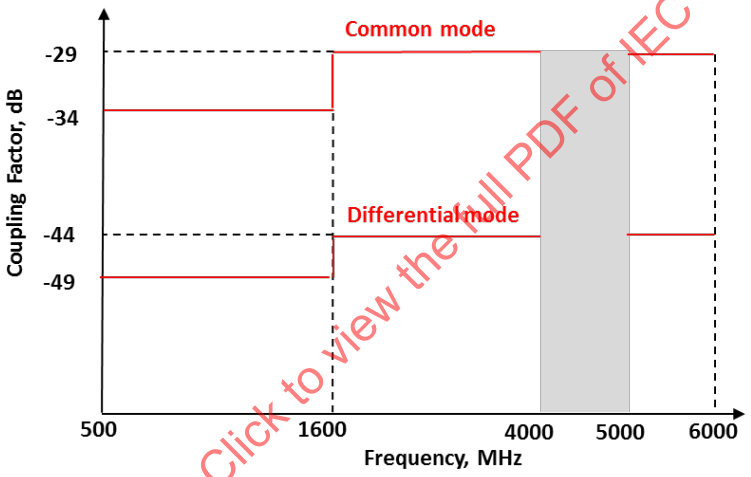
Pour être conformes, tous les ensembles câble-connecteurs USB Type-C ***doivent*** satisfaire à l'essai d'efficacité de l'écrantage. La Figure 3-65 représente les critères de réussite et d'échec pour (a) les ensembles câble-connecteurs USB Type-C vers USB Type-C, (b) les ensembles câble-connecteurs USB Type-C vers USB existant et (c) les ensembles adaptateurs USB Type-C vers embase ***USB 3.1*** Standard-A. Noter que l'efficacité de l'écrantage pour la bande de fréquences comprise entre 4 GHz et 5 GHz n'est pas spécifiée, car aucune antenne ne fonctionne dans cette plage de fréquences.

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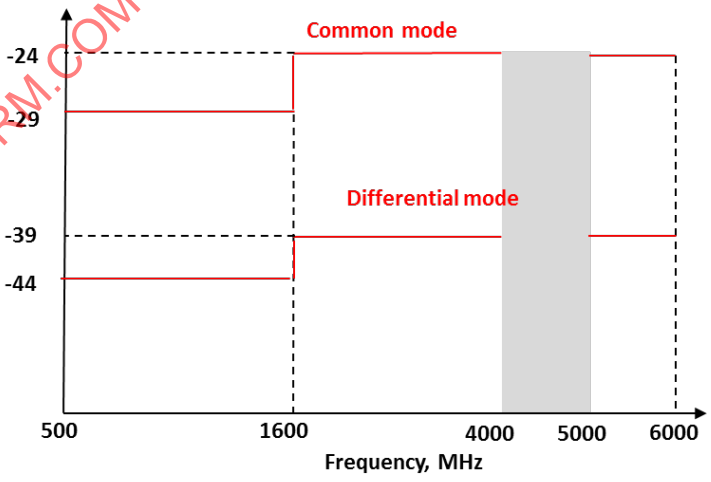
Figure 3-65 Critères de réussite et d'échec pour l'efficacité de l'écrantage



(a) For USB Type-C to USB Type-C Cable Assemblies



(b) For USB Type-C to legacy USB Cable Assemblies



(c) For USB Type-C to USB3.1 Standard-A Receptacle Adapter Assembly

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Anglais	Français
Coupling Factor	Facteur de couplage
Frequency, MHz	Fréquence, MHz
For USB Type-C to USB Type-C Cable Assemblies	Pour les ensembles câble-connecteurs USB Type-C vers USB Type-C
For USB Type-C to legacy USB Cable Assemblies	Pour les ensembles câble-connecteurs USB Type-C vers USB existant
For USB Type-C to USB3.1 Standard-A Receptacle Adapter Assembly	Pour les ensembles adaptateurs USB Type-C vers embase USB 3.1 Standard-A
Common Mode	Mode commun
Differential Mode	Mode différentiel

3.7.8 Exigences électriques en courant continu (*normatives*)

Sauf indication contraire, les essais décrits ci-dessous sont réalisés sur des paires de connecteurs couplés.

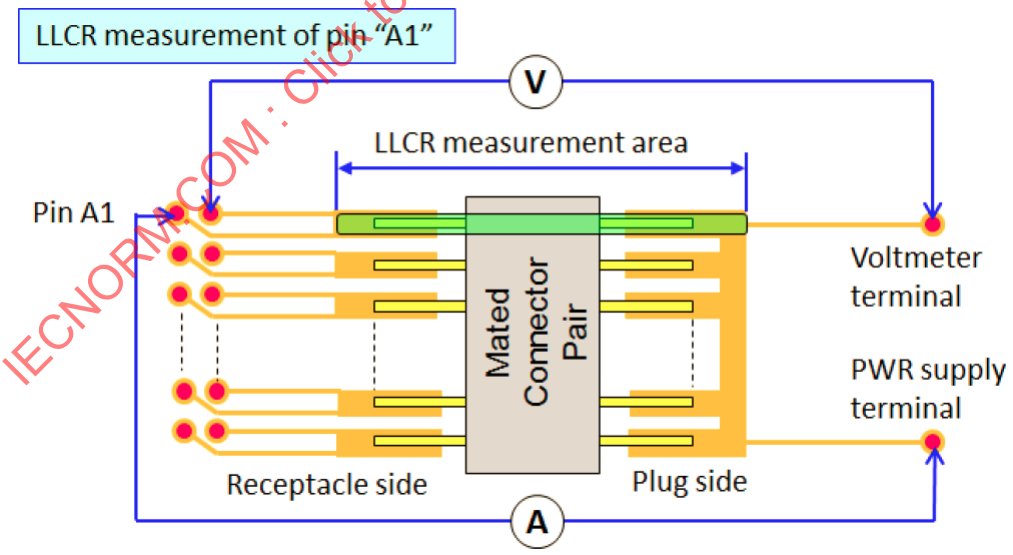
3.7.8.1 Résistance de contact à faible niveau (EIA 364-23B)

Le mesurage de la résistance de contact à faible niveau (LLCR) est réalisé sur les contacts couplés de la fiche et de l'embase. Il ne s'applique pas aux cartes d'accès internes ni aux sous-couches de la fiche ou de l'embase. Voir la Figure 3-66. Les mesures suivantes s'appliquent aux contacts d'alimentation et de signal:

- 40 mΩ (valeur maximale) initiaux pour les contacts V, GND et tous les autres;
- 50 mΩ (valeur maximale) après l'application de contraintes environnementales;
- mesure à 20 mV (valeur maximale) en circuit ouvert à 100 mA.

Pour obtenir les exigences environnementales et les séquences d'essai, voir 3.8.

Figure 3-66 Diagramme de mesure de la LLCR



Anglais	Français
LLCR measurement of pin "A1"	Mesurage de la LLCR sur la broche "A1"
Pin A1	Broche A1

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Anglais	Français
LLCR measurement area	Zone de mesure de la LLCR
Receptacle side	Côté embase
Mated Connector Pair	Paire de connecteurs couplés
Plug side	Côté fiche
Voltmeter terminal	Borne du voltmètre
PWR supply terminal	Borne d'alimentation PWR

3.7.8.2 Rigidité diélectrique (EIA 364-20)

Aucune panne ***ne doit*** se produire lors de l'application d'une tension alternative de 100 V (valeur efficace) entre les contacts adjacents des connecteurs couplés et non couplés.

3.7.8.3 Résistance d'isolation (EIA 364-21)

Une résistance d'isolation minimale de 100 MΩ est exigée entre les contacts adjacents des connecteurs couplés et non couplés.

3.7.8.4 Courant assigné des contacts

L'essai portant sur le courant assigné du connecteur USB Type-C (fiche et embase) ***doit*** être réalisé conformément aux procédures et au montage suivants:

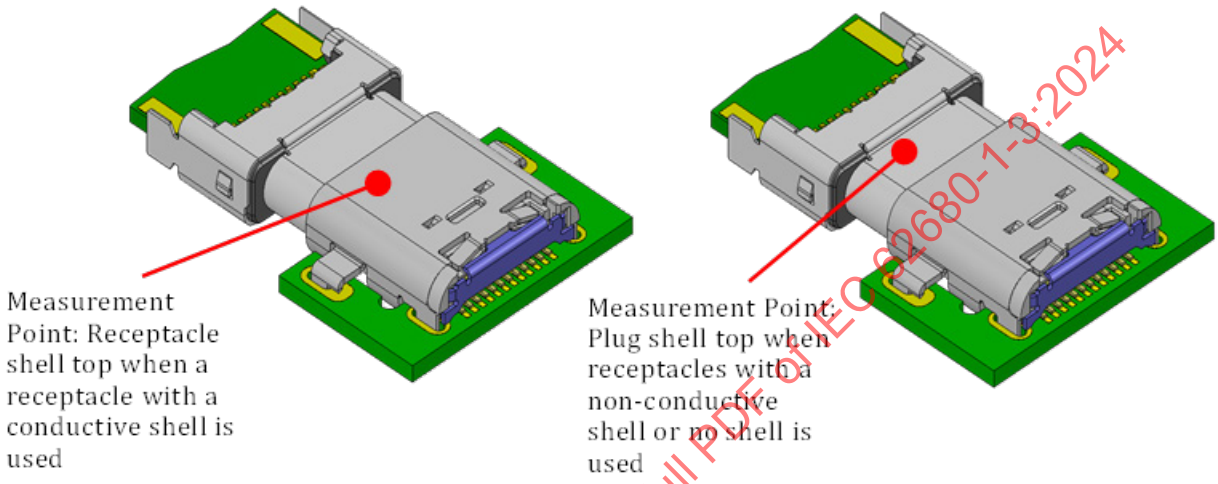
- Un courant de 5 A ***doit*** être appliqué collectivement aux broches VBUS (à savoir aux broches A4, A9, B4 et B9) et un courant de 1,25 A ***doit*** être appliqué à la broche VCONN (à savoir à la broche B5), le cas échéant, terminés par les broches GND correspondantes (à savoir les broches A1, A12, B1 et B12). Un courant minimal de 0,25 A ***doit*** également, le cas échéant, être appliqué séparément à tous les autres contacts. Lorsque le courant est appliqué aux contacts, la température de la paire de connecteurs ***doit*** pouvoir se stabiliser. L'échauffement de la surface de l'enveloppe externe de la paire couplée au-dessus des contacts VBUS et GND ***ne doit pas*** dépasser la température ambiante de 30 °C. La Figure 3-67 représente l'emplacement de mesure.
- Le mesurage ***doit*** être réalisé sous air statique.
- Les connecteurs ***doivent*** être orientés de telle sorte que la surface de l'enveloppe externe accessible soit sur le dessus, horizontalement par rapport au sol.
- La fiche et l'embase ***peuvent*** exiger une modification pour accéder aux connexions brasées ou aux points de raccordement du câble.
- La méthode par thermocouple ou imagerie thermique (préférentielle) ***peut*** être utilisée pour mesurer la température.
- Pour la certification, le fabricant du connecteur ***doit*** fournir les échantillons de l'embase et de la fiche en essai, montés sur une CCI d'essai du courant assigné, sans plaque de cuivre. Les différents points de branchement de la fiche de câble ***peuvent*** être raccordés par des fils courts, en lieu et place d'une CCI d'essai du courant assigné.

Les CCI d'essai du courant assigné ***doivent*** avoir une structure à 2 couches. Si la structure à deux couches n'est pas possible, en raison de la configuration des connexions brasées, les pistes VBUS et de masse ***doivent*** se situer sur les couches externes, les couches internes étant réservées aux pistes de signal, selon les exigences. Les pistes VCONN ***peuvent*** être routées sur les couches internes ou externes. Le Tableau 3-36 définit les exigences relatives à l'épaisseur et aux pistes de la CCI d'essai. La longueur de piste s'applique à chaque CCI (CCI de l'embase et CCI de la fiche) et court de la borne de contact jusqu'au point de raccordement de la source de courant.

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- Figure 3-68 représente la piste partielle ***informative*** de la CCI d'essai du courant assigné.
- Si la CCI d'essai du courant assigné est remplacée par des fils courts, la longueur de fil ***ne doit pas*** dépasser 70 mm, lorsqu'elle est mesurée du point de brasure du contact de la fiche jusqu'à l'autre extrémité du fil. Aucune carte d'accès ni aucun surmoulage ***ne doit*** être inclus dans le montage d'essai. Chaque connexion brasée de la fiche ***doit*** être branchée à un fil de calibre AWG 36 pour les signaux, AWG 32 pour l'alimentation (VBUS et VCONN) et AWG 30 pour la masse.

Figure 3-67 Point de mesure de la température



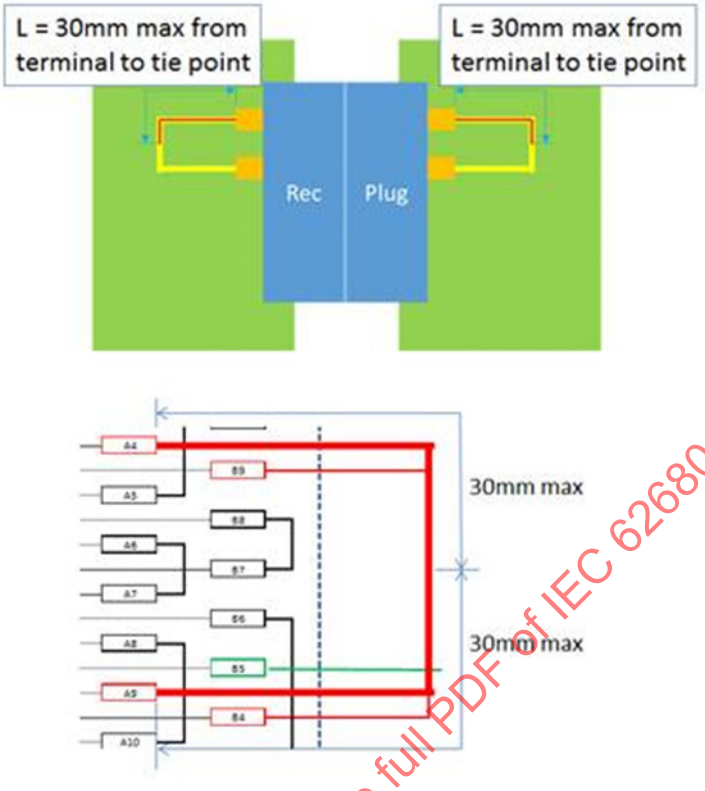
Anglais	Français
Measurement Point: Receptacle shell top when a receptacle with a conductive shell is used	Point de mesure: Haut de l'enveloppe de l'embase si une embase à enveloppe conductrice est utilisée
Measurement Point: Plug shell top when receptacles with a non-conductive shell or no shell is used	Point de mesure: Haut de l'enveloppe de la fiche si des embases à enveloppe non conductrice sont utilisées ou si aucune enveloppe n'est utilisée

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Tableau 3-36 CCI d'essai du courant assigné

Éléments	Largeur de piste (mm)	Longueur de piste (mm) sur chaque CCI	Épaisseur
Piste de signal	0,25 au maximum	13 au maximum	35 µm (1 oz de cuivre)
Piste de masse	1,57 au maximum	38 au maximum	35 µm (1 oz de cuivre)
VBUS et VCONN	1,25 au maximum	30 au maximum	35 µm (1 oz de cuivre)
CCI	***N/A***	***N/A***	0,80 mm à 1,20 mm

Figure 3-68 Exemple de configuration de la piste de montage pour l'essai du courant assigné



Anglais	Français
L = 30 mm max from terminal to tie point	L = 30 mm au maximum de la borne au point de raccordement
Rec	Embase
Plug	Fiche

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3.7.8.5 Résistance en courant continu de D+ et D–

La résistance en courant continu de D+ et D– dans les dispositifs USB Type-C compatibles ***USB 2.0*** à grande vitesse et les dispositifs USB Type-C captifs compatibles ***USB 2.0*** à grande vitesse ***doit*** être inférieure ou égale à la valeur maximale spécifiée dans le Tableau 3-37. La résistance en courant continu de D+ et D– est la combinaison série de toutes les résistances dans les commutateurs, multiplexeurs et la PHY USB.

Tableau 3-37 Exigence concernant la résistance en courant continu maximale (*normative*)

	Résistance en courant continu maximale
Hôtes, hubs ou hôtes/dispositifs double fonction USB Type-C (compatibles *USB 2.0* à grande vitesse)	13 Ω
Dispositif USB Type-C uniquement (compatible *USB 2.0* à grande vitesse)	17 Ω
Dispositif USB Type-C captif (compatible *USB 2.0* à grande vitesse)	23 Ω

Un hôte USB Type-C qui fonctionne en mode ***USB 2.0*** à grande vitesse ***doit*** mettre en œuvre le niveau de tension de seuil de déconnexion (V_{HSDSC}) défini dans l'ECN DCR ***USB 2.0***.

3.8 Exigences mécaniques et environnementales (*normatives*)

Les exigences décrites dans le présent paragraphe s'appliquent à tous les connecteurs et/ou ensembles câble-connecteurs USB Type-C, sauf spécification contraire. Pour les fiches et les ensembles câble-connecteurs USB Type-C, les méthodes d'essai reposent sur l'hypothèse que le câble sort du surmoulage dans la même direction de couplage vers une embase USB Type-C (donc il sort tout droit de la partie arrière du surmoulage). Pour les fiches et les ensembles câble-connecteurs USB Type-C dont le câble ne sort pas directement de l'arrière du surmoulage (donc en angle droit par rapport à la direction de couplage), les montages et les procédures d'essai ***doivent*** être modifiés selon les besoins pour réaliser le mesurage.

3.8.1 Exigences mécaniques

3.8.1.1 Force d'insertion (EIA 364-13)

La force d'insertion du connecteur initial ***doit*** être comprise entre 5 N et 20 N à un débit maximal de 12,5 mm (0,492") par minute. Cette exigence ne s'applique pas lorsque les connecteurs sont utilisés dans une station d'accueil.

Il est recommandé d'enduire le mécanisme de verrouillage d'un lubrifiant sans silicium afin de réduire l'usure. ***Il convient de*** limiter l'usage des lubrifiants aux caractéristiques d'insertion et d'extraction, et ***il convient*** qu'ils n'augmentent pas la résistance de la connexion couplée.

3.8.1.2 Force d'extraction (EIA 364-13)

La force d'extraction du connecteur initial ***doit*** être comprise entre 8 N et 20 N, mesurée par suite d'un préconditionnement en cinq cycles d'insertion/extraction (soit la sixième extraction). Après vingt-cinq cycles d'insertion/extraction supplémentaires, la force d'extraction ***doit*** à nouveau être mesurée (soit la 32e extraction). Elle ***doit***:

a. correspondre à 33 % du relevé initial; et

b. être comprise entre 8 N et 20 N.

La force d'extraction ***doit*** être comprise entre 6 N et 20 N après 10 000 cycles d'insertion/extraction. La force d'extraction ***doit*** être mesurée à une vitesse maximale de 12,5 mm (0,492") par minute. L'exigence concernant la force d'extraction ne s'applique pas lorsque les connecteurs sont utilisés dans une station d'accueil mécanique.

Il est recommandé d'enduire le mécanisme de verrouillage d'un lubrifiant sans silicium afin de réduire l'usure. ***Il convient de*** limiter l'usage des lubrifiants aux caractéristiques d'insertion et d'extraction, et ***il convient*** qu'ils n'augmentent pas la résistance de la connexion couplée.

3.8.1.3 Durabilité ou cycles d'insertion/extraction (EIA 364-09)

La valeur assignée de durabilité ***doit*** être de 10 000 cycles au minimum pour la famille de connecteurs USB Type-C. L'essai de durabilité ***doit*** être réalisé à un débit de (500 ± 50) cycles par heure. Aucune partie du connecteur ni de l'ensemble câble-connecteurs ne ***doit*** subir de dommage physique.

3.8.1.4 Flexion du câble (EIA 364-41, Condition 1)

L'ensemble câble-connecteurs ne ***doit*** subir aucun dommage physique ni aucune discontinuité de plus de 1 ms pendant sa flexion, avec une dimension X = 22 mm et 500 cycles dans chacun des deux plans.

3.8.1.5 Arrachement du câble (EIA 364-38, Méthode A)

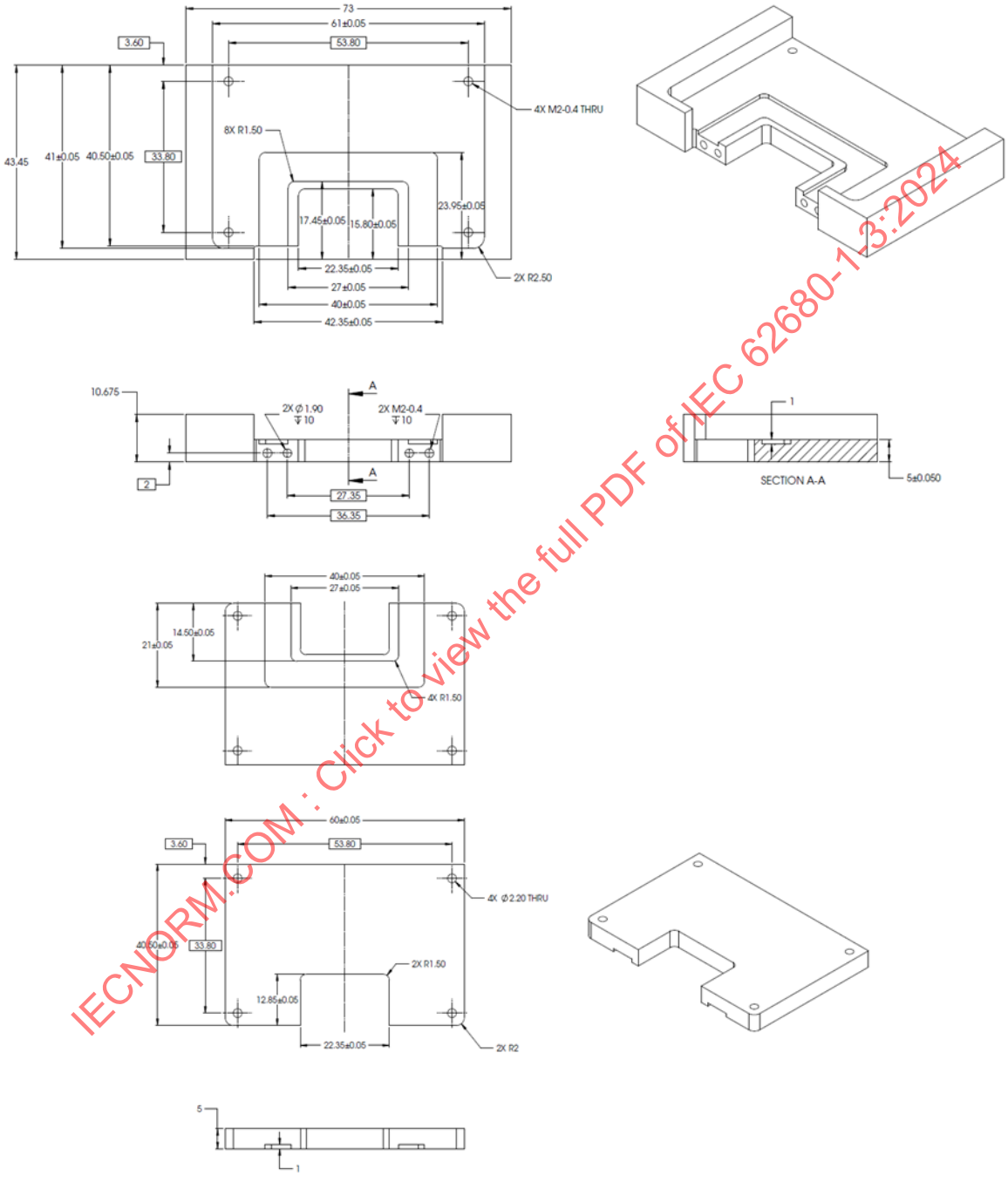
L'ensemble câble-connecteurs ne ***doit*** subir aucun dommage physique lorsqu'il est soumis à une charge axiale de 40 N pendant au moins 1 min lors du serrage d'une extrémité de la fiche de câble.

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3.8.1.6 Essai de continuité sur 4 axes

La famille de connecteurs USB Type-C ***doit*** être soumise à un essai de continuité sous contrainte, au moyen du montage d'essai représenté à la Figure 3-69, ou équivalent.

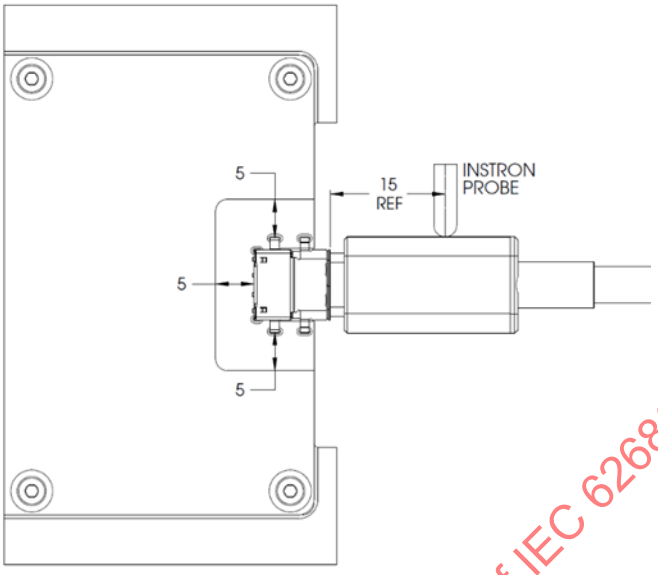
Figure 3-69 Exemple de montage d'essai de continuité sur 4 axes



Anglais	Français
Section A-A	Coupe A-A

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Figure 3-69 Exemple de montage d'essai de continuité sur 4 axes (suite)



Anglais	Français
INSTRON PROBE	SONDE INSTRON
REF	RÉF

Les fiches ***doivent*** être fournies avec un surmoulage représentatif ou être montées sur une carte de circuit imprimé (CCI) à deux couches dont l'épaisseur, le cas échéant, est comprise entre 0,8 mm et 1,0 mm. Une embase USB Type-C ***doit*** être montée sur une CCI à deux couches, dont l'épaisseur est comprise entre 0,8 mm et 1,0 mm. La CCI ***doit*** être serrée des trois côtés de l'embase à une distance maximale de 5 mm du contour de l'embase. La CCI de l'embase ***doit*** être initialement placée sur une surface horizontale, puis un moment perpendiculaire ***doit*** être appliqué à la fiche avec une sonde à bout arrondi de 5 mm pendant 10 s au moins, à une distance de 15 mm du bord de contact de l'enveloppe de l'embase, vers le bas et perpendiculairement à l'axe d'insertion. Voir le Tableau 3-38 pour obtenir la force et le moment à appliquer. Toutes les configurations d'embase à enveloppe non conductrice ***doivent*** être soumises à l'essai aux valeurs spécifiées pour la configuration d'embase verticale.

Tableau 3-38 Exigences relatives à la force et au moment

Configuration de l'embase par rapport à la surface de montage	Force à 15 mm du bord de contact de l'enveloppe de l'embase (N)	Moment par rapport au bord de contact de l'enveloppe de l'embase (Nm)
Angle droit	20	0,30
Verticale[1]	8	0,12

Notes:

1. Toutes les configurations d'embase à enveloppe non conductrice ***doivent*** être soumises à l'essai aux valeurs spécifiées pour la configuration d'embase verticale.

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La continuité sur chaque contact ***doit*** être mesurée en appliquant la force de traction. Chaque contact non relié à la masse ***doit*** également être soumis à l'essai pour confirmer qu'il ne crée pas de court-circuit dans l'enveloppe pendant les tensions. La CCI ***doit*** ensuite subir une rotation de 90° de sorte que le câble reste inséré horizontalement, et la force de traction indiquée dans le Tableau 3-38 ***doit*** être à nouveau appliquée vers le bas et la continuité mesurée comme précédemment. Cet essai est répété pour les rotations à 180° et à 270°. Les câbles traversants ***ne doivent*** présenter aucune discontinuité ni créer de court-circuit supérieur à 1 µs dans l'enveloppe, quelle que soit l'orientation.

L'une des méthodes de mesure de la continuité par les contacts consiste à court-circuiter tous les fils à l'extrémité de la fibre amorce du câble et d'appliquer une tension par la polarisation de chaque broche VBUS, USB D+,

USB D−, SBU, CC et TX/RX, les broches GND étant reliées à la masse.

D'autres méthodes sont admises pour vérifier la continuité par l'ensemble des broches.

3.8.1.7 Résistance à l'arrachement

Les fiches USB Type-C sur les ensembles câble-connecteurs et les fiches de montage sans surmoulage (y compris les fiches USB Type-C montées dans la CCI) ***doivent*** être soumises à l'essai au moyen du montage d'essai de la résistance à l'arrachement mécanique défini dans le document de conformité des connecteurs et des ensembles câble-connecteurs Universal Serial Bus Type-C. Pour les fiches sans surmoulage, le fournisseur ***doit*** fournir un montage d'essai de fiche conforme aux dimensions spécifiées pour le surmoulage de la fiche USB Type-C (voir la Figure 3-70). Le montage ***peut*** être en métal ou tout autre matériau adapté. Des moments perpendiculaires sont appliqués à la fiche avec une sonde à bout arrondi de 5 mm pendant au moins 10 s, le connecteur étant inséré dans le montage d'essai pour atteindre les moments définis dans les quatre directions, vers le haut ou vers le bas (c'est-à-dire perpendiculaire à l'axe long de l'ouverture de la fiche) et vers la gauche ou vers la droite (c'est-à-dire dans le plan de l'ouverture de la fiche). Les connecteurs conformes ***doivent*** satisfaire aux limites de force suivantes:

- Un moment de 0 Nm à 0,75 Nm (par exemple, 50 N à une distance de 15 mm du bord de l'embase) est appliqué à une fiche insérée dans le montage d'essai dans chacune des quatre directions. Une seule fiche ***doit*** être utilisée pour cet essai. Des déformations mécaniques ***peuvent*** se produire. La fiche ***doit*** être couplée avec le montage d'essai de continuité, après avoir appliqué les forces d'essai pour vérifier qu'aucun dommage ayant entraîné une discontinuité ou un court-circuit n'a été subi. Le montage d'essai de continuité ***doit*** posséder une surface plane côté couplage, située à une distance de 6,20 mm ± 0,20 mm du plan de référence A de l'embase, perpendiculairement à la direction d'insertion. Aucune force de moment n'est appliquée à la fiche pendant cet essai de continuité. La Figure 3-71 représente un exemple de montage pour l'essai de continuité. L'essai de tension de tenue diélectrique ***doit*** être réalisé après l'essai de continuité afin de vérifier la conformité de la fiche.

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Figure 3-70 Exemple de montage d'essai de résistance à l'arrachement pour les fiches sans surmoulage

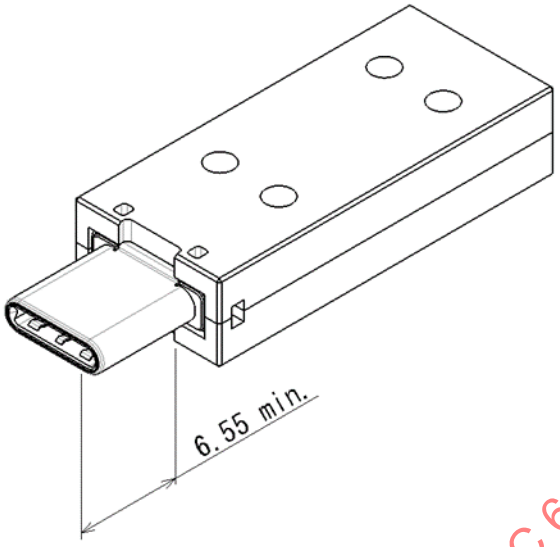
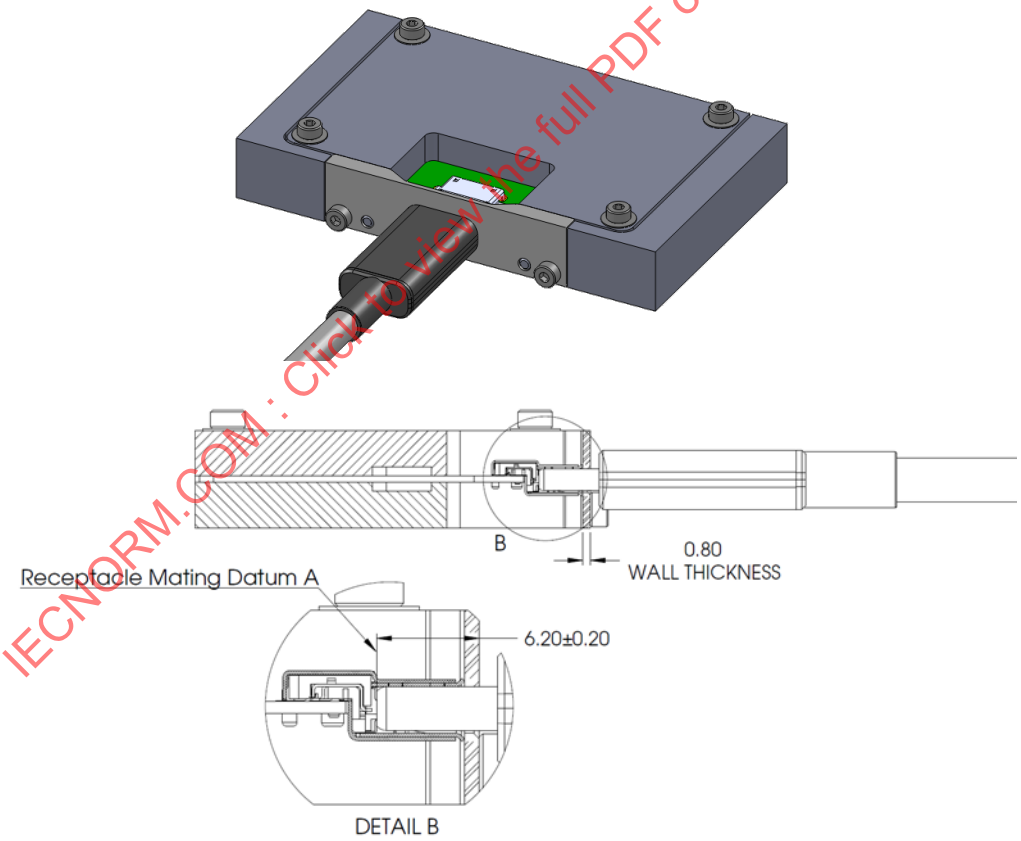


Figure 3-71 Montage d'essai de continuité/résistance à l'arrachement de référence



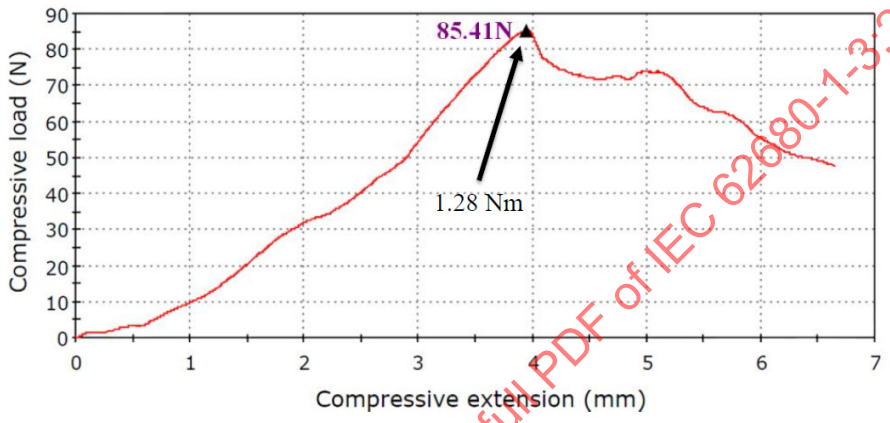
Anglais	Français
Receptacle Mating Datum A	Couplage de l'embase réf A
DETAIL B	ÉLÉMENT B

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Anglais	Français
WALL THICKNESS	ÉPAISSEUR DE LA PAROI

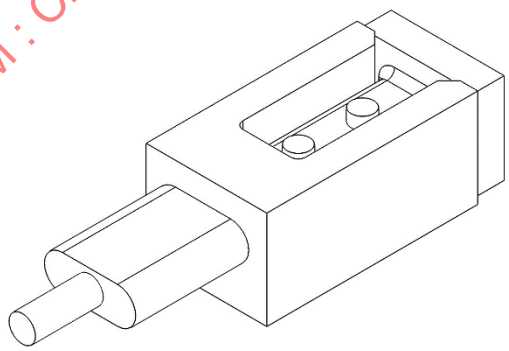
- La fiche ***doit*** être retirée du montage d'essai ou présenter une défaillance mécanique (c'est-à-dire la force appliquée pendant la procédure d'essai atteint la limite maximale et chute) lorsqu'un moment de 2,0 Nm est appliqué à la fiche vers le haut et vers le bas, et qu'un moment de 3,5 Nm est appliqué à la fiche vers la gauche et vers la droite. Une nouvelle fiche doit être utilisée pour chacune des quatre directions d'essai. La Figure 3-72 et la Figure 3-73 représentent un exemple de point de défaillance mécanique et un montage d'essai de résistance à l'arrachement.

Figure 3-72 Exemple de point de défaillance mécanique pour l'essai de résistance à l'arrachement



Anglais	Français
Compressive load (N)	Charge de compression (N)
Compressive extension (mm)	Déformation à la compression (mm)

Figure 3-73 Essai de résistance à l'arrachement avec un câble dans le montage



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3.8.1.8 Limitation de l'utilisation des substances dangereuses

Il est recommandé que les composants soient conformes à la directive RoHS.

3.8.2 Exigences environnementales

Les essais environnementaux portant sur l'interface des connecteurs ***doivent*** satisfaire à l'EIA 364-1000.01, "Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications".

Étant donné que le connecteur défini possède une surface de frottement de longueur supérieure à 0,127 mm, le Groupe d'essai 6 de l'EIA 364-1000.01 n'est pas exigé. Les valeurs de durée des essais Durée de température et Mélange de gaz sont tirées de l'EIA 364-1000.01, selon la température de champ du tableau suivant.

Tableau 3-39 Conditions d'essai environnementales

Température et durée pour l'essai Durée de température	105 °C pendant 120 heures
Température et durée pour l'essai Durée de température pour le préconditionnement	105 °C pendant 72 heures
Durée de l'essai Mélange de gaz	7 jours

Le critère de réussite et d'échec pour la résistance de contact à faible niveau (LLCR) est défini en 3.7.8.1. Les valeurs assignées de durabilité sont définies au 3.8.1.3.

3.8.2.1 Matériaux de référence (*informatifs*)

La présente spécification ne spécifie pas les matériaux des connecteurs et des câbles. ***Il convient que*** les fabricants de connecteurs et de câbles choisissent des matériaux appropriés en fonction de leurs exigences de performance. Les informations ci-dessous sont données à titre de référence uniquement.

Note: ***Il convient que*** les fabricants de connecteurs et de câbles répondent aux exigences de placage des contacts selon les options suivantes:

Option I

Embase: Zone de contact: (Min) 0,05 µm Au + (Min) 0,75 µm Ni-Pd sur (Min) 2,0 µm Ni

Fiche: Zone de contact: (Min) 0,05 µm Au + (Min) 0,75 µm Ni-Pd sur (Min) 2,0 µm Ni

Option II

Embase: Zone de contact: (Min) 0,75 µm Au sur (Min) 2,0 µm Ni

Fiche: Zone de contact: (Min) 0,75 µm Au sur (Min) 2,0 µm Ni

Les autres matériaux de référence, choisis par les fabricants de connecteurs et de câbles en fonction des paramètres de performance, répertoriés dans le Tableau 3-40 sont donnés à titre de référence uniquement.

Tableau 3-40 Matériaux de référence

Composant	Matériau
Câble	Conducteur: cuivre avec placage en plomb ou en argent
	Écrantage du SDP: Feuille d'aluminium ou feuille d'aluminium/de mylar
	Écrantage coaxial: toron de cuivre
	Tresse: Cuivre ou aluminium étamé
	Gaine: Matériau de substitution en PVC ou sans halogène
Surmoulage du câble	Plastique thermodurci ou thermoplastique
Enveloppes de connecteur	Acier inoxydable ou bronze phosphoreux
Verrou latéral de la fiche	Acier inoxydable
Plaque médiane de l'embase	Acier inoxydable
Ressort CEM interne de la fiche	Acier inoxydable ou alliage de cuivre hautement résistant à la déformation
Plaque CEM de l'embase	Acier inoxydable ou bronze phosphoreux
Enveloppe de l'embase	Acier inoxydable ou bronze phosphoreux

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Composant	Matériau
Languette de l'embase	Nylon chargé en verre
Boîtier	Thermoplastiques capables de supporter la température de brasure sans plomb
Note: ***Il convient de*** prendre en compte les matériaux sans halogène pour l'ensemble des plastiques.	

3.9 Applications d'accueil (*informatives*)

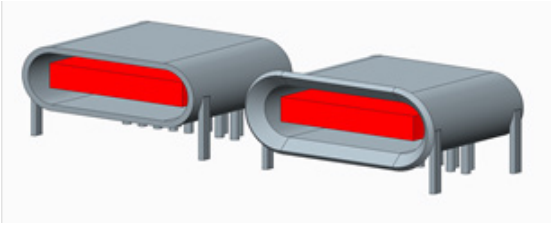
Dans la présente spécification, le terme "accueil" fait référence au branchement d'un dispositif directement dans une station d'accueil sans utiliser d'ensemble câble-connecteurs. Le connecteur USB Type-C est défini pour prendre en charge ces applications.

Il n'est qu'une partie d'une solution d'accueil. Au niveau du système, une solution d'accueil complète ***peut*** également inclure des mécanismes de maintien ou de verrouillage, des mécanismes d'alignement, des solutions de montage de fiche pour l'accueil et des protocoles pris en charge par le connecteur. La présente spécification n'essaie pas de normaliser les solutions d'accueil de système; il n'existe donc pas d'exigence d'interopérabilité pour les solutions d'accueil.

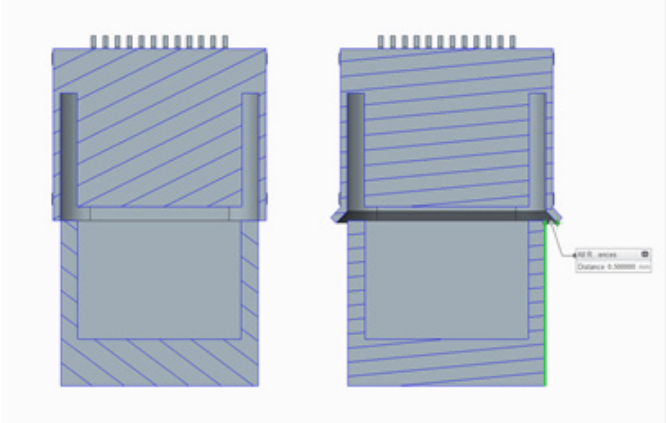
La liste suivante répertorie les exigences et les lignes directrices pour l'utilisation du connecteur USB Type-C à des fins d'accueil:

1. La fiche USB Type-C utilisée pour l'accueil ***doit*** fonctionner avec l'embase USB Type-C conforme. Elle ***doit*** satisfaire aux exigences dimensionnelles, électriques et mécaniques.
2. Si la fiche sur la station d'accueil ne possède pas de verrous latéraux, ***il convient que*** la station d'accueil comporte un mécanisme de maintien ou de verrouillage afin de fixer le dispositif à la fiche. Les verrous de maintien servent également de chemin de retour à la masse pour la CEM. ***Il convient que*** la conception de la station d'accueil assure des performances CEM adéquates sans les verrous latéraux, s'ils ne sont pas présents.
3. Les doigts CEM internes ne sont pas exigés pour la fiche d'accueil tant que les enveloppes de l'embase et de la fiche possèdent une connexion électrique adéquate.
4. L'alignement est un facteur important pour l'accueil. Selon la conception du système, les connecteurs USB Type-C normalisés seuls ***peuvent ne pas*** présenter un alignement adéquat pour le couplage. Un alignement au niveau du système est fortement recommandé. Les solutions d'alignement sont propres à chaque mise en œuvre.
5. Un alignement correct est fourni par le connecteur. La face avant de l'embase ***peut*** avoir des caractéristiques d'entrée pour permettre un bon alignement. La Figure 3-74 représente un exemple d'embase USB Type-C avec une collerette de guidage par comparaison à une embase sans collerette.

Figure 3-74 Exemple de collerette pour une embase de câble USB Type-C



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3.10 Notes relatives à la mise en œuvre et guides de conception

Le présent paragraphe fournit des notes relatives à la mise en œuvre et des guides de conception afin d'aider les utilisateurs à concevoir et à utiliser les connecteurs et câbles USB Type-C.

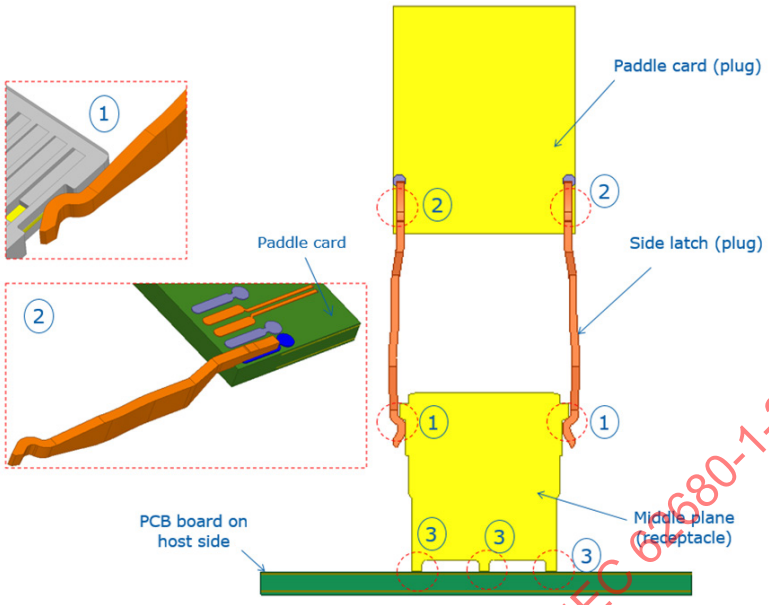
3.10.1 Gestion de la CEM (*informative*)

Il convient que les concepteurs de connecteurs et d'ensembles câble-connecteurs, ainsi que les responsables de la mise en œuvre des systèmes, prêtent attention à l'écrantage de l'embase et de l'ensemble câble-connecteurs afin d'assurer un chemin de mise à la masse de faible impédance. Les lignes directrices suivantes s'appliquent à la gestion de la CEM:

- ***Il convient de*** vérifier la qualité des câbles bruts. L'obliquité dans les paires ou la conversion du mode différentiel en mode commun des paires TX/RX a une incidence significative sur la CEM des câbles et ***il convient de*** les contrôler dans les limites de la présente spécification.
- ***Il convient que*** la tresse externe du câble soit physiquement connectée à l'enveloppe en métal de la fiche sous un angle qui approche autant que possible les 360°, afin de contrôler la CEM. En l'absence d'une terminaison de sortie convenablement écrantée, même un câble parfait sans aucune obliquité dans les paires ***peut*** ne pas satisfaire aux exigences de la CEM. Il ***peut*** être nécessaire d'utiliser un ruban de cuivre pour écranter la zone de la terminaison de la tresse.
- La terminaison du fil contribue au bruit de mode commun. ***Il convient de*** réduire le plus possible la distance de branchement de la terminaison du fil afin d'optimiser les performances de CEM et d'intégrité du signal. Si possible, ***il convient que*** les deux lignes d'une paire différentielle restent symétriques.
- Outre la fonction mécanique, les verrous latéraux sur la fiche et la plaque médiane dans l'embase jouent également un rôle dans la CEM. Ceci est représenté à la Figure 3-75:
    1. ***Il convient*** qu'une connexion électrique soit établie entre le verrou latéral et la plaque médiane de l'embase (une fiche d'accueil ***peut ne pas*** comporter de verrous latéraux).
    2. ***Il convient de*** raccorder le verrou latéral au plan GND de la carte d'accès à l'intérieur de la fiche.
    3. ***Il convient de*** relier directement la plaque médiane au plan GND de la CCI du système avec trois conducteurs/connexions brasés, ou plus.

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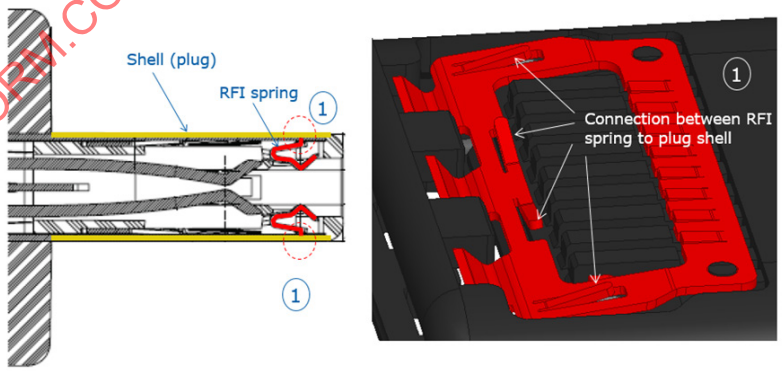
Figure 3-75 Lignes directrices relatives à la CEM pour les verrous latéraux et la plaque médiane



Anglais	Français
Paddle card	Carte d'accès
PCB board on host side	Support de la CCI côté hôte
Paddle card (plug)	Carte d'accès (fiche)
Side latch (plug)	Verrou latéral (fiche)
Middle plane (receptacle)	Plaque médiane (embase)

- ***Il convient que*** le doigt RFI interne, à l'intérieur de la fiche, possède des points de connexion adéquats sur la surface interne de l'enveloppe de la fiche. Quatre points de connexion ou plus sont recommandés, comme cela est représenté à la Figure 3-76.

Figure 3-76 Connexions du doigt CEM sur l'enveloppe de la fiche



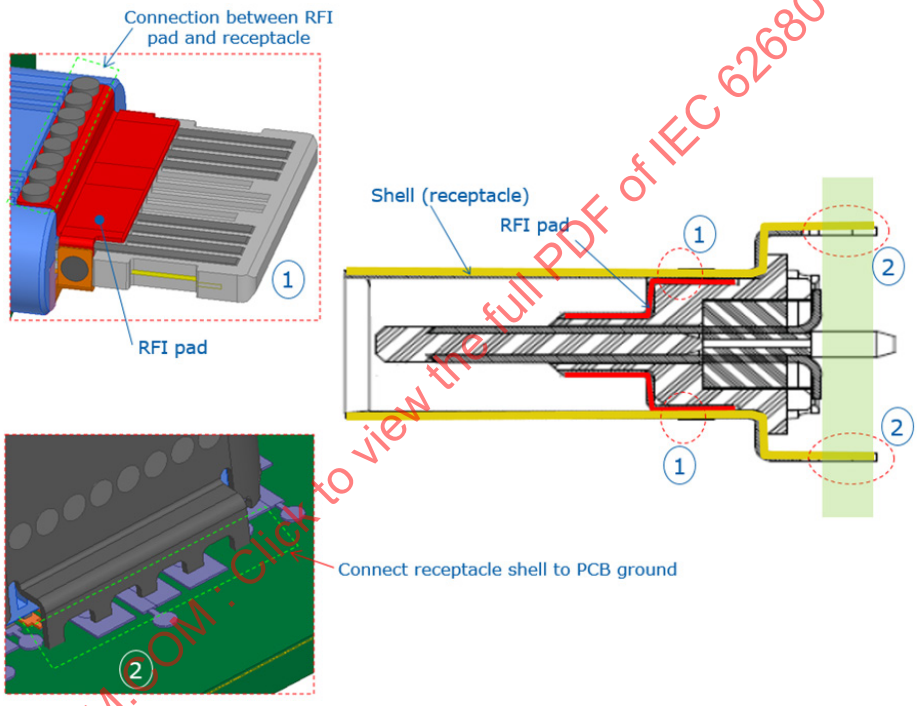
Anglais	Français
Shell (plug)	Enveloppe (fiche)
RFI spring	Ressort RFI

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Anglais	Français
Connection between RFI spring to plug shell	Connexion entre le ressort RFI et l'enveloppe de la fiche

- Les doigts CEM à l'intérieur de la fiche sont couplés avec la plaque CEM dans l'embase. Il est important que la plaque CEM possède des connexions adéquates sur l'enveloppe de l'embase. Comme cela est représenté à la Figure 3-77, plusieurs points de soudure laser se trouvent entre les plaques CEM et l'enveloppe de l'embase, en haut et en bas.
- ***Il convient que*** l'enveloppe de l'embase possède un nombre suffisant de points de connexion sur le plan GND de la CCI du système, avec des ouvertures aussi petites que possible. La Figure 3-77 représente un exemple de plusieurs connexions brasées, qui permettent de connecter l'enveloppe de l'embase au plan GND de la CCI du système.

Figure 3-77 Connexions de la plaque CEM sur l'enveloppe de l'embase

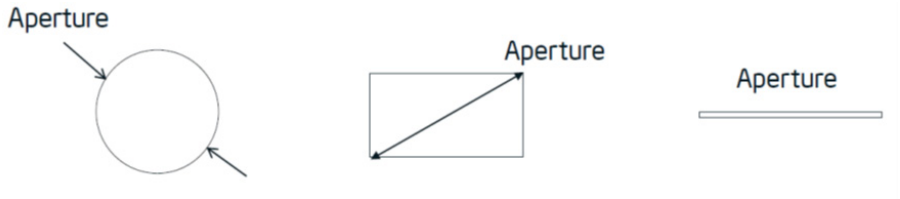


Anglais	Français
Connection between RFI pad and receptacle	Connexion entre la pastille RFI et l'embase
RFI pad	Pastille RFI
Shell (receptacle)	Enveloppe (embase)
Connect receptacle shell to PCB ground	Raccorder l'enveloppe de l'embase à la masse de la CCI

- ***Il convient de*** réduire le plus possible les ouvertures dans l'enveloppe des fiches et embases. Si les ouvertures sont inévitables, une taille d'ouverture maximale de 1,5 mm est recommandée. Pour obtenir des exemples d'ouvertures, voir la Figure 3-78. Du ruban de cuivre ***peut*** être appliqué pour sceller les ouvertures à l'intérieur de la fiche de câble.

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Figure 3-78 Exemples d'ouvertures de connecteur



Anglais	Français
Aperture	Ouverture

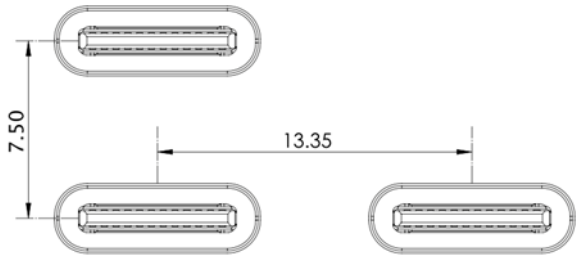
- ***Il convient de*** connecter les embases au châssis en métal ou aux boîtiers, par des doigts de mise à la masse, des vis ou toute autre méthode permettant de gérer la CEM.

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3.10.2 Espacement physique des connecteurs empilés et adjacents (*informatif*)

Les connecteurs USB empilés et adjacents sont couramment utilisés dans les systèmes PC. La Figure 3-79 représente l'espacement recommandé entre les connecteurs pour les configurations empilées et adjacentes.

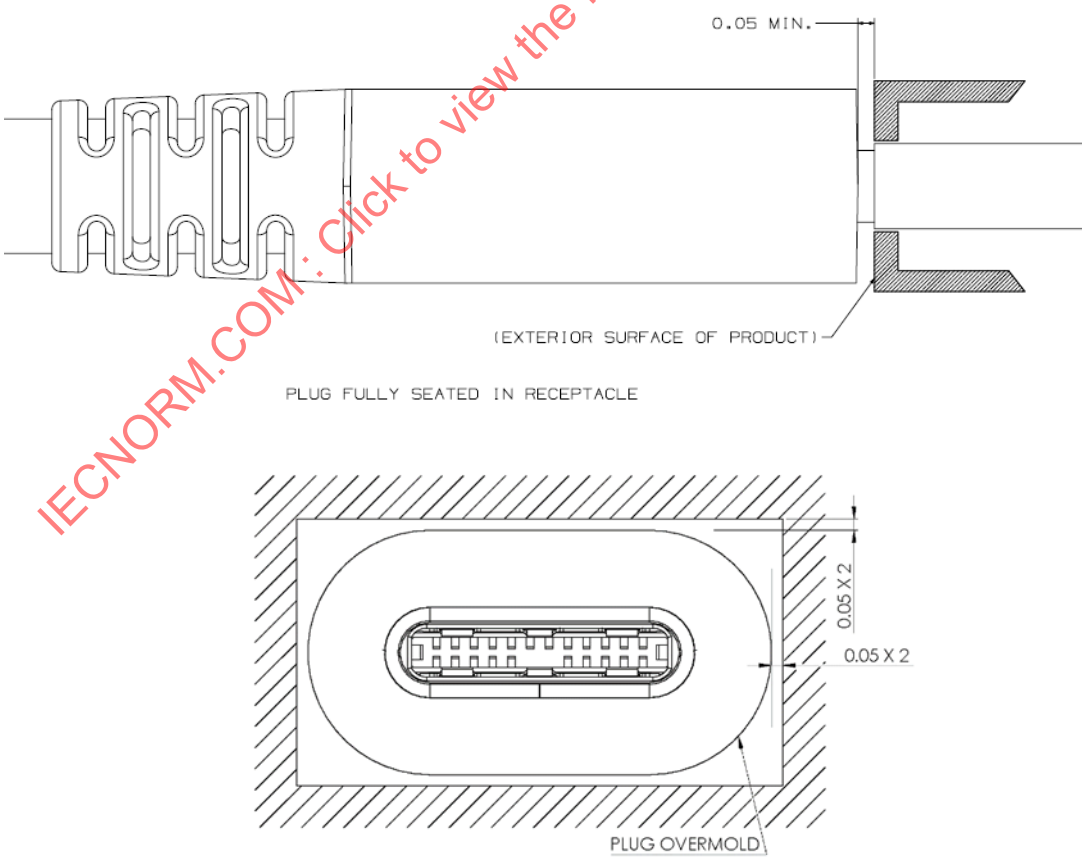
Figure 3-79 Espacement minimal recommandé entre les connecteurs



3.10.3 Remarques sur le couplage des câbles (*informatives*)

Il est nécessaire de prendre en considération l'emplacement de montage de l'embase, les surfaces extérieures du produit, le surmoulage des câbles et la longueur de couplage des fiches pour pouvoir insérer complètement la fiche USB Type-C dans l'embase USB Type-C. La Figure 3-80 représente l'espace minimal recommandé pour le surmoulage de la fiche afin d'éviter les interférences entre le surmoulage de la fiche et l'ouverture du boîtier, de manière à permettre l'insertion complète de la fiche de câble dans l'embase du produit.

Figure 3-80 Espace minimal recommandé pour le surmoulage de la fiche

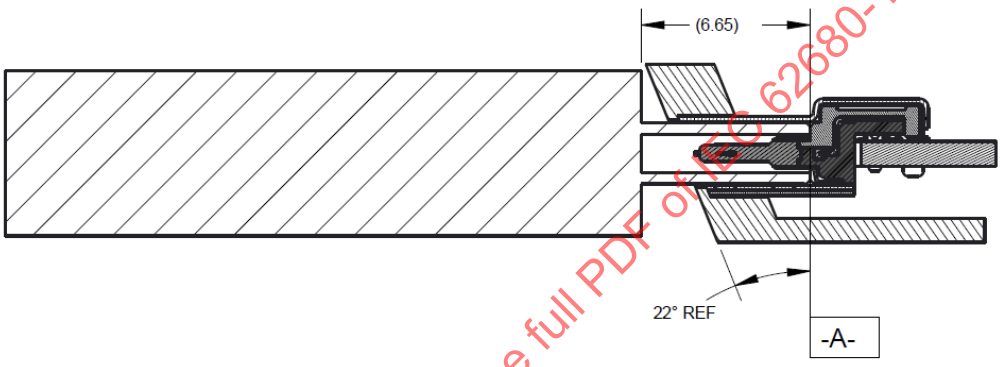


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Anglais	Français
Exterior surface of product	Surface extérieure du produit
Plug fully seated in receptacle	Fiche installée dans l'embase
Plug overmold	Surmoulage de la fiche

La Figure 3-81 représente les considérations particulières exigées lorsque les parois externes sont inclinées. Pour ces applications, la protection par l'alignement mécanique de la languette sur l'enveloppe de l'embase USB Type-C ***peut ne pas*** être aussi efficace que pour une conception avec enveloppe intégrale. Les options de conception qui permettent à l'embase de répondre aux exigences d'essai mécanique incluent de relâcher la surface de la paroi extérieure pour permettre d'utiliser l'enveloppe intégrale de l'embase ou une embase spécialement conçue pour cette application.

Figure 3-81 Surmoulage de la fiche de câble et surface inclinée



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3.11 Câbles EPR (Extended Power Range)

3.11.1 Exigences électriques

Les câbles EPR font l'objet d'exigences supplémentaires permettant d'assurer qu'ils peuvent fournir toute la plage de tensions et de courants définie pour le fonctionnement EPR ***USB PD***.

Les câbles EPR ***doivent*** assurer la prise en charge fonctionnelle d'un fonctionnement à 50 V et 5 A. Un câble ***doit*** prendre en charge une tension fonctionnelle d'au moins 50,9 V. ***Il convient que*** les composants électriques qui se trouvent éventuellement dans le chemin de VBUS d'un câble EPR (les condensateurs de découplage, par exemple) présentent une tension assignée d'au moins 63 V.

Pour plus d'informations relatives à la conception ***USB PD*** haute tension et à l'atténuation des dommages dus à la formation d'arcs lors du retrait du câble, voir l'Annexe H.

3.11.2 Exigences d'identification du câble EPR

Tous les câbles EPR ***doivent*** comporter un marquage électronique et inclure des informations spécifiques à EPR dans le marqueur électronique comme cela est défini dans la spécification ***USB PD***. Comme cela est indiqué dans la spécification ***USB PD***, les câbles EPR sont marqués à 50 V et 5 A.

Voir 3.4.1.1 et 3.4.2.1 pour la certification et l'identification des câbles.

4 Fonctionnel

Le présent article traite des exigences fonctionnelles concernant la signalisation sur les câbles et connecteurs USB Type-C®. Elles incluent la définition du signal fonctionnel, les processus de découverte et de configuration, ainsi que l'alimentation.

4.1 Récapitulatif des signaux

Le Tableau 4-1 récapitule la liste des signaux utilisés sur les connecteurs USB Type-C.

Tableau 4-1 Liste des signaux utilisés sur les connecteurs USB Type-C

Groupe de signaux	Signal	Description
USB 3.2/USB4	**TXp1, TXn1** **RXp1, RXn1** **TXp2, TXn2** **RXp2, RXn2**	Les interfaces de données en série ***USB 3.2*** SuperSpeed USB et ***USB4*** définissent une paire d'émission différentielle et une paire de réception différentielle par voie. Sur une embase USB Type-C, deux ensembles de broches de signal sont définis pour prendre en charge le fonctionnement à double voie et activer la fonctionnalité de retournement des fiches.
USB 2.0	**Dp1, Dn1** **Dp2, Dn2**	L'interface de données en série ***USB 2.0*** définit une paire différentielle. Sur une embase USB Type-C, deux ensembles de broches de signal ***USB 2.0*** sont définis pour activer la fonctionnalité de retournement des fiches.
Configuration	**CC1, CC2** (embase) **CC** (fiche)	Canal CC dans la fiche utilisé pour la détection des connexions, la configuration de l'interface et VCONN.
Signaux auxiliaires	**SBU1, SBU2**	Utilisation en bande latérale. Dans le cadre de l'***USB4***, ces signaux sont utilisés pour SBTX et SBRX.
Alimentation	**VBUS**	Alimentation de bus du câble USB
	VCONN (fiche)	Alimentation de la fiche USB
	GND	Chemin du courant de retour du câble USB

4.2 Description des broches de signal

4.2.1 Broches *USB 3.2/USB4*

TXp1, TXn1
TXp2, TXn2

Ces broches doivent mettre en œuvre le chemin d'émission du système d'une interface ***USB 3.2*** SuperSpeed ou ***USB4*** TX/RX. La paire différentielle de transmission dans un port est routée vers la paire différentielle de réception dans le port à l'extrémité opposée du chemin. En fonction de la connexion établie, la spécification ***USB 3.2*** ou la spécification ***USB4*** définit l'ensemble des caractéristiques électriques et des fonctionnalités d'énumération, de protocole et de gestion pour cette interface.

Deux paires de broches sont définies pour activer le fonctionnement à double voie (voir 4.5.1.1 pour une définition complète).

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RXp1, RXn1
RXp2, RXn2

Ces broches doivent mettre en œuvre le chemin de réception du système d'une interface ***USB 3.2*** SuperSpeed ou ***USB4*** TX/RX. La paire différentielle de réception dans un port est routée vers la paire différentielle de transmission dans le port à l'extrémité opposée du chemin. En fonction de la connexion établie, la spécification ***USB 3.2*** ou la spécification ***USB4*** définit l'ensemble des caractéristiques électriques et des fonctionnalités d'énumération, de protocole et de gestion pour cette interface.

Deux paires de broches sont définies pour activer le fonctionnement à double voie (voir 4.5.1.1 pour une définition complète).

4.2.2 Broches *USB 2.0*

Dp1, Dn1
(Dp2, Dn2)

Ces broches doivent mettre en œuvre la fonctionnalité ***USB 2.0***. Les trois modes de l'***USB 2.0*** (LS, FS et HS) sont pris en charge. La spécification ***USB 2.0*** définit l'ensemble des caractéristiques électriques et des fonctionnalités d'énumération, de protocole de bus et de gestion de bus pour cette interface.

Deux paires de broches sont définies pour activer la fonctionnalité de retournement des fiches (voir 4.5.1.1 pour une définition complète).

4.2.3 Broches de signal auxiliaire

SBU1, SBU2

Ces broches sont affectées à l'utilisation en bande latérale. Dans le cadre de l'***USB4***, ces signaux sont utilisés pour SBTX et SBRX. Voir 4.3 pour obtenir les exigences fonctionnelles.

4.2.4 Broches d'alimentation et de masse

VBUS

Ces broches sont destinées à l'alimentation de bus du câble USB définie par les spécifications USB. La VBUS n'est présente que lorsqu'une connexion source-destinataire est établie sur le canal CC (voir 4.5.1.2.1). Voir 4.4.2 pour obtenir les exigences fonctionnelles de VBUS.

VCONN

La tension VCONN est appliquée à la broche CC inutilisée pour alimenter la fiche locale. Voir 4.4.3 pour obtenir les exigences fonctionnelles de VCONN.

GND

Chemin du courant de retour.

4.2.5 Broches de configuration

CC1, CC2, CC

Ces broches sont utilisées pour détecter les connexions et pour configurer l'interface sur les câbles et connecteurs USB Type-C. Voir 4.5 pour obtenir la définition fonctionnelle. Lorsqu'une connexion est établie, CC1 ou CC2 sont réaffectées à l'alimentation de la fiche par la broche VCONN (voir 4.5.1.2.1).

4.3 Utilisation en bande latérale (SBU)

Les broches SBU (SBU1 et SBU2) sont limitées aux utilisations définies par la présente spécification. Une fonctionnalité supplémentaire est définie dans la spécification ***USB4***. Voir l'Annexe E pour plus d'informations sur l'utilisation des broches SBU en ***modes alternatifs***.

Les broches SBU sur un port ***doivent*** être en circuit ouvert ou avoir une faible dépolarisation à la masse, moins puissante que ***zSBUTermination*** dans ***USB 3.2*** ou ***USB 2.0***.

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Ces broches sont prébranchées dans le câble USB Type-C Complet normalisé en tant que fils distincts à extrémité unique (SBU_A et SBU_B). Noter que SBU1 et SBU2 sont interconnectés dans le câble.

Lorsque l'***USB4*** est utilisé, ces broches sont utilisées comme canal en bande latérale ***USB4*** avec mise en correspondance de SBU1 vers SBTX et de SBU2 vers SBRX. Les exigences fonctionnelles SBTX et SBRX sont définies dans la spécification ***USB4***. Lorsqu'un port détermine que la fiche insérée localement est retournée (c'est-à-dire CC1 est ouvert, CC2 est terminé), la spécification ***USB4*** (inversion de la voie de canal en bande latérale de référence) exige que le port retourne les mises en correspondance de SBTX et SBRX vers SBU1 et SBU2 afin d'assurer l'opération d'émission-réception en bande latérale de bout en bout appropriée.

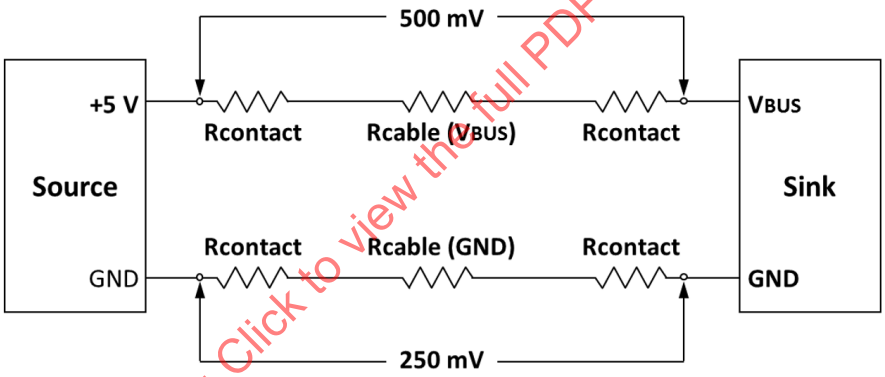
4.4 Alimentation et masse

4.4.1 Chute de tension ohmique

La chute de tension ohmique de câble maximale admissible pour la masse (y compris sur un câble captif) ***doit*** être de 250 mV et de 500 mV pour VBUS par le câble, pour la capacité maximale de courant VBUS assigné. Lorsque la VCONN est alimentée, la chute de tension ohmique pour la masse ***doit*** toujours être observée en prenant en compte un éventuel courant de retour VCONN supplémentaire.

La Figure 4-1 représente les paramètres qui contribuent à la chute de tension ohmique et où la mesure ***doit*** s'effectuer. La chute de tension ohmique inclut la résistance de contact des fiches et embases couplées à chaque extrémité.

Figure 4-1 Chute de tension ohmique d'un câble

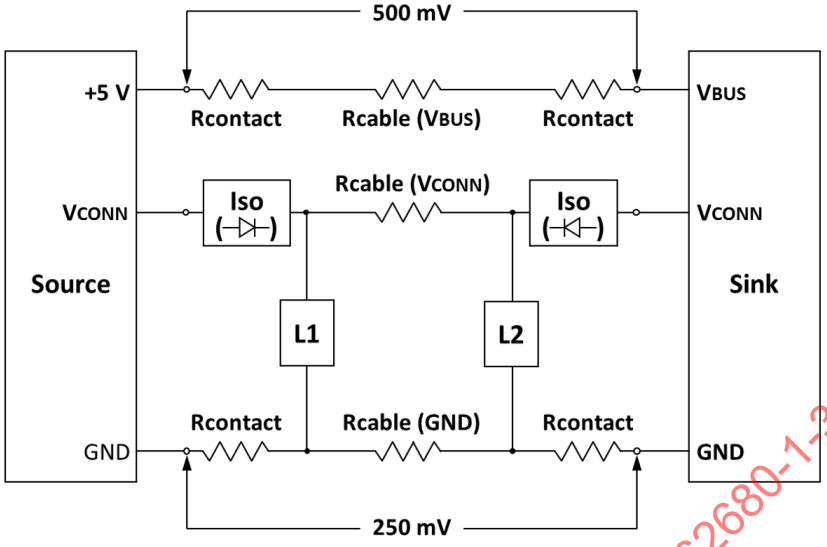


Anglais	Français
Sink	Destinataire

La Figure 4-2 représente les paramètres qui contribuent à la chute de tension ohmique d'un câble alimenté et où la mesure ***doit*** s'effectuer. Noter que le câble alimenté inclut des éléments d'isolation (Iso) et des charges (L1 et L2) pour les fonctions du câble alimenté, tels les contrôleurs ***USB PD***. La chute de tension ohmique ***doit*** rester inférieure à 250 mV dans tous les cas.

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Figure 4-2 Chute de tension ohmique des câbles alimentés



Anglais	Français
Sink	Destinataire

4.4.2 VBUS

La plage de tensions VBUS admissible par défaut, mesurée au niveau de l'embase de la source, ***doit*** être celle définie par les spécifications ***USB 2.0*** et ***USB 3.2***. Dans le cadre de l'***USB4***, la spécification ***USB 3.2*** est utilisée pour cette exigence. Noter qu'en raison des courants plus élevés admis, les dispositifs existants ***peuvent*** supporter une tension plus élevée (jusqu'à 5,5 V au maximum) à des charges légères.

La broche VBUS de l'embase USB Type-C de la source ***doit*** rester hors tension et ***doit*** limiter la capacité entre VBUS et GND, conformément au Tableau 4-2, tant qu'un destinataire n'est pas branché. La broche VBUS ***doit*** revenir à l'état hors tension lorsque le destinataire est débranché. Le Tableau 4-32 contient les valeurs de temporisation de VBUS. Ces deux exigences ne s'appliquent pas aux hôtes/chargeurs existants qui alimentent par défaut la broche VBUS lorsqu'ils sont connectés par un connecteur USB existant (Standard-A, Micro-B, etc.) à un câble ou un adaptateur USB Type-C.

Une DRP ou une source (ou un dispositif avec prise en charge des accessoires) qui applique une polarisation ***Rp*** comme méthode de détection des connexions ***doit*** fournir une impédance entre les broches VBUS et GND de son embase, conformément au Tableau 4-2, lorsqu'il ou elle ne source pas l'alimentation sur la VBUS (à savoir à l'état ***Unattached.SRC*** ou ***Unattached.Accessory***).

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Tableau 4-2 Caractéristiques d'une source VBUS

	Valeur minimale	Valeur maximale	Notes
Impédance de fuite de VBUS	72,4 kΩ		Fuite entre les broches VBUS et GND sur l'embase lorsque la tension VBUS n'est pas alimentée.
Capacité VBUS		3 000 µF	Capacité pour les ports source uniquement entre les broches VBUS et GND sur l'embase lorsque la tension VBUS n'est pas alimentée.

	Valeur minimale	Valeur maximale	Notes
		10 µF	Capacité pour les ports DRP entre les broches VBUS et GND sur l'embase lorsque la tension VBUS n'est pas alimentée.

Le Tableau 4-3 spécifie les caractéristiques du destinataire VBUS par rapport au comportement de déconnexion en fonction de la surveillance de VBUS. Les destinataires ***peuvent*** surveiller la broche CC, le retrait de ***Rp*** par la source étant un indice supplémentaire de déconnexion.

Tableau 4-3 Caractéristiques d'un destinataire VBUS

	Valeur minimale	Valeur maximale	Notes
tSinkDisconnect		40 ms	Limite de temps pour la transition de ***Attached.SNK*** vers ***Unattached.SNK***
vSinkDisconnect[1]	0,8 V	3,67 V	Seuil utilisé pour la transition de ***Attached.SNK*** vers ***Unattached.SNK*** lorsque VBUS est de 5 V. Il s'applique également pour les contrats ***USB PD*** à 5 V. Pour les contrats ***USB PD*** à 5 V, le destinataire ***doit*** prendre en compte la chute de tension ohmique et la marge lors du choix de ce seuil.
		PPS_APDO_Min_Voltage * 0,95	Seuil utilisé pour la transition de ***Attached.SNK*** vers ***Unattached.SNK***. Il s'applique aux contrats PPS ***USB PD*** pour une tension de sortie du RDO inférieure ou égale à 5 V. Il s'applique également aux contrats PPS ***USB PD*** qui fonctionnent en mode de limite du courant. Le destinataire ***doit*** prendre en compte la chute de tension ohmique et la marge lors du choix de ce seuil.
vSinkPD_min[1]		vNew – 750 mV + vValid	Tension VBUS valide minimale lue par le destinataire lors de la négociation par l'***USB PD***. vNew = vSrcNew (min) ou vPpsNew (min) comme cela est défini dans l'***USB PD***. 750 mV = 500 mV + 250 mV (chute de tension ohmique maximale) vValid = vSrcValid (min) ou vPpsValid (min) comme cela est défini dans l'***USB PD***.
vSinkDisconnectPD[1]	90 % de ***vSinkPD_min***	***vSinkPD_min***	Seuil de déconnexion de VBUS lorsque la tension VBUS a été négociée par l'***USB PD*** à une valeur supérieure à 5 V. Il s'applique aux contrats PPS ***USB PD*** pour une tension de sortie du RDO supérieure à 5 V. Il s'applique également aux contrats PPS ***USB PD*** qui fonctionnent en mode de tension constante.
Capacité VBUS		10 µF	Capacité entre les broches VBUS et GND sur l'embase lorsque ***Attached.SNK*** n'est pas activé.

Note 1: Pour l'applicabilité de cette exigence, voir 4.5.2.2.5.2.

4.4.3 VCONN

La tension VCONN est fournie par la source pour alimenter les câbles dont la fiche comporte des composants électroniques. Elle est fournie par la broche CC qui est désignée pour ne pas être connectée au fil CC du câble.

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Dans un premier temps, la VCONN est alimentée sur les embases USB Type-C de la source, conformément aux exigences relatives à l'état ***Attached.SRC*** de 4.5.2.2.9.1. Par la suite, si la VCONN n'est pas explicitement exigée par le câble ou le dispositif comme cela est indiqué dans son marqueur électronique, elle ***peut*** être retirée comme cela est décrit dans le Tableau 4-4. La commande ***USB PD VCONN_Swap*** permet également à la source de demander que le destinataire branché alimente la VCONN.

Tableau 4-4 Récapitulatif des exigences de tension VCONN du port Source USB Type-C

D+/D–	TX/RX, VPD	> 3 A	Exigences VCONN
Non	Non	Non	Non exigé pour alimenter la VCONN
Oui	Non	Non	Non exigé pour alimenter la VCONN
Oui	Oui	Non	Exigé pour fournir 1 W pour les mises en œuvre x1 et 1,5 W pour les mises en œuvre x2. Après avoir lu le marqueur électronique du câble, si la source a déterminé qu'il ne s'agit pas d'un câble ***VPD*** et que la valeur du champ Type de terminaison de câble est 00b, l'alimentation VCONN ***peut*** être retirée.
Non	Non	Oui	Exigé pour fournir 100 mW. L'alimentation VCONN ***peut*** être retirée lorsque la source a lu le marqueur électronique du câble et déterminé le courant admissible du câble.
Oui	Non	Oui	Exigé pour fournir 100 mW. L'alimentation VCONN ***peut*** être retirée lorsque la source a lu le marqueur électronique du câble et déterminé le courant admissible du câble.
Oui	Oui	Oui	Exigé pour fournir 1 W pour les mises en œuvre x1 et 1,5 W pour les mises en œuvre x2. Après avoir lu le marqueur électronique du câble, si la source a déterminé le courant admissible du câble, qu'il ne s'agit pas d'un câble ***VPD*** et que la valeur du champ Type de terminaison de câble est 00b, l'alimentation VCONN ***peut*** être retirée.

Le Tableau 4-5 indique les exigences de tension et d'alimentation qui ***doivent*** être respectées pour VCONN. Pour plus d'informations sur les câbles avec marquage électronique, voir 4.9. Pour plus d'informations sur la prise en charge ***facultative*** d'une plage de tensions VCONN étendue en ***modes alternatifs***, voir l'Annexe E.

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Tableau 4-5 Caractéristiques d'une source VCONN

	Valeur minimale	Valeur maximale	Notes
vVCONNValid	3,0 V	5,5 V	Plage de tensions dans laquelle VCONN est interprétée comme valide.
Alimentation des sources avec signaux TX/RX	x1 1 W		La source ***peut*** verrouiller VCONN si la quantité d'alimentation puisée dépasse les valeurs spécifiées de courant d'appel et de tension. La source ***peut*** désactiver VCONN conformément au Tableau 4-4. Les modes alternatifs ***peuvent*** exiger une alimentation plus élevée.
	x2 1,5 W		
Alimentation des sources avec prise en charge des VPD	1 W		La source ***peut*** verrouiller VCONN si la quantité d'alimentation puisée dépasse les valeurs spécifiées de courant d'appel et de tension.
Alimentation des sources en mode veille USB ou sans signaux TX/RX	100 mW		La source d'alimentation minimale doit être fournie en mode veille USB ou sans signaux TX/RX.[1] La source ***peut*** désactiver VCONN conformément au Tableau 4-4.
Rdch	30 Ω	6 120 Ω	Résistance de décharge appliquée dans ***UnattachedWait.SRC*** entre la broche CC en cours de déchargement et GND.
Note 1: Lors du passage de U3 à U0, la source VCONN ***doit*** fournir une puissance U0 maximale.			

Pour aider à réduire la puissance associée à l'alimentation de la VCONN, une source peut soit ne pas alimenter la VCONN, soit la désactiver dans l'une des conditions suivantes:

- la ***Ra*** n'est pas détectée sur la broche CC à l'issue du délai ***tCCDebounce*** lorsque l'autre broche CC est à l'état ***SRC.Rd***; ou
- aucune réponse GoodCRC n'a été donnée aux messages de ***découverte d'identité*** de l'***USB PD*** envoyés sur SOP'.

Si la source d'alimentation utilisée pour alimenter VCONN est une source d'alimentation partagée avec d'autres sorties USB VCONN et VBUS, elle doit être découplée avec une capacité identique aux exigences de capacité VBUS définies en 11.4.4 Dynamic Attach and Detach de l'***USB 3.2***. La capacité de dérivation des sources d'alimentation VCONN doit être isolée des broches CC lorsque VCONN n'est pas fournie.

Le Tableau 4-6 fournit les exigences qui ***doivent*** être respectées pour les câbles qui consomment de l'alimentation VCONN.

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Tableau 4-6 Caractéristiques d'un destinataire VCONN de câble

	Valeur minimale	Valeur maximale	Notes
Tension	3,0 V	5,5 V	Plage de tensions (vVCONNValid) lorsque VCONN est valide.
Capacité d'appel		10 µF	Un câble ***ne doit pas*** présenter une capacité d'appel supérieure à celle de la source VCONN. Le câble actif est responsable du déchargement de sa capacité.
Alimentation des câbles passifs avec marquage électronique		20 mW	Voir 4.9. Mesurée sans trafic ***USB PD*** au moins ***tRaWeaken*** après l'application de VCONN. Note: Puissance maximale de 75 mW admise pendant les premières ***tRaWeaken*** après l'application de VCONN.
Alimentation *USB 3.2* pour les câbles actifs à l'état U		Voir le Tableau 6-6	U0, U1, U2, U3, Rx.Detect et eSS.Disabled.
tVCONNDischarge		230 ms	Durée entre la déconnexion du câble et le moment auquel ***vVCONNDischarge*** est atteint.
vVCONNDischarge		800 mV	Tension VCONN après ***tVCONNDischarge***
vVCONNDisconnect	1 V	2,4 V	Seuil utilisé pour détecter les déconnexions de VCONN.
iRaDetect		10 mA	Courant maximal puisé de VCONN lorsque la tension est inférieure à vVCONNValid. Note: Ce courant est inférieur aux 75 mW admis pendant les premières 500 ms à 5,5 V.
tRaReconnect		1 ms	Durée entre le moment où VCONN devient inférieur à ***vVCONNDisconnect*** au niveau de la fiche de câble et où le câble a réappliqué ***Ra***.
tRaWeaken	21 ms	1,2 s	Durée entre le moment où VCONN dépasse ***vVCONNDisconnect*** et où le câble est retiré ou affaiblit ***Ra***.
tVCONNSwitch		***tVCONNStable***	Les câbles qui utilisent VBUS ***de manière facultative doivent*** être alimentés depuis VCONN dans ***tVCONNStable***.

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Le câble ***doit*** retirer ou affaiblir ***Ra*** en fonction du comportement de diagramme d'états en 4.5.2.5. Le câble ***doit*** de nouveau appliquer ***Ra*** en fonction du comportement de diagramme d'états en 4.5.2.5. Le câble ***doit*** décharger VCONN à une valeur inférieure à ***vVCONNDischarge*** lors de la déconnexion du câble. Le câble ***doit*** contrôler ***Ra*** à chacune de ses extrémités indépendamment en fonction de la VCONN sur cette extrémité.

Note de mise en œuvre: L'augmentation de ***Ra*** à 20 KΩ satisfait à l'alimentation dissipée pour les câbles passifs avec marquage électronique et à la décharge de 10 µF inférieure à ***vVCONNDischarge*** dans ***tVCONNDischarge***

Tableau 4-7 Caractéristiques d'un destinataire VPA (accessoire alimenté par VCONN)

	Valeur minimale	Valeur maximale	Notes
Tension	3,0 V	5,5 V	Plage de tensions (vVCONNValid) lorsque VCONN est valide.
Capacité d'appel		10 µF	Un accessoire ***ne doit pas*** présenter une capacité d'appel supérieure à celle de la source VCONN. L'accessoire est responsable du déchargement de sa capacité.
Alimentation avant l'entrée en mode alternatif		35 mW	Alimentation maximale en mode veille USB. Note: L'alimentation ***doit*** être réduite 5 s après l'application de VCONN, si le passage en ***mode alternatif*** ne s'est pas effectué. Une mise sous/hors tension de VCONN ***peut*** être exigée pour réactiver la communication ***USB PD***. Note: Puissance maximale de 75 mW admise pendant les premières 500 ms après l'application de VCONN.
tVCONNDischarge		230 ms	Délai entre la déconnexion du ***VPA*** et le moment auquel ***vVCONNDischarge*** est atteint.
vVCONNDischarge		800 mV	Tension VCONN à l'issue du délai ***tVCONNDischarge***.
iRaDetect		10 mA	Courant maximal puisé de VCONN lorsque la tension est inférieure à vVCONNValid. Note: Ce courant est inférieur aux 75 mW admis pendant les premières 500 ms à 5,5 V.
vRaReconnect	800 mV		Tension à laquelle le ***VPA*** ***doit*** réappliquer ***Ra*** sur le bord descendant de VCONN.
tRaWeaken		1,2 s	Durée entre le moment où VCONN dépasse ***vVCONNDisconnect*** et où le ***VPA*** est retiré ou affaiblit ***Ra***.
vVCONNDisconnect	1 V	2,4 V	Seuil utilisé pour détecter les déconnexions de VCONN.

Le ***VPA*** ***doit*** retirer ou affaiblir ***Ra*** dans les limites de ***tRaWeaken*** (comme cela est défini dans le Tableau 4-7) lorsque VCONN est entré dans la plage de tensions valides (***vVCONNValid***).

Le ***VPA*** ***doit*** réappliquer ***Ra*** lorsque VCONN chute au-dessous de vRaReconnect, comme cela est défini dans le Tableau 4-7. Le ***VPA*** ***doit*** décharger VCONN à une valeur inférieure à ***vVCONNDischarge*** dans les limites de ***tVCONNDischarge*** lors de la déconnexion du câble. Le ***VPA*** ***doit*** prendre en compte la capacité VCONN présente dans l'accessoire lors du déchargement de VCONN.

La consommation électrique maximale en ***mode alternatif*** est définie par la spécification relative au ***mode alternatif*** utilisé.

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Tableau 4-8 Caractéristiques d'un destinataire VPD (dispositif alimenté par VCONN)

	Valeur minimale	Valeur maximale	Notes
Tension	3,0 V	5,5 V	Plage de tensions (vVCONNValid) lorsque VCONN est valide.
Capacité d'appel		10 µF	Un dispositif ***ne doit pas*** présenter une capacité d'appel supérieure à celle de la source VCONN. Le dispositif est responsable du déchargement de sa capacité.
Alimentation avant l'énumération USB		35 mW	Alimentation maximale en mode veille USB. Note: Puissance maximale de 75 mW admise pendant les premières 500 ms après l'application de VCONN.
Alimentation en activité		500 mW (***USB 2.0***) 750 mW (***USB 3.2***)	Un ***VPD*** ***doit*** uniquement exposer une interface à faible alimentation par USB.
tVCONNDischarge		230 ms	Délai entre la déconnexion du ***VPD*** et le moment auquel ***vVCONNDischarge*** est atteint.
vVCONNDischarge		800 mV	Tension VCONN à l'issue du délai ***tVCONNDischarge***.
iRaDetect		10 mA	Courant maximal puisé de VCONN lorsque la tension est inférieure à vVCONNValid. Note: Ce courant est inférieur aux 75 mW admis pendant les premières 500 ms à 5,5 V.
vRaReconnect	800 mV		Tension à laquelle le ***VPD*** ***doit*** réappliquer ***Ra*** sur le bord descendant de VCONN.
tRaWeaken		1,2 s	Durée entre le moment où VCONN dépasse ***vVCONNDisconnect*** et où le ***VPD*** est retiré ou affaiblit ***Ra***.
vVCONNDisconnect	1 V	2,4 V	Seuil utilisé pour détecter les déconnexions de VCONN.

Le ***VPD*** ***doit*** retirer ou affaiblir ***Ra*** dans les limites de ***tRaWeaken*** (comme cela est défini dans le Tableau 4-8) lorsque VCONN est entré dans la plage de tensions valides (***vVCONNValid***).

Le ***VPD*** ***doit*** réappliquer ***Ra*** lorsque VCONN chute au-dessous de vRaReconnect, comme cela est défini dans le Tableau 4-8. Le ***VPD*** ***doit*** décharger VCONN à une valeur inférieure à ***vVCONNDischarge*** dans les limites de ***tVCONNDischarge*** lors de la déconnexion du câble. Le ***VPD*** ***doit*** prendre en compte la capacité VCONN présente dans le dispositif lors du déchargement de VCONN.

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4.5 Canal de configuration (CC)

4.5.1 Vue d'ensemble de l'architecture

Pour la solution USB Type-C, deux broches sur le connecteur, CC1 et CC2, sont utilisées pour établir et gérer la connexion de la source au destinataire. Lorsque le dispositif est connecté par un hub, la connexion entre un destinataire (UFP) sur le hub et la source (port hôte), et la connexion entre le destinataire (port dispositif) et une source (DFP sur le hub), sont traitées séparément. Sur le plan fonctionnel, le canal de configuration permet d'atteindre les objectifs suivants:

- détecter le branchement d'un port USB, d'une source à un destinataire par exemple;
- résoudre l'orientation du câble et les connexions torsadées pour établir le routage du bus de données USB;
- établir des rôles de données entre deux ports branchés;
- découvrir et configurer VBUS: modes de ***courant USB Type-C*** ou ***USB Power Delivery***;
- configurer VCONN; et
- découvrir et configurer les modes alternatif et accessoire ***facultatifs***.

4.5.1.1 Interface de bus de données USB et capacité de retournement des fiches USB Type-C

Étant donné que la fiche USB Type-C peut être insérée vers le haut ou vers le bas, les hôtes et dispositifs qui prennent en charge la fonctionnalité de bus de données USB doivent s'exécuter sur les broches de signal qui sont connectées de bout en bout. Dans le cas de l'***USB 2.0***, les deux broches de signal D+ et les deux broches de signal D− sont court-circuitées ensemble dans les embases de l'hôte et du dispositif. Dans le cas des signaux ***USB 3.2*** SuperSpeed ou des signaux ***USB4*** TX/RX en fonctionnement à voie unique, l'équivalent fonctionnel d'un commutateur est exigé dans l'hôte et le dispositif afin de router de manière appropriée les paires de signaux TX et RX vers le chemin connecté par le câble. Pour une mise en œuvre ***USB 3.2*** SuperSpeed ou ***USB4*** à double voie, l'hôte et/ou le dispositif résolvent l'ordre des voies.

La Figure 4-3 représente le modèle de bus de données logique d'un hôte USB Type-C connecté à un dispositif USB Type-C qui ne peut fonctionner qu'en USBSuperSpeed à voie unique. Le câble USB qui se trouve entre un hôte et un dispositif peut être dans l'un des quatre états connectés possibles du point de vue de l'hôte:

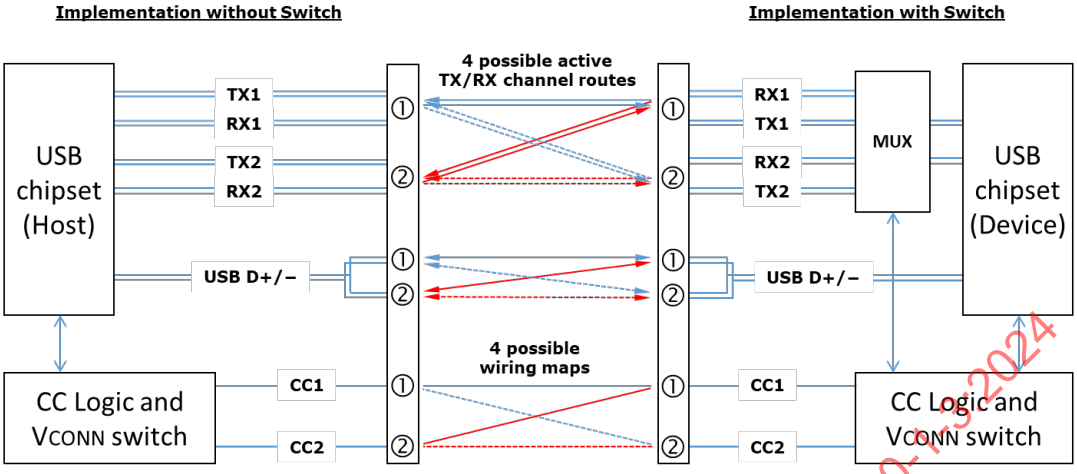
- liaison directe non retournée – Position ① ⇔ Position ①;
- liaison torsadée non retournée – Position ① ⇔ Position ②;
- liaison directe retournée – Position ② ⇔ Position ②;
- liaison torsadée retournée – Position ② ⇔ Position ①.

Pour établir un routage approprié du bus de données USB actif de l'hôte vers le dispositif, le câble USB Type-C normalisé est branché de sorte qu'un seul fil CC est aligné sur les premières paires de signaux TX/RX (TXp1/TXn1 et RXp1/RXn1). De cette façon, le fil CC et les fils du bus de données TX/RX qui sont utilisés pour la signalisation en fonctionnement à voie unique dans le câble suivent l'orientation et la torsion du câble. En étant capable de détecter quelle broche CC (CC1 ou CC2) au niveau de l'embase est terminée par le dispositif, l'hôte peut déterminer les signaux TX/RX qui doivent être utilisés pour la connexion à voie unique. L'hôte peut également contrôler le commutateur fonctionnel pour le routage des paires de signaux TX/RX. De la même façon dans le dispositif, la détection de la broche CC, au niveau de l'embase, terminée par l'hôte permet au dispositif de contrôler le commutateur fonctionnel qui route ses paires de signaux TX/RX.

Pour une mise en œuvre à double voie, la paire de signaux TX/RX dans le câble/la fiche aligné(e) sur le fil/la broche CC est "Lane 0" et, en référence à l'***USB 3.2***, ***doit*** être identifiée comme la voie de configuration. La seconde paire de signaux TX/RX (TXp2/TXn2 et RXp2/RXn2) dans le câble/la fiche est "Lane 1" pour une configuration à double voie.

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Figure 4-3 Modèle logique du routage du bus de données à voie unique sur les ports USB Type-C



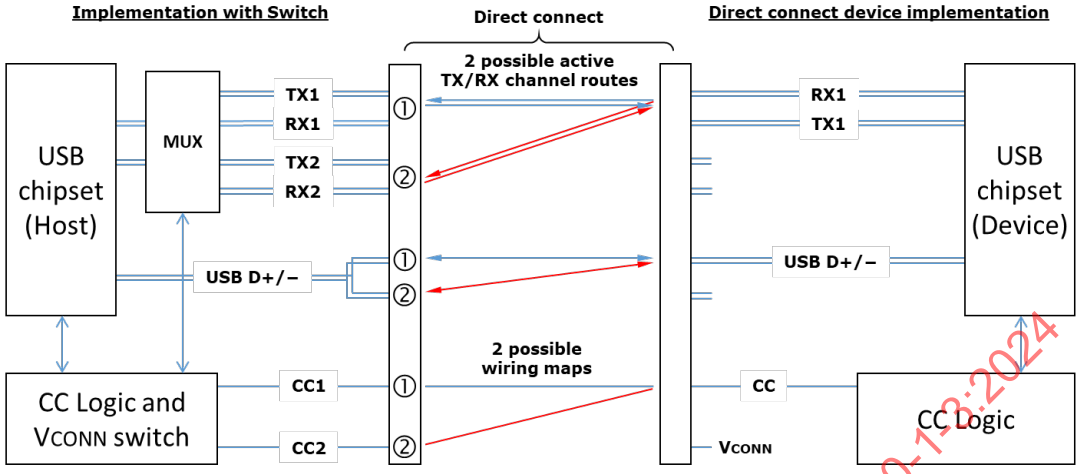
Anglais	Français
Implementation without Switch	Mise en œuvre sans commutateur
Implementation with Switch	Mise en œuvre avec commutateur
USB chipset (Host)	Jeu de puces USB (hôte)
CC Logic and VCONN switch	Logique CC et commutateur VCONN
4 possible active TX/RX channel routes	4 canaux TX/RX actifs possibles
4 possible wiring maps	4 plans de câblage possibles
USB chipset (Device)	Jeu de puces USB (dispositif)

Tandis que la Figure 4-3 représente le modèle fonctionnel d'un hôte connecté à un dispositif, ce modèle s'applique également aux ports en aval d'un hub USB.

La Figure 4-4 représente le modèle de bus de données logique d'un dispositif USB Type-C à voie unique (mis en œuvre avec une fiche USB Type-C physiquement incorporée au dispositif ou connectée de façon permanente en tant que câble captif) directement connecté à un hôte USB Type-C. Pour le dispositif, l'emplacement du bus de données TX/RX, du bus de données ***USB 2.0*** et des broches CC et VCONN est défini à la conception. Étant donné que l'emplacement des broches du dispositif est fixe, seuls deux états de connexion possibles sont disponibles du point de vue de l'hôte.

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Figure 4-4 Modèle logique des ports USB Type-C du dispositif à voie unique et connexion directe



Anglais	Français
Implementation without Switch	Mise en œuvre sans commutateur
Direct connect device implementation	Mise en œuvre d'un dispositif à connexion directe
USB chipset (Host)	Jeu de puces USB (hôte)
CC Logic and VCONN switch	Logique CC et commutateur VCONN
Direct connect	Connexion directe
2 possible active TX/RX channel routes	2 canaux TX/RX actifs possibles
2 possible wiring maps	2 plans de câblage possibles
USB chipset (Device)	Jeu de puces USB (dispositif)
CC Logic	Logique CC

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Les exigences fonctionnelles concernant la mise en œuvre du routage du bus de données TX/RX pour l'embase USB Type-C ne relèvent pas du domaine d'application de la présente spécification. Ce modèle logique peut reposer sur plusieurs architectures d'hôte, de dispositif et de hub, qui peuvent inclure la commutation discrète ou intégrée, et l'intégration de cette fonctionnalité à d'autres éléments de conception ***USB 3.2*** ou ***USB4***, comme un répéteur de bus par exemple.

Les exigences fonctionnelles concernant l'adressage du routage SBU1 et SBU2 ne relèvent pas du domaine d'application de la présente spécification. Pour ***USB4***, où SBTX et SBRX sont mis en correspondance vers SBU1 et SBU2, le réglage de la mise en correspondance de ces signaux en fonction de l'état de connexion (retournée et/ou torsadée) du câble est défini par la spécification ***USB4*** (inversion de la voie de canal en bande latérale de référence).

4.5.1.2 Connexion des sources et des destinataires

Étant donné que les fiches et embases USB Type-C ne font plus la différence entre les rôles hôte et dispositif en fonction de la forme du connecteur (les connecteurs USB Type-A et Type-B par exemple), deux ports équipés d'embases USB Type-C peuvent être connectés ensemble avec un câble USB Type-C normalisé. Le Tableau 4-9 récapitule les résultats attendus lors de l'interconnexion de ports Source, Destinataire et DRP.

Tableau 4-9 Interopérabilité d'un port USB Type-C

	Source uniquement	Destinataire uniquement	DRP (alimentation double fonction)
Source uniquement	Non fonctionnel	Fonctionnel	Fonctionnel
Destinataire uniquement	Fonctionnel	Non fonctionnel	Fonctionnel
DRP (alimentation double fonction)	Fonctionnel	Fonctionnel	Fonctionnel[1]
Note 1: La résolution des rôles ***peut*** être automatique ou manuelle.			

Dans les cas où l'interconnexion ne fonctionne pas, aucun des ports ne ***doit*** être utilisé. L'utilisateur doit trouver lui-même la combinaison invalide et prendre les mesures de résolution appropriées. Bien que ces deux combinaisons incorrectes imitent l'USB traditionnel où les connexions entre hôtes et entre dispositifs ne sont pas destinées à fonctionner, la solution USB Type-C non détrompée n'empêche pas l'utilisateur de tenter ces interconnexions. Les tensions VBUS et VCONN ***ne doivent pas*** être appliquées par une source (hôte) dans ces cas.

Le processus classique de configuration de l'interface dans le cas général d'une connexion USB entre une source (hôte) et un destinataire (dispositif) est le suivant:

1. Détecter une connexion valide entre les ports (déterminer notamment l'orientation du câble et la relation source-destinataire et DFP-UFP)
2. Découvrir, ***de manière facultative***, les capacités du câble
3. Établir, ***de manière facultative***, des alternatives à l'alimentation traditionnelle par USB (voir 4.6.2)
    a. Communication ***USB PD*** par CC pour la négociation de l'alimentation électrique avancée
    b. Modes de ***courant USB Type-C***
    c. ***USB BC 1.2***
4. Procéder à la récupération des informations du dispositif USB

Lorsque les ports DRP (alimentation double fonction) sont branchés à un port Source uniquement, destinataire uniquement ou autre DRP, le processus est fondamentalement le même, à l'exception près que lors de l'étape de détection d'une connexion valide, la DRP alterne entre le fonctionnement en tant que source pour détecter un destinataire branché, et la présentation en tant que destinataire pour être détecté par une source branchée. Finalement, une connexion source-destinataire est établie.

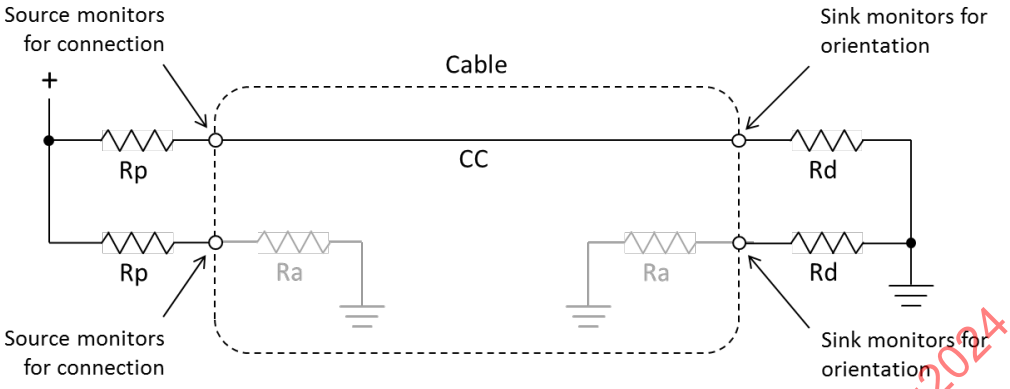
4.5.1.2.1 Détection d'une connexion source-destinataire valide

Le concept général de configuration d'une connexion valide entre une source et un destinataire repose sur la capacité à détecter les terminaisons qui figurent dans le produit actuellement branché.

Pour faciliter la définition du comportement fonctionnel du CC, un modèle de terminaison de polarisation (***Rp***) et de dépolarisation (***Rd***) est utilisé. La mise en œuvre réelle dans les hôtes et les dispositifs ***peut*** varier. Par exemple, la terminaison de polarisation peut être remplacée par une source de courant. La Figure 4-5 et la Figure 4-6 représentent deux modèles: le premier modèle repose sur une résistance de polarisation dans la source et le second modèle remplace cette résistance par une source de courant.

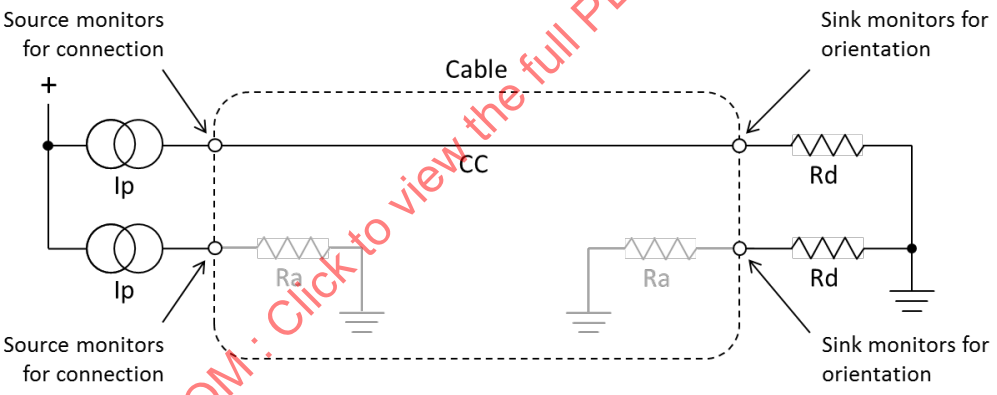
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Figure 4-5 Modèle CC de polarisation/dépolarisation



Anglais	Français
Source monitors for connection	La source détecte la connexion
Sink monitors for orientation	Le destinataire détecte l'orientation
Cable	Câble

Figure 4-6 Modèle CC de source de courant/dépolarisation



Anglais	Français
Source monitors for connection	La source détecte la connexion
Sink monitors for orientation	Le destinataire détecte l'orientation
Cable	Câble

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À l'origine, une source expose les terminaisons ***Rp*** indépendantes sur ses broches CC1 et CC2, et un destinataire expose les terminaisons ***Rd*** indépendantes sur ses broches CC1 et CC2. La combinaison source-destinataire de cette configuration de circuit représente une connexion valide. Pour détecter cette connexion, la source surveille CC1 et CC2 afin d'identifier une tension inférieure à sa tension non terminée. La ***Rp*** est déterminée en fonction de la tension de terminaison de polarisation et du circuit de détection de la source. Elle indique qu'un destinataire, un câble alimenté ou un destinataire connecté par un câble alimenté a été branché.

Avant l'application de VCONN, un câble alimenté expose ***Ra*** sur sa broche VCONN. La ***Ra*** représente la charge sur VCONN à laquelle s'ajoutent les éventuels éléments résistifs reliés à la masse. Dans certaines fiches de câbles, elle peut être purement résistive et dans d'autres, il ***peut*** tout simplement s'agir de la charge.

La source doit être capable de faire la différence entre la présence de ***Rd*** et de ***Ra***, pour savoir si un destinataire est branché et à quel endroit appliquer VCONN. Il n'est pas exigé que la source détecte VCONN à moins que ***Ra*** ne soit détecté.

Deux combinaisons de terminaisons spéciales sur les broches CC, du point de vue de la source, sont définies pour des modes spécifiques: ***Ra***/***Ra*** pour le mode ***accessoire d'adaptateur audio*** (Annexe A) et ***Rd***/***Rd*** pour le ***mode accessoire de débogage*** (Annexe B).

La source utilise des temporisateurs antirebond pour détecter de manière fiable l'état des broches CC, afin de neutraliser les rebonds de la connexion (***tCCDebounce***) et masquer les communications BMC ***USB PD*** (***tPDDebounce***).

Le Tableau 4-10 récapitule l'état des ports du point de vue de la source.

Tableau 4-10 Point de vue de la source

CC1	CC2	État	Position
Ouverte	**Ouverte**	Aucun branchement	***N/A***
Rd	**Ouverte**	Destinataire branché	①
Ouverte	**Rd**		②
Ouverte	**Ra**	Câble alimenté sans destinataire branché ou pour le ***mode inhibition de corrosion liquide*** (Annexe A)	①
Ra	**Ouverte**		②
Rd	**Ra**	Câble alimenté avec un destinataire, un ***accessoire alimenté par VCONN*** (***VPA***) ou un ***dispositif USB alimenté par VCONN*** (***VPD***) branché	①
Ra	**Rd**		②
Rd	**Rd**	***Mode accessoire de débogage*** branché (Annexe B)	***N/A***
Ra	**Ra**	***Mode inhibition de corrosion liquide*** branché (Annexe A)	***N/A***

Après alimentation, le destinataire surveille CC1 et CC2 pour identifier une tension supérieure à la tension de masse locale. La broche CC dont la tension est la plus élevée (donc polarisée par ***Rp*** dans la source) indique l'orientation de la fiche.

Le Tableau 4-11 récapitule les comportements types de sources (hôtes) et de destinataires (dispositifs) simples pour chaque état décrit dans le Tableau 4-10.

Tableau 4-11 Comportements de la source (hôte) et du destinataire (dispositif) par état

État	Comportement de la source	Comportement du destinataire
Aucun branchement	• Détecte les broches CC pour le branchement • N'applique pas VBUS ou VCONN	• Détecte VBUS pour le branchement

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État	Comportement de la source	Comportement du destinataire
Destinataire branché	• Détecte CC pour l'orientation • Détecte CC pour le débranchement • Applique VBUS et VCONN	• Détecte les broches CC pour l'orientation • Détecte la perte de VBUS pour le débranchement
Câble alimenté sans destinataire branché	• Détecte les broches CC pour le branchement • N'applique pas VBUS ou VCONN	• Détecte VBUS pour le branchement
Câble alimenté avec un destinataire, un *accessoire alimenté par VCONN* (*VPA*) ou un *dispositif USB alimenté par VCONN* (*VPD*) branché	• Détecte CC pour l'orientation • Détecte CC pour le débranchement • Applique VBUS et VCONN • Détecte *VPD* et retire VBUS	• Si les accessoires ou les *VPD* sont pris en charge, se référer à la colonne Comportement de la source, à l'exception de VBUS qui n'est pas appliqué. Sinon, ***N/A***.
***Mode accessoire de débogage* branché**	• Détecte les broches CC pour le débranchement • Reconfigure pour le débogage	• Détecte VBUS pour le débranchement • Reconfigure pour le débogage
***Mode inhibition de corrosion liquide* branché**	• Détecte les broches CC pour le débranchement • Reconfigure pour l'audio analogique	• Si les accessoires sont pris en charge, se référer à la colonne Comportement de la source. Sinon, ***N/A***

La Figure 4-3 représente comment l'orientation de la fiche insérée est détectée au niveau de l'embase de la source en identifiant sur laquelle des deux broches CC de l'embase la terminaison *Rd* est décelée. Quand la source (hôte) a reconnu qu'un destinataire (dispositif) est branché et quand l'orientation de la fiche est déterminée, la source configure le routage du bus de données TX/RX vers l'embase.

La source (hôte) active ensuite la VBUS. Pour les broches CC qui ne connectent pas la source au destinataire par câble, la source alimente la VCONN et ***peut*** retirer la terminaison. Lorsque le destinataire (dispositif) est sous tension, il configure le chemin de données USB. Cela finalise la connexion hôte-dispositif.

La source surveille le fil CC (perte de la terminaison de dépolarisation) afin de détecter tout débranchement. Lorsque le destinataire est retiré, le port source élimine toute tension appliquée sur la VBUS et la VCONN, réinitialise la configuration de son interface et reprend la recherche d'un nouveau branchement de destinataire.

Lorsqu'une connexion source-destinataire valide est établie, des alternatives aux alimentations USB traditionnelles (VBUS définie par les spécifications ***USB 2.0*** ou ***USB 3.2***) peuvent être disponibles en fonction des capacités de l'hôte et du dispositif. Il s'agit notamment du *courant USB Type-C*, de la ***charge des batteries par USB 1.2*** et de l'***USB Power Delivery***.

Lorsque l'***USB PD PR_Swap*** est utilisée pour permuter la source et le destinataire d'une VBUS, le fournisseur de la VCONN reste inchangé pendant et après la permutation d'alimentation de la VBUS. La nouvelle source surveille le fil CC et le nouveau destinataire surveille la VBUS afin de détecter tout débranchement. Lorsqu'un débranchement est détecté, toutes les tensions appliquées sur la VBUS et la VCONN sont éliminées, et chaque port réinitialise la configuration de son interface et reprend la recherche d'un nouveau branchement.

Lorsque l'***USB PD DR_Swap*** est utilisée pour permuter les rôles de données (DFP et UFP), la source de la VBUS et de la VCONN n'est pas modifiée après la permutation des rôles de transmission de données.

Lorsque l'***USB PD VCONN_Swap*** est utilisée pour permuter la source de la VCONN, la source/le destinataire de la VBUS et les rôles DFP/UFP sont conservés pendant et après la permutation de la VCONN.

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La dernière étape du processus de connexion normale par USB Type-C renvoie au dispositif USB à brancher et à énumérer conformément aux processus normalisés ***USB 2.0*** et ***USB 3.2***.

4.5.1.3 Modèles fonctionnels du canal de configuration

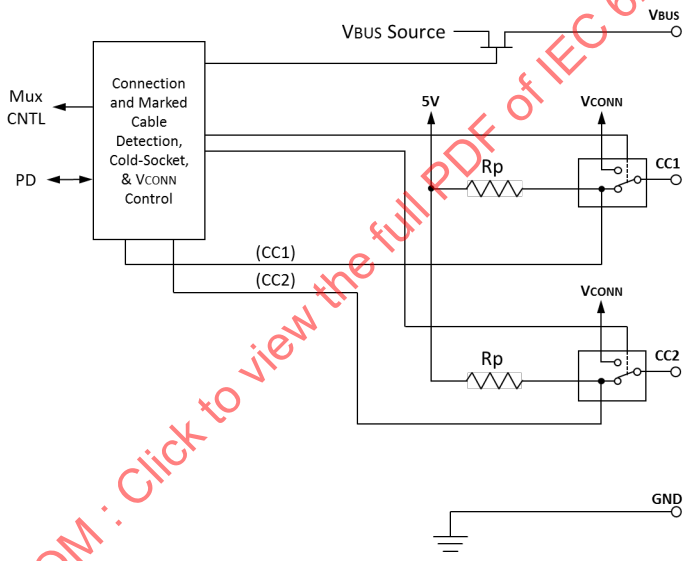
Les modèles fonctionnels relatifs au comportement du canal de configuration fondé sur les broches CC1 et CC2 sont décrits dans le présent paragraphe pour chaque type de port: Source, Destinataire et Alimentation double fonction (DRP).

Les figures suivantes représentent les routages CC1 et CC2 à la fin du processus de détection CC. Dans ces figures, les broches VBUS et VCONN ***peuvent*** ou ***peuvent ne pas*** être disponibles.

4.5.1.3.1 Modèle fonctionnel du canal de configuration d'une source

La Figure 4-7 représente le modèle fonctionnel des broches CC1 et CC2 d'un port source avant branchement. Cette image prend en compte l'***USB PD***.

Figure 4-7 Modèle fonctionnel des broches CC1 et CC2 d'une source



Anglais	Français
Connection and Marked Cable Detection, Cold-Socket, & VCONN Control	Détection de connexion et de câbles marqués électroniquement, prise commutée et contrôle de VCONN
VBUS Source	Source VBUS

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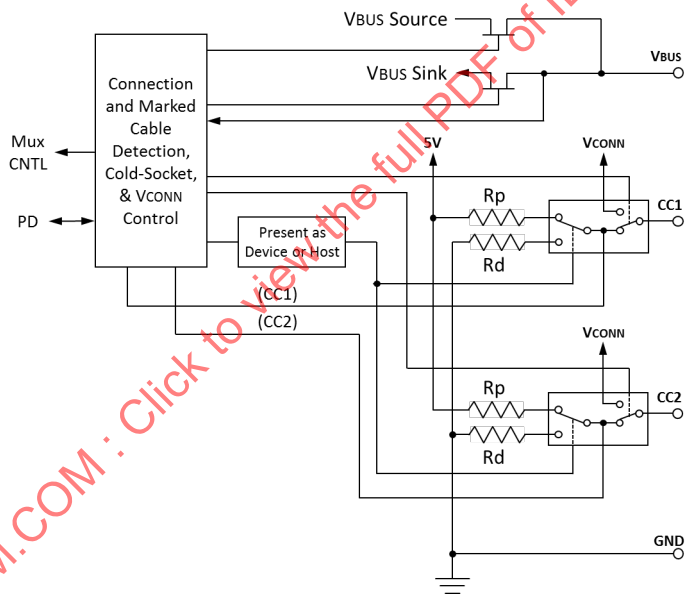
D'après la Figure 4-7, un port qui se comporte comme une source présente les caractéristiques fonctionnelles suivantes:

1. La source utilise un TEC pour activer/désactiver l'alimentation par la VBUS ou lorsque la source est initialement équipée d'une VBUS désactivée.
2. La source fournit les résistances de polarisation (***Rp***) sur les broches CC1 et CC2, et surveille ces dernières en vue de détecter un destinataire. La présence d'une résistance de dépolarisation (***Rd***) sur l'une des broches indique qu'un destinataire est branché. La valeur d'une ***Rp*** indique l'intensité initiale de ***courant USB Type-C*** prise en charge par l'hôte.

3. La source peut, ***de manière facultative***, bloquer la tension sur l'une ou l'autre de ses broches CC. La tension de blocage minimale ***doit*** être ***vCC-Clamp***. Le blocage est destiné à protéger le circuit Source associé à la fonctionnalité CC.
4. La source utilise la capacité de dépolarisation des broches CC pour détecter et établir le routage adapté au chemin de données USB TX/RX et déterminer quelle broche CC est destinée à alimenter la VCONN.
5. Dès lors qu'un destinataire est détecté, la source active la VBUS et la VCONN.
6. La source peut régler dynamiquement la valeur de la ***Rp*** pour indiquer une modification de ***courant USB Type-C*** disponible vers un destinataire.
7. La source surveille le maintien de la présence de ***Rd***, afin de détecter tout débranchement du destinataire. Lorsqu'un débranchement est détecté, la source élimine (le cas échéant) la VBUS et la VCONN et revient à l'étape 2.
8. Si la source prend en charge les fonctions avancées (par exemple, ***USB Power Delivery, USB4*** et ***modes alternatifs***), une communication ***USB PD*** est exigée.

La Figure 4-8 représente le modèle fonctionnel des broches CC1 et CC2 d'une source qui prend en charge l'***USB PD PR_Swap***.

Figure 4-8 Modèle fonctionnel d'une source prenant en charge *USB PD* PR_Swap



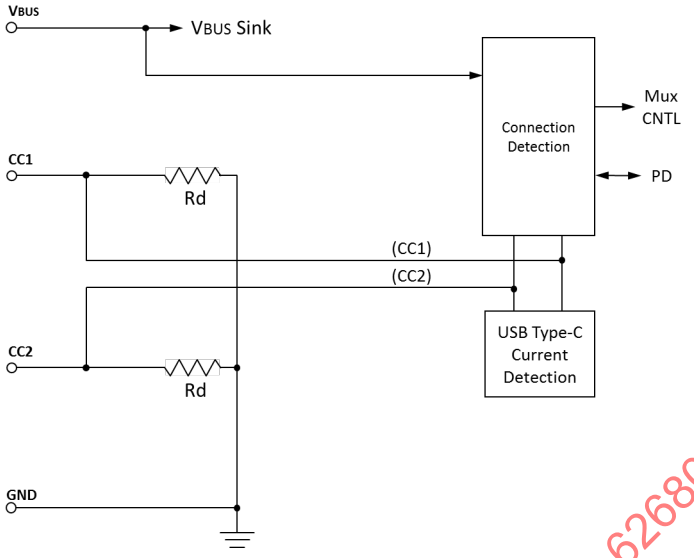
Anglais	Français
Connection and Marked Cable Detection, Cold-Socket, & VCONN Control	Détection de connexion et de câbles marqués électroniquement, prise commutée et contrôle de VCONN
Present as device or Host	Dispositif ou hôte présent
VBUS Source	Source VBUS
VBUS Sink	Destinataire VBUS

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4.5.1.3.2 Modèle fonctionnel du canal de configuration d'un destinataire

La Figure 4-9 représente le modèle fonctionnel des broches CC1 et CC2 d'un destinataire. Cette image prend en compte le ***courant USB Type-C*** et l'***USB PD***.

Figure 4-9 Modèle fonctionnel des broches CC1 et CC2 d'un destinataire



Anglais	Français
VBUS Sink	Destinataire VBUS
Connection Detection	Détection de connexion
USB Type-C Current Detection	Détection de courant USB Type-C

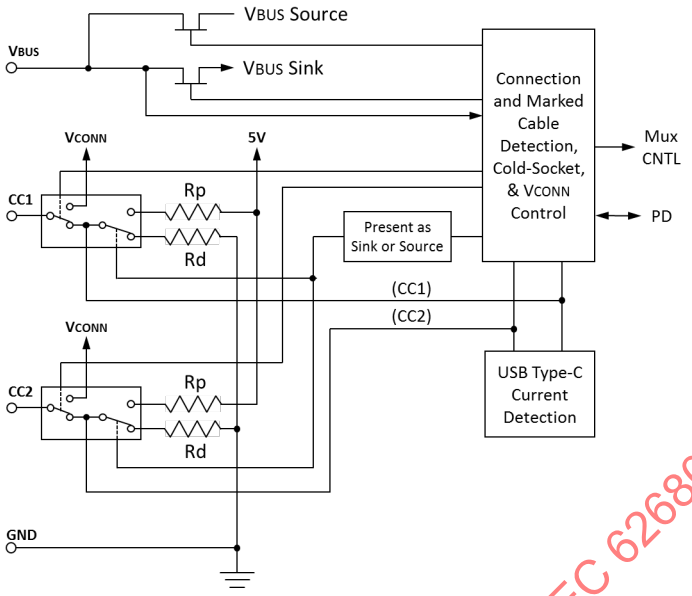
D'après la Figure 4-9, un port qui se comporte comme un destinataire présente les caractéristiques fonctionnelles suivantes:

1. Le destinataire termine les broches CC1 et CC2 vers la GND avec des résistances de dépolarisation.
2. Le destinataire détermine qu'une source est branchée par la présence d'une alimentation sur la VBUS.
3. Le destinataire utilise la caractéristique de polarisation des broches CC pour détecter et établir le routage adéquat au chemin de données USB TX/RX.
4. Le destinataire peut, ***de manière facultative***, surveiller les broches CC pour détecter un ***courant USB Type-C*** supérieur, disponible en provenance de la source. Le destinataire ***doit*** gérer sa charge afin de respecter la limite de courant de la source détectée.
5. Le destinataire peut, ***de manière facultative***, bloquer la tension sur l'une ou l'autre de ses broches CC. La tension de blocage minimale ***doit*** être ***vCC-Clamp***. Le blocage est destiné à protéger le circuit du destinataire associé à la fonctionnalité CC.
6. Si le destinataire prend en charge les fonctions avancées (par exemple, ***USB Power Delivery, USB4*** et ***modes alternatifs***), une communication ***USB PD*** est exigée.

La Figure 4-10 représente le modèle fonctionnel des broches CC1 et CC2 d'un destinataire qui prend en charge l'***USB PD PR_Swap*** et l'***USB PD VCONN_Swap*** avant branchement.

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Figure 4-10 Modèle fonctionnel d'un destinataire prenant en charge l'*USB PD* PR_Swap et VCONN_Swap



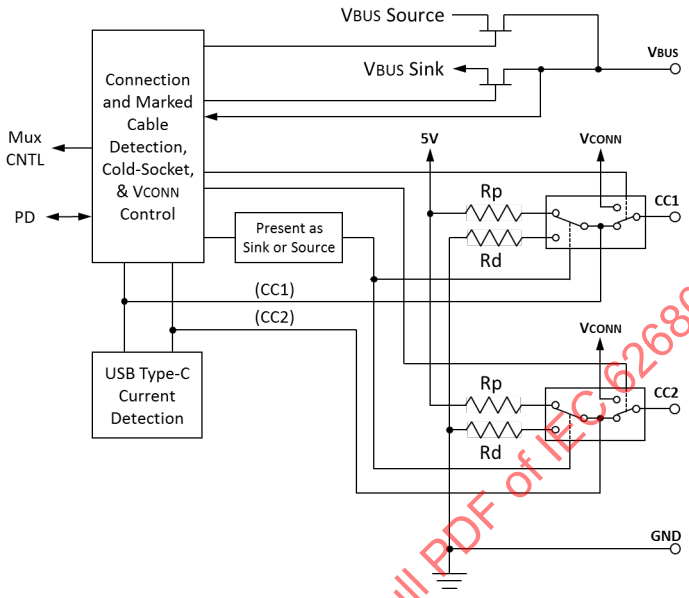
Anglais	Français
Connection and Marked Cable Detection, Cold-Socket, & VCONN Control	Détection de connexion et de câbles marqués électroniquement, prise commutée et contrôle de VCONN
Present as Sink or Source	Source ou destinataire présent
VBUS Source	Source VBUS
VBUS Sink	Destinataire VBUS
USB Type-C Current Detection	Détection de courant USB Type-C

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4.5.1.3.3 Modèle fonctionnel du canal de configuration de l'alimentation double fonction (DRP)

La Figure 4-11 représente le modèle fonctionnel des broches CC1 et CC2 d'une DRP apparaissant comme une source avant branchement. Cette image prend en compte les fonctionnalités de ***courant USB Type-C*** et ***USB PD***.

Figure 4-11 Modèle fonctionnel des broches CC1 et CC2 d'une DRP



Anglais	Français
Connection and Marked Cable Detection, Cold-Socket, & VCONN Control	Détection de connexion et de câbles marqués électroniquement, prise commutée et contrôle de VCONN
Present as Sink or Source	Source ou destinataire présent
VBUS Source	Source VBUS
VBUS Sink	Destinataire VBUS
USB Type-C Current Detection	Détection de courant USB Type-C

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D'après la Figure 4-11, un port qui peut alterner entre les comportements DFP et UFP présente les caractéristiques fonctionnelles suivantes:

1. La DRP utilise un TEC pour activer/désactiver l'alimentation par VBUS. En mode source, VBUS est initialement désactivée.
2. La DRP utilise des commutateurs pour apparaître comme une source ou un destinataire.
3. La DRP fait appel à une logique utilisée pendant le branchement initial pour alterner entre le fonctionnement source et destinataire:
    a. Jusqu'à ce qu'un état stable spécifique soit atteint, la DRP apparaît alternativement comme une source et un destinataire. La temporisation du processus est dictée par une période (***tDRP***), le pourcentage de temps d'exposition d'une ***Rp*** par la DRP (***dcSRC.DRP***) et le délai de transition des rôles (***tDRPTransition***).
    b. Lorsque la DRP apparaît comme une source, elle suit le fonctionnement d'une source pour détecter un destinataire branché (lorsqu'un destinataire est détecté, il applique VBUS et VCONN, et continue de fonctionner comme une source, par exemple interruption alternative).

c. Lorsque la DRP apparaît comme un destinataire, elle surveille VBUS pour détecter le branchement à une source (si une source est détectée, elle continue de fonctionner comme un destinataire, interruption alternative).

4. Si la DRP prend en charge les fonctions avancées (par exemple, ***USB Power Delivery, USB4*** et ***modes alternatifs***), une communication ***USB PD*** est exigée.

4.5.1.4 Rôles d'alimentation des ports USB Type-C et mécanismes de permutation des rôles

Les ports USB Type-C des produits (hôte USB, dispositifs USB, chargeurs USB, etc.) peuvent généralement se caractériser comme mettant en œuvre un des sept modèles de comportement des rôles d'alimentation:

- Source uniquement
- Source (par défaut): nette préférence pour le rôle de source, mais capacité à devenir par la suite un destinataire avec des mécanismes de permutation ***USB PD***
- Destinataire uniquement
- Destinataire (par défaut): nette préférence pour le rôle de destinataire, mais capacité à devenir par la suite une source par le biais des mécanismes de permutation ***USB PD***
- DRP: Alternance (source/destinataire)
- DRP: Dispositif d'alimentation
- DRP: Hôte destinataire

Deux ensembles indépendants de mécanismes de permutation sont définis pour les mises en œuvre de ports USB Type-C. Le premier repose sur la permutation des rôles dans le processus de connexion initiale avec diagramme d'états, le second sur l'utilisation ultérieure des mécanismes de permutation de l'***USB PD***.

4.5.1.4.1 Permutation des rôles fondée sur le diagramme d'états USB Type-C

Pendant le processus de connexion initiale avec diagramme d'états USB Type-C, les produits à connecter se terminent lorsque l'un des deux rôles suivants est associé à la terminaison de son port:

- ***Rp*** → source de la VBUS et de la VCONN qui se comporte comme un port orienté en aval (hôte USB);
- ***Rd*** → destinataire de la VBUS qui se comporte comme un port orienté en amont (dispositif USB).

Un produit DRP USB Type-C ***peut*** intégrer les mécanismes de permutation ***Try.SRC*** et ***Try.SNK*** pour affecter le rôle résultant. ***Try.SRC*** permet à une DRP avec préférence stratégique de constituer une source lorsqu'elle se connecte à une autre DRP pour effectuer une transition depuis un rôle de destinataire prévu vers le rôle de source. De son côté, ***Try.SNK*** permet à une DRP avec préférence stratégique de constituer un destinataire lorsqu'elle se connecte à une autre DRP pour effectuer une transition depuis un rôle de source prévu vers le rôle de destinataire. La temporisation de la connexion et d'autres facteurs sont impliqués dans ce processus, comme cela est défini pour le fonctionnement avec diagramme d'états USB Type-C (voir 4.5.2). Il est important de noter que ces fonctions (***Try.SRC*** et ***Try.SNK***) ne peuvent être utilisées qu'une seule fois dans le cadre du processus de connexion initiale. Lorsque les deux côtés prennent en charge ***USB PD***, les rôles pertinents ***peuvent*** ensuite être affinés ou permutés selon la spécification ***USB PD***.

Il convient qu'un produit DRP USB Type-C qui ne prend pas en charge ***USB PD*** mette en œuvre ***Try.SRC*** ou ***Try.SNK*** en fonction de sa préférence afin de garantir des rôles d'alimentation et de données prévisibles. Par exemple, ***il convient*** qu'un dispositif mobile de petite taille qui préfère assumer le rôle de destinataire ou d'UFP mette en œuvre ***Try.SNK*** de sorte que, lorsqu'il est branché à un système DRP, tel qu'un ordinateur portable, le dispositif mobile reste le destinataire de l'alimentation. Si le dispositif mobile est connecté à un port partenaire destinataire uniquement, la méthode ***Try.SNK*** échoue et le dispositif mobile finit par prendre le rôle de source. Si le dispositif mobile est connecté à un port partenaire qui met également en œuvre ***Try.SNK***, le dispositif mobile prendra, de façon aléatoire, le rôle de source ou de destinataire. De même, ***il convient*** qu'un hôte DRP, tel qu'un PC de bureau, qui ne consomme pas d'énergie sur le port mette en œuvre ***Try.SRC*** pour s'assurer qu'il finit toujours par agir comme DFP lorsqu'il est branché à des DRP.

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Un produit DRP USB Type-C, indépendamment de sa prise en charge de l'***USB PD***, ***peut*** également mettre en œuvre ***Try.SRC*** ou ***Try.SNK*** afin d'assumer, de préférence, un rôle de données lorsqu'il est connecté à une autre DRP qui ne prend pas en charge l'***USB PD***. Si ce produit ne prend en charge qu'un rôle de données spécifique (DFP ou UFP), ***il convient*** qu'il mette en œuvre ***Try.SRC*** ou ***Try.SNK*** afin d'assumer un rôle de données utilisable lorsqu'il est connecté à une autre DRP qui ne prend pas en charge l'***USB PD***. Dans ce dernier cas, ***il convient que*** l'utilisation du mécanisme Try visant à assurer un alignement correct sur le rôle de données d'un produit prévale sur l'utilisation du mécanisme Try visant à assurer un alignement correct sur le rôle d'alimentation préférentiel, car le mécanisme Try peut être pour le produit la seule occasion de jouer un rôle fonctionnel utilisable.

Le Tableau 4-12 récapitule la mise en œuvre recommandée de ***Try.SRC*** et de ***Try.SNK*** par les ports USB Type-C double fonction avec des rôles d'alimentation ou de données préférentiels. Pour les ports double fonction, où un seul rôle de données est pertinent sur le plan fonctionnel, ***il convient que*** ce rôle de données constitue le rôle de données préférentiel, par exemple un dispositif de stockage USB a un rôle de données préférentiel d'UFP sur son port.

Tableau 4-12 Mise en œuvre recommandée de Try.SRC et Try.SNK pour les ports double fonction avec rôles préférentiels

Rôles préférentiels actuels du port double fonction:	Recommandation
Source / Pas de préférence DR	Activer ***Try.SRC*** (pour devenir la source)
Source / DFP	Activer ***Try.SRC***
Source / UFP	Activer ***Try.SNK*** (pour devenir un UFP)
Destinataire / Pas de préférence DR	Activer ***Try.SNK*** (pour devenir le destinataire)
Destinataire / DFP	Activer ***Try.SNK*** (pour devenir un DFP)
Destinataire / UFP	Activer ***Try.SNK***
Pas de préférence PR / DFP	Activer ***Try.SNK*** (pour devenir un DFP)
Pas de préférence PR / UFP	Activer ***Try.SNK*** (pour devenir un UFP)

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4.5.1.4.2 Permutation des rôles d'alimentation, des rôles de données et de la VCONN *USB PD*

À l'issue du processus de connexion initiale avec diagramme d'états USB Type-C, les produits ***peuvent*** utiliser les mécanismes de permutation de l'***USB PD*** pour commander une modification des rôles d'alimentation, des rôles de données et de l'extrémité de câble qui alimente la VCONN. Ces mécanismes sont les suivants:

- ***USB PD PR_Swap***: permute la source (***Rp***) et le destinataire (***Rd***);
- ***USB PD DR_Swap***: permute les rôles DFP (données d'hôte) et UFP (données du dispositif);
- ***USB PD VCONN_Swap***: permute le port qui alimente la VCONN.

Le Tableau 4-13 récapitule les comportements d'un port en réponse aux trois commandes de permutation ***USB PD***.

Tableau 4-13 Récapitulatif du comportement de permutation des ports *USB PD*

	Rôles de données DFP/UFP	Rp/Rd	Source/destinataire VBUS	Source VCONN
PR_Swap	Sans modification	Permutation	Permutation	Sans modification
DR_Swap	Permutation	Sans modification	Sans modification	Sans modification

	Rôles de données DFP/UFP	Rp/Rd	Source/destinataire VBUS	Source VCONN
VCONN_Swap	Sans modification	Sans modification	Sans modification	Permutation[1]
Note 1: Permutation du port source VCONN				

Il convient qu'un produit USB Type-C double fonction qui prend en charge l'***USB PD*** utilise ***USB PD PR_Swap*** et ***DR_Swap*** pour garantir qu'il assume ses rôles d'alimentation et/ou de données préférentiels. Par exemple, ***il convient que*** l'UFP d'un hub ou l'UFP d'un moniteur qui préfère assumer le rôle de source initie ***PR_Swap*** si cela est nécessaire pour passer du rôle de destinataire au rôle de source préférentiel. De même, ***il convient*** qu'un petit dispositif mobile qui privilégie le rôle de destinataire initie ***PR_Swap*** pour passer du rôle de source au rôle de destinataire préférentiel.

Le Tableau 4-14 récapitule l'utilisation recommandée de la permutation des rôles d'alimentation et de données par les ports USB Type-C double fonction qui assument des rôles d'alimentation ou de données préférentiels. Pour les ports double fonction, où un seul rôle de données est pertinent sur le plan fonctionnel, ***il convient que*** ce rôle de données constitue le rôle de données préférentiel, par exemple le port en amont physique d'un hub a un rôle de données préférentiel d'UFP sur ce port.

Tableau 4-14 Utilisation de la permutation des rôles d'alimentation et de données pour les ports double fonction avec des rôles préférentiels

Rôles préférentiels du port double fonction:	Lorsque le port est initialement connecté à un ou une:	
	Source / DFP	Destinataire / UFP
Source / Pas de préférence DR	Émettre ***PR_Swap***	
Source / DFP	Émettre ***PR_Swap*** et ***DR_Swap***	
Source / UFP	Émettre ***PR_Swap***	Émettre ***DR_Swap***
Destinataire / Pas de préférence DR		Émettre ***PR_Swap***
Destinataire / DFP	Émettre ***DR_Swap***	Émettre ***PR_Swap***
Destinataire / UFP		Émettre ***PR_Swap*** et ***DR_Swap***
Pas de préférence PR / DFP	Émettre ***DR_Swap***	
Pas de préférence PR / UFP		Émettre ***DR_Swap***

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4.5.1.4.3 Récapitulatif du modèle comportemental des rôles d'alimentation

Le Tableau 4-15 récapitule les caractéristiques de définition des sept principaux rôles d'alimentation.

Tableau 4-15 Récapitulatif du modèle comportemental des rôles d'alimentation

Rôle d'alimentation	Alternance	PR_Swap	Hôte USB	Dispositif USB	DFP	UFP	DR_Swap	Try.SRC/ Try.SNK	Connexion à...
Source uniquement	Non	NA	Fac.	Fac.[1]	Exigé	Fac.	Fac.	NA	Destinataire ou DRP
Source (par défaut)	Non	Exigé	Fac.	Fac.[1]	Exigé	Fac.	Fac.	NA	Destinataire ou DRP

Rôle d'alimentation		Alternance	PR_Swap	Hôte USB	Dispositif USB	DFP	UFP	DR_Swap	Try.SRC/ Try.SNK	Connexion à...
Destinataire uniquement		Non	NA	Fac.[1]	Fac.	Fac.	Exigé	Fac.	NA	Source ou DRP
Destinataire (par défaut)		Non	Exigé	Fac.[1]	Fac.	Fac.	Exigé	Fac.	NA	Source ou DRP
DRP	**Alternance (source/destinataire)**	Exigé	Exigé	Fac.	Fac.	Exigé	Exigé	Exigé	Fac.	Source, destinataire ou DRP
	Dispositif d'alimentation	Exigé	Exigé	NA	Exigé	Exigé	Exigé	Exigé	Fac.	
	Hôte destinataire	Exigé	Exigé	Exigé	NA	Exigé	Exigé	Exigé	Fac.	
Note 1: Exige l'utilisation de ***DR_Swap***.										

4.5.2 Exigences fonctionnelles et comportementales des broches CC

Le présent paragraphe spécifie les exigences fonctionnelles et comportementales exigées pour la mise en œuvre des broches CC. La première partie fournit les diagrammes d'états de connexion qui constituent le socle des parties suivantes.

Les termes "Source" (SRC) et "Destinataire" (SNK) utilisés dans le présent paragraphe renvoient au rôle d'alimentation du port. Les termes "DFP" et "UFP" renvoient au rôle de données du port. Un port DRP (alimentation double fonction) est capable d'agir comme une source ou un destinataire. En général, les sources se trouvent sur les hôtes et alimentent la VBUS, alors que les destinataires se trouvent sur les dispositifs et consomment l'alimentation en provenance de la VBUS. Lors d'une connexion initiale, l'état d'alimentation initial du port et le rôle de données sont établis. L'***USB PD*** utilise trois commandes de permutation qui ***peuvent*** altérer le rôle d'alimentation ou de données d'un port:

- La commande ***PR_Swap*** modifie l'état d'alimentation du port, conformément aux diagrammes d'états ci-dessous. ***PR_Swap*** ne modifie pas le port d'alimentation de la VCONN.
- La commande ***DR_Swap*** n'a aucun effet sur les diagrammes d'états ci-dessous ni sur la VCONN, car elle ne modifie que le rôle de données du port.
- La commande ***VCONN_Swap*** modifie le port d'alimentation de la VCONN. Les commandes ***PR_Swap*** et ***DR_Swap*** n'ont aucun effet sur le port d'alimentation de la VCONN.

Note: Un ***dispositif USB alimenté par VCONN*** qui prend en charge la capacité de charge ***facultative***, après avoir été détecté par le biais de la messagerie ***USB PD***, modifie également l'état d'alimentation du port côté hôte sans affecter le port d'alimentation de la VCONN.

Note: L'***USB PD*** définit un autre mécanisme ***facultatif*** de permutation (***FR_Swap***), qui est utilisé dans les cas particuliers où une interaction utilisateur involontaire peut rendre nécessaire la modification de la source de la VBUS. Variante de ***PR_Swap***, ***FR_Swap*** procède de la même manière à la permutation de la source (***Rp***) et du destinataire (***Rd***) entre deux ports connectés. Pour les besoins de la présente spécification, seul ***PR_Swap*** est explicitement pris en compte dans les exigences comportementales. Le cas échéant, ***il convient que*** les mises en œuvre prenant en charge ***FR_Swap*** appliquent les comportements associés à ***PR_Swap*** à ***FR_Swap***. Voir la spécification ***USB PD*** pour plus d'informations sur ***FR_Swap***.

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Les diagrammes d'états de connexion et les descriptions du comportement des broches CC du présent paragraphe décrivent le comportement des embases des ports. La fiche d'un dispositif directement branché ou d'un dispositif connecté par un câble captif ***doit*** se comporter comme la fiche d'un câble branché à une embase à son autre extrémité, selon une orientation normale. Ces dispositifs ne ***doivent*** appliquer et détecter les niveaux de tension CC que sur la broche A5. La broche B5 ***doit*** avoir une impédance supérieure à ***zOPEN***, sauf s'il s'agit d'un ***dispositif USB alimenté par VCONN***. Dans ce cas, B5 ***doit*** avoir une impédance ***Ra***.

4.5.2.1 Diagrammes d'états de connexion

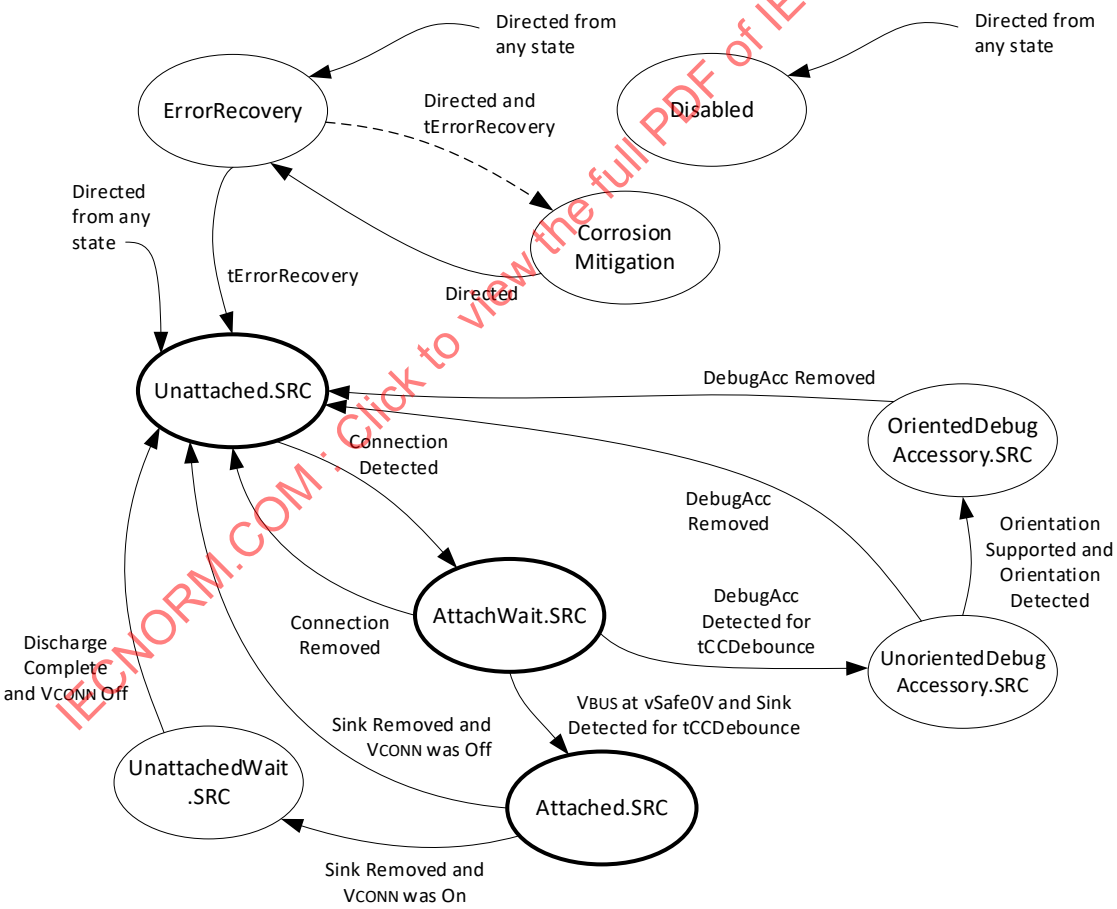
Le présent paragraphe fournit des diagrammes d'états de connexion de référence pour les comportements des broches CC.

Voir 4.5.2.2 pour les exigences de transition d'états spécifiques relatives à chaque état représenté dans les diagrammes.

Voir 4.5.2.6 pour une description des états obligatoires pour chaque type de port, ainsi qu'une liste des états où une communication ***USB PD*** est admise.

La Figure 4-12 représente un diagramme d'états de connexion d'une source (DFP d'hôte/hub).

Figure 4-12 Diagramme d'états de connexion: Source



Anglais	Français
Directed from any state	Induit depuis n'importe quel état

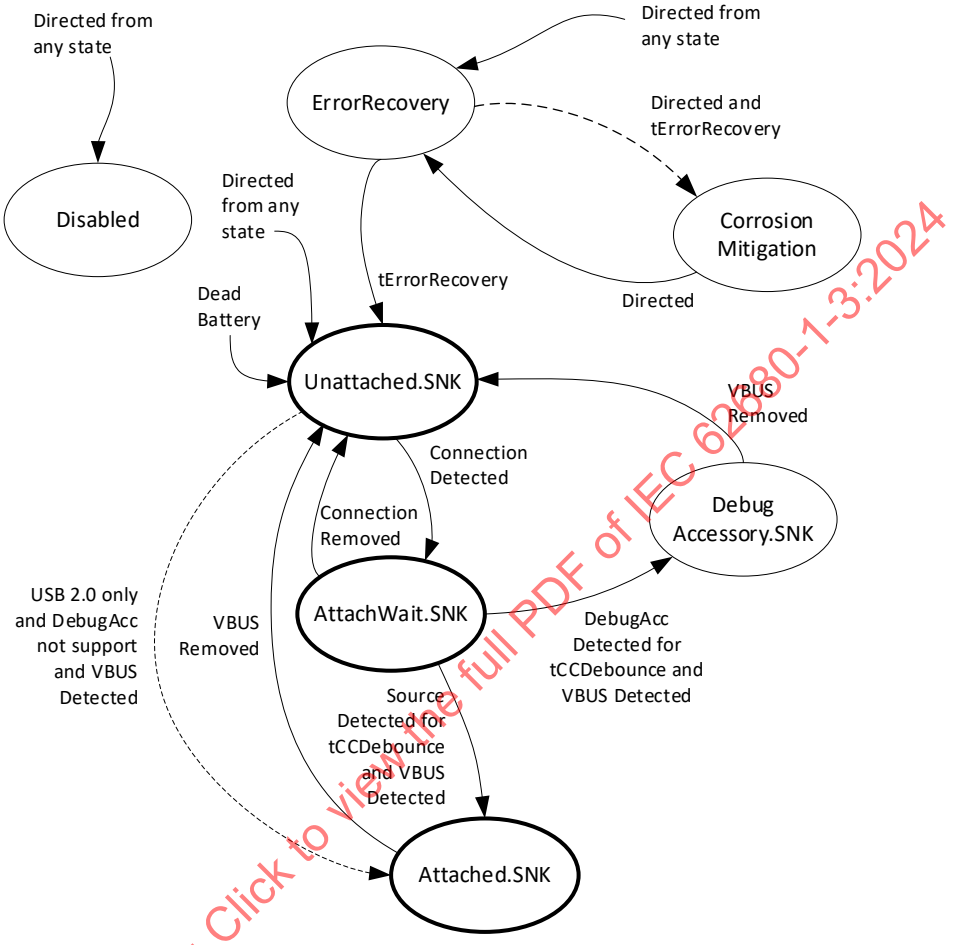
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Anglais	Français
Directed	Induit
Directed and tErrorRecovery	Induit et tErrorRecovery
Corrosion Mitigation	Atténuation de la corrosion
Disabled	Désactivé
Connection detected	Connexion détectée
DebugAcc Removed	DebugAcc retiré
DebugAcc Detected for tCCDebounce	DebugAcc détecté pour tCCDebounce
Connection Removed	Connexion supprimée
Orientation Supported and Orientation Detected	Orientation prise en charge et détectée
Connection Removed	Connexion supprimée
Discharge Complete and VCONN Off	Déchargement complet et VCONN désactivée
Sink Removed and VCONN was Off	Destinataire supprimé et VCONN désactivée
Sink Removed and VCONN was On	Destinataire supprimé et VCONN activée
VBUS at vSafe0V and Sink Detected for tCCDebounce	VBUS en état vSafe0V et destinataire détecté pour tCCDebounce

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La Figure 4-13 représente un diagramme d'états de connexion d'un destinataire simple (UFP de dispositif/hub).

Figure 4-13 Diagramme d'états de connexion: Destinataire

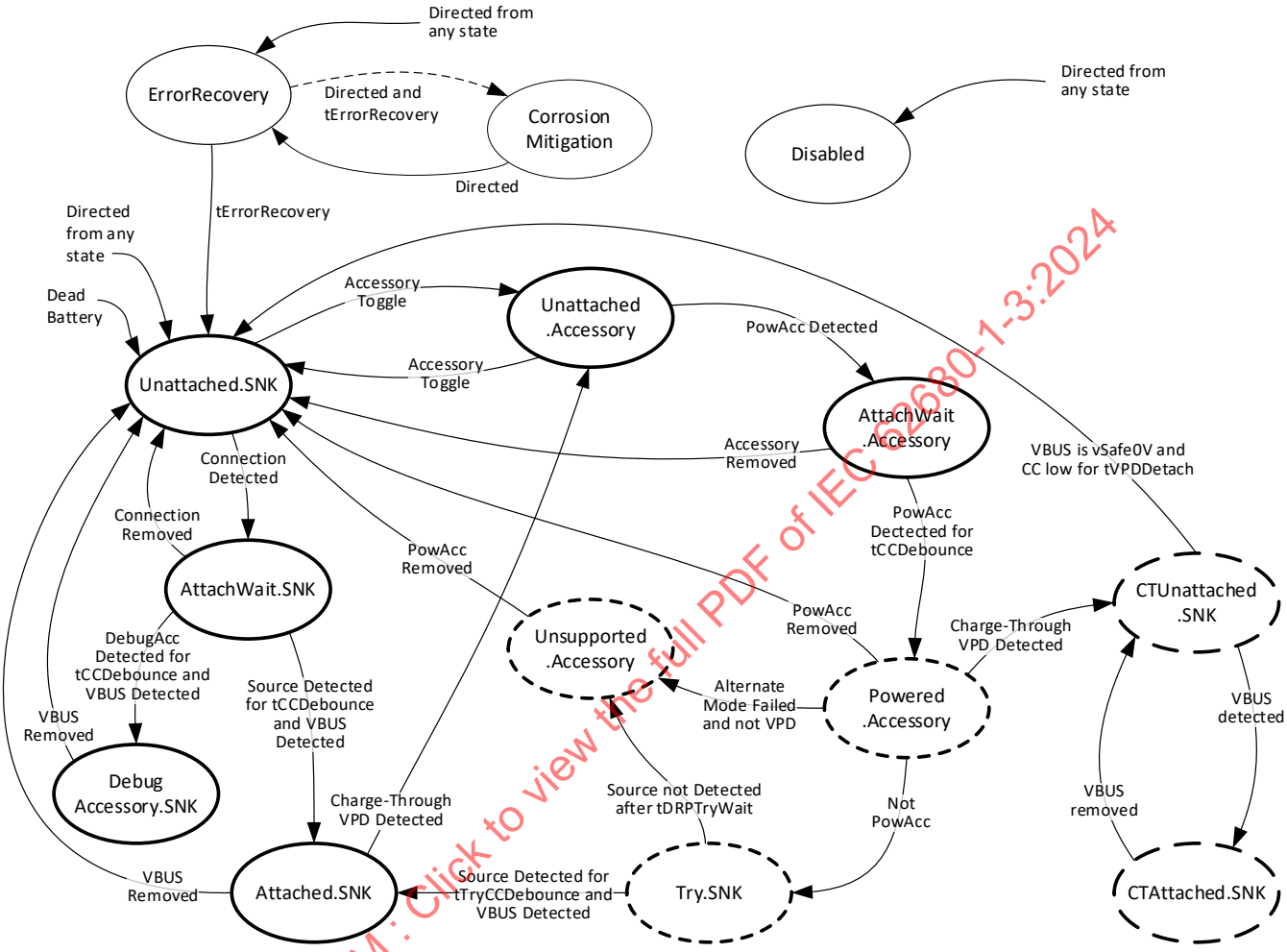


Anglais	Français
Disabled	Désactivé
Directed from any state	Induit depuis n'importe quel état
Directed and tErrorRecovery	Induit et tErrorRecovery
Corrosion Mitigation	Atténuation de la corrosion
Dead Battery	Batterie déchargée
USB 2.0 only and DebugAcc not support and VBUS Detected	USB 2.0 seul et DebugAcc non pris en charge et VBUS détectée
VBUS Removed	VBUS retirée
Connection Detected	Connexion détectée
Connection Removed	Connexion supprimée
Source Detected for tCCDebounce and VBUS Detected	Source détectée pour tCCDebounce et VBUS détectée
DebugAcc Detected for tCCDebounce and VBUS Detected	DebugAcc détecté pour tCCDebounce et VBUS détectée

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La Figure 4-14 représente un diagramme d'états de connexion d'un destinataire avec prise en charge des modes accessoires.

Figure 4-14 Diagramme d'états de connexion: Destinataire avec prise en charge des accessoires



Anglais	Français
Disabled	Désactivé
Corrosion Mitigation	Atténuation de la corrosion
Dead Battery	Batterie déchargée
Directed from any state	Induit depuis n'importe quel état
Directed and tErrorRecovery	Induit et tErrorRecovery
Accessory Toggle	Alternance accessoire
Connection Detected	Connexion détectée
Connection Removed	Connexion supprimée
Accessory Removed	Accessoire retiré
Accessory Toggle	Alternance accessoire
PowerAcc Detected	PowerAcc détecté
PowerAcc Detected for tCCDebounce	PowerAcc détecté pour tCCDebounce

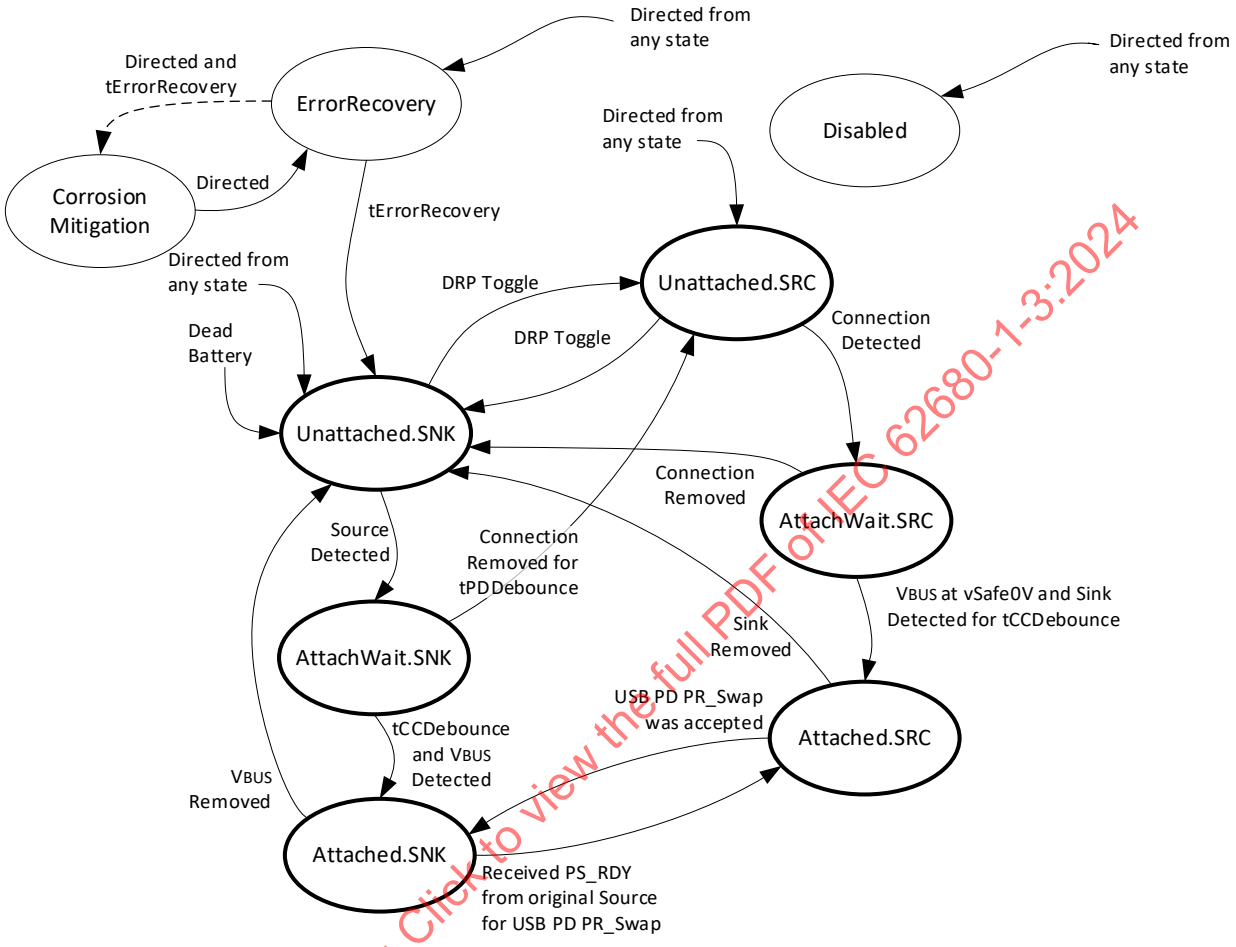
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Anglais	Français
Source Detected for tCCDebounce and VBUS Detected	Source détectée pour tCCDebounce et VBUS détectée
DebugAcc Detected for tCCDebounce and VBUS Detected	DebugAcc détecté pour tCCDebounce et VBUS détectée
VBUS Removed	VBUS retirée
VBUS removed	VBUS retirée
VBUS detected	VBUS détectée
Charge-through VPD detected	VPD de charge détectée
PowerAcc Removed	PowerAcc retirée
Unsupported accessory	Accessoire non pris en charge
Powered accessory	Accessoire sous tension
Alternate Mode failed	Échec du Mode Alternatif
Not PowerAcc	Pas de PowerAcc
Source not Detected after tDRPTryWait	Source non détectée après tDRPTryWait
Source Detected for tTryCCDebounce and VBUS Detected	Source détectée pour tTryCCDebounce et VBUS détectée
VBUS is vSafe0V and CC low for tVPDDetach	VBUS en état vSafe0V et tension continue faible pour tVPDDetach

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La Figure 4-15 représente un diagramme d'états de connexion d'un port DRP (alimentation double fonction) simple.

Figure 4-15 Diagramme d'états de connexion: DRP



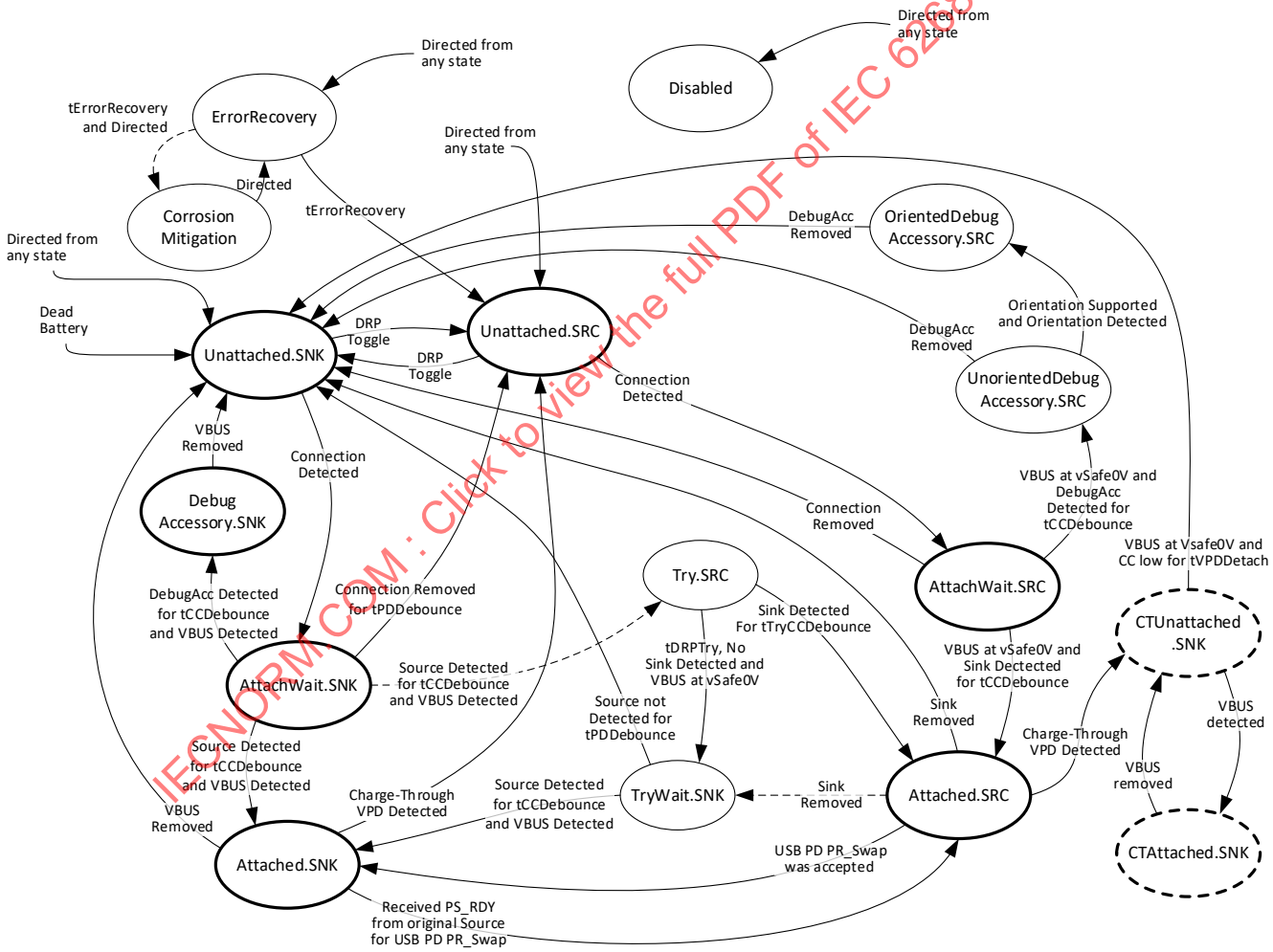
Anglais	Français
Disabled	Désactivé
Directed from any state	Induit depuis n'importe quel état
Directed	Induit
Corrosion Mitigation	Atténuation de la corrosion
Directed and tErrorRecovery	Induit et tErrorRecovery
DRP Toggle	Alternance DRP
Connection Detected	Connexion détectée
Connection Removed	Connexion supprimée
Connection Removed for tPDDebounce	Connexion supprimée pour tPDDebounce
Source Detected	Source détectée
Source Removed	Source retirée
Dead Battery	Batterie déchargée
Sink Removed	Destinataire retiré

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Anglais	Français
VBUS at vSafe0V and Sink Detected for tCCDebounce	VBUS en état vSafe0V et destinataire détecté pour tCCDebounce
USB PD PR_Swap was accepted	USB PD PR_Swap accepté
tCCDebounce and VBUS Detected	tCCDebounce et VBUS détectés
VBUS Removed	VBUS retirée
Received PS_RDY from original Source or USB PD PR_Swap	PS_RDY reçu depuis la Source originale ou USB PD PR_Swap

La Figure 4-16 représente un diagramme d'états de connexion d'une DRP avec prise en charge de l'état ***Try.SRC*** et des modes accessoires.

Figure 4-16 Diagramme d'états de connexion: DRP avec prise en charge de l'état Try.SRC et des modes accessoires



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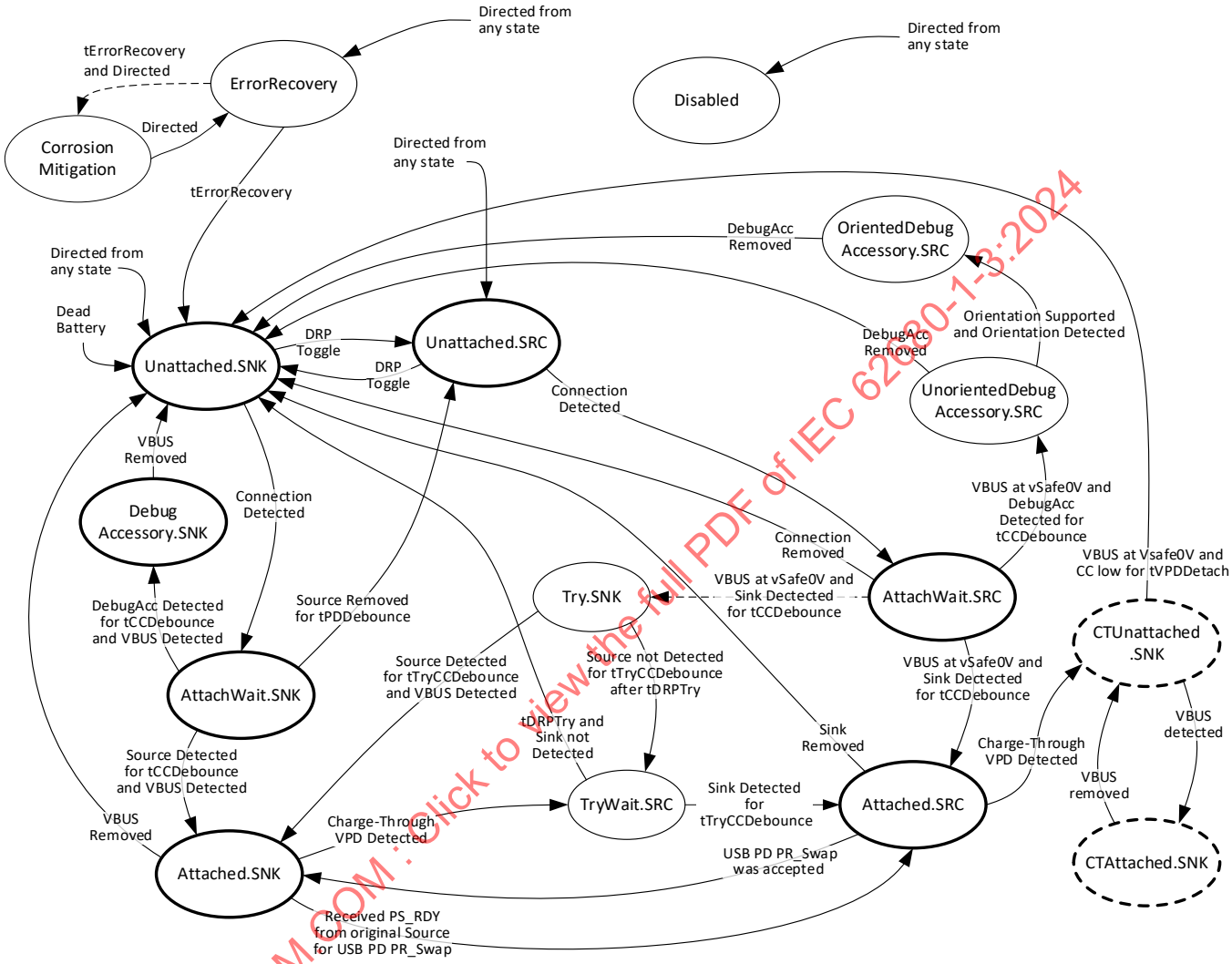
Anglais	Français
Disabled	Désactivé
Directed from any state	Induit depuis n'importe quel état

Anglais	Français
tErrorRecovery and Directed	tErrorRecovery et induit
Directed	Induit
Corrosion Mitigation	Atténuation de la corrosion
DRP Toggle	Alternance DRP
Connection Detected	Connexion détectée
Connection Removed	Connexion supprimée
Dead Battery	Batterie déchargée
DebugAcc Removed	DebugAcc retiré
Orientation Supported And Orientation Detected	Orientation prise en charge et détectée
Sink Removed	Destinataire retiré
VBUS at vSafe0V and Sink Detected for tCCDebounce	VBUS en état vSafe0V et destinataire détecté pour tCCDebounce
VBUS at vSafe0V and CC low for tVPDDetach	VBUS en état vSafe0V et tension continue faible pour tVPDDetach
VBUS removed	VBUS retirée
VBUS detected	VBUS détectée
Charge-Through VPD Detected	VPD de charge détectée
USB PD PR_Swap was accepted	USB PD PR_Swap accepté
VBUS Removed	VBUS retirée
Received PS_RDY from original Source or USB PD PR_Swap	PS_RDY reçu depuis la Source originale ou USB PD PR_Swap
DebugAcc Removed	DebugAcc retiré
DebugAcc Detected for tCCDebounce	DebugAcc détecté pour tCCDebounce
Connection Removed for tCCDebounce	Connexion supprimée pour tCCDebounce
Source Detected for tCCDebounce and VBUS detected	Source détectée pour tCCDebounce et VBUS détectée
Sink Detected for tCCDebounce	Destinataire détecté pour tCCDebounce
Source not Detected for tPDDebounce	Source non détectée pour tCCDebounce
No Sink Detected and VBUS at vSafe0V	Aucun destinataire détecté et VBUS en état vSafe0V
Sink Detected For tTryCCDebounce	Destinataire détecté pour tTryCCDebounce
VBUS is vSafe0V and CC low for sVPDDetach	VBUS en état vSafe0V et tension continue faible pour sVPDDetach

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La Figure 4-17 représente un diagramme d'états de connexion d'une DRP avec prise en charge de l'état ***Try.SNK*** et des modes accessoires.

Figure 4-17 Diagramme d'états de connexion: DRP avec prise en charge de l'état Try.SNK et des modes accessoires



Anglais	Français
Disabled	Désactivé
Directed from any state	Induit depuis n'importe quel état
Corrosion Mitigation	Atténuation de la corrosion
tErrorRecovery and Directed	tErrorRecovery et induit
Directed	Induit
DRP Toggle	Alternance DRP
Connection Detected	Connexion détectée
Connection Removed	Connexion supprimée
Debug Accessory.SNK	Débugger Accessory.SNK
Dead Battery	Batterie déchargée

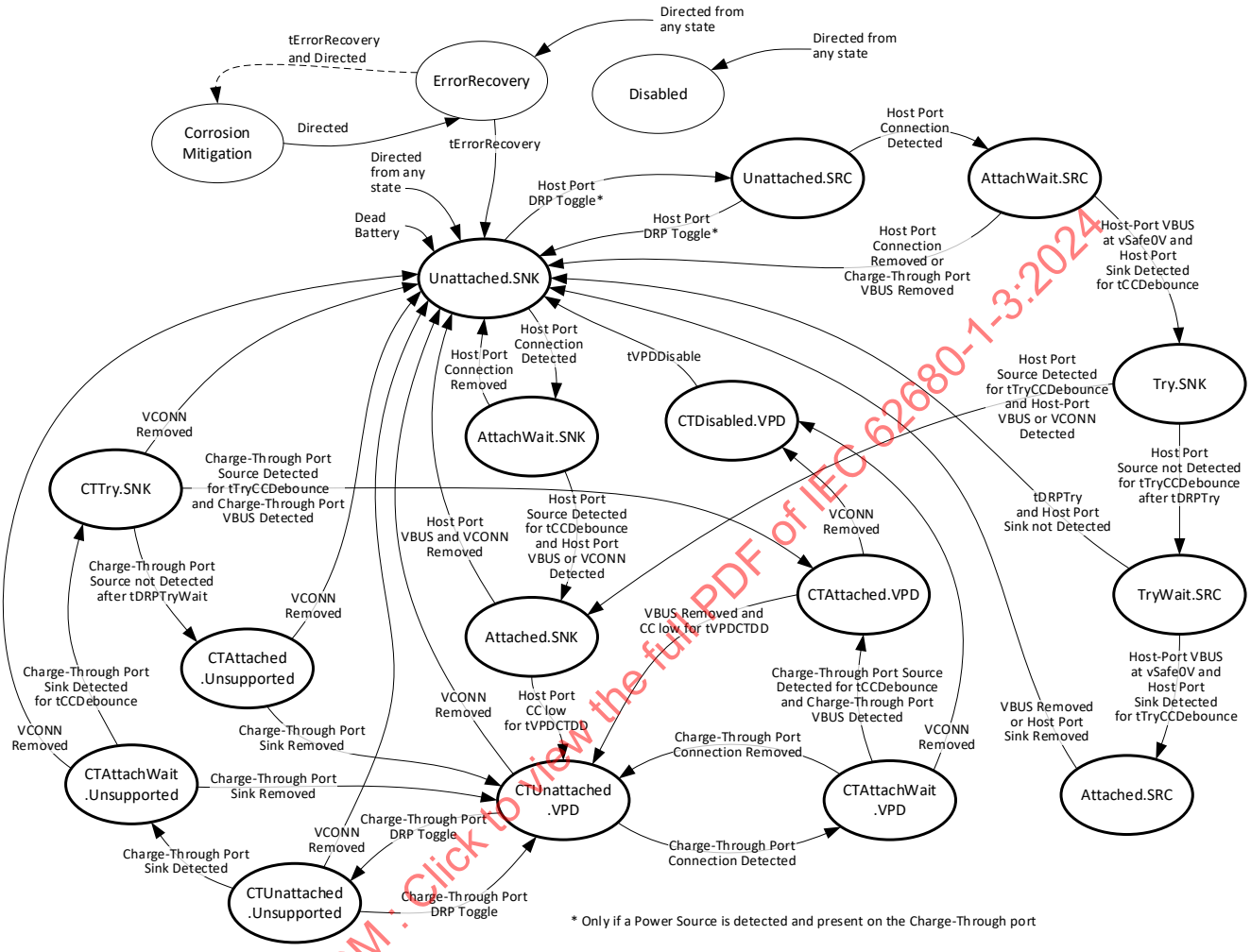
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Anglais	Français
DebugAcc Removed	DebugAcc retiré
Orientation Supported And Orientation Detected	Orientation prise en charge et détectée
Sink Removed	Destinataire retiré
VBUS at vSafe0V and Sink Detected for tCCDebounce	VBUS en état vSafe0V et destinataire détecté pour tCCDebounce
VBUS at vSafe0V and DebugAcc Detected for tCCDebounce	VBUS en état vSafe0V et DebugAcc détecté pour tCCDebounce
VBUS Removed	VBUS retirée
Received PS_RDY from original Source for USB PD PR_Swap	PS_RDY reçu depuis la Source originale ou USB PD PR_Swap
USB PF PR_Swap was accepted	USB PF PR_Swap accepté
Charge-Through VPD Detected	VPD de charge détectée
DebugAcc Detected for tCCDebounce and VBUS Detected	DebugAcc détecté pour tCCDebounce et VBUS détectée
DebugAcc Detected for tCCDebounce	DebugAcc détecté pour tCCDebounce
Source Removed for tCCDebounce	Source supprimée pour tCCDebounce
Source Detected for tCCDebounce and VBUS detected	Source détectée pour tCCDebounce et VBUS détectée
Sink Detected for tTryCCDebounce	Destinataire détecté pour tTryCCDebounce
Source not Detected for tTryCCDebounce after tDRPTry	Source non détectée pour tCCDebounce après tDRPTry
tDRPTry and Sink not Detected	tDRPTry et Destinataire non détectés
Sink Detected for tCCDebounce	Destinataire détecté pour tCCDebounce
VBUS Removed	VBUS retirée
VBUS Detected	VBUS détectée
Source Detected for tTryCCDebounce and VBUS detected	Source détectée pour tTryCCDebounce et VBUS détectée
VBUS at vSafe0V and CC low for tVPDDetach	VBUS en état vSafe0V et tension continue faible pour tVPDDetach

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La Figure 4-18 représente un diagramme d'états de connexion d'un ***dispositif USB alimenté par VCONN*** de charge.

Figure 4-18 Diagramme d'états de connexion: VPD de charge



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Anglais	Français
Disabled	Désactivé
Directed from any state	Induit depuis n'importe quel état
Corrosion Mitigation	Atténuation de la corrosion
tErrorRecovery and Directed	tErrorRecovery et induit
Host Port DRP Toggle*	Port hôte Alternance DRP*
DRP Toggle	Alternance DRP
Host Port Connection Removed or Charge-Through Port VBUS Removed	Connexion au port hôte supprimée ou VBUS du port de charge retirée
Host Port VBUS at vSafe0V and Host Port Slink Detected for tCCDebounce	VBUS du port hôte en état vSafe0V et port hôte destinataire détecté pour tCCDebounce
Host Port Connection Detected	Connexion au port hôte détectée
Host Port Connection Removed	Connexion au port hôte supprimée
tVPDDisable	tVPDDisable
Charge-Through Port Source Detected for tTryCCDebounce and Charge-Through Port VBUS Detected	Port de charge source détecté pour tTryCCDebounce et VBUS de port de charge détecté
Dead Battery	Batterie déchargée
DebugAcc Removed	DebugAcc retiré
Orientation Supported And Orientation Detected	Orientation prise en charge et détectée
Sink Removed	Destinataire retiré
VBUS at vSafe0V and Sink Detected for tCCDebounce	VBUS en état vSafe0V et destinataire détecté pour tCCDebounce
USB PD PR_Swap was accepted	USB PD PR_Swap accepté
VBUS Removed	VBUS retirée
Vconn Removed	VCONN retirée
Received PS_RDY from original Source or USB PD PR_Swap	PS_RDY reçu depuis la Source originale ou USB PD PR_Swap
DebugAcc Detected for tCCDebounce and VBUS Detected	DebugAcc détecté pour tCCDebounce et VBUS détectée
AudioAcc Removed	AudioAcc retiré
AudioAcc Detected for tCCDebounce	AudioAcc détecté pour tCCDebounce
DebugAcc Detected for tCCDebounce	DebugAcc détecté pour tCCDebounce
Connection Removed for tCCDebounce	Connexion supprimée pour tCCDebounce
Source Detected for tCCDebounce and VBUS detected	Source détectée pour tCCDebounce et VBUS détectée
Sink Detected for tTryCCDebounce	Destinataire détecté pour tTryCCDebounce
Source not Detected for tTryCCDebounce after tDRPTry	Source non détectée pour tCCDebounce après tDRPTry
Charge-Through Port Slink Detected	Destinataire du port de charge détecté
tDRPTry and Sink not Detected	tDRPTry et Destinataire non détectés
Sink Detected for tCCDebounce	Destinataire détecté pour tCCDebounce
Source Detected for tTryCCDebounce and VBUS detected	Source détectée pour tTryCCDebounce et VBUS détectée

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Anglais	Français
Only if a power source is detected and present on the charge-through port	Uniquement si une source d'alimentation est détectée et présente sur le port de charge

4.5.2.2 Exigences relatives aux diagrammes d'états de connexion

Le passage à un état de déconnexion "induit depuis n'importe quel état" ***ne doit pas*** être utilisé pour écraser une alternance ***tDRP***.

Une DRP ou un destinataire ***peuvent*** consommer l'alimentation par défaut de la VBUS dans n'importe quel état, lorsque la mise à disposition de la VBUS n'est pas exigée.

Les deux tableaux suivants définissent les états électriques d'une broche CC d'une source et d'un destinataire. Chaque port est équipé de broches CC1 et CC2; chaque broche dispose de son propre état de broche CC. La combinaison de l'état des broches CC1 et CC2 d'un port est utilisée pour définir les conditions de transition d'un port d'un état à un autre.

Tableau 4-16 États des broches CC d'un port source

État des broches CC	Terminaison CC du port partenaire	Tension détectée sur les broches CC lorsque le port affirme la Rp
SRC.Open	**Ouverte, Rp**	Supérieure à ***vOPEN***
SRC.Rd	**Rd**	Dans la plage ***vRd*** (à savoir entre la ***vRd*** minimale et la ***vRd*** maximale)
SRC.Ra	**Ra**	Inférieure à la ***vRa*** maximale

Tableau 4-17 États des broches CC d'un port destinataire

État des broches CC	Terminaison CC du port partenaire	Tension détectée sur les broches CC lorsque le port affirme la Rd
SNK.Rp	**Rp**	Supérieure à la ***vRd-Connect*** minimale
SNK.Open	**Ouverte, Ra, Rd**	Inférieure à la ***vRa*** maximale

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4.5.2.2.1 État Désactivé

Cet état est représenté à la Figure 4-12, à la Figure 4-13, à la Figure 4-14, à la Figure 4-15, à la Figure 4-16, à la Figure 4-17 et à la Figure 4-18.

L'état ***Disabled*** correspond aux situations où le port empêche la connexion en retirant toutes les terminaisons des broches CC.

Il convient que le port passe à l'état ***Disabled*** depuis n'importe quel autre état en cas de demande. Lorsque le port passe à l'état ***Disabled*** depuis l'état ***Attached.SNK***, aucune terminaison de câble ne ***doit*** être en contact avec les broches CC, pendant un délai d'au moins ***tErrorRecovery***.

Un port ***peut*** choisir de ne pas prendre en charge l'état ***Disabled***. Si l'état ***Disabled*** n'est pas pris en charge, le port ***doit*** être mis à l'état ***Unattached.SNK*** ou ***Unattached.SRC*** après mise sous tension.

4.5.2.2.1.1 Exigences relatives à l'état Désactivé

Le port ***ne doit pas*** piloter la VBUS ou la VCONN et ***doit*** présenter une impédance de mise à la masse élevée (supérieure à ***zOPEN***) sur ses broches CC1 et CC2.

4.5.2.2.1.2 Sortie de l'état Disabled

Un destinataire ***doit*** passer à l'état ***Unattached.SNK*** en cas de demande.

Une source ***doit*** passer à l'état ***Unattached.SRC*** en cas de demande.

Une DRP ***doit*** passer à l'état ***Unattached.SNK*** ou ***Unattached.SRC*** en cas de demande.

4.5.2.2.2 État ErrorRecovery

Cet état est représenté à la Figure 4-12, à la Figure 4-13, à la Figure 4-14, à la Figure 4-15, à la Figure 4-16, à la Figure 4-17 et à la Figure 4-18.

L'état ***ErrorRecovery*** désigne la situation où le port extrait ses terminaisons de câbles des broches CC1 et CC2 pendant le délai ***tErrorRecovery***, avant de passer à l'état ***Unattached.SNK*** ou ***Unattached.SRC*** approprié selon le type de port. Il s'agit de l'équivalent d'un débranchement forcé avec recherche d'un nouveau branchement. Le port peut alternativement passer de l'état ***ErrorRecovery*** à l'état ***CorrosionMitigation*** en cas de demande.

Les ports qui prennent en charge ***USB Power Delivery doivent*** prendre en charge l'état ***ErrorRecovery***.

Les ports qui prennent en charge l'état ***ErrorRecovery*** ***doivent*** passer à l'état ***ErrorRecovery*** depuis n'importe quel autre état en cas de demande.

Un port qui ne prend pas en charge ***USB Power Delivery peut*** choisir de ne pas prendre en charge l'état ***ErrorRecovery***. Si l'état ***ErrorRecovery*** n'est pas pris en charge, le port ***doit*** être mis à l'état ***Disabled*** si celui-ci est pris en charge. Si l'état ***Disabled*** n'est pas pris en charge, le port ***doit*** être mis à l'état ***Unattached.SNK*** ou ***Unattached.SRC***.

4.5.2.2.2.1 Exigences relatives à l'état ErrorRecovery

Le port ***ne doit pas*** piloter la VBUS ou la VCONN et ***doit*** présenter une impédance de mise à la masse élevée (supérieure à ***zOPEN***) sur ses broches CC1 et CC2.

4.5.2.2.2.2 Sortie de l'état ErrorRecovery

Un destinataire ***doit*** passer à l'état ***Unattached.SNK*** à l'issue du délai ***tErrorRecovery*** ou ***doit*** passer à l'état ***CorrosionMitigation*** à l'issue du délai ***tErrorRecovery*** en cas de demande.

Une source ***doit*** passer à l'état ***Unattached.SRC*** à l'issue du délai ***tErrorRecovery*** ou ***doit*** passer à l'état ***CorrosionMitigation*** à l'issue du délai ***tErrorRecovery*** en cas de demande.

Une DRP (Figure 4-15) et une DRP avec prise en charge de l'état ***Try.SNK*** et des modes accessoires (Figure 4-17) ***doivent*** passer à l'état ***Unattached.SNK*** à l'issue du délai ***tErrorRecovery*** ou ***doit*** passer à l'état ***CorrosionMitigation*** à l'issue du délai ***tErrorRecovery*** en cas de demande.

Une DRP avec prise en charge de l'état ***Try.SRC*** et des modes accessoires (Figure 4-16) ***doit*** passer à l'état ***Unattached.SRC*** à l'issue du délai ***tErrorRecovery*** ou ***doit*** passer à l'état ***CorrosionMitigation*** à l'issue du délai ***tErrorRecovery*** en cas de demande.

Un ***dispositif USB alimenté par VCONN*** de charge (Figure 4-18) ***doit*** passer à l'état ***Unattached.SNK*** à l'issue du délai ***tErrorRecovery*** ou ***doit*** passer à l'état ***CorrosionMitigation*** à l'issue du délai ***tErrorRecovery*** en cas de demande.

4.5.2.2.3 État Unattached.SNK

Cet état est représenté à la Figure 4-13, à la Figure 4-14, à la Figure 4-15, à la Figure 4-16, à la Figure 4-17 et à la Figure 4-18.

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À l'état ***Unattached.SNK***, le port attend de détecter la présence d'une source.

Un port dont la batterie est déchargée ***doit*** passer à cet état lorsqu'il est hors tension.

4.5.2.2.3.1 Exigences relatives à l'état Unattached.SNK

Le port ***ne doit pas*** piloter la VBUS ou VCONN.

Les deux broches CC1 et CC2 ***doivent*** être mises à la masse de manière indépendante par le biais de la ***Rd***.

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** isoler son port côté hôte de son port de charge, y compris les broches CC et VBUS, et mettre à la masse les broches CC1 et CC2 de son port de charge et la broche CC de son port côté hôte, de façon indépendante, par le biais de la ***Rd***.

4.5.2.2.3.2 Sortie de l'état Unattached.SNK

S'il prend en charge l'***USB PD*** ou les modes accessoires, le port ***doit*** passer à l'état ***AttachWait.SNK*** lorsque l'état ***SNK.Rp*** est présent sur au moins l'une de ses broches CC.

Les délais suivants sont les délais maximaux qu'un port ***doit*** attendre pour passer à l'état ***AttachWait.SNK***:

- ***tNoToggleConnect*** lorsqu'aucun des deux ports partenaires n'est alterné;
- ***tOnePortToggleConnect*** lorsqu'un seul port partenaire est alterné.

Lorsque les deux ports partenaires sont alternés, ***il convient*** qu'un port passe à l'état ***AttachWait.SNK*** avant la fin du délai ***tTwoPortToggleConnect***. Lorsque les deux ports partenaires sont des DRP, il n'est pas déterminé si le port local va passer à l'état ***AttachWait.SRC*** ou ***AttachWait.SNK***.

Note: Les délais ***tOnePortToggleConnect*** et ***tTwoPortToggleConnect*** sont liés aux délais de synchronisation et de détection d'une connexion dont les ports alternés ***peuvent*** avoir besoin.

Un destinataire ***USB 2.0*** exclusif qui ne prend pas en charge des accessoires, qui est autoalimenté ou exige uniquement une alimentation par défaut et qui ne prend pas en charge l'***USB PD***, ***peut*** directement passer à l'état ***Attached.SNK*** lorsque la VBUS est détectée.

Une DRP ***doit*** passer à l'état ***Unattached.SRC*** dans le délai ***tDRPTransition***, après basculement des deux broches CC à l'état ***SNK.Open*** pendant le délai ***tDRP*** – ***dcSRC.DRP*** · ***tDRP***, ou en cas de demande.

Un destinataire avec prise en charge des accessoires ***doit*** passer à l'état ***Unattached.Accessory*** dans le délai ***tDRPTransition***, après basculement des deux broches CC1 et CC2 à l'état ***SNK.Open*** pendant le délai ***tDRP*** – ***dcSRC.DRP*** · ***tDRP***, ou en cas de demande.

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***Unattached.SRC*** dans le délai ***tDRPTransition***, après basculement de la broche CC du port côté hôte à l'état ***SNK.Open*** pendant le délai ***tDRP*** – ***dcSRC.DRP*** · ***tDRP***, et lorsque les deux situations suivantes sont détectées sur le port de charge:

- l'état ***SNK.Rp*** est détecté sur exactement l'une des broches CC1 ou CC2 pendant au moins le délai ***tCCDebounce***;
- la VBUS est détectée.

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***Attached.SNK*** lorsqu'une connexion source est détectée, comme l'indique l'état ***SNK.Rp*** sur la broche CC de son port côté hôte.

4.5.2.2.4 État AttachWait.SNK

Cet état est représenté à la Figure 4-13, à la Figure 4-14, à la Figure 4-15, à la Figure 4-16, à la Figure 4-17 et à la Figure 4-18.

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À l'état ***AttachWait.SNK***, le port détecte l'état ***SNK.Rp*** sur au moins l'une de ses broches CC et attend la VBUS.

À l'état ***AttachWait.SNK***, le ***dispositif USB alimenté par VCONN*** de charge a détecté l'état ***SNK.Rp*** sur la broche CC de son port côté hôte et attend la VBUS côté hôte.

4.5.2.2.4.1 Exigences relatives à l'état AttachWait.SNK

Le port ***ne doit pas*** piloter la VBUS ou VCONN.

Les deux broches CC1 et CC2 ***doivent*** être mises à la masse de manière indépendante par le biais de la ***Rd***.

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** isoler son port côté hôte de son port de charge, y compris les broches CC et VBUS, et mettre à la masse les broches CC1 et CC2 de son port de charge et la broche CC de son port côté hôte, de façon indépendante, par le biais de la ***Rd***.

Il est vivement recommandé qu'un dispositif ***USB 3.2*** SuperSpeed suspende la détection de la VBUS sur le contrôleur du dispositif jusqu'à atteindre l'état ***Attached.SNK*** ou ***DebugAccessory.SNK*** (à savoir l'état d'au moins une broche CC est ***SNK.Rp***). Sinon, il ***peut*** se connecter en ***USB 2.0*** lorsqu'il est branché au DFP d'un hôte/hub existant.

4.5.2.2.4.2 Sortie de l'état AttachWait.SNK

Un destinataire ***doit*** passer à l'état ***Unattached.SNK*** lorsque l'état des deux broches CC1 et CC2 est ***SNK.Open*** pendant un délai d'au moins ***tPDDebounce***.

Une DRP ***doit*** passer à l'état ***Unattached.SRC*** lorsque l'état des deux broches CC1 et CC2 est ***SNK.Open*** pendant un délai d'au moins ***tPDDebounce***.

Le port ***doit*** passer à l'état ***Attached.SNK*** lorsque l'état d'une seule des broches CC1 ou CC2 est ***SNK.Rp*** pendant un délai d'au moins ***tCCDebounce*** et que la VBUS est détectée. Noter que la source ***peut*** initier une communication ***USB PD***, qui entraîne de courtes périodes à l'état ***SNK.Open*** sur l'une des broches CC, tandis que l'état de la seconde broche CC reste ***SNK.Open***; toutefois, cet événement ne dépasse pas le délai ***tPDDebounce***.

Lorsque le port est un ***accessoire alimenté par VCONN*** ou un ***dispositif USB alimenté par VCONN***, il ***doit*** passer à l'état ***Attached.SNK*** lorsque la VCONN ou la VBUS est détectée. Le port ***peut*** changer d'état sans attendre le délai ***tCCDebounce*** sur les broches CC.

Lorsqu'il prend en charge le ***mode accessoire de débogage***, le port ***doit*** passer à l'état ***DebugAccessory.SNK***, si l'état des broches CC1 et CC2 est ***SNK.Rp*** pendant un délai d'au moins ***tCCDebounce*** et que la VBUS est détectée. Noter que la source DAM ***peut*** initier une communication ***USB PD***, qui entraîne de courtes périodes à l'état ***SNK.Open*** sur l'une des broches CC, tandis que l'état de la seconde broche CC reste ***SNK.Rp***; toutefois, cet événement ne dépasse pas le délai ***tPDDebounce***.

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***Attached.SNK*** après basculement de la broche CC de port côté hôte à l'état ***SNK.Rp*** pendant un délai d'au moins ***tCCDebounce*** et lorsque la VCONN ou la VBUS a été détectée côté hôte.

Une DRP qui privilégie fortement le rôle de source ***peut***, ***de manière facultative***, passer à l'état ***Try.SRC*** plutôt qu'à l'état ***Attached.SNK***, lorsque l'état d'une broche CC a été ***SNK.Rp*** pendant un délai d'au moins ***tCCDebounce*** et que la VBUS est détectée.

4.5.2.2.5 État Attached.SNK

Cet état est représenté à la Figure 4-13, à la Figure 4-14, à la Figure 4-15, à la Figure 4-16, à la Figure 4-17 et à la Figure 4-18.

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À l'état ***Attached.SNK***, le port est branché et fonctionne comme un destinataire. Lorsque le port entre initialement dans cet état, il fonctionne également comme un UFP. Les rôles d'alimentation et de données peuvent être modifiés avec les commandes ***USB PD***.

Un port qui passe à cet état directement depuis l'état ***Unattached.SNK*** en raison de la détection de la VBUS ***ne doit pas*** déterminer l'orientation ou la disponibilité d'une alimentation USB supérieure à celle par défaut et ***ne doit pas*** utiliser l'***USB PD***.

4.5.2.2.5.1 Exigences relatives à l'état Attached.SNK

S'il est nécessaire que le port détermine l'orientation du connecteur, il ne ***doit*** le faire qu'au moment où il passe à cet état en détectant laquelle des broches CC1 ou CC2 est connectée par le câble (à savoir la broche CC dont l'état est ***SNK.Rp***).

S'il prend en charge la signalisation sur paires USB TX/RX, le port ***doit*** connecter les paires USB TX/RX de manière fonctionnelle et gérer la connexion pendant et après une ***USB PD PR_Swap***.

Si le port est passé à l'état ***Attached.SNK*** depuis l'état ***AttachWait.SNK*** ou ***TryWait.SNK***, une seule des broches CC1 ou CC2 se trouve à l'état ***SNK.Rp***. Le port ***doit*** continuer à mettre la broche CC à la masse par le biais de la ***Rd***.

Si le port est passé à l'état ***Attached.SNK*** depuis l'état ***Attached.SRC*** à l'issue d'une ***USB PD PR_Swap***, le port ***doit*** mettre à la masse la broche CC connectée par le biais de la ***Rd***.

Le port ***doit*** satisfaire aux exigences relatives au ***sous-état Sink Power*** spécifiées en 4.5.2.2.3.

Lorsque le port est un ***dispositif USB alimenté par VCONN***, il ***doit*** répondre aux requêtes d'identité du câble ***USB PD*** sur SOP'. Il ***ne doit pas*** envoyer de messages ni y répondre sur SOP'. Il ***doit*** assurer une capacité suffisante sur la broche CC afin de satisfaire aux exigences cReceiver définies dans l'***USB PD***.

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** isoler son port côté hôte de son port de charge, y compris les broches CC et VBUS, présenter une impédance de mise à la masse élevée (supérieure à ***zOPEN***) sur les broches CC1 et CC2 de son port de charge et mettre à la masse la broche CC de son port côté hôte par le biais de la ***Rd***.

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** démarrer un temporisateur de prise en charge de la charge lorsqu'il passe à l'état ***Attached.SNK***. Si un ***dispositif USB alimenté par VCONN*** de charge ne parvient pas à quitter l'état ***Attached.SNK*** avant que le temporisateur de prise en charge de la charge ne dépasse le délai ***tAMETimeout***, il ***doit*** présenter une interface ***USB Billboard Device Class*** qui indique qu'il ne prend pas en charge la charge.

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** réinitialiser le temporisateur de prise en charge de la charge lorsqu'il reçoit pour la première fois une commande de VDM structuré ***USB PD*** qu'il prend en charge. Si un ***dispositif USB alimenté par VCONN*** de charge reçoit une commande de VDM structuré plusieurs fois, il ne ***doit*** réinitialiser le temporisateur de prise en charge de la charge qu'une seule fois. Cela assure qu'un ***dispositif USB alimenté par VCONN*** de charge présente une interface ***USB Billboard Device Class*** s'il ne parvient pas à quitter l'état ***Attached.SNK*** tout en recevant des commandes de VDM structuré répétées ou continues (de ***découverte d'identité***, par exemple).

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** réinitialiser le temporisateur de prise en charge de la charge lorsqu'il reçoit un message de données qu'il prend en charge. Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** maintenir la réinitialisation du temporisateur de prise en charge de la charge lorsqu'il est en mode BIST ***USB PD***.

À l'exception d'un ***dispositif USB alimenté par VCONN*** ou d'un ***dispositif USB alimenté par VCONN*** de charge, le port ***peut*** négocier une ***USB PD PR_Swap***, ***DR_Swap*** ou ***VCONN_Swap***.

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Si le port prend en charge un ***dispositif USB alimenté par VCONN*** de charge et que la négociation d'un contrat ***USB PD*** explicite a échoué, le port ***doit*** interroger l'identité du câble par le biais de l'***USB PD*** sur SOP'.

Par défaut et en cas d'entrée depuis l'état ***AttachWait.SNK*** ou ***Unattached.SNK***, la VCONN ***ne doit pas*** être alimentée à l'état ***Attached.SNK***. En cas de passage à l'état ***Attached.SNK*** depuis l'état ***Attached.SRC*** par suite d'une ***USB PD PR_Swap***, il ***doit*** conserver l'état d'alimentation de la VCONN, si elle est sous tension ou hors tension, son rôle de données et ses connexions. Une ***USB PD DR_Swap*** n'a aucun effet sur l'identité du port qui alimente VCONN.

Le port ***peut*** négocier une ***USB PD VCONN_Swap.*** Lorsque le port qui n'alimente pas la VCONN exécute correctement une opération ***USB PD VCONN_Swap***, il ***doit*** commencer à alimenter la VCONN dans le délai ***tVCONNON***. Le port ***doit*** exécuter une commande ***VCONN_Swap*** dans une séquence de contact avec chevauchement afin de maintenir actifs les câbles USB Type-C vers USB Type-C alimentés. Lorsque le port qui alimentait VCONN exécute correctement une opération ***USB PD VCONN_Swap***, il ***doit*** arrêter d'alimenter VCONN dans le délai ***tVCONNOFF***.

4.5.2.2.5.2 Sortie de l'état Attached.SNK

Lorsqu'un port n'est pas un ***dispositif USB alimenté par VCONN*** et n'est pas concerné par une ***USB PD PR_Swap***, une ***USB PD*** Hard Reset ou une ***USB PD FR_Swap***, il ***doit*** passer à l'état ***Unattached.SNK*** dans le délai ***tSinkDisconnect*** lorsque la VBUS chute au-dessous de ***vSinkDisconnect*** pour une VBUS fonctionnant à 5 V au maximum ou à une valeur inférieure au ***vSinkDisconnectPD*** lorsque l'***USB PD*** a négocié un fonctionnement au-dessus de 5 V.

Un ***dispositif USB alimenté par VCONN*** ***doit*** revenir à l'état ***Unattached.SNK*** lorsque la VBUS a chuté au-dessous de ***vSinkDisconnect*** et que la VCONN a chuté au-dessous de ***vVCONNDisconnect***.

Un port qui est entré en communication ***USB PD*** avec la source et qui a enregistré une tension CC supérieure à ***vRd-USB*** ***peut*** surveiller la broche CC pour détecter une déconnexion de câble en plus de contrôler VBUS.

Un port qui surveille la tension CC à la recherche de déconnexion (mais qui n'est pas concerné par une ***USB PD PR_Swap*** ou une ***USB PD FR_Swap***) ***doit*** passer à l'état ***Unattached.SNK*** dans le délai ***tSinkDisconnect*** après maintien de la tension CC au-dessous de ***vRd-USB*** pendant le délai ***tPDDebounce***.

S'il alimente la VCONN, le port ***doit*** interrompre l'alimentation dans le délai ***tVCONNOFF*** à compter de la sortie de l'état ***Attached.SNK***.

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTUnattached.VPD*** si la VCONN est présente et que l'état de la broche CC de son port côté hôte est ***SNK.Open*** pendant le délai ***tVPDCTDD***.

Un port qui, par l'intermédiaire de SOP', a détecté un ***dispositif USB alimenté par VCONN*** de charge branché ***doit*** passer à l'état ***TryWait.SRC*** s'il est mis en œuvre ou à l'état ***Unattached.SRC*** ou ***Unattached.Accessory*** si ***TryWait.SRC*** n'est pas pris en charge. Ce basculement ***peut*** être retardé jusqu'à ce que le dispositif dispose de la charge de batterie nécessaire pour rester alimenté jusqu'à ce qu'il atteigne l'état ***CTAttached.SNK***.

Après avoir reçu un ***USB PD*** PS_RDY de la source originale pendant une ***USB PD PR_Swap***, le port ***doit*** directement passer à l'état ***Attached.SRC*** (à savoir retirer la ***Rd*** de la broche CC, affirmer la ***Rp*** sur la broche CC et alimenter la VBUS); toutefois, il ***doit*** conserver l'état d'alimentation de la VCONN, si elle est sous tension ou hors tension, son rôle de données et ses connexions.

4.5.2.2.6 État UnattachedWait.SRC

Cet état est représenté à la Figure 4-12.

À l'état ***UnattachedWait.SRC***, le port décharge la broche CC qui fournissait la VCONN dans le précédent état ***Attached.SRC***.

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4.5.2.2.6.1 Exigences relatives à l'état UnattachedWait.SRC

Le port ***ne doit pas*** activer la VBUS ou la VCONN.

Le port ***doit*** achever la mise hors tension de la VCONN initiée lors de la sortie du précédent état ***Attached.SRC***.

Le port ***doit*** continuer à fournir une terminaison ***Rp***, définie dans le Tableau 4-27, sur la broche CC non déchargée.

Le port ***ne doit pas*** fournir de terminaison ***Rp*** sur la broche CC déchargée.

Le port ***doit*** fournir une terminaison ***Rdch*** sur la broche CC déchargée.

Le port ***doit*** décharger la broche CC déchargée au-dessous de ***vVCONNDischarge***.

4.5.2.2.6.2 Sortie de l'état UnattachedWait.SRC

Le port ***doit*** passer à l'état ***Unattached.SRC*** lorsque la VCONN est au-dessous de ***vVCONNDischarge***. Le port ***peut*** retarder ce passage pour donner plus de temps à la fiche de câble pour réappliquer ***Ra***.

4.5.2.2.7 État Unattached.SRC

Cet état est représenté à la Figure 4-12, à la Figure 4-15, à la Figure 4-16, à la Figure 4-17 et à la Figure 4-18.

À l'état ***Unattached.SRC***, le port attend de détecter la présence d'un destinataire ou d'un accessoire.

À l'état ***Unattached.SRC***, le ***dispositif USB alimenté par VCONN*** de charge a détecté une source sur son port de charge et surveille de manière indépendante son port côté hôte pour détecter la présence d'un destinataire.

4.5.2.2.7.1 Exigences relatives à l'état Unattached.SRC

Le port ***ne doit pas*** piloter la VBUS ou VCONN.

Le port ***doit*** fournir le courant des broches CC1 et CC2 de manière indépendante.

Le port ***doit*** fournir une terminaison ***Rp*** distincte sur les broches CC1 et CC2, conformément au Tableau 4-27.
Note: Une source équipée d'un câble captif ou d'une simple fiche présente une terminaison ***Rp*** unique sur sa broche CC (A5).

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** isoler son port côté hôte de son port de charge, y compris les broches CC et VBUS. Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** assurer qu'il est alimenté par VBUS à partir du port de charge.

Dès l'entrée dans cet état, le ***dispositif USB alimenté par VCONN*** de charge ***doit*** retirer la terminaison ***Rd*** à la masse de la broche CC du port côté hôte. Il ***doit*** fournir une terminaison ***Rp*** au lieu d'annoncer la puissance USB par défaut, conformément au Tableau 4-27. Il ***doit*** aussi continuer à mettre à la masse les broches CC1 et CC2 de son port de charge de façon indépendante par le biais de la ***Rd***.

4.5.2.2.7.2 Sortie de l'état Unattached.SRC

Le port ***doit*** passer à l'état ***AttachWait.SRC*** lorsque:

- l'état ***SRC.Rd*** est présent sur la broche CC1 ou CC2; ou
- l'état ***SRC.Ra*** est présent sur les deux broches CC1 et CC2.

Les délais suivants sont les délais maximaux pendant lesquels un port ***doit*** attendre avant de passer à l'état ***AttachWait.SRC***:

- ***tNoToggleConnect*** lorsqu'aucun des deux ports partenaires n'est alterné;

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- ***tOnePortToggleConnect*** lorsqu'un seul port partenaire est alterné.

Lorsque les deux ports partenaires sont alternés, ***il convient*** qu'un port passe à l'état ***AttachWait.SRC*** dans le délai ***tTwoPortToggleConnect***. Lorsque les deux ports partenaires sont des DRP, il n'est pas déterminé si le port local va passer à l'état ***AttachWait.SRC*** ou ***AttachWait.SNK***.

Note: Les délais ***tOnePortToggleConnect*** et ***tTwoPortToggleConnect*** sont liés aux délais de synchronisation et de détection d'une connexion dont les ports alternés ***peuvent*** avoir besoin.

Note: Un câble sans dispositif branché peut être détecté lorsque l'état ***SRC.Ra*** est détecté sur l'une des broches CC1 ou CC2, et que l'état de l'autre broche CC est ***SRC.Open***. Dans ce cas, toutefois, le port ***ne doit pas*** passer à l'état ***AttachWait.SRC***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***AttachWait.SRC*** lorsque la VBUS côté hôte est ***vSafe0V*** et que l'état ***SRC.Rd*** est détecté sur la broche CC du port côté hôte.

Une DRP ***doit*** passer à l'état ***Unattached.SNK*** dans le délai ***tDRPTransition***, à l'issue du délai ***dcSRC.DRP*** · ***tDRP*** ou en cas de demande.

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***Unattached.SNK*** dans le délai ***tDRPTransition***, à l'issue du délai ***dcSRC.DRP*** · ***tDRP*** ou si la broche VBUS de charge est retirée.

4.5.2.2.8 État AttachWait.SRC

Cet état est représenté à la Figure 4-12, à la Figure 4-15, à la Figure 4-16, à la Figure 4-17 et à la Figure 4-18.

L'état ***AttachWait.SRC*** est utilisé pour assurer que l'état des deux broches CC1 et CC2 est stable après la connexion d'un destinataire.

À l'état ***AttachWait.SRC***, le ***dispositif USB alimenté par VCONN*** de charge assure que l'état de la broche CC du port côté hôte est stable après la connexion d'un destinataire.

4.5.2.2.8.1 Exigences relatives à l'état AttachWait.SRC

Le port ***ne doit pas*** piloter la VBUS ou VCONN.

Le port ***doit*** appliquer une charge à la VBUS pour s'assurer qu'il atteindra ***vSafe0V*** dans le délai ***tVsafe0V***. (Note: Une charge résiduelle jusqu'à ***vSafe5V*** peut demeurer dans les condensateurs du port destinataire connecté, qui empêche le port source de passer à l'état ***Attached.SRC***.)

Le port ***doit*** fournir le courant des broches CC1 et CC2 de manière indépendante.

Le port ***doit*** fournir une terminaison ***Rp*** distincte sur les broches CC1 et CC2, conformément au Tableau 4-27. Note: Une source équipée d'un câble captif ou d'une simple fiche présente une terminaison ***Rp*** unique sur sa broche CC (A5).

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** isoler son port côté hôte de son port de charge, y compris les broches CC et VBUS. Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** assurer qu'il est alimenté par VBUS à partir du port de charge.

Dès l'entrée dans cet état, le ***dispositif USB alimenté par VCONN*** de charge ***doit*** retirer la terminaison ***Rd*** à la masse de la broche CC du port côté hôte. Il ***doit*** fournir une terminaison ***Rp*** au lieu d'annoncer la puissance USB par défaut, conformément au Tableau 4-27. Il ***doit*** aussi continuer à mettre à la masse les broches CC1 et CC2 de son port de charge de façon indépendante par le biais de la ***Rd***.

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4.5.2.2.8.2 Sortie de l'état AttachWait.SRC

Le port ***doit*** passer à l'état ***Attached.SRC*** lorsque la VBUS est ***vSafe0V*** et que l'état ***SRC.Rd*** est détecté sur exactement l'une des broches CC1 ou CC2 pendant un délai d'au moins ***tCCDebounce***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***Try.SNK*** lorsque la VBUS côté hôte est ***vSafe0V*** et que l'état ***SRC.Rd*** est détecté sur la broche CC du port côté hôte pendant un délai d'au moins ***tCCDebounce***.

Si le port prend en charge le ***mode accessoire de débogage***, il ***doit*** passer à l'état ***UnorientedDebugAccessory.SRC*** lorsque la VBUS est ***vSafe0V*** et que l'état ***SRC.Rd*** est détecté sur les deux broches CC1 et CC2 pendant un délai d'au moins ***tCCDebounce***.

Une source ***doit*** passer à l'état ***Unattached.SRC*** et une DRP à l'état ***Unattached.SNK*** lorsque l'état ***SRC.Open*** est détecté sur les deux broches CC1 et CC2. La source ***doit*** détecter l'état ***SRC.Open*** dans le délai ***tSRCDisconnect***; toutefois, il ***convient*** que la détection soit la plus rapide possible.

Une source ***doit*** passer à l'état ***Unattached.SRC*** et une DRP à l'état ***Unattached.SNK*** lorsque l'état ***SRC.Open*** est détecté sur l'une des broches CC1 ou CC2 et que l'état de l'autre broche CC est ***SRC.Ra***. La source ***doit*** détecter l'état ***SRC.Open*** dans le délai ***tSRCDisconnect***; toutefois, il ***convient*** que la détection soit la plus rapide possible.

Le port ***peut*** sortir de l'état ***ErrorRecovery*** ou ***Disabled*** si la tension de la VBUS n'a pas atteint ***vSafe0V*** dans le délai (maximal) ***tVBUSOFF*** après le passage à l'état ***AttachWait.SRC***.

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***Unattached.SNK*** lorsque l'état ***SRC.Open*** est détecté sur la broche CC du port côté hôte ou si la VBUS de charge chute au-dessous de ***vSinkDisconnect***. Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** détecter l'état ***SRC.Open*** dans le délai ***tSRCDisconnect***; toutefois, il ***convient*** que la détection soit la plus rapide possible.

Une DRP qui privilégie fortement le rôle de destinataire ***peut***, ***de manière facultative***, passer à l'état ***Try.SNK*** plutôt qu'à l'état ***Attached.SRC*** lorsque la VBUS est ***vSafe0V*** et que l'état ***SRC.Rd*** est détecté sur exactement l'une des broches CC1 ou CC2 pendant un délai d'au moins ***tCCDebounce***.

4.5.2.2.9 État Attached.SRC

Cet état est représenté à la Figure 4-12, à la Figure 4-15, à la Figure 4-16, à la Figure 4-17 et à la Figure 4-18.

À l'état ***Attached.SRC***, le port est branché et fonctionne comme une source. Lorsque le port entre initialement dans cet état, il fonctionne également comme un DFP. Puis, les rôles d'alimentation et de données initiaux peuvent être modifiés à l'aide des commandes ***USB PD***.

À l'état ***Attached.SRC***, le ***dispositif USB alimenté par VCONN*** de charge a détecté un destinataire sur son port côté hôte et a connecté la broche VBUS du port de charge à la broche VBUS du port côté hôte.

4.5.2.2.9.1 Exigences relatives à l'état Attached.SRC

S'il est nécessaire que le port détermine l'orientation du connecteur, il ***doit*** uniquement le faire lorsqu'il passe à l'état ***Attached.SRC*** en détectant laquelle des broches CC1 ou CC2 est connectée par le câble (à savoir la broche CC dont l'état est ***SRC.Rd***).

Si le port est passé à cet état depuis l'état ***AttachWait.SRC*** ou l'état ***Try.SRC***, une seule des broches CC1 ou CC2 se trouve à l'état ***SRC.Rd***. Le port ***doit*** fournir le courant de cette broche CC et surveiller son état.

Si le port est passé à cet état depuis l'état ***Attached.SNK*** à l'issue d'une ***USB PD PR_Swap***, le port ***doit*** fournir le courant de la broche CC connectée et surveiller son état.

Le port ***doit*** fournir une ***Rp*** définie dans le Tableau 4-27.

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Le port ***doit*** alimenter VBUS en courant au niveau annoncé sur la ***Rp***.

Le port ***doit*** alimenter la VBUS dans le délai ***tVBUSON*** à compter de l'entrée dans cet état et tant qu'il fonctionne comme une source d'alimentation.

Le port ***ne doit pas*** initier de communication ***USB PD*** jusqu'à ce que la VBUS atteigne ***vSafe5V***.

S'il prend en charge la signalisation sur paires RX SuperSpeed, le port ***doit***:

- connecter les paires USB TX/RX de manière fonctionnelle;
- pour la VCONN, exécuter l'une des actions suivantes:
    - alimenter la VCONN de manière inconditionnelle sur la broche CC qui ne se trouve pas à l'état ***SRC.Rd***; ou
    - alimenter la VCONN sur la broche CC qui se trouve à l'état ***SRC.Ra***.

Un port qui ne prend pas en charge la signalisation sur paires USB TX/RX ***peut*** alimenter la VCONN comme cela est décrit ci-dessus.

Le port ***peut*** négocier une ***USB PD PR_Swap***, ***DR_Swap*** ou ***VCONN_Swap***.

Si le port alimente la VCONN, il ***doit*** le faire dans le délai ***tVCONNON***.

Le port ***peut*** interroger l'identité du câble par l'***USB PD*** sur SOP'. S'il détecte que celui-ci est connecté à un ***dispositif USB alimenté par VCONN***, le port ***peut*** retirer la VBUS et la décharger à ***vSafe0V*** tout en continuant dans cet état avec la VCONN appliquée. Le port ***peut*** également initier d'autres communications SOP'.

Le port ***ne doit pas*** alimenter la VCONN si elle est entrée dans cet état du fait d'une ***USB PD PR_Swap*** et qu'il n'alimentait par la VCONN auparavant. Une ***USB PD DR_Swap*** n'a aucun effet sur l'identité du port qui alimente VCONN.

Le port ***peut*** négocier une ***USB PD VCONN_Swap***. Lorsque le port qui alimentait VCONN exécute correctement une opération ***USB PD VCONN_Swap***, il ***doit*** arrêter d'alimenter VCONN dans le délai ***tVCONNOFF***. Le port ***doit*** exécuter une commande ***VCONN_Swap*** dans une séquence de contact avec chevauchement afin de maintenir actifs les câbles USB Type-C vers USB Type-C alimentés. Lorsque le port qui n'alimentait pas la VCONN exécute correctement une opération ***USB PD VCONN_Swap***, il ***doit*** commencer à alimenter la VCONN dans le délai ***tVCONNON***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** continuer à isoler la broche CC de son port côté hôte des broches CC de son port de charge.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** maintenir la terminaison ***Rp*** qui annonce la puissance USB par défaut sur la broche CC du port côté hôte. Il ***doit*** aussi continuer à mettre à la masse les broches CC1 et CC2 de son port de charge de façon indépendante par le biais de la ***Rd***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** immédiatement connecter la broche VBUS du port de charge à la broche VBUS du port côté hôte.

Le ***dispositif USB alimenté par VCONN*** de charge **doit** assurer qu'il est entièrement alimenté par VBUS.

Le ***dispositif USB alimenté par VCONN*** de charge doit uniquement répondre aux requêtes de **découverte d'identité USB PD** sur SOP' sur son port côté hôte et terminer toutes les requêtes actives avant de quitter cet état. Il ***doit*** assurer une capacité suffisante sur la broche CC du port côté hôte afin de satisfaire aux exigences cReceiver définies dans l'***USB PD***.

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4.5.2.2.9.2 Sortie de l'état Attached.SRC

Une source qui alimente la VCONN ou qui a confié la responsabilité d'alimentation de la VCONN au destinataire par le biais de la messagerie ***USB PD VCONN_Swap doit*** passer à l'état ***UnattachedWait.SRC*** lorsque l'état ***SRC.Open*** est détecté sur la broche CC surveillée. La source ***doit*** détecter l'état ***SRC.Open*** dans le délai ***tSRCDisconnect***; toutefois, il ***convient*** que la détection soit la plus rapide possible.

Une source qui n'alimente pas la VCONN ou qui n'a pas confié la responsabilité de la VCONN au destinataire par le biais de la messagerie ***USB PD VCONN_Swap doit*** passer à l'état ***Unattached.SRC*** lorsque l'état ***SRC.Open*** est détecté sur la broche CC surveillée. La source ***doit*** détecter l'état ***SRC.Open*** dans le délai ***tSRCDisconnect***; toutefois, il ***convient*** que la détection soit la plus rapide possible.

Lorsque l'état ***SRC.Open*** est détecté sur la broche CC surveillée, une DRP ***doit*** passer à l'état ***Unattached.SNK***, sauf si elle privilégie fortement le rôle de source. Dans ce cas, elle ***doit*** passer à l'état ***TryWait.SNK***. Cette transition vers l'état ***TryWait.SNK*** est nécessaire pour que deux dispositifs privilégiant le rôle de source ne bouclent pas indéfiniment entre la source et le destinataire. En d'autres termes, une DRP qui passe à l'état ***Try.SRC*** depuis l'état ***AttachWait.SNK*** ***doit*** passer à l'état ***TryWait.SNK*** pour le débranchement d'un destinataire de l'état ***Attached.SRC***.

Une DRP qui prend en charge un ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTUnattached.SNK*** si le dispositif connecté s'identifie comme un ***dispositif USB alimenté par VCONN*** de charge dans sa réponse à la commande de ***découverte d'identité***. La DRP ***peut*** retarder ce basculement pour effectuer d'autres communications SOP'.

Le port ***doit*** interrompre l'alimentation de la VBUS dans le délai ***tVBUSOFF*** à compter de la sortie de l'état ***Attached.SRC***.

S'il alimente la VCONN, le port ***doit*** interrompre l'alimentation dans le délai ***tVCONNOFF*** à compter de la sortie de l'état ***Attached.SRC***, sauf s'il existe du fait d'une ***USB PD PR_Swap*** ou qu'il passe à l'état ***CTUnattached.SNK***.

Après acceptation d'une ***USB PD PR_Swap*** (à savoir par réception ou confirmation d'un message d'***acceptation***), une DRP ***doit*** directement passer à l'état ***Attached.SNK*** (c'est-à-dire retirer la ***Rp*** de la broche CC, affirmer la ***Rd*** sur la broche CC et interrompre l'alimentation de la VBUS) et conserver son rôle de données, l'état de connexion et l'état d'alimentation de la VCONN.

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***Unattached.SNK*** lorsque la VBUS chute au-dessous de ***vSinkDisconnect*** ou que l'état de la broche CC du port côté hôte est ***SRC.Open***. Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** détecter l'état ***SRC.Open*** dans le délai ***tSRCDisconnect***; toutefois, il ***convient*** que la détection soit la plus rapide possible.

4.5.2.2.10 État Try.SRC

Cet état est représenté à la Figure 4-16.

À l'état ***Try.SRC***, le port détermine (par interrogation) si le port partenaire prend en charge le rôle de destinataire.

Note: Si les mécanismes ***Try.SRC*** et ***Try.SNK*** sont mis en œuvre, le port ne ***doit*** activer que l'un d'entre eux, et ce à tout moment. Le choix du mécanisme à activer est propre à la conception du produit.

4.5.2.2.10.1 Exigences relatives à l'état Try.SRC

Le port ***ne doit pas*** piloter la VBUS ou VCONN.

Le port ***doit*** fournir le courant des broches CC1 et CC2 de manière indépendante.

Le port ***doit*** fournir une ***Rp*** définie dans le Tableau 4-27.

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4.5.2.2.10.2 Sortie de l'état Try.SRC

Le port ***doit*** passer à l'état ***Attached.SRC*** lorsque l'état ***SRC.Rd*** est détecté sur exactement l'une des broches CC1 ou CC2 pendant un délai d'au moins ***tTryCCDebounce***.

Le port ***doit*** passer à l'état ***TryWait.SNK*** à l'issue du délai ***tDRPTry***, lorsque l'état ***SRC.Rd*** n'a pas été détecté et que la VBUS est dans ***vSafe0V***, ou à l'issue du délai ***tTryTimeout*** lorsque l'état ***SRC.Rd*** n'a pas été détecté.

4.5.2.2.11 État TryWait.SNK

Cet état est représenté à la Figure 4-16.

À l'état ***TryWait.SNK***, le port n'a pas réussi à devenir une source et attend de se brancher comme un destinataire. À défaut, le port répond au retrait du destinataire à l'état ***Attached.SRC***.

4.5.2.2.11.1 Exigences relatives à l'état TryWait.SNK

Le port ***ne doit pas*** piloter la VBUS ou VCONN.

Les deux broches CC1 et CC2 ***doivent*** être mises à la masse de manière indépendante par le biais de la ***Rd***.

4.5.2.2.11.2 Sortie de l'état TryWait.SNK

Le port ***doit*** passer à l'état ***Attached.SNK*** à l'issue du délai ***tCCDebounce*** si ou lorsque la VBUS est détectée. Noter que la source ***peut*** initier une communication ***USB PD***, qui entraîne de courtes périodes à l'état ***SNK.Open*** sur les deux broches CC1 et CC2; toutefois, cet événement ne dépasse pas le délai ***tPDDebounce***.

Le port ***doit*** passer à l'état ***Unattached.SNK*** lorsque l'état des deux broches CC1 et CC2 est ***SNK.Open*** pendant un délai d'au moins ***tPDDebounce***.

4.5.2.2.12 État Try.SNK

Cet état est représenté à la Figure 4-14, à la Figure 4-17 et à la Figure 4-18.

À l'état ***Try.SNK***, le port détermine (par interrogation) si le port partenaire prend en charge le rôle de source.

À l'état ***Try.SNK***, le ***dispositif USB alimenté par VCONN*** de charge effectue une requête pour déterminer si le port partenaire sur le port côté hôte prend en charge le rôle de source.

Note: Si les mécanismes ***Try.SRC*** et ***Try.SNK*** sont mis en œuvre, le port ne ***doit*** activer que l'un d'entre eux, et ce à tout moment. Le choix du mécanisme à activer est propre à la conception du produit.

4.5.2.2.12.1 Exigences relatives à l'état Try.SNK

Le port ***ne doit pas*** piloter la VBUS ou VCONN.

Les deux broches CC1 et CC2 ***doivent*** être mises à la masse de manière indépendante par le biais de la ***Rd***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** isoler son port côté hôte de son port de charge, y compris les broches CC et VBUS. Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** assurer qu'il est alimenté par VBUS à partir du port de charge.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** retirer la terminaison ***Rp*** (annonce de la puissance USB par défaut) de la broche CC du port côté hôte. Il ***doit*** à la place fournir une terminaison ***Rd*** à la masse définie dans le Tableau 4-27. Il ***doit*** aussi continuer à mettre à la masse les broches CC1 et CC2 de son port de charge de façon indépendante par le biais de la ***Rd***.

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4.5.2.2.12.2 Sortie de l'état Try.SNK

Le port ***doit*** attendre le délai ***tDRPTry*** et, seulement après, commencer à surveiller l'affectation de l'état ***SNK.Rp*** aux broches CC1 et CC2.

Le port ***doit*** ensuite passer à l'état ***Attached.SNK*** lorsque l'état ***SNK.Rp*** est détecté sur exactement l'une des broches CC1 ou CC2 pendant un délai d'au moins ***tTryCCDebounce*** et que la VBUS est détectée.

À défaut, le port ***doit*** passer à l'état ***TryWait.SRC*** si l'état ***SNK.Rp*** n'est pas détecté pendant le délai ***tTryCCDebounce***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** attendre le délai ***tDRPTry*** et, seulement après, commencer à surveiller l'affectation de l'état ***SNK.Rp*** à la broche CC du port côté hôte.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** ensuite passer à l'état ***Attached.SNK*** lorsque l'état ***SNK.Rp*** est détecté sur la broche CC du port côté hôte pendant un délai d'au moins ***tTryCCDebounce***, et que la VBUS ou la VCONN est détectée sur le port côté hôte.

À défaut, le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***TryWait.SRC*** si l'état ***SNK.Rp*** côté hôte n'est pas détecté pendant le délai ***tTryCCDebounce***.

Un destinataire avec prise en charge des accessoires ***doit*** passer à l'état ***Unsupported.Accessory*** si l'état ***SNK.Rp*** n'est pas détecté pendant le délai ***tDRPTryWait***.

Note: La source ***peut*** initier une communication ***USB PD***, qui entraîne de courtes périodes à l'état ***SNK.Open*** sur les deux broches CC1 et CC2; toutefois, cet événement ne dépasse pas le délai ***tTryCCDebounce***.

4.5.2.2.13 État TryWait.SRC

Cet état est représenté à la Figure 4-17 et à la Figure 4-18.

À l'état ***TryWait.SRC***, le port n'a pas réussi à devenir un destinataire et attend de se brancher comme une source.

À l'état ***TryWait.SRC***, le ***dispositif USB alimenté par VCONN*** de charge n'a pas réussi à devenir un destinataire sur son port côté hôte et attend de se brancher comme une source sur ce même port.

4.5.2.2.13.1 Exigences relatives à l'état TryWait.SRC

Les exigences relatives à cet état sont identiques à celles de l'état ***Unattached.SRC***.

4.5.2.2.13.2 Sortie de l'état TryWait.SRC

Le port ***doit*** passer à l'état ***Attached.SRC*** lorsque la VBUS est ***vSafe0V*** et que l'état ***SRC.Rd*** est détecté sur exactement l'une des broches CC pendant un délai d'au moins ***tTryCCDebounce***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***Attached.SRC*** lorsque la VBUS côté hôte est ***vSafe0V*** et que l'état ***SRC.Rd*** est détecté sur la broche CC du port côté hôte pendant un délai d'au moins ***tTryCCDebounce***.

Le port ***doit*** passer à l'état ***Unattached.SNK*** à l'issue du délai ***tDRPTry*** si aucune des broches CC1 et CC2 ne se trouve à l'état ***SRC.Rd***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***Unattached.SNK*** à l'issue du délai ***tDRPTry*** si la broche CC du port côté hôte n'est pas à l'état ***SRC.Rd***.

4.5.2.2.14 État Unattached.Accessory

Cet état est représenté à la Figure 4-14.

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L'état ***Unattached.Accessory*** permet qu'un destinataire avec prise en charge des modes accessoires se connecte à des ***accessoires alimentés par VCONN***.

Cet état est l'équivalent fonctionnel de l'état ***Unattached.SRC*** dans une DRP, sauf que l'état ***Attached.SRC*** n'est pas pris en charge.

4.5.2.2.14.1 Exigences relatives à l'état Unattached.Accessory

Le port ***ne doit pas*** piloter la VBUS ou VCONN.

Le port ***doit*** fournir le courant des broches CC1 et CC2 de manière indépendante.

Le port ***doit*** fournir une ***Rp*** définie dans le Tableau 4-27.

4.5.2.2.14.2 Sortie de l'état Unattached.Accessory

Un port prenant en charge les ***accessoires alimentés par VCONN*** ***doit*** également passer à l'état ***AttachWait.Accessory*** lorsque l'état de l'une des broches CC1 ou CC2 est ***SRC.Ra*** et que l'état de l'autre broche CC est ***SRC.Rd***.

Le délai maximal pendant lequel le port local ***doit*** attendre pour passer de l'état ***Unattached.Accessory*** à l'état ***AttachWait.Accessory*** lorsqu'un ***accessoire alimenté par VCONN*** est présent est ***tOnePortToggleConnect***.

À défaut, le port ***doit*** passer à l'état ***Unattached.SNK*** dans le délai ***tDRPTransition***, à l'issue du délai ***dcSRC.DRP*** · ***tDRP*** ou en cas de demande.

4.5.2.2.15 État AttachWait.Accessory

Cet état est représenté à la Figure 4-14.

L'état ***AttachWait.Accessory*** est utilisé pour assurer que l'état des deux broches CC1 et CC2 est stable après le branchement d'un câble.

4.5.2.2.15.1 Exigences relatives à l'état AttachWait.Accessory

Les exigences relatives à cet état sont identiques à celles de l'état ***Unattached.Accessory***.

4.5.2.2.15.2 Sortie de l'état AttachWait.Accessory

Le port ***doit*** passer à l'état ***Unattached.SNK*** lorsque l'état de l'une des broches CC1 ou CC2 est ***SRC.Open*** pendant un délai d'au moins ***tCCDebounce***.

Si le port prend en charge les ***accessoires alimentés par VCONN***, il ***doit*** également passer à l'état ***PoweredAccessory*** lorsque l'état de l'une des broches CC1 ou CC2 est ***SRC.Rd*** et que l'autre broche CC est simultanément à l'état ***SRC.Ra*** pendant un délai d'au moins ***tCCDebounce***.

4.5.2.2.16 État CorrosionMitigation

Cet état est représenté à la Figure 4-12, à la Figure 4-14, à la Figure 4-16, à la Figure 4-17 et à la Figure 4-18.

L'état ***CorrosionMitigation*** est utilisé avec le ***mode inhibition de corrosion liquide*** défini dans l'Annexe A.

4.5.2.2.16.1 Exigences relatives à l'état CorrosionMitigation

Le port ***doit*** reconfigurer ses broches comme cela est décrit à l'Annexe A.

Le port ***ne doit pas*** piloter la VBUS ou VCONN.

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Le port ***doit*** effectuer l'une des mises en œuvre suivantes:

1. Le port ***doit*** réguler la tension à la baisse, avec une résistance sur les broches CC1 et CC2 qui est inférieure ou égale à l'impédance maximale de la ***Ra***, comme cela est spécifiée dans le Tableau 4-29. **Il convient que** le port régule la tension à la baisse avec une résistance supérieure à la ***Ra***.
2. Le port ***doit*** réguler la tension à la baisse avec une résistance sur une seule des broches CC1 ou CC2, l'autre broche étant ouverte (présentant une impédance à la masse supérieure à ***zOPEN***). Dans cette mise en œuvre de simple régulation de tension, le destinataire ***doit*** surveiller la tension sur la broche CC ouverte et ***doit*** permuter la résistance et s'ouvrir d'une broche CC à l'autre lorsque l'état ***SNK.Rp*** est détecté.

4.5.2.2.16.2 Sortie de l'état CorrosionMitigation

Le port doit passer à l'état ***ErrorRecovery*** en cas de demande.

4.5.2.2.17 État UnorientedDebugAccessory.SRC

Cet état est représenté à la Figure 4-12, à la Figure 4-16 et à la Figure 4-17.

L'état ***UnorientedDebugAccessory.SRC*** est utilisé avec le ***mode accessoire de débogage*** défini dans l'Annexe B.

4.5.2.2.17.1 Exigences relatives à l'état UnorientedDebugAccessory.SRC

Ce mode sert uniquement à des fins de débogage et ***ne doit pas*** être utilisé pour communiquer avec des produits commerciaux.

Le port ***doit*** fournir une ***Rp*** définie dans le Tableau 4-27 sur les broches CC1 et CC2, et les surveiller en vue de détecter lorsque l'état de l'une des deux broches est ***SRC.Open***.

Le port ***doit*** alimenter VBUS en courant au niveau annoncé sur la ***Rp***. Le port ne ***doit pas*** piloter la VCONN.

Le port ***peut*** connecter les signaux de débogage non spécifiques de l'orientation pour un fonctionnement en ***mode accessoire de débogage*** uniquement après être passé à cet état.

4.5.2.2.17.2 Sortie de l'état UnorientedDebugAccessory.SRC

Si le port est une source, il ***doit*** passer à l'état ***Unattached.SRC*** lorsque l'état ***SRC.Open*** est détecté sur l'une des broches CC1 ou CC2.

Si le port est une DRP, il doit passer à l'état ***Unattached.SNK*** lorsque l'état ***SRC.Open*** est détecté sur l'une des broches CC1 ou CC2.

Le port ***doit*** passer à l'état ***OrientedDebugAccessory.SRC*** si l'orientation est exigée et détectée comme cela est décrit en B.2.6.1.2.

4.5.2.2.18 État OrientedDebugAccessory.SRC

Cet état est représenté à la Figure 4-12, à la Figure 4-16 et à la Figure 4-17.

L'état ***OrientedDebugAccessory.SRC*** est utilisé avec le ***mode accessoire de débogage*** défini dans l'Annexe B.

4.5.2.2.18.1 Exigences relatives à l'état OrientedDebugAccessory.SRC

Ce mode sert uniquement à des fins de débogage et ***ne doit pas*** être utilisé pour communiquer avec des produits commerciaux.

Le port ***doit*** fournir une ***Rp*** définie dans le Tableau 4-27 sur les broches CC1 et CC2, et les surveiller en vue de détecter lorsque l'état de l'une des deux broches est ***SRC.Open***.

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Le port ***doit*** alimenter VBUS en courant au niveau annoncé sur la ***Rp***. Le port ne ***doit pas*** piloter la VCONN.

Le port ***doit*** connecter les signaux de débogage spécifiques de l'orientation pour un fonctionnement en ***mode accessoire de débogage*** uniquement après être passé à cet état. Tout signal de débogage non spécifique de l'orientation pour un fonctionnement en ***mode accessoire de débogage*** ***doit*** être ou rester connecté à cet état.

S'il est nécessaire que le port établisse une communication ***USB PD***, il ***doit*** uniquement le faire après être passé à cet état. Le port ***ne doit pas*** initier de communication ***USB PD*** jusqu'à ce que la VBUS atteigne ***vSafe5V***. Dans cet état, le port assume le rôle ***USB PD*** initial du DFP/de la source.

4.5.2.2.18.2 Sortie de l'état OrientedDebugAccessory.SRC

Si le port est une source, il ***doit*** passer à l'état ***Unattached.SRC*** lorsque l'état ***SRC.Open*** est détecté sur l'une des broches CC1 ou CC2.

Si le port est une DRP, il doit passer à l'état ***Unattached.SNK*** lorsque l'état ***SRC.Open*** est détecté sur l'une des broches CC1 ou CC2.

4.5.2.2.19 État DebugAccessory.SNK

Cet état est représenté à la Figure 4-13, à la Figure 4-14, à la Figure 4-16 et à la Figure 4-17.

L'état ***DebugAccessory.SNK*** est utilisé avec le ***mode accessoire de débogage*** défini dans l'Annexe B.

4.5.2.2.19.1 Exigences relatives à l'état DebugAccessory.SNK

Ce mode sert uniquement à des fins de débogage et ***ne doit pas*** être utilisé pour communiquer avec des produits commerciaux.

Le port ***ne doit pas*** piloter la VBUS ou VCONN.

Le port ***doit*** fournir une ***Rd***, comme cela est spécifié dans le Tableau 4-28, sur les broches CC1 et CC2.

Lorsqu'elle est prise en charge, l'orientation est déterminée conformément à B.2.6.1.1. Le port ***doit*** connecter les signaux de débogage pour un fonctionnement en ***mode accessoire de débogage*** uniquement après être passé à cet état.

4.5.2.2.19.2 Sortie de l'état DebugAccessory.SNK State

Le port ***doit*** passer à l'état ***Unattached.SNK*** lorsque la VBUS n'est plus présente.

4.5.2.2.20 État PoweredAccessory

Cet état est représenté à la Figure 4-14.

À l'état ***PoweredAccessory***, le port alimente un ***accessoire alimenté par VCONN*** ou un ***dispositif USB alimenté par VCONN***.

4.5.2.2.20.1 Exigences relatives à l'état PoweredAccessory

S'il est nécessaire que le port détermine l'orientation du connecteur, il ***doit*** uniquement le faire lorsqu'il passe à l'état ***PoweredAccessory*** en détectant laquelle des broches CC1 ou CC2 est connectée par le câble (à savoir la broche CC dont l'état est ***SRC.Rd***).

L'état ***SRC.Rd*** est détecté sur une seule des broches CC1 ou CC2. Le port ***doit*** annoncer 1,5 A ou 3,0 A (voir le Tableau 4-27) sur cette broche CC et surveiller son état.

Le port ***doit*** alimenter la VCONN sur la broche CC inutilisée dans le délai ***tVCONNON-PA*** à compter du passage à l'état ***PoweredAccessory***.

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Le port ***ne doit pas*** piloter la VBUS.

Lorsqu'il passe initialement à l'état ***PoweredAccessory***, le port ***doit*** fonctionner comme une source ***USB Power Delivery*** avec un rôle de données DFP. En outre, le port ***doit*** prendre en charge au moins l'une des actions suivantes:

- utiliser l'***USB PD*** pour établir un contrat explicite, puis utiliser des messages définis par le fournisseur structurés (VDM structurés) pour identifier un ***accessoire alimenté par VCONN*** et entrer dans un ***mode alternatif***;
- utiliser l'***USB PD*** pour interroger l'identité d'un ***dispositif USB alimenté par VCONN*** (qui fonctionne comme la fiche d'un câble qui répond sur SOP').

4.5.2.2.20.2 Sortie de l'état PoweredAccessory

Le port ***doit*** passer à l'état ***Unattached.SNK*** lorsque l'état ***SRC.Open*** est détecté sur la broche CC surveillée.

Le port ***doit*** passer à l'état ***Try.SNK*** si le dispositif branché n'est pas un ***accessoire alimenté par VCONN*** ou un ***dispositif USB alimenté par VCONN***. Par exemple, le dispositif branché ne prend pas en charge l'***USB PD*** ou ne répond pas aux commandes ***USB PD*** exigées pour un ***accessoire alimenté par VCONN*** (découverte de SVID, recherche de modes, par exemple) ou il s'agit d'un destinataire ou d'une DRP branchée par un câble alimenté.

Le port ***doit*** passer à l'état ***Unsupported.Accessory*** si le dispositif branché est un ***accessoire alimenté par VCONN***, mais que le port n'a pas réussi à entrer dans un ***mode alternatif*** dans le délai ***tAMETimeout*** (voir l'Annexe E).

Un port qui prend en charge un ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTUnattached.SNK*** si le dispositif connecté s'identifie comme un ***dispositif USB alimenté par VCONN*** de charge dans sa réponse à la commande de ***découverte d'identité***. Le port ***peut*** retarder ce basculement pour effectuer d'autres communications SOP'.

Le port ***doit*** interrompre l'alimentation de la VCONN dans le délai ***tVCONNOFF*** après être sorti de l'état ***PoweredAccessory***, sauf s'il passe à l'état ***CTUnattached.SNK***.

4.5.2.2.21 État Unsupported.Accessory

Cet état est représenté à la Figure 4-14.

Si un ***accessoire alimenté par VCONN*** n'entre pas dans un ***mode alternatif***, l'état ***Unsupported.Accessory*** est utilisé pour attendre que l'accessoire soit débranché avant de poursuivre.

4.5.2.2.21.1 Exigences relatives à l'état Unsupported.Accessory

Une seule des broches CC1 ou CC2 ***doit*** être à l'état ***SRC.Rd***. Le port ***doit*** annoncer la puissance USB par défaut (voir le Tableau 4-27) sur cette broche CC et surveiller sa tension.

Le port ***ne doit pas*** piloter la VBUS ou VCONN.

Un destinataire prenant en charge un ***accessoire alimenté par VCONN*** ou un ***dispositif USB alimenté par VCONN*** ***doit*** fournir une notification utilisateur indiquant qu'elle ne reconnaît ou ne prend pas en charge l'accessoire ou le dispositif branché.

4.5.2.2.21.2 Sortie de l'état Unsupported.Accessory

Le port ***doit*** passer à l'état ***Unattached.SNK*** lorsque l'état ***SRC.Open*** est détecté sur la broche CC surveillée.

4.5.2.2.22 État CTUnattached.VPD

Cet état est représenté à la Figure 4-18.

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Dans l'état ***CTUnattached.VPD***, le ***dispositif USB alimenté par VCONN*** de charge a détecté l'état ***SNK.Open*** sur son port hôte pendant le délai ***tVPDCTDD***. Cela indique qu'il est connecté à une source compatible avec la charge, et qu'il surveille de manière indépendante son port de charge en vue de détecter la présence d'une source d'alimentation de transfert.

Cet état ***peut*** aussi avoir été activé par le débranchement d'une source d'alimentation sur le port de charge ou par le débranchement d'un destinataire du port de charge du ***CTVPD***.

4.5.2.2.22.1 Exigences relatives à l'état CTUnattached.VPD

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** isoler son port côté hôte de son port de charge, y compris les broches CC et VBUS. Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** assurer qu'il est alimenté par VCONN, que sa consommation ne dépasse pas Iccs (***USB 3.2***)/Iccsh (***USB 2.0***) de VBUS pour la surveillance, et qu'il est suffisamment isolé de VBUS afin de tolérer des tensions élevées pendant l'opération de charge.

Dès l'entrée dans cet état, le dispositif ***doit*** retirer la terminaison ***Rd*** à la masse (le cas échéant) de la broche CC du port côté hôte. Il doit à la place fournir une terminaison ***Rp*** qui annonce 3,0 A conformément au Tableau 4-27. Noter que, comme la VBUS n'est pas fournie, les signaux de la terminaison ***Rp*** ont continué à se connecter au port partenaire, mais ne s'accompagnent d'aucune annonce de courant.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** uniquement répondre aux requêtes de ***découverte d'identité USB PD*** sur SOP' sur son port côté hôte. Il ***doit*** assurer une capacité suffisante sur la broche CC du port côté hôte afin de satisfaire aux exigences cReceiver définies dans l'***USB PD***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** mettre les deux broches CC1 et CC2 du port de charge à la masse, de façon indépendante, par le biais de la ***Rd***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** fournir une capacité de découplage de CCTB sur les broches VBUS du port de charge.

4.5.2.2.22.2 Sortie de l'état CTUnattached.VPD

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTAttachWait.VPD*** lorsque la connexion d'une source est détectée sur le port de charge, comme l'indique l'état ***SNK.Rp*** sur exactement l'une des broches CC du port de charge.

Les accessoires de débogage ne sont pas pris en charge sur le port de charge.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***Unattached.SNK*** si VCONN chute au-dessous de ***vVCONNDisconnect***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTUnattached.Unsupported*** dans le délai ***tDRPTransition***, après basculement des deux broches CC1 et CC2 du port de charge à l'état ***SNK.Open*** pendant le délai ***tDRP*** – ***dcSRC.DRP*** · ***tDRP*** ou en cas de demande.

4.5.2.2.23 État CTAttachWait.VPD

Cet état est représenté à la Figure 4-18.

À l'état ***CTAttachWait.VPD***, le dispositif détecte l'état ***SNK.Rp*** sur exactement l'une des broches CC du port de charge et attend la VBUS sur le port de charge.

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4.5.2.2.23.1 Exigences relatives à l'état CTAttachWait.VPD

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** isoler son port côté hôte de son port de charge, y compris les broches CC et VBUS. Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** assurer qu'il est alimenté par VCONN, que sa consommation ne dépasse pas Iccs (***USB 3.2***)/Iccsh (***USB 2.0***) de VBUS pour la surveillance, et qu'il est suffisamment isolé de VBUS afin de tolérer des tensions élevées pendant l'opération de charge.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** maintenir la terminaison ***Rp*** qui annonce 3,0 A sur la broche CC du port côté hôte. Il ***doit*** aussi continuer à mettre les broches CC1 et CC2 de son port de charge à la masse, de façon indépendante, par le biais de la ***Rd***.

Le ***dispositif USB alimenté par VCONN*** de charge doit uniquement répondre aux requêtes de **découverte d'identité USB PD** sur SOP' sur son port côté hôte et terminer toutes les requêtes actives avant de quitter cet état. Il ***doit*** assurer une capacité suffisante sur la broche CC du port côté hôte afin de satisfaire aux exigences cReceiver définies dans l'***USB PD***.

4.5.2.2.23.2 Sortie de l'état CTAttachWait.VPD

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTUnattached.VPD*** lorsque l'état des broches CC1 et CC2 du port de charge sont à l'état ***SNK.Open*** pendant un délai d'au moins ***tPDDebounce***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTAttached.VPD*** lorsqu'une seule des broches CC1 et CC2 du port de charge est passée à l'état ***SNK.Rp*** pendant un délai d'au moins ***tCCDebounce*** et que la VBUS du port de charge est détectée.

Noter que la source de charge ***peut*** initier une communication ***USB PD***, qui entraîne de courtes périodes à l'état ***SNK.Open*** sur l'une des broches CC du port de charge, tandis que l'état de la seconde broche CC reste ***SNK.Open***; toutefois, cet événement ne dépasse pas le délai ***tPDDebounce***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTDisabled.VPD*** si VCONN chute au-dessous de ***vVCONNDisconnect***.

4.5.2.2.24 État CTAttached.VPD

Cet état est représenté à la Figure 4-18.

À l'état ***CTAttached.VPD***, le ***dispositif USB alimenté par VCONN*** de charge a détecté une source d'alimentation sur son port de charge et a connecté les broches CC et VBUS du port de charge directement aux broches CC et VBUS du port côté hôte. Par conséquent, l'ensemble des alimentations électriques, négociations et communications ***USB PD*** sont directement effectuées entre l'unité sur le port côté hôte et la source d'alimentation connectée au port de charge.

4.5.2.2.24.1 Exigences relatives à l'état CTAttached.VPD

Dès l'entrée dans cet état, le ***dispositif USB alimenté par VCONN*** de charge ***doit*** détecter laquelle des broches CC1 ou CC2 du port de charge est connectée par le câble (à savoir la broche CC qui se trouve dans l'état ***SNK.Rp***). Le dispositif ***doit*** alors, immédiatement et dans l'ordre suivant:

1. supprimer ou réduire toute capacité supplémentaire sur le port CC côté hôte qui a été ajoutée afin de satisfaire aux exigences cReceiver définies dans l'***USB PD***, et afin de présenter sur la broche CC une valeur inférieure ou égale à deux fois la valeur maximale de cCablePlug_CC;
2. désactiver la terminaison ***Rp*** qui annonce 3,0 A sur la broche CC du port hôte;
3. multiplexer de manière passive la broche CC détectée du port de charge à la broche CC du port hôte avec une impédance inférieure à celle de RccCON;
4. désactiver la ***Rd*** sur les broches CC1 et CC2 du port de charge;
5. connecter la broche VBUS du port de charge à la broche VBUS du port hôte.

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Ces étapes ***doivent*** être accomplies dans le délai ***tVPDDetach*** minimal après l'entrée dans cet état.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** assurer qu'il est alimenté par VCONN, que sa consommation ne dépasse pas Iccs (***USB 3.2***)/Iccsh (***USB 2.0***) de VBUS pour la surveillance, et qu'il est suffisamment isolé de VBUS afin de tolérer des tensions élevées pendant l'opération de charge.

Le ***dispositif USB alimenté par VCONN*** de charge ***ne doit pas*** répondre à une communication ***USB PD*** sur une broche CC dans cet état. Toute requête active sur SOP' ***doit*** avoir été effectuée avant d'être passée à cet état.

4.5.2.2.24.2 Sortie de l'état CTAttached.VPD

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTUnattached.VPD*** lorsque la VBUS chute au-dessous de ***vSinkDisconnect*** ou que l'état de la broche CC traversée est ***SNK.Open*** pendant le délai ***tVPDCTDD***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTDisabled.VPD*** si VCONN chute au-dessous de ***vVCONNDisconnect***.

4.5.2.2.25 État CTDisabled.VPD

Cet état est représenté à la Figure 4-18.

À l'état ***CTDisabled.VPD***, le ***dispositif USB alimenté par VCONN*** de charge a détecté une déconnexion sur son port côté hôte, mais ***peut*** encore être connecté à une source d'alimentation sur le port de charge. Cela permet d'assurer que la VBUS de la source d'alimentation est retirée.

4.5.2.2.25.1 Exigences relatives à l'état CTDisabled.VPD

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** isoler son port côté hôte de son port de charge, y compris les broches CC et VBUS.

Le dispositif ***doit*** présenter une impédance de mise à la masse élevée (supérieure à ***zOPEN***) sur la broche CC du port côté hôte, et sur les broches CC1 et CC2 du port de charge.

Le ***dispositif USB alimenté par VCONN*** de charge **doit** assurer qu'il est entièrement alimenté par VBUS.

4.5.2.2.25.2 Sortie de l'état CTDisabled.VPD

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***Unattached.SNK*** à l'issue du délai ***tVPDDisable***.

4.5.2.2.26 État CTUnattached.SNK

Cet état est représenté à la Figure 4-14, à la Figure 4-16 et à la Figure 4-17.

À l'état ***CTUnattached.SNK***, le port a détecté qu'il est branché à un ***dispositif USB alimenté par VCONN*** de charge et qu'il est prêt si une source d'alimentation est branchée au ***dispositif USB alimenté par VCONN*** de charge.

Cet état ***peut*** aussi s'activer en cas de débranchement d'une source d'alimentation de charge.

4.5.2.2.26.1 Exigences relatives à l'état CTUnattached.SNK

Dès l'entrée dans cet état, le port ***doit*** retirer sa terminaison ***Rp*** (le cas échéant) et mettre la broche CC à la masse par de biais de la ***Rd***.

Le port ***doit*** continuer à fournir la VCONN.

Le port ***doit*** cesser d'alimenter ou de collecter la VBUS et de la décharger.

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Dans l'***USB PD*** version 2.0, le port ***doit*** initier les messages PD.

Le port ***peut*** interroger l'état du ***dispositif USB alimenté par VCONN*** branché en envoyant des messages SOP' sur l'***USB PD*** afin de lire le marqueur électronique du ***VPD***.

4.5.2.2.26.2 Sortie de l'état CTUnattached.SNK

Le ***doit*** passer à l'état ***CTAttached.SNK*** lorsque la VBUS n'est plus présente. Noter qu'à ce stade, le ***dispositif USB alimenté par VCONN*** a déjà éliminé les rebonds de la broche CC traversée.

Le port ***doit*** passer à l'état ***Unattached.SNK*** si l'état de la broche CC est ***SNK.Open*** pendant le délai ***tVPDDetach*** lorsque VBUS est ***vSafe0V***.

4.5.2.2.27 État CTAttached.SNK

Cet état est représenté à la Figure 4-14, à la Figure 4-16 et à la Figure 4-17.

À l'état ***CTAttached.SNK***, le port est connecté à un ***dispositif USB alimenté par VCONN*** de charge qui à son tour passe par la connexion à une source d'alimentation.

4.5.2.2.27.1 Exigences relatives à l'état CTAttached.SNK

Le port ***doit*** continuer à mettre la broche CC à la masse par le biais de la ***Rd***. Étant donné qu'une source d'alimentation est maintenant connectée aux broches VBUS et CC, le port ***doit*** fonctionner dans l'un des ***sous-états Sink Power*** indiqués à la Figure 4-19 et demeurer dans l'un des ***sous-états Sink Power*** jusqu'à ce que la broche VBUS soit retirée ou qu'un contrat ***USB PD*** soit établi avec la source.

Le port ***ne doit pas*** négocier une tension sur la VBUS supérieure à la tension maximale spécifiée dans la réponse à la commande de ***découverte d'identité*** du ***dispositif USB alimenté par VCONN*** de charge.

Le port ***doit*** continuer à fournir la VCONN.

Le port ***doit*** rejeter une demande de permutation VCONN.

Le port ***ne doit pas*** effectuer de détection primaire ***USB BC 1.2***, car cela interfère avec la fonctionnalité du ***VPD***.

Dans l'***USB PD*** version 2.0, le port ***ne doit pas*** initier les messages ***USB PD***, même s'il reste un DFP pour les données USB.

Le port ne ***doit*** ni initier ni répondre à une communication SOP'.

Le port ***doit*** satisfaire aux exigences relatives au ***sous-état Sink Power*** spécifiées en 4.5.2.3.

Le port ***doit*** satisfaire aux contraintes de courant maximal supplémentaires décrites en 4.6.2.5.

Le port ***doit*** satisfaire aux restrictions sur les messages ***USB PD*** décrites en 4.10.2.

Le port ***doit*** modifier ses capacités annoncées par le rôle d'UFP/de destinataire uniquement comme cela est décrit en 4.10.2.

4.5.2.2.27.2 Sortie de l'état CTAttached.SNK

Lorsqu'un port n'est pas concerné par une réinitialisation ***USB PD*** Hard Reset, il ***doit*** passer à l'état ***CTUnattached.SNK*** dans le délai ***tSinkDisconnect*** lorsque la VBUS chute au-dessous de ***vSinkDisconnect*** pour une VBUS inférieure ou égale à 5 V ou au-dessous de ***vSinkDisconnectPD*** lorsque l'***USB PD*** a négocié un fonctionnement au-dessus de 5 V.

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Un port qui est entré en communication ***USB PD*** avec la source et qui a enregistré une tension CC supérieure à ***vRd-USB*** ***peut*** surveiller la broche CC pour détecter une déconnexion de câble en plus de contrôler VBUS.

Un port qui surveille la tension CC à la recherche de déconnexion ***doit*** passer à l'état ***CTUnattached.SNK*** dans le délai ***tSinkDisconnect*** après maintien de la tension CC au-dessous de ***vRd-USB*** pendant le délai ***tPDDebounce***.

4.5.2.2.28 État CTUnattached.Unsupported

Cet état est représenté à la Figure 4-18.

À l'état ***CTUnattached.Unsupported***, le ***dispositif USB alimenté par VCONN*** de charge a précédemment détecté l'état ***SNK.Open*** sur son port hôte pendant le délai ***tVPDCTDD***. Cela indique qu'il est connecté à une source compatible avec la charge, et qu'il surveille désormais son port de charge en vue de détecter la présence d'un destinataire non pris en charge.

Un ***dispositif USB alimenté par VCONN*** de charge ne prend en charge ni les destinataires ni le ***mode accessoire de débogage***.

4.5.2.2.28.1 Exigences relatives à l'état CTUnattached.Unsupported

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** isoler son port côté hôte de son port de charge, y compris les broches CC et VBUS. Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** assurer qu'il est alimenté par VCONN, que sa consommation ne dépasse pas Iccs (***USB 3.2***) / Iccsh (***USB 2.0***) de VBUS pour la surveillance, et qu'il est suffisamment isolé de VBUS afin de tolérer des tensions élevées pendant l'opération de charge.

Dès l'entrée dans cet état, le ***dispositif USB alimenté par VCONN*** de charge ***doit*** maintenir la terminaison ***Rp*** qui annonce 3,0 A sur la broche CC du port côté hôte. Il ***doit*** retirer la terminaison ***Rd*** à la masse des broches CC1 et CC2 du port de charge. Il ***doit*** à la place fournir une terminaison ***Rp*** qui annonce la puissance USB par défaut.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** uniquement répondre aux requêtes de ***découverte d'identité USB PD*** sur SOP' sur son port côté hôte. Il ***doit*** assurer une capacité suffisante sur la broche CC du port côté hôte afin de satisfaire aux exigences cReceiver définies dans l'***USB PD***.

4.5.2.2.28.2 Sortie de l'état CTUnattached.Unsupported

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTAttachWait.Unsupported*** lorsqu'une connexion de destinataire est détectée sur le port de charge, comme l'indique l'état ***SRC.Rd*** sur au moins l'une des broches CC du port de charge ou l'état ***SRC.Ra*** sur les deux broches CC1 et CC2.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***Unattached.SNK*** si VCONN chute au-dessous de ***vVCONNDisconnect***.

Sinon, un ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTUnattached.VPD*** dans le délai ***tDRPTransition***, à l'issue du délai ***dcSRC.DRP*** · ***tDRP*** ou cas de demande.

4.5.2.2.29 État CTAttachWait.Unsupported

Cet état est représenté à la Figure 4-18.

L'état ***CTAttachWait.Unsupported*** est utilisé pour assurer que l'état des deux broches CC1 et CC2 du port de charge est stable pendant un délai d'au moins ***tCCDebounce***.

4.5.2.2.29.1 Exigences relatives à l'état CTAttachWait.Unsupported

Les exigences relatives à cet état sont identiques à celles de l'état ***CTUnattached.Unsupported***.

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4.5.2.2.29.2 Sortie de l'état CTAttachWait.Unsupported

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTTry.SNK*** si l'état d'au moins l'une des broches CC du port de charge est ***SRC.Rd***, ou si l'état des deux broches CC1 et CC2 est ***SRC.Ra*** pendant un délai d'au moins ***tCCDebounce***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTUnattached.VPD*** lorsque l'état de la broche CC1 ou CC2 du port de charge est ***SRC.Open*** pendant un délai d'au moins ***tCCDebounce***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***Unattached.SNK*** si VCONN chute au-dessous de ***vVCONNDisconnect***.

4.5.2.2.30 État CTTry.SNK

Cet état est représenté à la Figure 4-18.

À l'état ***CTTry.SNK***, le ***dispositif USB alimenté par VCONN*** de charge effectue une requête pour déterminer si le port partenaire sur le port de charge prend en charge le rôle de source.

4.5.2.2.30.1 Exigences relatives à l'état CTTry.SNK

Les exigences relatives à cet état sont identiques à celles de l'état ***CTUnattached.VPD***.

4.5.2.2.30.2 Sortie de l'état CTTry.SNK

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** attendre le délai ***tDRPTry*** et, seulement après, commencer à surveiller l'affectation de l'état ***SNK.Rp*** à la broche CC du port de charge.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** ensuite passer à l'état ***CTAttached.VPD*** lorsque l'état ***SNK.Rp*** est détecté sur les broches CC du port de charge pendant un délai d'au moins ***tTryCCDebounce*** et que la VBUS est détectée sur le port de charge.

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTAttached.Unsupported*** si l'état ***SNK.Rp*** n'est pas détecté pendant le délai ***tDRPTryWait***.

Note: La source ***peut*** initier une communication ***USB PD***, qui entraîne de courtes périodes à l'état ***SNK.Open*** sur les deux broches CC1 et CC2; toutefois, cet événement ne dépasse pas le délai ***tTryCCDebounce***.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***Unattached.SNK*** si VCONN chute au-dessous de ***vVCONNDisconnect***.

4.5.2.2.31 État CTAttached.Unsupported

Cet état est représenté à la Figure 4-18.

Si le port partenaire du port de charge du ***dispositif USB alimenté par VCONN*** de charge ne prend pas en charge le rôle d'alimentation source ou n'a pas réussi à négocier le rôle de source, l'état ***CTAttached.Unsupported*** est utilisé pour attendre que ce dispositif soit débranché avant de continuer.

4.5.2.2.31.1 Exigences relatives à l'état CTAttached.Unsupported

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** isoler son port côté hôte de son port de charge, y compris les broches CC et VBUS. Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** assurer qu'il est alimenté par VCONN, que sa consommation ne dépasse pas Iccs (***USB 3.2***)/Iccsh (***USB 2.0***) de VBUS pour la surveillance, et qu'il est suffisamment isolé de VBUS afin de tolérer des tensions élevées pendant l'opération de charge.

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Dès l'entrée dans cet état, le ***dispositif USB alimenté par VCONN*** de charge ***doit*** maintenir la terminaison ***Rp*** qui annonce 3,0 A sur la broche CC du port côté hôte. Il ***doit*** retirer la terminaison ***Rd*** à la masse des broches CC1 et CC2 du port de charge. Il ***doit*** à la place fournir une terminaison ***Rp*** qui annonce la puissance USB par défaut.

Au moins une des broches CC1 ou CC2 bascule dans l'état ***SRC.Rd*** ou les deux broches basculent dans l'état ***SRC.Ra***. Le port de charge ***doit*** annoncer la puissance USB par défaut (voir le Tableau 4-27) sur ses broches CC et surveiller leur tension.

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** présenter une interface ***USB Billboard Device Class*** qui indique qu'il ne reconnaît ni ne prend en charge l'accessoire ou le dispositif branché.

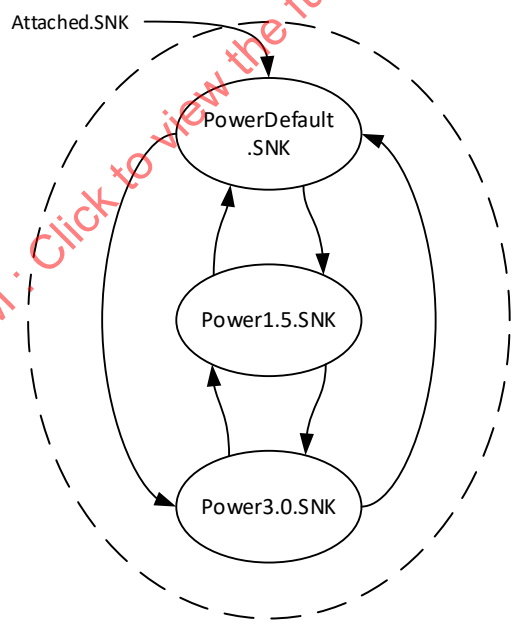
4.5.2.2.31.2 Sortie de l'état CTAttached.Unsupported

Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** passer à l'état ***CTUnattached.VPD*** lorsque l'état ***SRC.Open*** est détecté sur les deux broches CC du port de charge, ou lorsque l'état ***SRC.Open*** est détecté sur l'une des broches CC et l'état ***SRC.Ra*** est détecté sur l'autre broche CC.

4.5.2.3 Exigences relatives au sous-état Sink Power

À l'état ***Attached.SNK*** ou ***CTAttached.SNK*** et lorsque la source alimente la VBUS par défaut, le port ***doit*** fonctionner dans l'un des sous-états représentés à la Figure 4-19. Le ***sous-état Sink Power*** initial est ***PowerDefault.SNK***. Puis, le ***sous-état Sink Power*** est déterminé par l'annonce de courant USB Type-C de la source. Le port à l'état ***Attached.SNK*** ***doit*** rester dans le ***sous-état Sink Power*** jusqu'au retrait de la VBUS ou jusqu'à l'établissement du contrat ***USB PD*** avec la source.

Figure 4-19 Sous-états Sink Power



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Le destinataire n'est exigé que pour la mise en œuvre des transitions avec le ***sous-état Sink Power***, lorsque le destinataire demande à puiser un courant USB supérieur à celui par défaut.

Noter que pour l'état ***CTAttached.SNK***, il existe d'autres limitations concernant le courant maximal (voir 4.6.2.5).

4.5.2.3.1 Sous-état PowerDefault.SNK

Ce sous-état prend en charge les destinataires qui consomment un courant dans la plage minimale (par défaut) de courants, fournie par la source.

4.5.2.3.1.1 Exigences relatives au sous-état PowerDefault.SNK

Le port ne ***doit*** pas puiser plus que l'alimentation USB par défaut de VBUS. Voir 4.6.2.1.

Si le port demande à consommer une alimentation USB supérieure à celle établie par défaut, il ***doit*** surveiller la ***vRd*** pour déterminer si la source est en capacité de fournir un courant supérieur.

4.5.2.3.1.2 Sortie du sous-état PowerDefault.SNK

Pour toute modification de ***vRd*** indiquant une variation de l'alimentation admissible, le port ***ne doit pas*** changer d'état tant que la nouvelle ***vRd*** n'a pas été stable pendant un délai d'au moins ***tRpValueChange***.

Pour une ***vRd*** dans la plage ***vRd-1.5***, le port ***doit*** basculer vers le sous-état ***Power1.5.SNK***.

Pour une ***vRd*** dans la plage ***vRd-3.0***, le port ***doit*** basculer vers le sous-état ***Power3.0.SNK***.

4.5.2.3.2 Sous-état Power1.5.SNK

Ce sous-état prend en charge les destinataires qui consomment un courant dans les deux plages de courants les plus basses (par défaut et 1,5 A), fournies par la source.

4.5.2.3.2.1 Exigences relatives au sous-état Power1.5.SNK

Le port ne ***doit*** pas puiser plus que 1,5 A de VBUS.

Le port ***doit*** surveiller les deux tensions ***vRd*** lorsqu'il est dans ce sous-état.

4.5.2.3.2.2 Sortie du sous-état Power1.5.SNK

Pour toute modification de ***vRd*** indiquant une variation de l'alimentation admissible, le port ***ne doit pas*** changer d'état tant que la nouvelle ***vRd*** n'a pas été stable pendant un délai d'au moins ***tRpValueChange***.

Pour une ***vRd*** dans la plage ***vRd-USB***, le port ***doit*** basculer vers le sous-état ***PowerDefault.SNK*** et réduire sa consommation électrique à la nouvelle plage dans le délai ***tSinkAdj***.

Pour une ***vRd*** dans la plage ***vRd-3.0***, le port ***doit*** basculer vers le sous-état ***Power3.0.SNK***.

4.5.2.3.3 Sous-état Power3.0.SNK

Ce sous-état prend en charge les destinataires qui consomment un courant dans les trois plages (par défaut, 1,5 A et 3,0 A) de courants, fournies par la source.

4.5.2.3.3.1 Exigences relatives au sous-état Power3.0.SNK

Le port ne ***doit*** pas puiser plus que 3,0 A de VBUS.

Le port ***doit*** surveiller les deux tensions ***vRd*** lorsqu'il est dans ce sous-état.

4.5.2.3.3.2 Sortie du sous-état Power3.0.SNK

Pour toute modification de ***vRd*** indiquant une variation de l'alimentation admissible, le port ***ne doit pas*** changer d'état tant que la nouvelle ***vRd*** n'a pas été stable pendant un délai d'au moins ***tRpValueChange***.

Pour une ***vRd*** dans la plage ***vRd-USB***, le port ***doit*** basculer vers le sous-état ***PowerDefault.SNK*** et réduire sa consommation électrique à la nouvelle plage dans le délai ***tSinkAdj***.

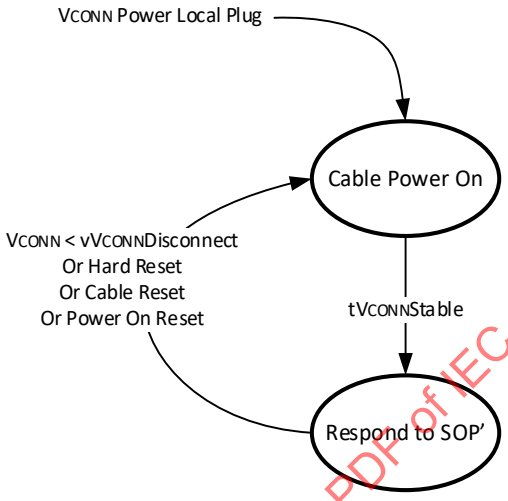
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Pour une ***vRd*** dans la plage ***vRd-1,5***, le port ***doit*** basculer vers le sous-état ***Power1.5.SNK*** et réduire sa consommation électrique à la nouvelle plage dans le délai ***tSinkAdj***.

4.5.2.4 Exigences relatives aux diagrammes d'états du marqueur électronique des câbles

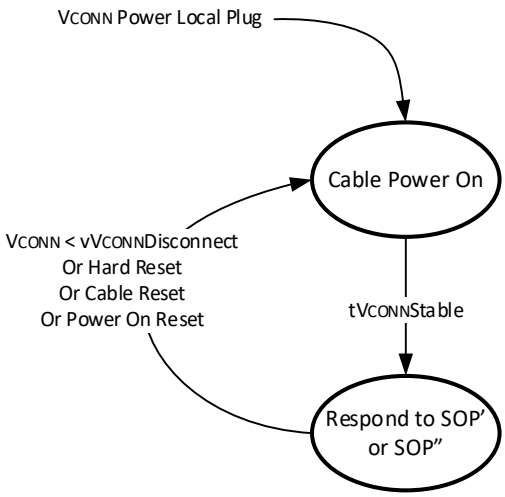
La Figure 4-20 et la Figure 4-21 représentent les diagrammes d'états de connexion par câble avec marqueur électronique pour des câbles actifs et passifs, respectivement.

Figure 4-20 Diagramme d'états de connexion par câble passif avec marqueur électronique



Anglais	Français
VCONN Power Local Plug	Fiche VCONN Power
Cable Power On	Câble d'alimentation branché
Respond to SOP'	Répondre à SOP'
Or Hard Reset Or Cable Reset Or Power On Reset	Ou réinitialisation matérielle Ou réinitialisation par câble Ou réinitialisation de l'alimentation

Figure 4-21 Diagramme d'états de connexion par câble actif avec marqueur électronique



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Anglais	Français
VCONN Power Local Plug	Fiche VCONN Power
Cable Power On	Câble d'alimentation branché
Respond to SOP' or SOP"	Répondre à SOP' ou SOP''
Or Hard Reset Or Cable Reset Or Power On Reset	Ou réinitialisation matérielle Ou réinitialisation par câble Ou réinitialisation de l'alimentation

4.5.2.4.1 État Cable Power On

Cet état est représenté à la Figure 4-20. Il s'agit de l'état de mise sous tension initiale pour chaque marqueur électronique du câble lorsque la VCONN est appliquée.

4.5.2.4.1.1 Exigences relatives à l'état Cable Power On

Chaque marqueur électronique du câble ***doit*** se mettre sous tension.

Dans cet état, le câble ***ne doit pas*** répondre aux commandes SOP' et SOP".

4.5.2.4.1.2 Sortie de l'état Cable Power On

Chaque marqueur électronique d'un câble passif ou actif ***doit*** passer à l'état Assign Cable SOP* lorsqu'il a terminé son processus d'amorçage. Chaque marqueur électronique ***doit*** passer à l'état Assign Cable SOP* dans le délai ***tVCONNStable***.

4.5.2.4.2 État Respond to Respond to SOP'/SOP''

Cet état est représenté à la Figure 4-20 et à la Figure 4-21.

Un câble passif ne compte qu'un seul marqueur électronique alimenté à la fois. Dans cet état, ce marqueur électronique d'un câble passif ***doit*** répondre à SOP'.

Chaque marqueur électronique d'un câble actif ***doit*** répondre à un SOP' ou SOP'' prédéfini. S'il n'existe qu'un seul marqueur électronique dans le câble, il ne ***doit*** répondre qu'à SOP'.

Les concepteurs de câble ***doivent*** veiller au bon fonctionnement des marqueurs électroniques en présence de masse et en cas de chute de tension ohmique maximale de VCONN.

4.5.2.4.2.1 Exigences relatives à l'état Respond to SOP'/SOP”

Le marqueur électronique d'un câble passif ou actif ***doit*** être capable de répondre à une communication ***USB PD*** envoyée à son SOP' ou SOP'' prédéfini. Pour un câble passif, ***il convient*** d'alimenter un seul marqueur électronique à la fois et celui-ci ne ***doit*** répondre qu'à SOP'. Si deux marqueurs électroniques existent dans un câble passif ou actif, et sont alimentés en même temps, un seul ***doit*** répondre à SOP' tandis que l'autre ***doit*** répondre à SOP''. L'affectation des SOP' et SOP'' est fixée pour chaque marqueur électronique d'un câble et ***ne doit pas*** être définie de manière dynamique lorsque l'alimentation est appliquée à VCONN.

4.5.2.4.2.2 Sortie de l'état Respond to SOP'/SOP”

Chaque marqueur électronique du câble ***doit*** passer à l'état Cable Power On lors de la détection d'une VCONN inférieure à ***vVCONNDisconnect*** ou lors d'un événement Power On Reset.

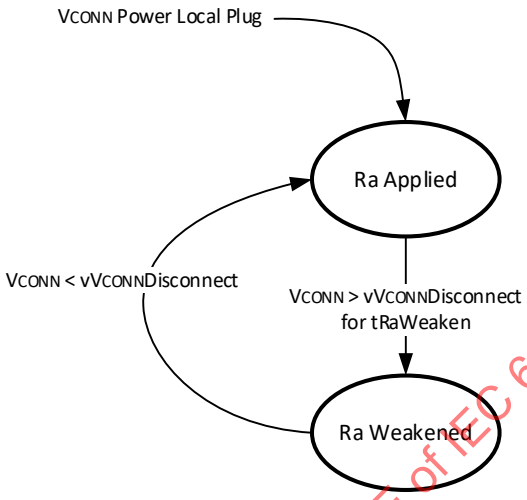
Chaque marqueur électronique du câble ***doit*** passer à l'état Cable Power On lors de la détection d'une réinitialisation Hard Reset ou Cable Reset.

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4.5.2.5 Exigences relatives aux diagrammes d'états de gestion de câble Ra

La Figure 4-22 représente le diagramme d'états de marqueur électronique de câble pour appliquer et affaiblir ou retirer ***Ra***. Ce diagramme d'états fonctionne indépendamment du diagramme d'états du marqueur électronique de câble décrit en 4.5.2.4.

Figure 4-22 Diagramme d'états de gestion de câble Ra



Anglais	Français
VCONN Power Local Plug	Fiche VCONN Power
Ra Applied	Ra Applied
for	pour
Ra Weakened	Ra Weakened

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4.5.2.5.1 État Ra Applied

Cet état est représenté à la Figure 4-22. Il s'agit de l'état initial à la mise sous tension pour chaque marqueur électronique du câble.

4.5.2.5.1.1 Exigences relatives à l'état Ra Applied

Chaque marqueur électronique du câble ***doit*** appliquer ***Ra*** à la VCONN dans le délai ***tRaReconnect***.

4.5.2.5.1.2 Sortie de l'état Ra Applied

Chaque marqueur électronique d'un câble passif ou actif ***doit*** passer à l'état ***Ra*** Weakened lorsque la VCONN est supérieure à ***vVCONNDisconnect*** pendant un délai ***tRaWeaken***.

4.5.2.5.2 État Ra Weakened

Cet état est représenté à la Figure 4-22.

4.5.2.5.2.1 Exigences relatives à l'état Ra Weakened

Le marqueur électronique du câble ***doit*** retirer ou affaiblir ***Ra***.

Les câbles passifs ***doivent*** satisfaire à l'Alimentation des câbles passifs avec marquage électronique définie dans le Tableau 4-6. Les câbles actifs ***doivent*** satisfaire à l'Alimentation des câbles actifs définie dans le Tableau 4-6.

4.5.2.5.2.2 Sortie de l'état Ra Weakened

Chaque marqueur électronique d'un câble passif ou actif ***doit*** passer à l'état ***Ra*** Applied lorsque la VCONN est inférieure à ***vVCONNDisconnect***.

4.5.2.6 Récapitulatif des états de connexion

Le Tableau 4-18 définit les états obligatoires et ***facultatifs*** pour chaque type de port.

Tableau 4-18 États obligatoires et facultatifs

	SOURCE	DESTINATAIRE	DRP	Communications *USB PD*
Disabled	***Facultatif***	***Facultatif***	***Facultatif***	Non admis
ErrorRecovery	Obligatoire[10]	Obligatoire[10]	Obligatoire[10]	Non admis
Unattached.SNK	***N/A***	Obligatoire	Obligatoire	Non admis
AttachWait.SNK	***N/A***	Obligatoire[1]	Obligatoire	Non admis
Attached.SNK	***N/A***	Obligatoire	Obligatoire	Admis
UnattachedWait.SRC	Obligatoire ou ***N/A***[7]	***N/A***	***N/A***	Non admis
Unattached.SRC	Obligatoire	***N/A***	Obligatoire	Non admis
AttachWait.SRC	Obligatoire	***N/A***	Obligatoire	Non admis
Attached.SRC	Obligatoire	***N/A***	Obligatoire	Admis
Try.SRC[4]	***N/A***	***N/A***	***Facultatif***	Non admis
TryWait.SNK[2]	***N/A***	***N/A***	***Facultatif***	Non admis
Try.SNK[4, 8]	***N/A***	***N/A***	***Facultatif***	Non admis
TryWait.SRC[5, 8]	***N/A***	***N/A***	***Facultatif***	Non admis
CorrosionMitigation	***Facultatif***	***Facultatif***	***Facultatif***	Non admis
UnorientedDebugAccessory.SRC	Facultatif[6]	***N/A***	Facultatif[6]	Non admis
OrientedDebugAccessory.SRC	Facultatif[6]	***N/A***	Facultatif[6]	Admis
DebugAccessory.SNK	***N/A***	***Facultatif***	***Facultatif***	Admis
Unattached.Accessory	***N/A***	***Facultatif***	***N/A***	Non admis
AttachWait.Accessory	***N/A***	***Facultatif***	***N/A***	Non admis
PoweredAccessory	***N/A***	***Facultatif***	***N/A***	Admis
Unsupported.Accessory[3]	***N/A***	***Facultatif***	***N/A***	Non admis
CTUnattached.VPD	***N/A***	***N/A***	***Facultatif***	SOP' admis
CTAttachWait.VPD[8]	***N/A***	***N/A***	***Facultatif***	SOP' admis
CTAttached.VPD[8]	***N/A***	***N/A***	***Facultatif***	Non admis
CTDisabled.VPD[8]	***N/A***	***N/A***	***Facultatif***	Non admis
CTUnattached.SNK	***N/A***	***N/A***	***Facultatif***	SOP' admis
CTAttached.SNK[9]	***N/A***	***N/A***	***Facultatif***	Admis

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	SOURCE	DESTINATAIRE	DRP	Communications *USB PD*
CTUnattached.Unsupported[8]	***N/A***	***N/A***	***Facultatif***	SOP' admis
CTAttachWait.Unsupported[8]	***N/A***	***N/A***	***Facultatif***	SOP' admis
CTTry.SNK[8]	***N/A***	***N/A***	***Facultatif***	SOP' admis
CTAttached.Unsupported[8]	***N/A***	***N/A***	***Facultatif***	SOP' admis
PowerDefault.SNK	***N/A***	Obligatoire	Obligatoire	Admis
Power1.5.SNK	***N/A***	***Facultatif***	***Facultatif***	Admis
Power3.0.SNK	***N/A***	***Facultatif***	***Facultatif***	Admis

Notes:

1. ***Facultatif*** pour les applications UFP classées ***USB 2.0*** exclusives qui consomment une alimentation USB par défaut et qui ne prennent pas en charge l'***USB PD*** ni les accessoires.
2. L'état *TryWait.SNK* est obligatoire lorsque l'état *Try.SRC* est pris en charge.
3. L'état *Unsupported.Accessory* est obligatoire lorsque l'état *PoweredAccessory* est pris en charge.
4. Les états *Try.SRC* et *Try.SNK* ***ne doivent pas*** être pris en charge simultanément, et ce même si un dispositif non branché ***peut*** effectuer un choix dynamique entre les diagrammes d'états *Try.SRC* et *Try.SNK* à partir de facteurs externes.
5. L'état *TryWait.SRC* est obligatoire lorsque l'état *Try.SNK* est pris en charge.
6. L'état *UnorientedDebugAccessory.SRC* est exigé pour toute source ou DRP prenant en charge le *mode accessoire de débogage*. L'état *OrientedDebugAccessory.SRC* n'est exigé que si la détection de l'orientation est nécessaire en *mode accessoire de débogage*.
7. Obligatoire avec un DFP qui a fourni une VCONN à l'état *Attached.SRC* précédent. ***N/A*** avec un DFP qui n'a pas fourni de VCONN à l'état *Attached.SRC* précédent.
8. *CTAttachWait.VPD*, *CTAttached.VPD*, *CTDisabled.VPD*, *Try.SNK*, *TryWait.SRC*, *CTUnattached.Unsupported*, *CTAttachWait.Unsupported*, *CTAttached.Unsupported* et *CTTry.SNK* sont obligatoires lorsque *CTUnattached.VPD* est pris en charge.
9. L'état *CTAttached.SNK* est obligatoire lorsque l'état *CTUnattached.SNK* est pris en charge.
10. ***Facultatif*** pour les mises en œuvre non ***USB4*** et non ***USB PD***.

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4.5.3 Comportement d'interopérabilité des ports USB

Le présent paragraphe décrit le comportement d'interopérabilité entre les ports USB Type-C et les ports USB Type-C, et entre les ports USB Type-C et les ports USB existants.

4.5.3.1 Comportements d'interopérabilité entre les ports USB Type-C et les ports USB Type-C

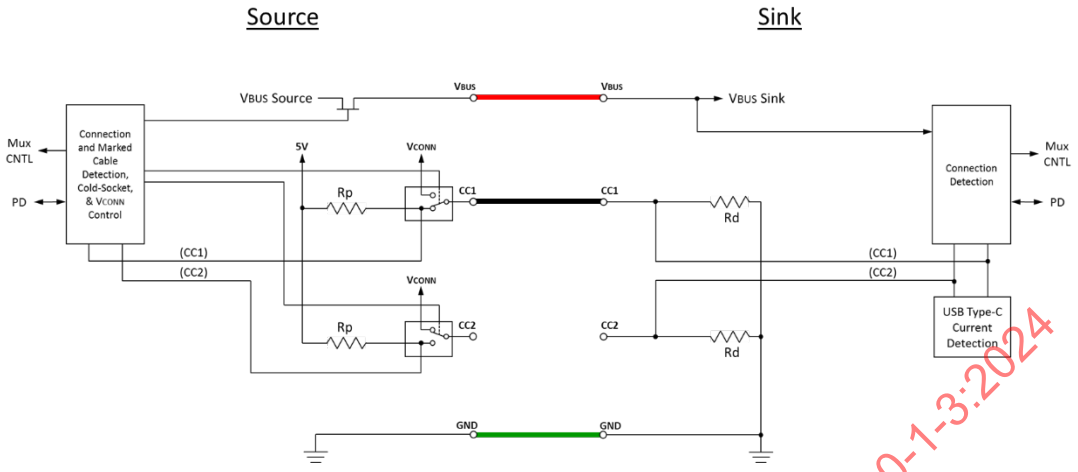
Les paragraphes suivants décrivent les comportements d'interopérabilité types entre deux ports pour les différentes combinaisons de source, de destinataire et de DRP USB Type C présentées dans le Tableau 4-9. Pour tous les comportements décrits, l'incidence des permutations ***USB PD*** (***PR_Swap***, ***DR_Swap*** ou ***VCONN_Swap***) n'est pas prise en compte.

Les figures suivantes représentent les routages CC1 et CC2 à la fin du processus de détection CC.

4.5.3.1.1 Comportement source-destinataire

La Figure 4-23 représente le modèle fonctionnel d'une source connectée à un destinataire. Le fil CC unique, utilisé dans un câble normalisé, n'est représenté que pour l'un des quatre chemins de connexion possibles, CC1 à CC1.

Figure 4-23 Modèle fonctionnel d'une source branchée à un destinataire



Anglais	Français
Source	Source
Sink	Destinataire
VBUS Source	Source VBUS
VBUS Sink	Destinataire VBUS
Connection and Marked Cable Detection, Cold-Socket, & VCONN Control	Détection de connexion et de câbles marqués électroniquement, prise commutée et contrôle de VCONN
Connection Detection	Détection de connexion
USB Type-C Current Detection	Détection de courant USB Type-C

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Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une source est connectée à un destinataire.

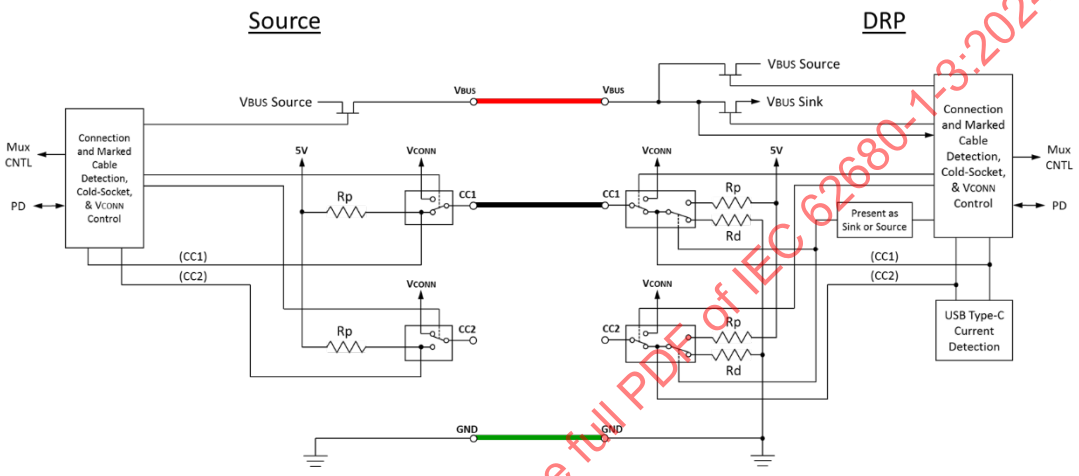
1. La source et le destinataire sont débranchés.
2. La source passe de l'état ***Unattached.SRC*** à l'état ***Attached.SRC***, en passant par l'état ***AttachWait.SRC***.
   - La source détecte la dépolarisation du destinataire sur la broche CC et passe à l'état ***Attached.SRC***, en passant par l'état ***AttachWait.SRC***.
   - La source active VBUS et VCONN.
3. Le destinataire passe de l'état ***Unattached.SNK*** à l'état ***Attached.SNK*** en passant par l'état ***AttachWait.SNK***. Le destinataire ***peut*** ignorer l'état ***AttachWait.SNK*** s'il est ***USB 2.0*** exclusif et qu'il ne prend pas en charge les accessoires.
   - Le destinataire détecte la VBUS et passe à l'état ***Attached.SNK***, en passant par l'état ***AttachWait.SNK***.
4. Lorsque la source et le destinataire sont branchés:
   - La source ajuste la ***Rp*** en fonction des besoins, afin de limiter le courant qui ***peut*** être puisé par le destinataire.
   - Le destinataire détecte et surveille la ***vRd*** par rapport au courant disponible sur la VBUS.

- La source surveille la broche CC afin de détecter un débranchement; si un débranchement est détecté, elle passe à l'état ***Unattached.SRC***.
- Le destinataire surveille la broche VBUS afin de détecter un débranchement; si un débranchement est détecté, il passe à l'état ***Unattached.SNK***.

4.5.3.1.2 Comportement source-DRP

La Figure 4-24 représente le modèle fonctionnel d'une source connectée à une DRP. Le fil CC unique, utilisé dans un câble normalisé, n'est représenté que pour l'un des quatre chemins de connexion possibles, CC1 à CC1.

Figure 4-24 Modèle fonctionnel d'une source branchée à une DRP



Anglais	Français
Source	Source
DRP	DRP
VBUS Source	Source VBUS
VBUS Sink	Destinataire VBUS
Connection and Marked Cable Detection, Cold-Socket, & VCONN Control	Détection de connexion et de câbles marqués électroniquement, prise commutée et contrôle de VCONN
Present as Sink or Source	Source ou destinataire présent
USB Type-C Current Detection	Détection de courant USB Type-C

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Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une source est connectée à une DRP.

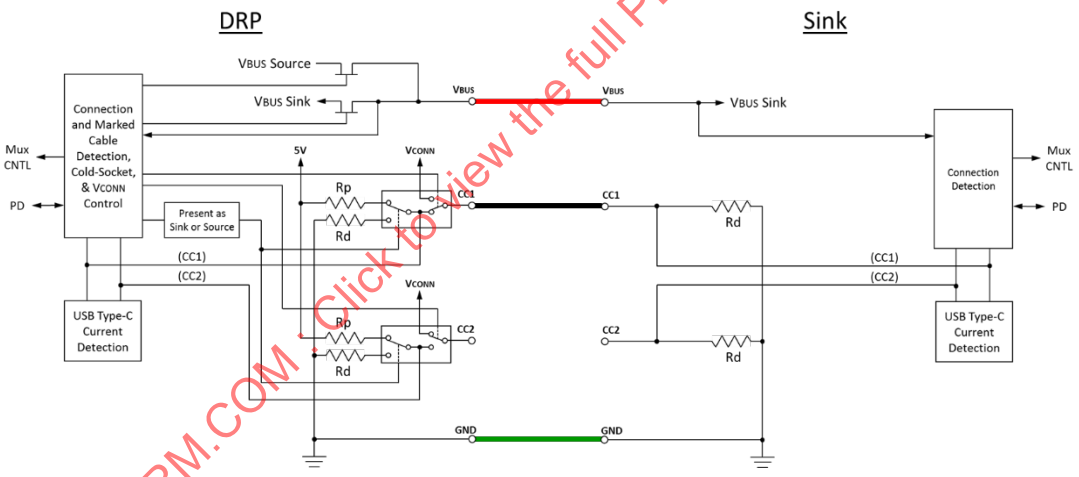
1. La source et la DRP sont débranchées:
   - La DRP alterne entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***.
2. La source passe de l'état ***Unattached.SRC*** à l'état ***Attached.SRC***, en passant par l'état ***AttachWait.SRC***.
   - La source détecte la dépolarisation de la DRP sur la broche CC et passe à l'état ***AttachWait.SRC***. À l'issue du délai ***tCCDebounce***, elle passe à l'état ***Attached.SRC***.
   - La source active VBUS et VCONN.

3. La DRP passe de l'état ***Unattached.SNK*** à l'état ***Attached.SNK*** en passant par l'état ***AttachWait.SNK***.
    - La DRP à l'état ***Unattached.SNK*** détecte la polarisation sur la broche CC et passe à l'état ***AttachWait.SNK***. Après être restée dans cet état pendant le délai ***tCCDebounce*** et détection de la VBUS, elle passe à l'état ***Attached.SNK***.
4. Lorsque la source et la DRP se trouvent dans leurs états de connexion respectifs:
    - La source ajuste la ***Rp*** en fonction des besoins, afin de limiter le courant qui ***peut*** être puisé par la DRP (en tant que destinataire).
    - La DRP (en tant que destinataire) détecte et surveille ***vRd*** par rapport au courant disponible sur la VBUS.
    - La source surveille la broche CC afin de détecter un débranchement; si un débranchement est détecté, elle passe à l'état ***Unattached.SRC***.
    - La DRP (en tant que destinataire) surveille la VBUS afin de détecter un débranchement; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK*** (et recommence à alterner entre l'état ***Unattached.SNK*** et à l'état ***Unattached.SRC***).

4.5.3.1.3 Comportement DRP-destinataire

La Figure 4-25 représente le modèle fonctionnel d'une DRP branchée à un destinataire. Le fil CC unique, utilisé dans un câble normalisé, n'est représenté que pour l'un des quatre chemins de connexion possibles, CC1 à CC1.

Figure 4-25 Modèle fonctionnel d'une DRP branchée à un destinataire



Anglais	Français
DRP	DRP
Sink	Destinataire
Connection and Marked Cable Detection, Cold-Socket, & VCONN Control	Détection de connexion et de câbles marqués électroniquement, prise commutée et contrôle de VCONN
Present as Sink or Source	Source ou destinataire présent
VBUS Source	Source VBUS
VBUS Sink	Destinataire VBUS
Connection detection	Détection de connexion
USB Type-C Current Detection	Détection de courant USB Type-C

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Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une DRP est connectée à un destinataire.

1. La DRP et le destinataire sont débranchés.
    - La DRP alterne entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***.
2. La DRP passe de l'état ***Unattached.SRC*** à l'état ***AttachWait.SRC***, puis à l'état ***Attached.SRC***.
    - La DRP à l'état ***Unattached.SRC*** détecte l'une des dépolarisations du destinataire sur la broche CC qui se trouve à l'état ***Unattached.SNK*** et la DRP passe à l'état ***AttachWait.SRC***.
    - La DRP à l'état ***AttachWait.SRC*** détecte le maintien de la dépolarisation sur la broche CC pendant le délai ***tCCDebounce***. Elle passe alors à l'état ***Attached.SRC***, puis active la VBUS et la VCONN.
3. Le destinataire passe de l'état ***Unattached.SNK*** à l'état ***Attached.SNK***, en passant par l'état ***AttachWait.SNK***, si exigé:
    - Le destinataire détecte VBUS et passe à l'état ***Attached.SNK***.
4. Lorsque la DRP et le destinataire se trouvent dans leur état de connexion respectif:
    - La DRP (en tant que source) ajuste la ***Rp*** en fonction des besoins, afin de limiter le courant qui ***peut*** être puisé par le destinataire.
    - Le destinataire détecte et surveille la ***vRd*** par rapport au courant disponible sur la VBUS.
    - La DRP (en tant que source) surveille la broche CC afin de détecter un débranchement; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK*** (et recommence à alterner entre l'état ***Unattached.SNK*** et l'état ***Unattached.SRC***).
    - Le destinataire surveille la broche VBUS afin de détecter un débranchement; si un débranchement est détecté, il passe à l'état ***Unattached.SNK***.

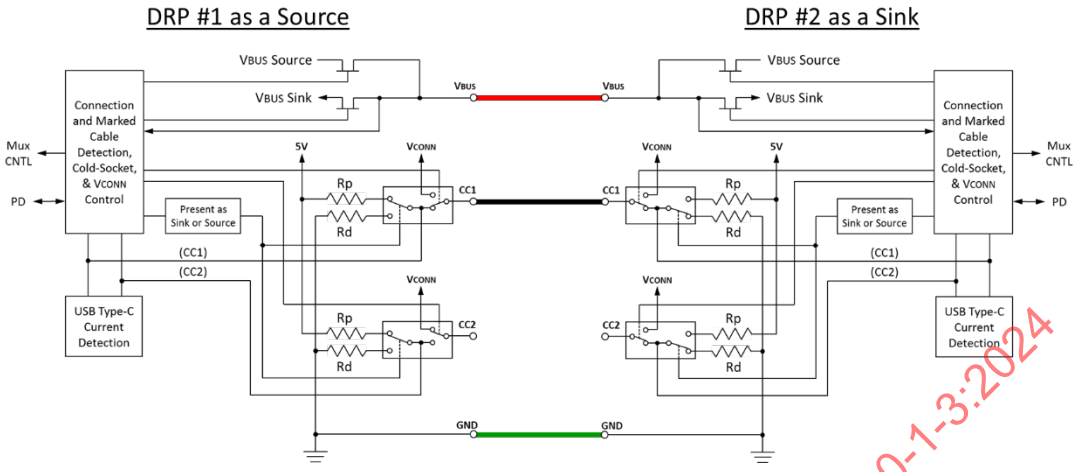
4.5.3.1.4 Comportement DRP-DRP

Les informations suivantes décrivent deux comportements issus des diagrammes d'états de connexion. Dans le premier cas, les deux DRP acceptent la relation source-destinataire obtenue de manière aléatoire; dans le second cas, la DRP n° 2 choisit d'amener le résultat aléatoire vers le résultat opposé avec le mécanisme ***Try.SRC***.

La Figure 4-26 représente le modèle fonctionnel d'une DRP connectée à une DRP dans le cadre du premier cas. Le fil CC unique, utilisé dans un câble normalisé, n'est représenté que pour l'un des quatre chemins de connexion possibles, CC1 à CC1. Sur le diagramme, les numéros de port ont été affectés de manière arbitraire afin de simplifier la compréhension du processus par le lecteur.

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Figure 4-26 Modèle fonctionnel d'une DRP branchée à une DRP – CAS n° 1



Anglais	Français
DRP #1 as a source	DRP n° 1 en tant que source
DRP #2 as a sink	DRP n° 2 en tant que destinataire
Connection and Marked Cable Detection, Cold-Socket, & VCONN Control	Détection de connexion et de câbles marqués électroniquement, prise commutée et contrôle de VCONN
Present as sink or source	Source ou destinataire présent
VBUS Source	Source VBUS
VBUS Sink	Destinataire VBUS
USB Type-C Current Detection	Détection de courant USB Type-C

CAS n° 1: Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une DRP est connectée à une autre DRP. Dans ce processus, les deux DRP acceptent la relation source-destinataire résultante obtenue de manière aléatoire.

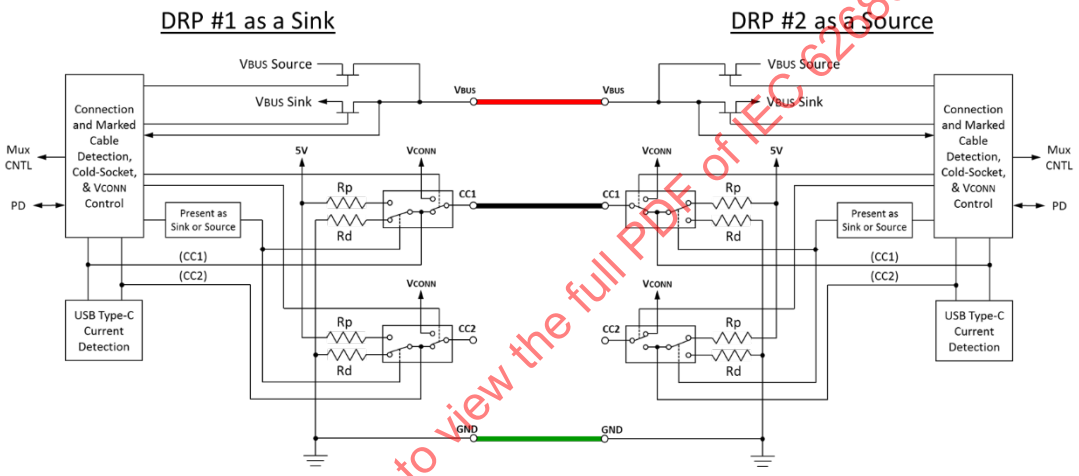
1. Les deux DRP sont débranchées.
   - La DRP n° 1 et la DRP n° 2 alternent entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***.
2. La DRP n° 1 passe de l'état ***Unattached.SRC*** à l'état ***AttachWait.SRC***.
   - La DRP n° 1 à l'état ***Unattached.SRC*** détecte la dépolarisation de la DRP n° 2 sur la broche CC à l'état ***Unattached.SNK*** et passe à l'état ***AttachWait.SRC***.
3. La DRP n° 2 passe de l'état ***Unattached.SNK*** à l'état ***AttachWait.SNK***.
   - La DRP n° 2 à l'état ***Unattached.SNK*** détecte la polarisation sur la broche CC et passe à l'état ***AttachWait.SNK***.
4. La DRP n° 1 passe de l'état ***AttachWait.SRC*** à l'état ***Attached.SRC***.
   - La DRP n °1 à l'état ***AttachWait.SRC*** constate le maintien de la dépolarisation de la DRP n° 2 sur la broche CC pendant le délai ***tCCDebounce***, passe à l'état ***Attached.SRC***, puis active VBUS et VCONN.
5. La DRP n° 2 passe de l'état ***AttachWait.SNK*** à l'état ***Attached.SNK***.
   - Après avoir été à l'état ***AttachWait.SNK*** pendant le délai ***tCCDebounce*** et après avoir détecté la VBUS, la DRP n° 2 passe à l'état ***Attached.SNK***.

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6. Lorsque les DRP se trouvent dans leurs états de connexion respectifs:
    - La DRP n° 1 (en tant que source) ajuste la ***Rp*** en fonction des besoins afin de limiter le courant qui ***peut*** être puisé par la DRP n° 2 (en tant que destinataire).
    - La DRP n° 2(en tant que destinataire) détecte et surveille ***vRd*** par rapport au courant disponible sur la VBUS.
    - La DRP n° 1 (en tant que source) surveille la broche CC afin de détecter un débranchement; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK*** (et recommence à alterner entre l'état ***Unattached.SNK*** et l'état ***Unattached.SRC***).
    - La DRP n° 2 (en tant que destinataire) surveille VBUS afin de détecter un débranchement; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK*** (et recommence à alterner entre l'état ***Unattached.SNK*** et à l'état ***Unattached.SRC***).

La Figure 4-27 représente le modèle fonctionnel d'une DRP connectée à une DRP dans le cadre du second cas.

Figure 4-27 Modèle fonctionnel d'une DRP branchée à une DRP – CAS n° 2 et 3



Anglais	Français
DRP #1 as a sink	DRP n° 1 en tant que destinataire
DRP #2 as a source	DRP n° 2 en tant que source
Connection and Marked Cable Detection, Cold-Socket, & VCONN Control	Détection de connexion et de câbles marqués électroniquement, prise commutée et contrôle de VCONN
Present as sink or source	Source ou destinataire présent
VBUS Source	Source VBUS
VBUS Sink	Destinataire VBUS
USB Type-C Current Detection	Détection de courant USB Type-C

CAS n° 2: Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une DRP est connectée à une autre DRP. Dans ce processus, la DRP n° 2 choisit d'amener le résultat aléatoire vers le résultat opposé avec le mécanisme ***Try.SRC***.

1. Les deux DRP sont débranchées.
    - La DRP n° 1 et la DRP n° 2 alternent entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***.

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2. La DRP n° 1 passe de l'état ***Unattached.SRC*** à l'état ***AttachWait.SRC***.
   - La DRP n° 1 à l'état ***Unattached.SRC*** détecte la dépolarisation de la DRP n° 2 sur la broche CC à l'état ***Unattached.SNK*** et passe à l'état ***AttachWait.SRC***.
3. La DRP n° 2 passe de l'état ***Unattached.SNK*** à l'état ***AttachWait.SNK***.
   - La DRP n° 2 à l'état ***Unattached.SNK*** détecte la polarisation sur la broche CC et passe à l'état ***AttachWait.SNK***.
4. La DRP n° 1 passe de l'état ***AttachWait.SRC*** à l'état ***Attached.SRC***.
   - La DRP n °1 à l'état ***AttachWait.SRC*** constate le maintien de la dépolarisation de la DRP n° 2 sur la broche CC pendant le délai ***tCCDebounce***, passe à l'état ***Attached.SRC***, puis active VBUS et VCONN.
5. La DRP n° 2 passe de l'état ***AttachWait.SNK*** à l'état ***Try.SRC***.
   - La DRP n° 2, à l'état ***AttachWait.SNK***, reste dans cet état pendant le délai ***tCCDebounce*** et détecte la VBUS, mais privilégie fortement le rôle de source et passe alors à l'état ***Try.SRC***.
   - La DRP n° 2 à l'état ***Try.SRC*** annonce la polarisation de la broche CC et attend.
6. La DRP n° 1 passe de l'état ***Attached.SRC*** à l'état ***Unattached.SNK***, puis à l'état ***AttachWait.SNK***.
   - La DRP n° 1, à l'état ***Attached.SRC***, ne détecte plus la dépolarisation de la DRP n° 2 sur la broche CC et passe à l'état ***Unattached.SNK***.
   - La DRP n° 1 à l'état ***Unattached.SNK*** désactive la VBUS et la VCONN, puis applique une dépolarisation sur la broche CC.
   - La DRP n° 1 à l'état ***Unattached.SNK*** détecte la polarisation sur la broche CC et passe à l'état ***AttachWait.SNK***.
7. La DRP n° 2 passe de l'état ***Try.SRC*** à l'état ***Attached.SRC***.
   - La DRP n° 2 à l'état ***Try.SRC*** détecte la dépolarisation de la DRP n° 1 sur la broche CC à l'état ***Unattached.SNK***, puis passe à l'état ***Attached.SRC***.
   - La DRP n° 2, à l'état ***Attached.SRC*** active VBUS et VCONN.
8. La DRP n° 1 passe de l'état ***AttachWait.SNK*** à l'état ***Attached.SNK***.
   - À l'issue du délai ***tCCDebounce*** et de la détection de la VBUS, la DRP n° 1 à l'état ***AttachWait.SNK*** passe à l'état ***Attached.SNK***.
9. Lorsque les DRP se trouvent dans leurs états de connexion respectifs:
   - La DRP n° 2 (en tant que source) ajuste la ***Rp*** en fonction des besoins afin de limiter le courant qui ***peut*** être puisé par la DRP n° 1 (en tant que destinataire).
   - La DRP n° 1(en tant que destinataire) détecte et surveille ***vRd*** par rapport au courant disponible sur la VBUS.
   - La DRP n° 2 (en tant que source) surveille la broche CC afin de détecter un débranchement; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK*** (et recommence à alterner entre l'état ***Unattached.SNK*** et l'état ***Unattached.SRC***).
   - La DRP n° 1 (en tant que destinataire) surveille VBUS afin de détecter un débranchement; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK*** (et recommence à alterner entre l'état ***Unattached.SNK*** et à l'état ***Unattached.SRC***).

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CAS n° 3: Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une DRP est connectée à une autre DRP. Dans ce processus, la DRP n° 1 choisit d'amener le résultat aléatoire vers le résultat opposé avec le mécanisme ***Try.SNK***.

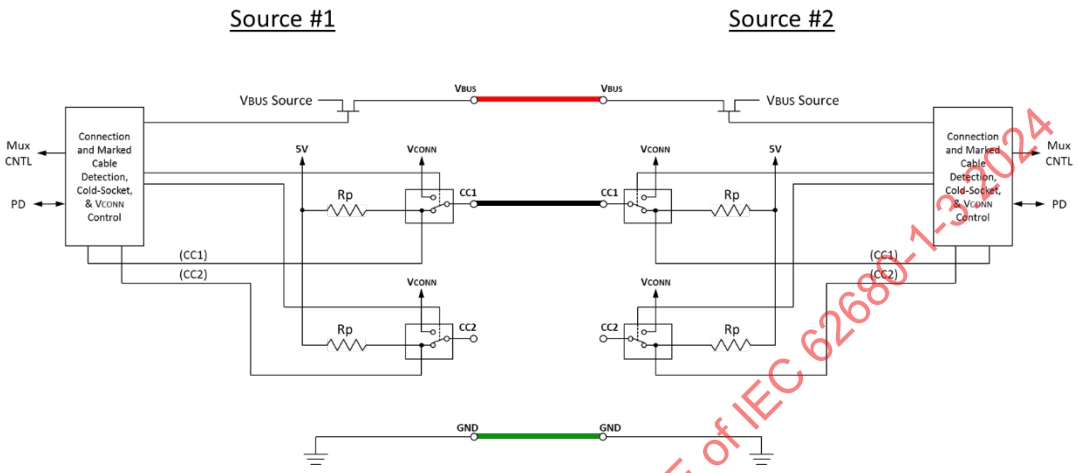
1. Les deux DRP sont débranchées.
    - La DRP n° 1 et la DRP n° 2 alternent entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***.
2. La DRP n° 1 passe de l'état ***Unattached.SRC*** à l'état ***AttachWait.SRC***.
    - La DRP n° 1 à l'état ***Unattached.SRC*** détecte la dépolarisation de la DRP n° 2 sur la broche CC à l'état ***Unattached.SNK*** et passe à l'état ***AttachWait.SRC***.
3. La DRP n° 2 passe de l'état ***Unattached.SNK*** à l'état ***AttachWait.SNK***.
    - La DRP n° 2 à l'état ***Unattached.SNK*** détecte la polarisation sur la broche CC et passe à l'état ***AttachWait.SNK***.
4. La DRP n° 1 passe de l'état ***AttachWait.SRC*** à l'état ***Try.SNK***.
    - Après être restée à l'état ***AttachWait.SRC*** pendant le délai ***tCCDebounce***, la DRP n° 1 détecte la dépolarisation de la DRP n° 2 sur la broche CC, mais privilégie fortement le rôle de destinataire et passe alors à l'état ***Try.SNK***.
    - La DRP n° 1 à l'état ***Try.SNK*** annonce la polarisation de la broche CC et attend.
5. La DRP n° 2 passe de l'état ***AttachWait.SNK*** à l'état ***Unattached.SRC***, puis à l'état ***AttachWait.SRC***.
    - La DRP n° 2 à l'état ***AttachWait.SNK*** ne détecte plus la dépolarisation de la DRP n° 1 sur la broche CC et passe à l'état ***Unattached.SRC***.
    - La DRP n° 2 à l'état ***Unattached.SRC*** applique une polarisation sur la broche CC.
    - La DRP n° 2 à l'état ***Unattached.SRC*** détecte une dépolarisation sur la broche CC et passe à l'état ***AttachWait.SRC***.
    - La DRP n° 1 détecte la polarisation de la DRP n° 2 sur la broche CC et reste à l'état ***Try.SNK***.
6. La DRP n° 2 passe de l'état ***AttachWait.SRC*** à l'état ***Attached.SRC***.
    - La DRP n° 2, à l'état ***AttachWait.SRC***, arrive à expiration (***tCCDebounce***) et passe à l'état ***Attached.SRC***.
    - La DRP n° 2, à l'état ***Attached.SRC*** active VBUS et VCONN.
7. La DRP n° 1 passe de l'état ***Try.SNK*** à l'état ***Attached.SNK***.
    - La DRP n° 1 à l'état ***Try.SNK***, après avoir détecté la VBUS, passe à l'état ***Attached.SNK***.
8. Lorsque les DRP se trouvent dans leurs états de connexion respectifs:
    - La DRP n° 2 (en tant que source) ajuste la ***Rp*** en fonction des besoins afin de limiter le courant qui ***peut*** être puisé par la DRP n° 1 (en tant que destinataire).
    - La DRP n° 1(en tant que destinataire) détecte et surveille ***vRd*** par rapport au courant disponible sur la VBUS.
    - La DRP n° 2 (en tant que source) surveille la broche CC afin de détecter un débranchement; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK*** (et recommence à alterner entre l'état ***Unattached.SNK*** et l'état ***Unattached.SRC***).
    - La DRP n° 1 (en tant que destinataire) surveille VBUS afin de détecter un débranchement; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK*** (et recommence à alterner entre l'état ***Unattached.SNK*** et à l'état ***Unattached.SRC***).

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4.5.3.1.5 Comportement source-source

La Figure 4-28 représente le modèle fonctionnel d'une source connectée à une source. Le fil CC unique, utilisé dans un câble normalisé, n'est représenté que pour l'un des quatre chemins de connexion possibles, CC1 à CC1. Sur le diagramme, les numéros de port ont été affectés de manière arbitraire afin de simplifier la compréhension du processus par le lecteur.

Figure 4-28 Modèle fonctionnel d'une source branchée à une source



Anglais	Français
Source #	Source n°
Connection and Marked Cable Detection, Cold-Socket, & VCONN Control	Détection de connexion et de câbles marqués électroniquement, prise commutée et contrôle de VCONN
VBUS Source	Source VBUS
VBUS Sink	Destinataire VBUS

Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une source est connectée à une autre source.

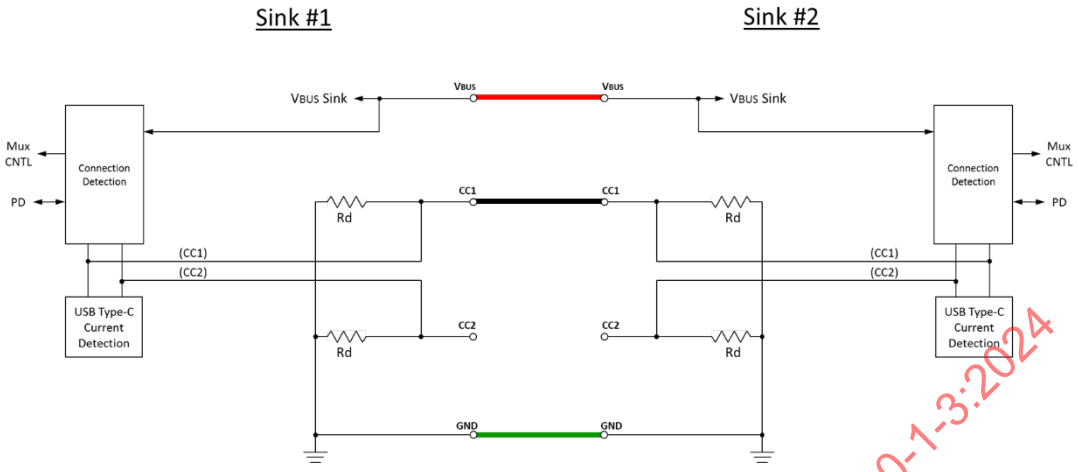
1. Les deux sources sont débranchées.
    - La source n° 1 ne parvient pas à détecter la dépolarisation du destinataire sur la broche CC et reste à l'état ***Unattached.SRC***.
    - La source n° 2 ne parvient pas à détecter la dépolarisation du destinataire sur la broche CC et reste à l'état ***Unattached.SRC***.

4.5.3.1.6 Comportement destinataire-destinataire

La Figure 4-29 représente le modèle fonctionnel d'un destinataire connecté à un destinataire. Le fil CC unique, utilisé dans un câble normalisé, n'est représenté que pour l'un des quatre chemins de connexion possibles, CC1 à CC1. Sur le diagramme, les numéros de port ont été affectés de manière arbitraire afin de simplifier la compréhension du processus par le lecteur.

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Figure 4-29 Modèle fonctionnel d'un destinataire branché à un destinataire



Anglais	Français
Sink #	Destinataire n°
VBUS Source	Source VBUS
VBUS Sink	Destinataire VBUS
Connection detection	Détection de connexion
USB Type-C Current Detection	Détection de courant USB Type-C

Les informations suivantes décrivent le comportement de l'ensemble lorsqu'un destinataire est connecté à un autre destinataire.

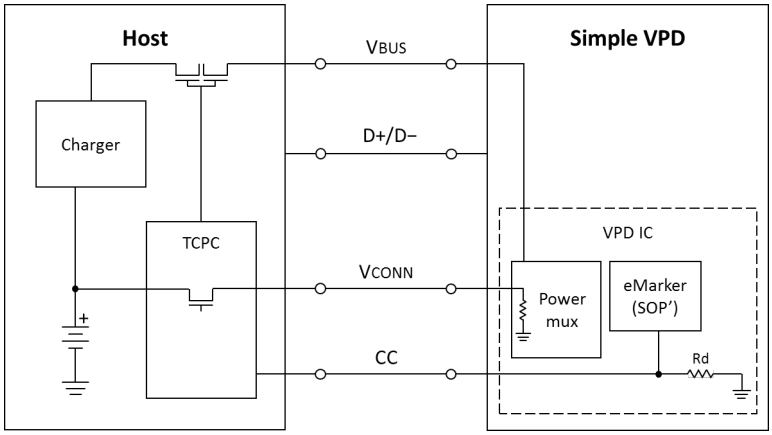
1. Les deux destinataires sont débranchés.
    - Le destinataire n° 1 ne parvient pas à détecter une polarisation sur la broche CC ou sur la broche VBUS alimentée par une source et reste à l'état ***Unattached.SNK***.
    - Le destinataire n° 2 ne parvient pas à détecter une polarisation sur la broche CC ou sur la broche VBUS alimentée par une source et reste à l'état ***Unattached.SNK***.

4.5.3.1.7 Comportement DRP-dispositif USB alimenté par VCONN (VPD)

La Figure 4-30 représente le modèle fonctionnel d'une DRP connectée à un ***dispositif USB alimenté par VCONN***, qui ne propose pas de fonctionnalité de charge.

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Figure 4-30 Modèle fonctionnel d'une DRP branchée à un VPD



Anglais	Français
Host	Hôte
Simple VPD	VPD simple
Charger	Chargeur
Power mux	Mux alimentation
eMarker (SOP')	Marqueur électronique (SOP')

Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une DRP qui prend en charge des ***VPD*** est connectée à un ***VPD***.

1. La DRP et le ***VPD*** sont débranchés.
   - La DRP alterne entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***.
2. La DRP passe de l'état ***Unattached.SRC*** à l'état ***Attached.SRC*** en passant par l'état ***AttachWait.SRC***.
   - La DRP à l'état ***Unattached.SRC*** détecte la dépolarisation du ***VPD*** sur la broche CC qui se trouve à l'état ***Unattached.SNK*** et la DRP passe à l'état ***AttachWait.SRC***.
   - La DRP à l'état ***AttachWait.SRC*** détecte le maintien de la dépolarisation sur la broche CC pendant le délai ***tCCDebounce***. Elle passe alors à l'état ***Attached.SRC***, puis active la VBUS et la VCONN.
3. Le ***VPD*** passe de l'état ***Unattached.SNK*** à l'état ***Attached.SNK*** en passant par l'état ***AttachWait.SNK***.
   - Le ***VPD*** détecte la VCONN et passe à l'état ***Attached.SNK***.
4. Lorsque la DRP et le ***VPD*** se trouvent dans leurs états de connexion respectifs, la DRP découvre le ***VPD*** et retire la VBUS.
   - La DRP (en tant que source) interroge l'identité du câble par l'***USB PD*** sur SOP'.
   - Le ***VPD*** répond sur SOP' en annonçant qu'il est un ***dispositif USB alimenté par VCONN*** qui ne prend pas en charge la fonctionnalité de charge.
   - La DRP (en tant que source) retire la VBUS.
   - La DRP (en tant que source) conserve sa ***Rp***.

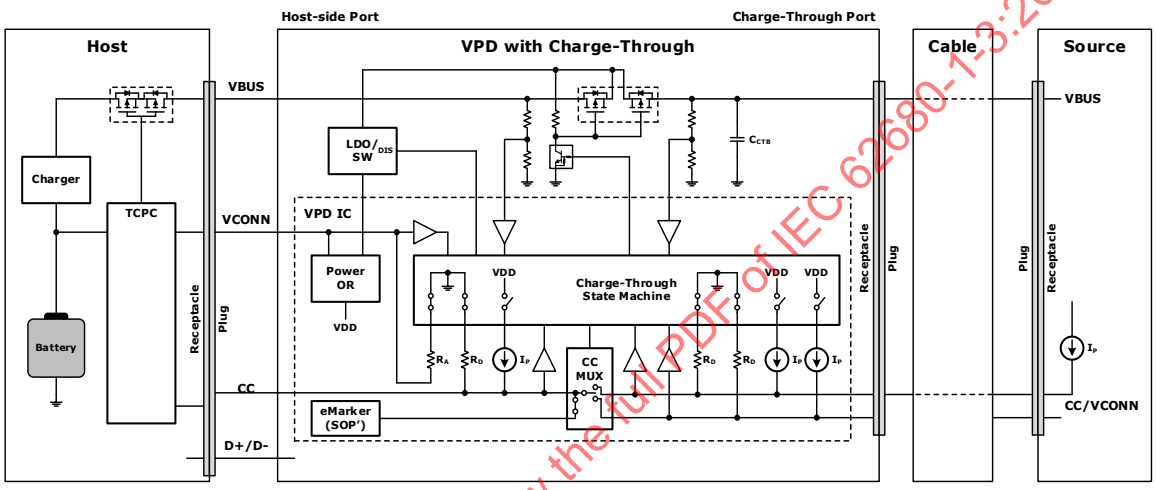
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5. La DRP et le ***VPD*** effectuent une surveillance afin de détecter un débranchement.
    - La DRP (en tant que source) surveille la broche CC afin de détecter un débranchement; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK*** (et recommence à alterner entre l'état ***Unattached.SNK*** et l'état ***Unattached.SRC***).
    - Le ***VPD*** surveille la broche VCONN afin de détecter un débranchement; si un débranchement est détecté, il passe à l'état ***Unattached.SNK***.

4.5.3.1.8 Comportement DRP-dispositif USB alimenté par VCONN de charge (CTVPD)

La Figure 4-31 représente le modèle fonctionnel d'une DRP connectée à un ***dispositif USB alimenté par VCONN de charge***, avec une source branchée au port de charge sur le ***dispositif USB alimenté par VCONN***.

Figure 4-31 Exemple de modèle de DRP-VPD de charge



Anglais	Français
Host	Hôte
Host-side port	Port côté hôte
Charge-through port	Port de charge
VPD with charge-through	VPD avec charge
Cable	Câble
Charger	Chargeur
Charge-through state machine	Diagramme d'états de charge
eMarker (SOP')	Marqueur électronique (SOP')
Battery	Batterie
Receptacle	Embase
Plug	Fiche

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CAS n° 1: Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une DRP est connectée à un ***dispositif USB alimenté par VCONN*** de charge (***CTVPD***) sans source d'alimentation branchée au port de charge sur le ***CTVPD***.

1. La DRP et le ***CTVPD*** sont débranchés.
    a. La DRP alterne entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***.

b. Le ***CTVPD*** a appliqué la ***Rd*** sur les broches CC1 et CC2 de son port de charge et la ***Rd*** sur la broche CC du port côté hôte.

2. La DRP passe de l'état ***Unattached.SRC*** à l'état ***Attached.SRC*** en passant par l'état ***AttachWait.SRC***.

   a. La DRP à l'état ***Unattached.SRC*** détecte une dépolarisation du ***CTVPD*** sur la broche CC qui se trouve à l'état ***Unattached.SNK*** et la DRP passe à l'état ***AttachWait.SRC***.

   b. La DRP à l'état ***AttachWait.SRC*** constate le maintien de la dépolarisation sur la broche CC pendant le délai ***tCCDebounce***, passe à l'état ***Attached.SRC***, puis active la VBUS et la VCONN.

3. Le ***CTVPD*** passe de l'état ***Unattached.SNK*** à l'état ***Attached.SNK*** en passant par l'état ***AttachWait.SNK***.

   a. Le ***CTVPD*** détecte la polarisation de la broche CC côté hôte de la DRP et le ***CTVPD*** passe à l'état ***AttachWait.SNK***.

   b. Le ***CTVPD*** à l'état ***AttachWait.SNK*** constate le maintien de la polarisation de la broche CC du port côté hôte pendant le délai ***tCCDebounce***, détecte la présence de VCONN et passe à l'état ***Attached.SNK***.

   c. Le ***CTVPD*** présente une impédance de mise à la masse élevée (supérieure à ***zOPEN***) sur les broches CC1 et CC2 de son port de charge.

4. Lorsque la DRP et le ***CTVPD*** se trouvent dans leurs états de connexion respectifs, la DRP découvre le ***CTVPD*** et passe à l'état ***CTUnattached.SNK***.

   a. La DRP (en tant que source) interroge l'identité du dispositif par l'***USB PD*** (commande de découverte d'identité de dispositif) sur SOP'.

   b. Le ***CTVPD*** répond sur SOP' en annonçant qu'il est un ***dispositif USB alimenté par VCONN de charge***.

   c. La DRP (en tant que source) retire la VBUS.

   d. La DRP (en tant que source) modifie sa ***Rp*** par une ***Rd***.

   e. La DRP (en tant que destinataire) continue à fournir VCONN et passe à l'état ***CTUnattached.SNK***.

5. Le ***CTVPD*** passe à l'état ***CTUnattached.VPD***.

   a. Le ***CTVPD*** détecte le retrait de la VBUS, la présence de la VCONN et la faible tension de la broche CC côté hôte, et passe à l'état ***CTUnattached.VPD***.

   b. Le ***CTVPD*** modifie sa ***Rd*** côté hôte en une ***Rp*** annonçant 3,0 A.

   c. Le ***CTVPD*** s'isole de VBUS.

   d. Le ***CTVPD*** applique la ***Rd*** sur les broches CC1 et CC2 de son port de charge.

6. Lorsque le ***CTVPD*** est à l'état ***CTUnattached.VPD*** et la DRP à l'état ***CTUnattached.SNK***:

   a. Le ***CTVPD*** surveille les broches CC de charge pour détecter une source ou un destinataire; lorsqu'une connexion de source d'alimentation est détectée, il passe à l'état ***CTAttachWait.VPD***; lorsqu'un destinataire est détecté, il passe à l'état ***CTAttachWait.Unsupported***.

   b. Le ***CTVPD*** surveille la broche VCONN afin de détecter un débranchement de l'hôte; si un débranchement est détecté, il passe à l'état ***Unattached.SNK***.

   c. La DRP surveille la broche VBUS et la broche CC afin de détecter une déconnexion du ***CTVPD*** pendant le délai ***tVPDDetach***; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK***.

   d. La DRP surveille la broche VBUS afin de détecter une connexion de la source d'alimentation; en cas de déconnexion détectée, elle passe à l'état ***CTAttached.SNK***.

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CAS n° 2: Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une source d'alimentation est connectée à un ***dispositif USB alimenté par VCONN*** de charge (***CTVPD***), avec un hôte déjà branché au port côté hôte sur le ***CTVPD***.

1. La DRP est à l'état ***CTUnattached.SNK***, le ***CTVPD*** est à l'état ***CTUnattached.VPD*** et la source d'alimentation est débranchée:
    a. Le ***CTVPD*** a appliqué la ***Rd*** sur les broches CC1 et CC2 du port de charge et la terminaison ***Rp*** qui annonce 3,0 A sur la broche CC du port côté hôte.
2. La source d'alimentation passe de l'état ***Unattached.SRC*** à l'état ***Attached.SRC***, en passant par l'état ***AttachWait.SRC***.
    a. La source d'alimentation détecte la dépolarisation du ***CTVPD*** sur la broche CC et passe à l'état ***AttachWait.SRC***.
    b. La source d'alimentation à l'état ***AttachWait.SRC*** constate le maintien de la dépolarisation sur la broche CC pendant le délai ***tCCDebounce***, passe à l'état ***Attached.SRC*** et active VBUS.
3. Le ***CTVPD*** passe de l'état ***CTUnattached.VPD*** à ***CTAttachWait.VPD*** en passant par l'état ***CTAttached.VPD***.
    a. Le ***CTVPD*** détecte la ***Rp*** de la source sur l'une de ses broches CC de charge et passe à l'état ***CTAttachWait.VPD***.
    b. Le ***CTVPD*** termine toute communication ***USB PD*** active sur SOP' et cesse de répondre aux requêtes SOP'.
    c. Le ***CTVPD*** à l'état ***CTAttachWait.VPD*** constate le maintien de la polarisation sur la broche CC de charge pendant le délai ***tCCDebounce***, détecte VBUS et passe à l'état ***CTAttached.VPD***.
    d. Le ***CTVPD*** connecte la broche CC de charge active à la broche CC du port côté hôte.
    e. Le ***CTVPD*** désactive sa terminaison ***Rp*** qui annonce 3,0 A sur la broche CC du port côté hôte.
    f. Le ***CTVPD*** désactive sa ***Rd*** sur les broches CC de charge.
    g. Le ***CTVPD*** connecte VBUS du côté charge au côté hôte.
4. La DRP (en tant que destinataire) passe à l'état ***CTAttached.SNK***.
    a. La DRP (en tant que destinataire) détecte la VBUS, surveille la ***vRd*** par rapport au courant disponible et passe à l'état ***CTAttached.SNK***.
5. Lorsque les dispositifs se trouvent dans leurs états de connexion respectifs:
    a. Le ***CTVPD*** surveille la broche VCONN afin de détecter un débranchement de l'hôte de la DRP; si un débranchement est détecté, il passe à l'état ***CTDisabled.VPD***.
    b. Le ***CTVPD*** surveille la broche VBUS et la broche CC afin de détecter un débranchement de la source d'alimentation; si un débranchement est détecté, il passe à l'état ***CTUnattached.VPD*** dans le délai ***tVPDCTDD***.
    c. La DRP (en tant que destinataire) surveille la broche VBUS afin de détecter un débranchement de la source d'alimentation de charge; si un débranchement est détecté, elle passe à l'état ***CTUnattached.SNK***.
    d. La DRP (en tant que destinataire) surveille la broche Vbus et la broche CC afin de détecter un débranchement du ***CTVPD***; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK*** (et recommence à alterner entre l'état ***Unattached.SNK*** et à l'état ***Unattached.SRC***).
    e. La source d'alimentation surveille la broche CC afin de détecter un débranchement du ***CTVPD***; si un débranchement est détecté, elle passe à l'état ***Unattached.SRC***.

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CAS n° 3: Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une source d'alimentation est connectée à un ***dispositif USB alimenté par VCONN*** de charge (***CTVPD***), sans hôte branché au port côté hôte sur le ***CTVPD***.

1. Le ***CTVPD*** et la source d'alimentation sont débranchés.
    a. Le ***CTVPD*** a appliqué la ***Rd*** sur les broches CC1 et CC2 de son port de charge et la ***Rd*** sur la broche CC du port côté hôte.
2. La source d'alimentation passe de l'état ***Unattached.SRC*** à l'état ***Attached.SRC***, en passant par l'état ***AttachWait.SRC***.
    a. La source d'alimentation détecte la dépolarisation du ***CTVPD*** sur la broche CC et passe à l'état ***AttachWait.SRC***.
    b. La source d'alimentation à l'état ***AttachWait.SRC*** constate le maintien de la dépolarisation sur la broche CC pendant le délai ***tCCDebounce***, passe à l'état ***Attached.SRC*** et active VBUS.
3. La ***CTVPD*** alterne entre l'état ***Unattached.SNK*** et l'état ***Unattached.SRC***.
    a. La ***CTVPD*** détecte la ***Rp*** de la source sur l'une de ses broches CC de charge, détecte VBUS pendant le délai ***tCCDebounce***, puis commence à alterner entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***.
4. Lorsque le ***CTVPD*** alterne entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***, et que la source d'alimentation est à l'état ***Attached.SRC***:
    a. Le ***CTVPD*** surveille la broche CC du port côté hôte afin de détecter une connexion de dispositif; en cas de connexion détectée, il passe à l'état ***AttachWait.SRC***.
    b. Le ***CTVPD*** surveille la broche VBUS afin de détecter un débranchement de la source d'alimentation; si un débranchement est détecté, il passe à l'état ***Unattached.SNK***.
    c. La source d'alimentation surveille la broche CC afin de détecter un débranchement du ***CTVPD***; si un débranchement est détecté, elle passe à l'état ***Unattached.SRC***.

CAS n° 4: Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une DRP est connectée à un ***dispositif USB alimenté par VCONN*** de charge (***CTVPD***) avec une source d'alimentation déjà branchée au côté charge sur le ***CTVPD***.

1. La DRP et le ***CTVPD*** sont débranchés et la source d'alimentation est à l'état ***Attached.SRC***.
    a. La DRP alterne entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***.
    b. Le ***CTVPD*** alterne entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***.
    c. Le ***CTVPD*** a appliqué la ***Rd*** sur les broches CC1 et CC2 de son port de charge.
    d. La source d'alimentation a appliqué la VBUS.
2. La DRP passe de l'état ***Unattached.SNK*** à l'état ***AttachWait.SNK***.
    a. La DRP à l'état ***Unattached.SNK*** détecte la polarisation du ***CTVPD*** sur la broche CC qui se trouve à l'état ***Unattached.SRC*** et la DRP passe à l'état ***AttachWait.SNK***.
3. Le ***CTVPD*** passe de l'état ***Unattached.SRC*** à l'état ***Try.SNK*** en passant par l'état ***AttachWait.SRC***.
    a. Le ***CTVPD*** à l'état ***Unattached.SRC*** détecte la dépolarisation de la DRP sur la broche CC qui se trouve à l'état ***Unattached.SNK*** et le ***CTVPD*** passe à l'état ***AttachWait.SRC***.
    b. Le ***CTVPD*** à l'état ***AttachWait.SRC*** constate le maintien de la dépolarisation sur la broche CC pendant le délai ***tCCDebounce*** et passe à l'état ***Try.SNK***.
    c. Le ***CTVPD*** désactive la terminaison ***Rp*** qui annonce la puissance USB par défaut sur la broche CC du port côté hôte.
    d. Le ***CTVPD*** active la ***Rd*** sur la broche CC du port côté hôte.

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4. La DRP passe de l'état ***AttachWait.SNK*** à l'état ***Attached.SRC*** en passant par l'état ***Unattached.SRC*** et l'état ***AttachWait.SRC***.
    a. La DRP à l'état ***AttachWait.SNK*** détecte le retrait de la polarisation du ***CTVPD*** sur la broche CC qui se trouve à l'état ***Try.SNK*** et la DRP passe à l'état ***Unattached.SRC***.
    b. La DRP à l'état ***Unattached.SRC*** détecte la dépolarisation du ***CTVPD*** sur la broche CC qui se trouve à l'état ***Try.SNK*** et la DRP passe à l'état ***AttachWait.SRC***.
    c. La DRP à l'état ***AttachWait.SRC*** détecte le maintien de la dépolarisation sur la broche CC pendant le délai ***tCCDebounce***. Elle passe alors à l'état ***Attached.SRC***, puis active VBUS et VCONN.
5. Le ***CTVPD*** passe de l'état ***Try.SNK*** à l'état ***Attached.SNK***.
    a. Le ***CTVPD*** constate le maintien de la polarisation de la DRP sur la broche CC pendant le délai ***tTryCCDebounce***.
    b. Le ***CTVPD*** détecte la VBUS sur le port côté hôte et passe à l'état ***Attached.SNK***.
6. Lorsque la DRP et le ***CTVPD*** se trouvent dans leurs états de connexion respectifs, la DRP découvre le ***CTVPD*** de charge et passe à l'état ***CTUnattached.SNK***.
    a. La DRP (en tant que source) interroge l'identité du dispositif par l'***USB PD*** (commande de ***découverte d'identité***) sur SOP'.
    b. Le ***CTVPD*** répond sur SOP' en annonçant qu'il est un ***dispositif USB alimenté par VCONN de charge***.
    c. La DRP (en tant que source) retire la VBUS.
    d. La DRP (en tant que source) modifie sa ***Rp*** par une ***Rd***.
    e. La DRP (en tant que destinataire) continue à fournir VCONN et passe à l'état ***CTUnattached.SNK***.
7. Le ***CTVPD*** passe à l'état ***CTUnattached.VPD***.
    a. Le ***CTVPD*** détecte le retrait de VBUS, la présence de VCONN et la faible tension de la broche CC de son port hôte, et passe à l'état ***CTUnattached.VPD***.
    b. Le ***CTVPD*** modifie sa ***Rd*** côté hôte en une terminaison ***Rp*** annonçant 3,0 A.
    c. Le ***CTVPD*** s'isole de VBUS.
8. Le ***CTVPD*** passe de l'état ***CTUnattached.VPD*** à ***CTAttachWait.VPD*** en passant par l'état ***CTAttached.VPD***.
    a. Le ***CTVPD*** détecte la ***Rp*** de la source sur l'une de ses broches CC de charge et passe à l'état ***CTAttachWait.VPD***.
    b. Le ***CTVPD*** à l'état ***CTAttachWait.VPD*** constate le maintien de la polarisation sur la broche CC de charge pendant le délai ***tCCDebounce***, détecte VBUS et passe à l'état ***CTAttached.VPD***.
    c. Le ***CTVPD*** termine toute communication ***USB PD*** active sur SOP' et cesse de répondre aux requêtes SOP'.
    d. Le ***CTVPD*** connecte la broche CC de charge active à la broche CC du port côté hôte.
    e. Le ***CTVPD*** désactive sa terminaison ***Rp*** qui annonce 3,0 A sur la broche CC du port côté hôte.
    f. Le ***CTVPD*** désactive sa ***Rd*** sur les broches CC de charge.
    g. Le ***CTVPD*** connecte VBUS du côté charge au côté hôte.
9. La DRP (en tant que destinataire) passe à l'état ***CTAttached.SNK***.
    a. La DRP (en tant que destinataire) détecte la VBUS et surveille la ***vRd*** par rapport au courant disponible et passe à l'état ***CTAttached.SNK***.

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10. Lorsque les dispositifs se trouvent dans leurs états de connexion respectifs:
    a. Le ***CTVPD*** surveille la broche VCONN afin de détecter un débranchement de l'hôte de la DRP; si un débranchement est détecté, il passe à l'état ***CTDisabled.VPD***.
    b. Le ***CTVPD*** surveille la broche VBUS et la broche CC afin de détecter un débranchement de la source d'alimentation; si un débranchement est détecté, il passe à l'état ***CTUnattached.VPD*** dans le délai ***tVPDCTDD***.
    c. La DRP (en tant que destinataire) surveille la broche VBUS afin de détecter un débranchement de la source d'alimentation de charge; si un débranchement est détecté, elle passe à l'état ***CTUnattached.SNK***.
    d. La DRP (en tant que destinataire) surveille la broche Vbus et la broche CC afin de détecter un débranchement du ***CTVPD***; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK*** (et recommence à alterner entre l'état ***Unattached.SNK*** et à l'état ***Unattached.SRC***).
    e. La source d'alimentation surveille la broche CC afin de détecter un débranchement du ***CTVPD***; si un débranchement est détecté, elle passe à l'état ***Unattached.SRC***.

CAS n° 5: Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une source d'alimentation est connectée à un ***dispositif USB alimenté par VCONN*** de charge (***CTVPD***), avec une DRP (dont la batterie est déchargée) branchée au port côté hôte sur le ***CTVPD***.

1. La DRP, le ***CTVPD*** et la source d'alimentation sont débranchés.
    a. La DRP applique la ***Rd*** de la batterie déchargée.
    b. Le ***CTVPD*** applique la ***Rd*** sur les broches CC1 et CC2 du port de charge et la ***Rd*** sur la broche CC du port côté hôte.
2. La source d'alimentation passe de l'état ***Unattached.SRC*** à l'état ***Attached.SRC***, en passant par l'état ***AttachWait.SRC***.
    a. La source d'alimentation détecte la dépolarisation du ***CTVPD*** sur la broche CC et passe à l'état ***AttachWait.SRC***.
    b. La source d'alimentation à l'état ***AttachWait.SRC*** constate le maintien de la dépolarisation sur la broche CC pendant le délai ***tCCDebounce***, passe à l'état ***Attached.SRC*** et active VBUS.
3. La ***CTVPD*** alterne entre l'état ***Unattached.SNK*** et l'état ***Unattached.SRC***.
    a. La ***CTVPD*** détecte la ***Rp*** de la source sur l'une de ses broches CC de charge, détecte VBUS pendant le délai ***tCCDebounce***, puis commence à alterner entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***.
4. Le ***CTVPD*** passe de l'état ***Unattached.SRC*** à l'état ***Try.SNK*** en passant par l'état ***AttachWait.SRC***.
    a. Le ***CTVPD*** à l'état ***Unattached.SRC*** détecte la dépolarisation de la DRP sur la broche CC qui se trouve à l'état ***Unattached.SNK*** et le ***CTVPD*** passe à l'état ***AttachWait.SRC***.
    b. Le ***CTVPD*** à l'état ***AttachWait.SRC*** constate le maintien de la dépolarisation sur la broche CC pendant le délai ***tCCDebounce*** et passe à l'état ***Try.SNK***.
    c. Le ***CTVPD*** désactive la terminaison ***Rp*** qui annonce la puissance USB par défaut sur la broche CC du port côté hôte.
    d. Le ***CTVPD*** active la ***Rd*** sur la broche CC du port côté hôte.
5. La DRP dont la batterie est déchargée reste à l'état ***Unattached.SNK***.
6. Le ***CTVPD*** passe de l'état ***Try.SNK*** à l'état ***Attached.SRC*** en passant par l'état ***TryWait.SRC***.
    a. Le ***CTVPD*** n'a pas détecté la polarisation de la DRP sur la broche CC pendant le délai ***tTryCCDebounce***, à l'issue du délai ***tDRPTry***, et passe à l'état ***TryWait.SRC***.
    b. Le ***CTVPD*** désactive la ***Rp*** sur la broche CC du port côté hôte.

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c. Le ***CTVPD*** active la terminaison ***Rp*** qui annonce la puissance USB par défaut sur la broche CC du port côté hôte.

d. Le ***CTVPD*** détecte la dépolarisation de la DRP sur la broche CC pendant le délai ***tTryCCDebounce*** et passe à l'état ***Attached.SRC***.

e. Le ***CTVPD*** connecte VBUS du côté charge au côté hôte.

7. La DRP passe de l'état ***Unattached.SNK*** à l'état ***Attached.SNK*** en passant par l'état ***AttachWait.SNK***.

a. La DRP à l'état ***Unattached.SNK*** détecte la polarisation du ***CTVPD*** sur la broche CC qui se trouve à l'état ***Attached.SRC*** et la DRP passe à l'état ***AttachWait.SNK***.

b. La DRP à l'état ***AttachWait.SNK*** constate le maintien de la polarisation de la broche CC pendant le délai ***tCCDebounce***, détecte la présence de la VBUS et passe à l'état ***Attached.SNK***.

8. Lorsque les dispositifs se trouvent dans leurs états de connexion respectifs:

a. Le ***CTVPD*** surveille la broche CC du port côté hôte afin de détecter une connexion de dispositif; en cas de connexion détectée, il passe à l'état ***Unattached.SNK***.

b. Le ***CTVPD*** surveille la broche VBUS afin de détecter un débranchement de la source d'alimentation; si un débranchement est détecté, il passe à l'état ***Unattached.SNK***.

c. La source d'alimentation surveille la broche CC afin de détecter un débranchement du ***CTVPD***; si un débranchement est détecté, elle passe à l'état ***Unattached.SRC***.

d. La DRP surveille la broche VBUS afin de détecter un débranchement du ***CTVPD***; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK***.

e. De plus, la DRP ***peut*** interroger l'identité du câble par l'***USB PD*** sur SOP'; lorsqu'elle dispose d'une batterie suffisante et lorsqu'un VPD de charge est identifié, elle passe à l'état ***TryWait.SRC*** si mis en œuvre ou à l'état ***Unattached.SRC*** lorsque l'état ***TryWait.SRC*** n'est pas pris en charge.

CAS n° 6: Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une DRP est connectée à un ***dispositif USB alimenté par VCONN*** de charge (***CTVPD***) avec un destinataire branché au port de charge sur le ***CTVPD***.

1. La DRP, le ***CTVPD*** et le destinataire sont débranchés.

a. La DRP alterne entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***.

b. Le ***CTVPD*** a appliqué la ***Rd*** sur les broches CC1 et CC2 de son port de charge et la ***Rd*** sur la broche CC du port côté hôte.

2. La DRP passe de l'état ***Unattached.SRC*** à l'état ***Attached.SRC*** en passant par l'état ***AttachWait.SRC***.

a. La DRP à l'état ***Unattached.SRC*** détecte la dépolarisation du ***CTVPD*** sur la broche CC qui se trouve à l'état ***Unattached.SNK*** et la DRP passe à l'état ***AttachWait.SRC***.

b. La DRP à l'état ***AttachWait.SRC*** détecte le maintien de la dépolarisation sur la broche CC pendant le délai ***tCCDebounce***. Elle passe alors à l'état ***Attached.SRC***, puis active VBUS et VCONN.

3. Le ***CTVPD*** passe de l'état ***Unattached.SNK*** à l'état ***Attached.SNK*** en passant par l'état ***AttachWait.SNK***.

a. Le ***CTVPD*** détecte la polarisation de la broche CC côté hôte de la DRP et le ***CTVPD*** passe à l'état ***AttachWait.SNK***.

b. Le ***CTVPD*** à l'état ***AttachWait.SNK*** constate le maintien de la polarisation de la broche CC du port côté hôte pendant le délai ***tCCDebounce***, détecte la présence de VCONN et passe à l'état ***Attached.SNK***.

c. Le ***CTVPD*** présente une impédance de mise à la masse élevée (supérieure à ***zOPEN***) sur les broches CC1 et CC2 de son port de charge.

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4. Lorsque la DRP et le ***CTVPD*** se trouvent dans leurs états de connexion respectifs, la DRP découvre le ***CTVPD*** de charge et passe à l'état ***CTUnattached.SNK***.
    a. La DRP (en tant que source) interroge l'identité du dispositif par l'***USB PD*** (commande de ***découverte d'identité***) sur SOP'.
    b. Le ***CTVPD*** répond sur SOP' en annonçant qu'il est un ***dispositif USB alimenté par VCONN de charge***.
    c. La DRP (en tant que source) retire la VBUS.
    d. La DRP (en tant que source) modifie sa ***Rp*** par une ***Rd***.
    e. La DRP (en tant que destinataire) continue à fournir VCONN et passe à l'état ***CTUnattached.SNK***.
5. Le ***CTVPD*** passe à l'état ***CTUnattached.VPD***.
    a. Le ***CTVPD*** détecte le retrait de VBUS, la présence de VCONN et la faible tension de la broche CC de son port hôte, et passe à l'état ***CTUnattached.VPD***.
    b. Le ***CTVPD*** modifie sa ***Rd*** côté hôte en une terminaison ***Rp*** annonçant 3,0 A.
    c. Le ***CTVPD*** s'isole de VBUS.
    d. Le ***CTVPD*** applique la ***Rd*** sur les broches CC1 et CC2 de son port de charge.
6. Le ***CTVPD*** alterne entre l'état ***CTUnattached.VPD*** et l'état ***CTUnattached.Unsupported***.
    a. Le ***CTVPD*** détecte l'état ***SRC.Open*** sur ses broches CC de charge et commence à alterner entre l'état ***CTUnattached.VPD*** et l'état ***CTUnattached.Unsupported***.
7. Le ***CTVPD*** passe de l'état ***CTUnattached.Unsupported*** à l'état ***CTTry.SNK*** en passant par l'état ***CTAttachWait.Unsupported***.
    a. Le ***CTVPD*** à l'état ***CTUnattached.Unsupported*** détecte la dépolarisation du destinataire sur la broche CC qui se trouve à l'état ***Unattached.SNK*** et le ***CTVPD*** passe à l'état ***CTAttachWait.Unsupported***.
    b. Le ***CTVPD*** à l'état ***CTAttachWait.Unsupported*** constate le maintien de la dépolarisation sur la broche CC pendant le délai ***tCCDebounce*** et passe à l'état ***CTTry.SNK***.
    c. Le ***CTVPD*** désactive la terminaison ***Rp*** qui annonce la puissance USB par défaut sur les broches CC du port de charge.
    d. Le ***CTVPD*** active la ***Rd*** sur les broches CC du port de charge.
8. Le ***CTVPD*** passe de l'état ***CTTry.SNK*** à l'état ***CTAttached.Unsupported***.
    a. Le ***CTVPD*** n'a pas détecté la polarisation de la source potentielle sur la broche CC pendant le délai ***tDRPTryWait***, à l'issue du délai ***tDRPTry***, et passe à l'état ***CTAttached.Unsupported***.
9. Lorsque le ***CTVPD*** est à l'état ***CTAttached.Unsupported***, la DRP à l'état ***CTUnattached.SNK*** et le destinataire à l'état ***Unattached.SNK***.
    a. Le ***CTVPD*** désactive la terminaison ***Rd*** sur les broches CC du port de charge et applique la terminaison ***Rp*** qui annonce la puissance USB par défaut.
    b. Le ***CTVPD*** expose une interface ***USB Billboard Device Class*** pour indiquer à la DRP qu'il est connecté à un dispositif non pris en charge sur son port en charge simultanée.
    c. Le ***CTVPD*** surveille les broches CC de charge afin de détecter un débranchement du destinataire; si un débranchement est détecté, il passe à l'état ***CTUnattached.VPD***.
    d. Le ***CTVPD*** surveille la broche VCONN afin de détecter un débranchement de l'hôte; si un débranchement est détecté, il passe à l'état ***Unattached.SNK***.
    e. La DRP surveille la broche CC afin de détecter une déconnexion du ***CTVPD*** pendant le délai ***tVPDDetach***; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK***.

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f. La DRP surveille la broche VBUS afin de détecter un branchement de la source du ***CTVPD***; en cas de déconnexion détectée, elle passe à l'état ***CTAttached.SNK***.

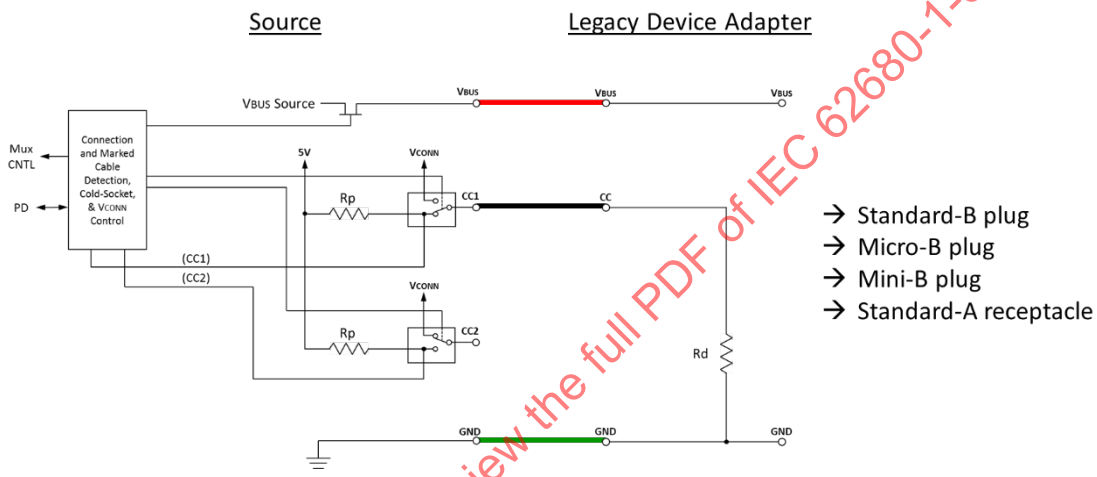
4.5.3.2 Comportements d'interopérabilité entre les ports USB Type-C et les ports USB existants

Les paragraphes suivants décrivent les comportements d'interopérabilité entre deux ports pour les différentes combinaisons de source, de destinataire et de DRP USB Type-C avec un port USB existant.

4.5.3.2.1 Comportement source-port de dispositif existant

La Figure 4-32 représente le modèle fonctionnel d'une source connectée à un port de dispositif existant. Ce modèle repose sur la présence d'un adaptateur comme destinataire de la source. Cet adaptateur est équipé d'une fiche USB Type-C sur une extrémité branchée à la source et d'une fiche USB Standard-B, d'une fiche USB Micro-B, d'une fiche USB Mini-B ou d'une embase USB Standard-A sur l'autre extrémité.

Figure 4-32 Modèle fonctionnel d'une source branchée à un port de dispositif existant



Anglais	Français
Source	Source
Legacy Device Adapter	Adaptateur pour dispositif existant
VBUS Source	Source VBUS
Connection and Marked Cable Detection, Cold-Socket, & VCONN Control	Détection de connexion et de câbles marqués électroniquement, prise commutée et contrôle de VCONN
Standard-B plug	Fiche Standard-B
Micro-B plug	Fiche Micro-B
Mini-B plug	Fiche Mini-B
Standard-A receptacle	Embase Standard-A

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Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une source est connectée à un adaptateur de dispositif existant, équipé d'une ***Rd*** à la masse destinée à reproduire le comportement d'un destinataire.

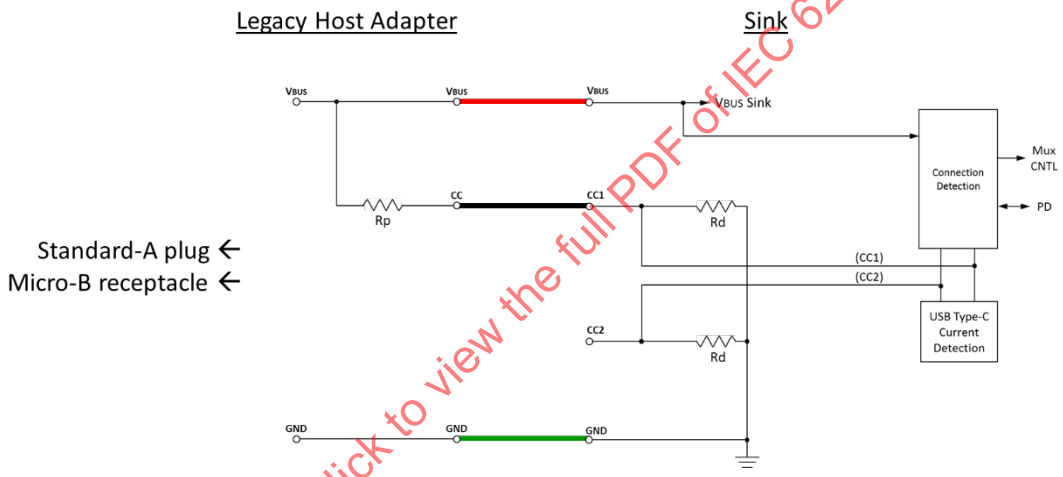
1. La source est débranchée.

2. La source passe de l'état ***Unattached.SRC*** à l'état ***Attached.SRC***, en passant par l'état ***AttachWait.SRC***.
   - La source détecte la dépolarisation du Destinataire sur la broche CC et passe à l'état ***AttachWait.SRC***. À l'issue du délai ***tCCDebounce***, elle passe à l'état ***Attached.SRC***.
   - La source active VBUS et VCONN.
3. Lorsque la source est branchée:
   - La source surveille la broche CC afin de détecter un débranchement; si un débranchement est détecté, elle passe à l'état ***Unattached.SRC***.

4.5.3.2.2 Comportement port hôte existant-destinataire

La Figure 4-33 représente le modèle fonctionnel d'un port hôte existant connecté à un destinataire. Ce modèle repose sur la présence d'un adaptateur comme source du destinataire. Cet adaptateur est équipé d'une fiche USB Standard-A existante ou d'une embase USB Micro-B existante sur une extrémité et d'une fiche USB Type-C sur l'autre extrémité branchée au destinataire.

Figure 4-33 Modèle fonctionnel d'un port hôte existant branché à un destinataire



Anglais	Français
Legacy Host Adapter	Adaptateur pour hôte existant
Sink	Destinataire
VBUS Sink	Destinataire VBUS
Connection Detection	Détection de connexion
USB Type-C Current Detection	Détection de courant USB Type-C
Standard-A plug	Fiche Standard-A
Micro-B receptacle	Embase Micro-B

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Les informations suivantes décrivent le comportement de l'ensemble lorsqu'un adaptateur hôte existant, équipé d'une ***Rp*** dont la VBUS est destinée à reproduire le comportement d'une source, est connecté à un destinataire. La valeur de la ***Rp*** ***doit*** annoncer la puissance USB par défaut (voir le Tableau 4-27), y compris si le câble peut transporter un courant de 3 A. En effet, le câble ne connaît pas les capacités de la source d'alimentation et tout courant supérieur est négocié par l'***USB BC 1.2***.

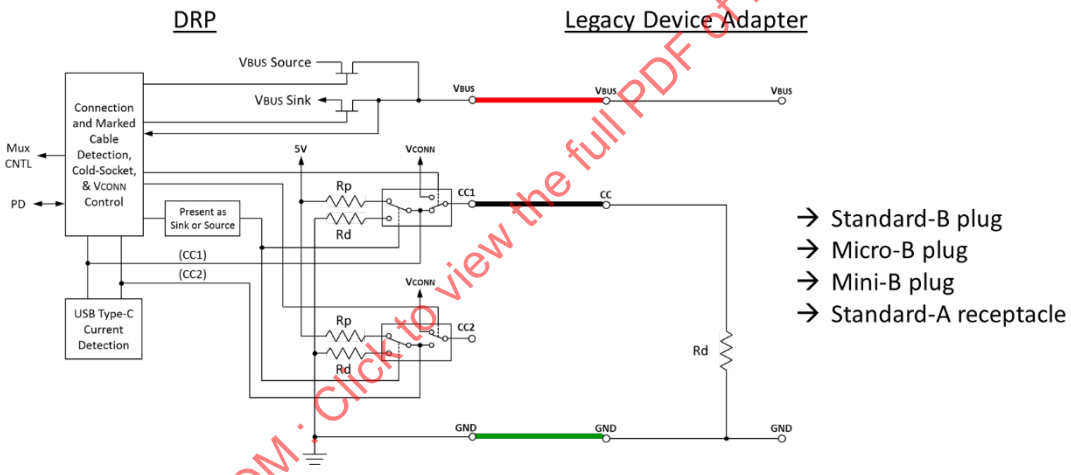
1. Le destinataire est débranché.

2. Le destinataire passe de l'état ***Unattached.SNK*** à l'état ***Attached.SNK*** en passant par l'état ***AttachWait.SNK***, le cas échéant.
   - À l'état ***Unattached.SNK***, et si le dispositif n'est pas exclusivement ***USB 2.0***, qu'il prend en charge les accessoires ou exige une alimentation supérieure à celle établie par défaut, le destinataire passe à l'état ***AttachWait.SNK*** lorsqu'il détecte une polarisation sur la broche CC et ignore la VBUS. Sinon, il ***peut*** passer directement à l'état ***Attached.SNK*** lorsque la VBUS est détectée.
   - Le destinataire détecte VBUS et passe à l'état ***Attached.SNK***.
3. Lorsque le destinataire est branché:
   - Le destinataire surveille la broche VBUS afin de détecter un débranchement; si un débranchement est détecté, il passe à l'état ***Unattached.SNK***.

4.5.3.2.3 Comportement DRP-port de dispositif existant

La Figure 4-34 représente le modèle fonctionnel d'une DRP branchée à un port de dispositif existant. Ce modèle repose sur la présence d'un adaptateur comme destinataire (le dispositif) de la DRP. Cet adaptateur est équipé d'une fiche USB Type-C sur une extrémité branchée à la DRP et d'une fiche USB Standard-B, d'une fiche USB Micro-B, d'une fiche USB Mini-B ou d'une embase USB Standard-A sur l'autre extrémité.

Figure 4-34 Modèle fonctionnel d'une DRP branchée à un port de dispositif existant



Anglais	Français
DRP	DRP
Legacy Device Adapter	Adaptateur pour dispositif existant
VBUS Source	Source VBUS
VBUS Sink	Destinataire VBUS
Connection and Marked Cable Detection, Cold-Socket, & VCONN Control	Détection de connexion et de câbles marqués électroniquement, prise commutée et contrôle de VCONN
Standard-B plug	Fiche Standard-B
Micro-B plug	Fiche Micro-B
Mini-B plug	Fiche Mini-B
Standard-A receptacle	Embase Standard-A
USB Type-C Current Detection	Détection de courant USB Type-C
Present as sink or source	Source ou destinataire présent

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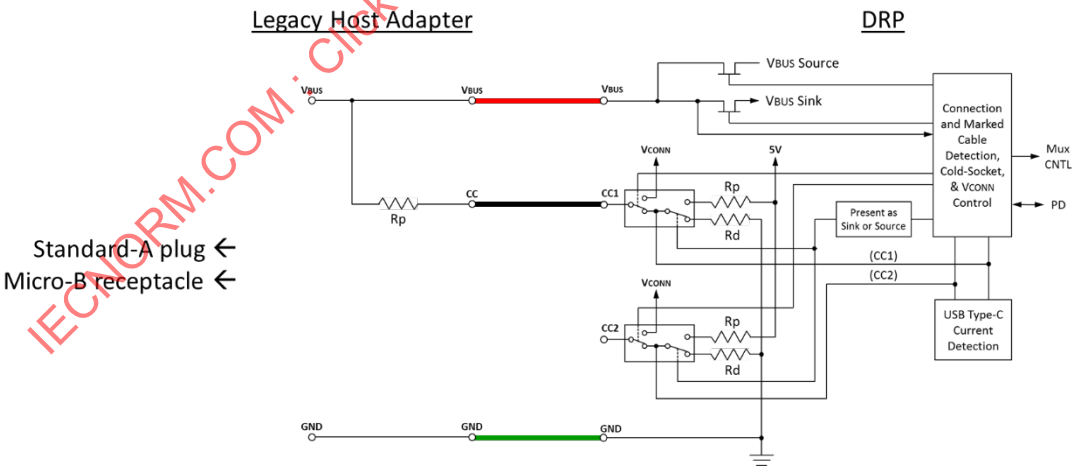
Les informations suivantes décrivent le comportement de l'ensemble lorsqu'une DRP est connectée à un adaptateur de dispositif existant, équipé d'une ***Rd*** à la masse destinée à reproduire le comportement d'un destinataire.

1. La DRP est débranchée.
   - La DRP alterne entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***.
2. La DRP passe de l'état ***Unattached.SRC*** à l'état ***Attached.SRC***.
   - La DRP à l'état ***Unattached.SRC*** détecte la dépolarisation de l'adaptateur sur la broche CC et passe à l'état ***AttachWait.SRC***.
   - La DRP à l'état ***AttachWait.SRC***, arrive à expiration (***tCCDebounce***) et passe à l'état ***Attached.SRC***.
   - La DRP à l'état ***Attached.SRC*** active la VBUS et la VCONN.
   - La DRP à l'état ***AttachWait.SRC*** ***peut*** prendre en charge l'état ***Try.SNK***; le cas échéant, elle ***peut*** basculer vers les états ***Try.SNK*** et ***TryWait.SRC*** avant de passer à l'état ***Attached.SRC***.
3. Lorsque la DRP est branchée:
   - La DRP surveille la broche CC afin de détecter un débranchement; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK*** (et recommence à alterner entre l'état ***Unattached.SNK*** et l'état ***Unattached.SRC***).

4.5.3.2.4 Comportement port hôte existant-DRP

La Figure 4-35 représente le modèle fonctionnel d'un port hôte existant connecté à une DRP fonctionnant comme un destinataire. Ce modèle repose sur la présence d'un adaptateur comme source (hôte) de la DRP fonctionnant comme un destinataire. Cet adaptateur est équipé d'une fiche USB Standard-A existante ou d'une embase USB Micro-B existante sur une extrémité et d'une fiche USB Type-C sur l'autre extrémité branchée à la DRP.

Figure 4-35 Modèle fonctionnel d'un port hôte existant branché à une DRP



Anglais	Français
Legacy Host Adapter	Adaptateur pour hôte existant
DRP	DRP
VBUS Source	Source VBUS

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Anglais	Français
VBUS Sink	Destinataire VBUS
Connection and Marked Cable Detection, Cold-Socket, & VCONN Control	Détection de connexion et de câbles marqués électroniquement, prise commutée et contrôle de VCONN
USB Type-C Current Detection	Détection de courant USB Type-C
Standard-A plug	Fiche Standard-A
Micro-B receptacle	Embase Micro-B
Present as sink or source	Source ou destinataire présent

Les informations suivantes décrivent le comportement de l'ensemble lorsqu'un adaptateur hôte existant, équipé d'une ***Rp*** dont la VBUS est destinée à reproduire le comportement d'une source, est connecté à une DRP. La valeur de la ***Rp*** ***doit*** annoncer la puissance USB par défaut (voir le Tableau 4-27), y compris si le câble peut transporter un courant de 3 A. En effet, le câble ne connaît pas les capacités de la source d'alimentation et tout courant supérieur est négocié par l'***USB BC 1.2***.

1. La DRP est débranchée.
   - La DRP alterne entre l'état ***Unattached.SRC*** et l'état ***Unattached.SNK***.
2. La DRP passe de l'état ***Unattached.SNK*** à l'état ***AttachWait.SNK*** en passant par l'état ***Attached.SNK***.
   - La DRP à l'état ***Unattached.SNK*** détecte la polarisation sur la broche CC et passe à l'état ***AttachWait.SNK***.
   - La DRP à l'état ***AttachWait.SNK*** détecte la VBUS et passe à l'état ***Attached.SNK***.
   - La DRP à l'état ***AttachWait.SNK*** ***peut*** prendre en charge l'état ***Try.SRC***; le cas échéant, elle ***peut*** basculer vers les états ***Try.SRC*** et ***TryWait.SNK*** avant de passer à l'état ***Attached.SNK***.
3. Lorsque la DRP est branchée:
   - La DRP surveille la VBUS afin de détecter un débranchement; si un débranchement est détecté, elle passe à l'état ***Unattached.SNK*** (et recommence à alterner entre l'état ***Unattached.SNK*** et à l'état ***Unattached.SRC***).

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4.6 Alimentation

L'alimentation électrique par connecteur USB Type-C repose sur les méthodes USB existantes, définies par les spécifications ***USB 2.0*** et ***USB 3.2***, la spécification ***USB BC 1.2*** et la spécification ***USB Power Delivery***. L'alimentation propre à l'***USB4*** nécessite un contrat ***USB PD*** explicite, défini en 5.3 et dans la spécification ***USB Power Delivery***. Avant de passer à un contrat ***USB PD*** explicite, un port ***USB4*** fonctionne comme un port ***USB 3.2*** en ce qui concerne l'alimentation.

Le mécanisme de ***courant USB Type-C*** permet à la source de fournir un courant supérieur aux exigences de la spécification ***USB BC 1.2***. Une source d'alimentation USB ***ne doit pas*** fournir une tension nominale supérieure à 48 V sur la VBUS. Les sources d'alimentation électrique par ***USB PD***, qui émettent par le biais d'un connecteur USB Type-C, ***doivent*** suivre les règles d'alimentation définies à l'Article 10 de la spécification ***USB Power Delivery***.

Tous les dispositifs USB Type-C ***doivent*** prendre en charge le ***courant USB Type-C*** et ***peuvent*** prendre en charge d'autres méthodes d'alimentation définies par USB. L'ordre de priorité ci-dessous relatif à la négociation d'alimentation ***doit*** être respecté: ***USB BC 1.2*** remplace les spécifications ***USB 2.0*** et ***USB 3.2***, le ***courant USB Type-C*** à 1,5 A et 3,0 A remplace l'***USB BC 1.2***, et l'***USB Power Delivery*** remplace le ***courant USB Type-C***. Le Tableau 4-19 récapitule l'ordre de priorité relatif à l'utilisation des sources d'alimentation.

Tableau 4-19 Ordre de priorité pour l'utilisation des sources d'alimentation

Ordre de priorité	Mode de fonctionnement		Tension nominale	Courant maximal
Maximale	***USB PD***		Paramétrable jusqu'à 48 V	5 A
	Courant USB Type-C de 3,0 A		5 V	3,0 A
↓	***Courant USB Type-C*** de 1,5 A		5 V	1,5 A
	USB BC 1.2		5 V	Jusqu'à 1,5 A[1]
	Puissance USB par défaut	***USB 3.2***	5 V	Voir ***USB 3.2***
Minimale		***USB 2.0***	5 V	Voir ***USB 2.0***

Note 1: L'***USB BC 1.2*** permet de désigner un fournisseur d'alimentation pour prendre en charge un niveau d'alimentation entre 0,5 A et 1,5 A. Si le fournisseur d'alimentation ***USB BC 1.2*** ne prend pas en charge 1,5 A, il doit respecter les exigences en matière de baisse d'alimentation. Un consommateur d'alimentation ***USB BC 1.2 peut*** consommer jusqu'à 1,5 A sous réserve que la tension ne chute pas au-dessous de 2 V, ce qui ***peut*** survenir à tout niveau d'alimentation supérieur à 0,5 A.

Par exemple, en cas de passage en mode ***USB PD*** (par exemple, lorsqu'un contrat d'alimentation a été négocié), le dispositif ***doit*** respecter le contrat d'alimentation et ignorer toute autre exigence précédemment imposée ou apportée par les spécifications ***courant USB Type-C***, ***USB BC 1.2*** ou ***USB 2.0*** et ***USB 3.2***. En cas de sortie du mode ***USB PD***, le dispositif ***doit*** se replier, dans l'ordre de priorité, en prenant en compte les niveaux de puissance des spécifications ***courant USB Type-C***, ***USB BC 1.2*** ou ***USB 2.0*** et ***USB 3.2***.

Tous les ports USB Type-C ***doivent*** permettre la connexion à une source d'alimentation USB qui fournit l'alimentation USB par défaut (par exemple, un hôte connecté à un chargeur USB existant qui alimente toujours la VBUS).

4.6.1 Exigences relatives à l'alimentation pendant la veille USB

Il est nécessaire de développer la définition d'une veille USB traditionnelle pour les mises en œuvre USB Type-C avec le ***courant USB Type-C***, l'***USB PD*** et la VCONN, ainsi qu'avec des câbles actifs.

4.6.1.1 Exigences relatives à la VBUS pendant la veille USB

Les spécifications ***USB 2.0*** et ***USB 3.2*** définissent la quantité de courant que peut consommer un destinataire en veille.

Les règles d'alimentation en cas de veille USB ***doivent*** s'appliquer lorsque le ***courant USB Type-C*** est au niveau de puissance USB par défaut ou lorsque l'***USB PD*** est utilisé et que le bit de veille est défini en conséquence.

Lorsque le ***courant USB Type-C*** est défini à 1,5 A ou à 3,0 A, le destinataire peut continuer à puiser le courant de la VBUS pendant la veille USB. Pendant la veille USB, les exigences du destinataire relatives au suivi et au respect des annonces de ***courant USB Type-C*** demeurent applicables (voir 4.5.2.3).

L'***USB PD*** fournit une méthode qui permet à la source d'indiquer au destinataire si le destinataire doit suivre les règles d'alimentation USB relatives à la veille.

4.6.1.2 Exigences relatives à la VCONN pendant la veille USB

Si la source fournit une alimentation à la VBUS au cours d'une veille USB, elle ***doit*** également alimenter la VCONN et satisfaire aux exigences définies dans le Tableau 4-5.

Les câbles avec marquage électronique ***doivent*** satisfaire aux exigences du Tableau 4-6 lors de la veille USB.

Les accessoires alimentés par la VCONN ***doivent*** satisfaire aux exigences définies dans le Tableau 4-7 lors de la veille USB.

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4.6.2 Alimentation de la VBUS par câble USB Type-C

Les exigences minimales relatives à l'alimentation de la VBUS par un ensemble câble-connecteurs USB Type-C correspondent aux exigences actuelles applicables aux VBUS alimentées par des ensembles câble-connecteurs USB existants.

L'***USB Power Delivery*** de la Standard Power Range (SPR) est destinée à fonctionner par câble USB Type-C à USB Type-C non modifié. Par conséquent, tout ensemble câble-connecteurs USB Type-C qui intègre des composants électriques ou électroniques ***doit*** assurer la tolérance d'une tension VBUS de 21 V, ou être protégé contre celle-ci.

Le fonctionnement de l'***USB Power Delivery*** en mode Extended Power Range (EPR) exige d'utiliser des câbles USB Type-C vers USB Type-C compatibles EPR. Un ensemble câble-connecteurs USB Type-C qui intègre des composants électriques ou électroniques et qui ***peut*** être alimenté par la VBUS ***doit*** pouvoir utiliser de manière fonctionnelle une tension VBUS maximale de 50,9 V (48 V + 5 % + 500 mV) ou en être protégé.

4.6.2.1 Courant USB Type-C

La tension et le courant USB par défaut sont définis par les spécifications ***USB 2.0*** et ***USB 3.2***. Toutes les annonces de ***courant USB Type-C*** sont à la tension USB de la VBUS définie par ces spécifications.

La fonctionnalité de ***courant USB Type-C*** fournit les extensions suivantes:

- courant supérieur à celui défini par les spécifications ***USB 2.0***, ***USB 3.2*** ou BC 1.2;
- source d'alimentation qui permet la gestion du courant fourni.

Le connecteur USB Type-C utilise les broches CC à des fins de configuration, avec possibilité pour une source d'annoncer la quantité de courant qu'elle ***doit*** fournir à son port partenaire (le destinataire):

- la valeur par défaut est celle configurée pour une valeur de courant en fonctionnement sous tension élevée et définie par une spécification USB (500 mA pour les ports ***USB 2.0***; 900 mA/1 500 mA pour les ports ***USB 3.2*** respectivement à voie unique/double voie);
- 1,5 A;
- 3,0 A.

Lorsqu'une source annonce un courant USB Type-C par défaut, le comportement du destinataire est défini comme suit:

- Il se connecte en tant que dispositif ***USB 2.0*** ou ***USB 3.2***; après quoi, le destinataire ***doit*** respecter la spécification USB appropriée.
- Il passe à un contrat ***USB PD***; après quoi, le destinataire ***doit*** respecter la spécification ***USB PD*** pour déterminer le courant (par exemple, ***Rp*** n'est plus la valeur par défaut, car elle est remplacée par le contrat ***USB PD***).
- Il détecte un port de charge ***USB BC 1.2***; après quoi, le destinataire ***doit*** respecter la spécification ***USB BC 1.2***.
- Il se connecte en tant que dispositif destinataire d'alimentation (PSD) USB Type-C; après quoi, le destinataire ***peut*** puiser jusqu'à 500 mA et ***doit*** satisfaire aux exigences de courant d'entrée pour ***USB 2.0***.

Un PSD ***doit*** prendre entièrement en charge le ***courant USB Type-C***; ***il convient*** qu'il prenne en charge l'***USB PD*** et il ***peut*** prendre en charge l'***USB BC 1.2***. Un PSD ***peut*** être un destinataire ou une DRP fonctionnant en mode destinataire. Un PSD ***ne doit pas*** avoir de fonction de communication USB ou USB Type-C en ***mode alternatif***.

La relation du ***courant USB Type-C*** avec sa valeur équivalente ***USB PD*** Power (PDP) est représentée dans le Tableau 4-20.

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Tableau 4-20 Annonce de courant USB Type-C et équivalent PDP

Courant USB Type-C		Équivalent PDP
Par défaut	500 mA (***USB 2.0***)	2,5 W
	900 mA (***USB 3.2*** à voie unique)	4,5 W
	1 500 mA (***USB 3.2*** à double voie)	7,5 W
1,5 A		7,5 W
3,0 A		15 W

Un destinataire qui utilise l'excédent de courant disponible (1,5 A ou 3,0 A, par exemple) ***doit*** surveiller les broches CC et ***doit*** adapter sa consommation de courant dans le délai ***tSinkAdj*** pour rester dans la plage de valeurs annoncée par la source. Lorsqu'un contrat ***USB PD*** existe, le destinataire ne doit pas surveiller les annonces de courant USB Type-C et il ***ne doit pas*** répondre aux annonces de courant USB Type C.

La source ***doit*** alimenter la VBUS jusqu'au destinataire dans le délai ***tVBUSON***. La VBUS ***doit*** se trouver dans la plage de tensions spécifiée pour le courant annoncé.

Une source (le port qui alimente la VBUS) ***doit*** se protéger des destinataires puisant un courant supérieur à l'annonce de ***courant USB Type-C*** du port.

La source ajuste la ***Rp*** (ou la source de courant) pour annoncer laquelle des trois intensités de courant elle prend en charge. Voir le Tableau 4-27 pour les exigences de terminaison qui permettent à la source d'annoncer un courant.

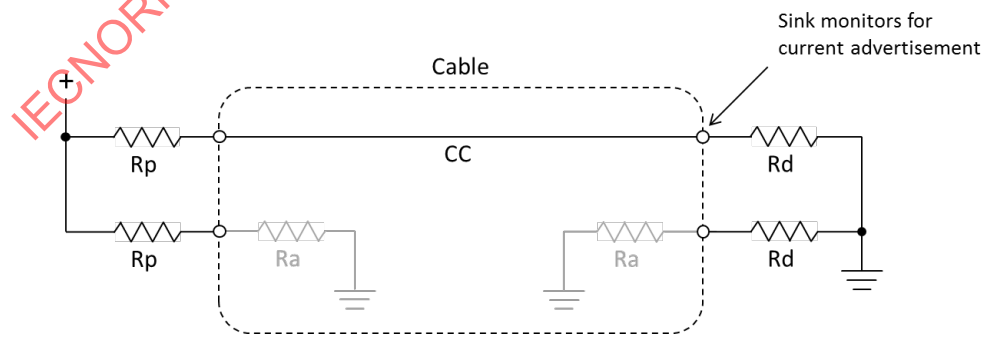
La valeur de la ***Rp*** établit une tension (***vRd***) sur la broche CC utilisée par le destinataire pour déterminer le courant maximal qu'elle ***peut*** puiser.

Le Tableau 4-38 définit la plage de tensions CC observées par un destinataire prenant uniquement en charge le courant USB par défaut.

Si le destinataire demande à utiliser un courant USB supérieur à celui par défaut, il ***doit*** surveiller la ***vRd*** pour déterminer le courant maximal qu'il ***peut*** puiser. Voir le Tableau 4-39.

La Figure 4-36 et la Figure 4-37 représentent les cas où le destinataire surveille la ***vRd*** de la broche CC afin de détecter si l'hôte annonce un courant USB supérieur à celui par défaut.

Figure 4-36 Surveillance du courant par le destinataire avec les modèles de broches CC à polarisation/dépolarisation

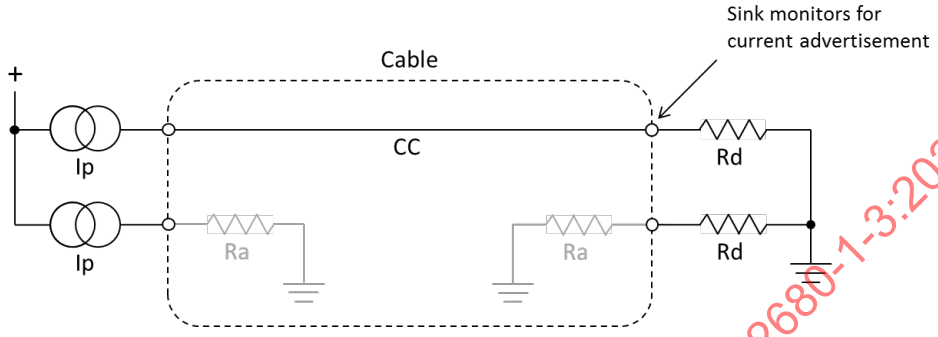


Anglais	Français
Cable	Câble

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Anglais	Français
Sink Monitors for current advertisement	Le destinataire surveille les annonces de courant

Figure 4-37 Surveillance du courant par le destinataire avec les modèles de broches CC à source de courant/dépolarisation



Anglais	Français
Cable	Câble
Sink Monitors for current advertisement	Le destinataire surveille les annonces de courant

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4.6.2.2 Charge des batteries par USB 1.2

La ***spécification USB Battery Charging, Révision 1.2*** définit une méthode qui utilise les broches ***USB 2.0*** D+ et D− pour annoncer que la VBUS peut fournir jusqu'à 1,5 A. La prise en charge de la charge ***USB BC 1.2*** est ***facultative***.

Un port USB Type-C qui met en œuvre l'***USB BC 1.2*** en mesure de fournir au moins 1,5 A ***doit*** annoncer un ***courant USB Type-C de 1,5 A*** dans le délai ***tVBUSON***, à compter du passage à l'état ***Attached.SRC***. Sinon, le port ***doit*** annoncer un ***courant USB Type-C*** au niveau de puissance USB par défaut. Un port USB Type-C qui met en œuvre l'***USB BC 1.2*** prenant également en charge le ***courant USB Type-C*** de 3,0 A ***peut*** annoncer un ***courant USB Type-C*** de 3,0 A.

Si un destinataire qui prend en charge la détection ***USB BC 1.2*** détecte une ***Rp*** au niveau de puissance USB par défaut et ne découvre pas de source conforme à l'***USB BC 1.2***, il ***doit*** limiter sa consommation maximale de courant au niveau USB normalisé, conformément au Tableau 4-19. Cela assure le respect des limites maximales de courant en cas de connexion à une source ne prenant pas en charge l'***USB BC 1.2***.

Un destinataire qui prend en charge la détection ***USB BC 1.2*** et puise un courant supérieur au ***courant USB Type-C*** par défaut ***doit*** surveiller la ***vRd*** sur les broches CC pour détecter la ***Rp*** de la source et ***doit*** mettre en œuvre les transitions avec le ***sous-état Sink Power*** (Figure 4-19). Si un destinataire qui prend en charge la détection ***USB BC 1.2*** et puise un courant maximal supérieur au ***courant USB Type-C*** par défaut détecte la ***Rp*** au ***courant USB Type-C*** aux niveaux 1,5 A ou 3,0 A, mais ne détecte pas une source ***USB BC 1.2***, il ***doit*** limiter sa consommation de courant maximale à l'intensité de ***courant USB Type-C*** appropriée annoncée, et ***doit*** adapter sa consommation de courant pour rester dans les limites de la valeur annoncée par la source sur les transitions de sous-état. Pour les transitions de sous-état qui commencent à partir d'un niveau de puissance maximal et qui se terminent par un niveau de puissance minimal, le destinataire ***doit*** réduire sa consommation électrique dans les limites de ***tSinkAdj***. Voir 4.5.2.3.2.2 et 4.5.2.3.3.2.

En mode ***USB Power Delivery***, un dispositif qui fait office de destinataire ***ne doit pas*** déclencher une détection ***USB BC 1.2*** tant que la paire de ports n'est pas débranchée ou qu'il existe un état Error Recovery ou Hard Reset.

4.6.2.3 Source d'alimentation propriétaire

Ce paragraphe est obsolète. Les dispositifs avec connecteurs USB Type-C ne ***doivent*** utiliser que les méthodes de signalisation définies par les spécifications USB pour négocier l'alimentation.

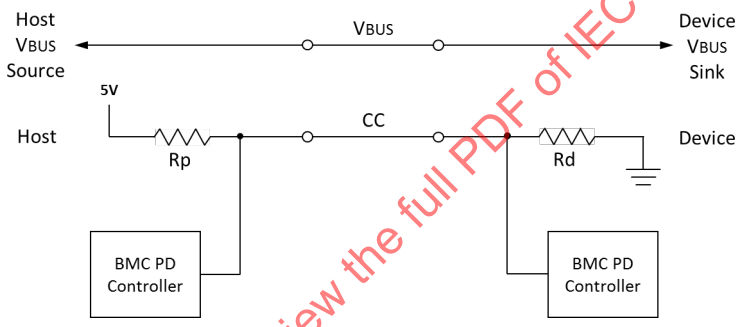
4.6.2.4 USB Power Delivery

L'***USB Power Delivery*** est une fonctionnalité des connecteurs USB Type-C. Lorsque l'***USB PD*** est mise en œuvre, le codage BMC (Biphase Mark Coding) ***USB PD*** transmis sur le fil CC ***doit*** être utilisé pour les communications ***USB PD*** entre les ports USB Type-C.

Lors du branchement, la VBUS ***doit*** être fonctionnellement stable avant d'initier une communication ***USB PD***.

La Figure 4-38 représente la manière dont la signalisation BMC ***USB PD*** est transmise sur le fil CC du câble USB Type-C.

Figure 4-38 *USB PD* sur les broches CC

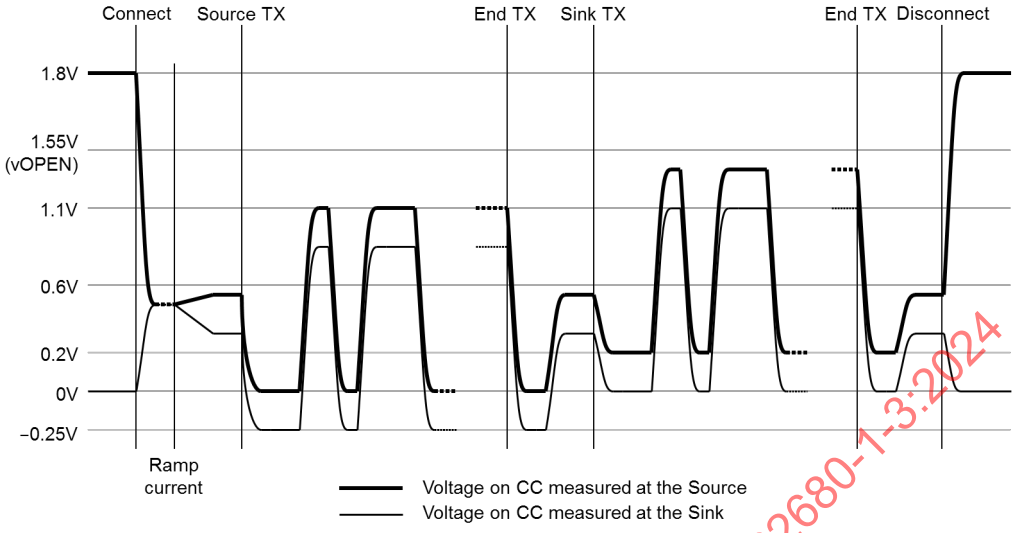


Anglais	Français
Host VBUS Source	Source VBUS de l'hôte
Host	Hôte
Device	Dispositif
BMC PD Controller	Contrôleur BMC PD
Device VBUS Sink	Destinataire VBUS du dispositif

La Figure 4-39 représente la signalisation BMC ***USB PD*** du point de vue de la broche CC de la source et du destinataire. Les ruptures de signalisation visent à représenter le passage du temps.

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Figure 4-39 Signalisation BMC *USB PD* sur les broches CC



Anglais	Français
Connect	Connexion
Source TX	Source TX
End TX	Terminaison TX
Sink TX	Destinataire TX
End TX	Terminaison TX
Disconnect	Déconnexion
Ramp current	Courant de rampe
Voltage on CC measured at the Source	Tension continue mesurée aux bornes de la Source
Voltage on CC measured at the Sink	Tension continue mesurée aux bornes du Destinataire

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En l'absence de contrat explicite, les sources ***USB PD*** qui peuvent fournir, en fonction de leur PDP:

- 5 V à 3 A ou plus, ***doivent*** annoncer un ***courant USB Type-C*** de 3 A;
- 5 V à 1,5 A ou plus et jusqu'à 3 A, ***doivent*** annoncer un ***courant USB Type-C*** de 1,5 A;
- 5 V à moins de 1,5 A, ***doivent*** annoncer un ***courant USB Type-C*** au niveau de puissance USB par défaut;

dans le délai ***tVBusON*** à compter du passage à l'état ***Attached.SRC***. Pour les chargeurs multiports à capacité partagée, une source ***USB PD*** qui peut fournir 5 V à 3 A ou plus ***peut*** annoncer un ***courant USB Type-C*** initial de 1,5 A, puis augmenter l'annonce après le branchement (voir 4.8.6.2). Lors d'une veille USB, une source ***USB PD peut*** fixer sa ***Rp*** à la valeur par défaut, afin d'indiquer que le destinataire ne ***doit*** puiser que le courant de veille USB défini en 4.6.1.1.

Lorsqu'un contrat ***USB PD*** explicite existe, une source conforme à la spécification ***USB PD***, révision 2, ***doit*** annoncer un ***courant USB Type-C*** de 1,5 A ou de 3,0 A. Lors de l'application d'un contrat explicite, la source conforme à la spécification ***USB PD***, révision 2, ***doit*** annoncer une ***Rp*** d'une valeur de 1,5 A ou de 3,0 A, après avoir reçu GoodCRC en réponse au premier message PS_RDY.

Lorsqu'un contrat ***USB PD*** explicite existe, une source conforme à la spécification ***USB PD***, révision 3, ***doit*** définir la ***Rp*** en fonction du schéma anticollision défini en 5.7 de la spécification ***USB PD***, révision 3. Lors de l'application d'un contrat explicite, la source conforme à la spécification ***USB PD***, révision 3, ***doit*** annoncer une ***Rp*** conforme au schéma anticollision de la spécification ***USB PD***, révision 3.

Voir 1.6 de la spécification ***USB Power Delivery*** pour connaître la définition d'un contrat explicite.

4.6.2.5 Limitations de courant des dispositifs USB alimentés par VCONN (CTVPD) de charge

Les ***dispositifs USB alimentés par VCONN*** de charge mettent en œuvre la charge en connectant passivement les broches CC et VBUS de la source à l'hôte. Ainsi, les ***dispositifs USB alimentés par VCONN*** augmentent effectivement l'impédance sur les broches VBUS, GND et CC entre la source d'alimentation et l'hôte. Cela se traduit par des impédances qui peuvent être supérieures à la valeur maximale admise pour les câbles. Pour éviter les problèmes de communication et de fausse déconnexion associés aux chutes au niveau des broches GND et VBUS à impédance accrue, les critères suivants ***doivent*** être respectés:

1. Le ***dispositif USB alimenté par VCONN*** de charge ***doit*** indiquer l'impédance des broches GND et VBUS la plus défavorable (y compris la paire supplémentaire de connecteurs couplés et de TEC) dans sa réponse de commande de ***découverte d'identité USB PD*** sur SOP'.
2. L'hôte qui prend en charge le ***dispositif USB alimenté par VCONN*** de charge ***doit*** utiliser ces informations, ainsi que les informations déduites sur le câble, pour limiter son courant maximal si la source d'alimentation annonce un courant supérieur à celui admis par le ***dispositif USB alimenté par VCONN*** de charge.

L'hôte n'a aucun moyen d'interroger le câble, car sa source VCONN est consommée par le ***dispositif USB alimenté par VCONN***. Au lieu de cela, l'hôte ***peut*** prendre pour hypothèse que le câble est de 5 A afin de calculer la limite de courant de charge uniquement s'il reçoit un PDO SourceCapability ***USB PD*** de plus de 3 A (même si l'hôte ne ***demande*** finalement pas ce PDO ou s'il demande un courant inférieur ou égal à 3 A).

L'hôte ***doit*** limiter encore son courant maximal au-dessus de la valeur annoncée par la source d'alimentation, en fonction de l'impédance indiquée pour la broche GND et de la capacité de câble déduite. L'impédance de la broche GND est indiquée dans la réponse de commande de ***découverte d'identité*** du ***VPD*** en incréments de 1 mΩ et est utilisée dans les formules suivantes:

- courant limité sur la GND avec un câble de 3 A déduits = 0,25 V/(0,25 V/3 A + VPD_GND_DCR);
- courant limité sur la GND avec un câble de 5 A déduits = 0,25 V/(0,25 V/5 A + VPD_GND_DCR).

Le Tableau 4-21 fournit quelques exemples.

Tableau 4-21 Limite de courant maximal du destinataire lorsqu'il est branché au CTVPD

Impédance indiquée pour la GND	Câble de 3 A déduits[1]	Câble de 5 A déduits[2]
0,010 Ω	2,679 A	4,167 A
0,015 Ω	2,542 A	3,846 A
0,020 Ω	2,419 A	3,571 A
0,025 Ω	2,308 A	3,333 A
0,030 Ω	2,206 A	3,125 A
0,035 Ω	2,113 A	2,941 A
0,040 Ω	2,027 A	2,778 A

Notes:

1. Calculé par 0,25 V / (0,25 V / 3 A + VPD_GND_DCR).
2. Calculé par 0,25 V / (0,25 V / 5 A + VPD_GND_DCR).

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De plus, l'impédance accrue de la broche VBUS peut entraîner une chute de la VBUS de plus de 1 V mesurée à l'entrée de l'hôte. Selon l'impédance de la broche VBUS indiquée dans la réponse de commande de ***découverte d'identité*** du ***VPD*** par incréments de 2 mΩ et selon la capacité de câble déduite, l'hôte ***doit*** abaisser son seuil de déconnexion VBUS ou limiter davantage son courant maximal à l'aide des formules suivantes:

- courant limité sur la VBUS et la GND avec un câble de 3 A
  déduits = 0,75 V/(0,75 V/3 A + VPD_VBUS_DCR + VPD_GND_DCR);
- courant limité sur la VBUS et la GND avec un câble de 5 A
  déduits = 0,75 V/(0,75 V/5 A + VPD_VBUS_DCR + VPD_GND_DCR).

Tableau 4-22 Exemples de courant maximal entre le VPD de charge et le destinataire selon l'impédance sur les broches VBUS et GND

Impédance indiquée pour la VBUS[4]	Impédance indiquée pour la GND[4]	Câble de 3 A déduits[1]	Câble de 5 A déduits[2]
0,020 Ω	0,010 Ω	2,679 A	4,167 A
0,030 Ω	0,015 Ω	2,542 A	3,846 A
0,040 Ω	0,020 Ω	2,419 A	3,571 A
0,050 Ω	0,025 Ω	2,308 A	3,333 A
0,060 Ω	0,030 Ω	2,206 A	3,125 A
0,070 Ω	0,035 Ω	2,113 A	2,941 A
0,080 Ω	0,040 Ω	2,027 A	2,778 A

Notes:

1. Calculé par 0,75 V / (0,75 V /3 A + VPD_VBUS_DCR + VPD_GND_DCR).
2. Calculé par 0,75 V / (0,75 V /5 A + VPD_VBUS_DCR + VPD_GND_DCR).
3. Le tableau ne présente pas toutes les combinaisons admissibles, mais uniquement un sous-ensemble fourni à titre de représentation.
4. Le rapport entre l'impédance indiquée pour la VBUS et l'impédance indiquée pour la GND est de 2:1.

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4.6.2.6 Exigences du destinataire USB Type-C pour une opération à haute tension

Le présent paragraphe définit les exigences électriques pour les destinataires USB Type-C qui prennent en charge l'opération à haute tension. Voir 3.11 pour les exigences EPR des câbles USB Type-C qui prennent en charge EPR.

Le destinataire ***doit*** maintenir la tension sur ses contacts VBUS dans les limites de 12 V de la tension sur le contact VBUS de la source au moment de retirer la fiche de câble pendant au moins 250 µs depuis le moment de la séparation des contacts VBUS (voir la Figure 3-1). Pour plus d'informations relatives aux lignes directrices en matière d'arc de contact haute tension et d'atténuation, voir l'Annexe H.

4.7 Hubs USB

Les hubs ***USB 2.0***, ***USB 3.2*** et ***USB4*** sont respectivement définis par les spécifications ***USB 2.0***, ***USB 3.2*** et ***USB4***. Les hubs USB mis en œuvre avec un ou plusieurs connecteurs USB Type-C ***doivent*** être conformes à ces spécifications concernant les mises en œuvre USB Type-C. ***Il convient que*** tous les ports USB Type-C en aval d'un hub USB prennent en charge la même fonctionnalité. Sinon, ces ports ***doivent*** être clairement marqués pour identifier la fonctionnalité prise en charge.

Les hubs USB ***doivent*** être équipés d'un port orienté en amont (pour se connecter à un hôte ou un hub supérieur dans l'arborescence USB), qui ***peut*** être un dispositif d'alimentation (voir 4.8.4). Le hub ***doit*** désigner clairement à l'utilisateur le port orienté en amont. Cette mesure ***peut*** s'effectuer par isolation physique et/ou étiquetage.

Les ports orientés en aval du hub USB ***ne doivent pas*** être équipés de capacités double fonction (DRD). Toutefois, ces ports ***peuvent*** être équipés de capacités d'alimentation double fonction (DRP).

Les broches CC sont utilisées pour les connexions port-port et ***doivent*** être prises en charge sur toutes les connexions USB Type-C du hub.

Pour les hubs ***USB 2.0*** et ***USB 3.2***, les ports orientés en aval ***ne doivent pas*** mettre en œuvre ni passer par un mode alternatif ou accessoire. Les broches SBU ***ne doivent pas*** être connectées (***zSBUTermination***) à un port de hub USB. Pour les hubs ***USB4***, voir 5.2.3 concernant la prise en charge des ***modes alternatifs***.

Les DFP du hub USB ***doivent*** prendre en charge les exigences relatives aux sources d'alimentation. Voir 4.8.1.

Les exigences supplémentaires concernant les hubs ***USB4*** sont indiquées à l'Article 5.

4.8 Alimentation et charge

Le présent paragraphe définit les exigences et les recommandations relatives à l'utilisation de ports USB Type-C à des fins d'alimentation. Tout port USB Type-C qui fournit un courant supérieur à celui par défaut et/ou prend en charge l'***USB Power Delivery doit*** satisfaire aux exigences comme s'il s'agissait d'un chargeur.

La liste ci-dessous répertorie les paragraphes généralement applicables aux ports USB Type-C sur:

- les systèmes hôtes: 4.8.1 et 4.8.5. Note: le paragraphe 4.8.6 ne concerne pas les systèmes hôtes;
- les dispositifs qui peuvent fournir une alimentation: 4.8.4;
- les hubs:
    - hubs traditionnels: si l'***USB BC 1.2*** est prise en charge, se reporter aux spécifications de base ***USB 2.0***/***USB 3.2*** et au 4.8.1 selon les besoins;
    - hubs qui peuvent fournir une alimentation supérieure aux spécifications de base: 4.8.1, 4.8.4, 4.8.5 et 4.8.6;
- les chargeurs spécifiques:
    - chargeurs à port simple: 4.8.1;
    - chargeurs multiports: 4.8.1 et 4.8.6.

4.8.1 DFP comme source d'alimentation

Les sources (chargeurs de batteries, ports en aval du hub et hôtes) ***peuvent*** toutes être utilisées pour charger une batterie. Lorsqu'un chargeur est mis en œuvre avec une embase USB Type-C ou un câble USB Type-C captif, il ***doit*** respecter l'ensemble des exigences applicables.

- Une source ***doit*** exposer ses capacités d'alimentation à partir de la méthode de ***courant USB Type-C*** et ***peut*** prendre en charge d'autres méthodes USB normalisées (***USB BC 1.2*** ou ***USB PD***).
- Une source annonçant sa capacité de courant avec l'***USB BC 1.2 doit*** satisfaire aux exigences du 4.6.2.2, en lien avec les annonces de ***courant USB Type-C***.
- Une source qui a négocié un contrat ***USB PD doit*** satisfaire aux exigences du 4.6.2.4, en lien avec les annonces de ***courant USB Type-C***.

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- Si une source est capable de fournir une tension supérieure à la VBUS par défaut, elle ***doit*** se conformer intégralement à la spécification ***USB PD*** et ne ***doit*** négocier ses contrats d'alimentation qu'avec l'***USB PD***.
- Une source en capacité d'inverser les rôles d'alimentation de source et de destinataire ***doit*** se conformer intégralement à la spécification ***USB PD*** et ne ***doit*** négocier ses contrats d'alimentation qu'avec l'***USB PD***.
- Si une source est capable de fournir un courant supérieur à 3,0 A, elle ***doit*** utiliser la technique de ***découverte d'identité USB PD*** pour déterminer le courant admissible du câble.

4.8.1.1 Chargeurs USB avec embases USB Type-C

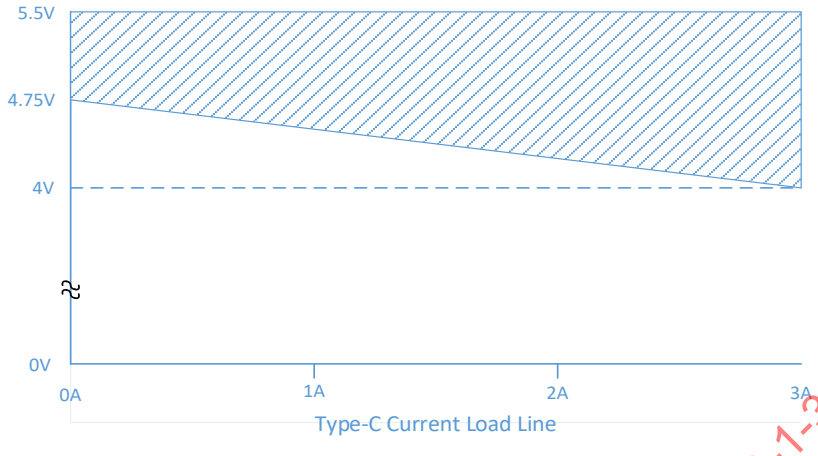
- Un chargeur USB avec embase USB Type-C (source) ne ***doit*** alimenter la VBUS que lorsqu'il détecte qu'un destinataire est branché. Il ***doit*** interrompre l'alimentation de la VBUS lorsqu'il détecte que le destinataire est débranché (***vOPEN***).
- Un chargeur USB avec embase USB Type-C ***ne doit pas*** annoncer de courant supérieur à 3,0 A, sauf lorsqu'il utilise la technique de ***découverte d'identité USB PD*** pour déterminer le courant admissible du câble. Il ***doit*** ensuite limiter le courant annoncé en conséquence.
- Un chargeur USB avec embase USB Type-C (source) qui ne peut pas communiquer des données ***doit*** annoncer un ***courant USB Type-C*** d'au moins 1,5 A, dans le délai ***tVBUSON*** à compter du passage à l'état ***Attached.SRC***. Il ***doit*** court-circuiter ensemble D+ et D− avec une résistance inférieure à 200 Ω. Cela assure la compatibilité ascendante des destinataires existants qui ***peuvent*** utiliser l'***USB BC 1.2*** pour la détection de chargeur.

4.8.1.2 Chargeurs USB avec câble USB Type-C captif

- Un chargeur USB avec câble actif USB Type-C ne ***doit*** alimenter la VBUS que lorsqu'il détecte qu'un destinataire est branché. Il ***doit*** interrompre l'alimentation de la VBUS lorsqu'il détecte que le destinataire est débranché (***vOPEN***).
- Un chargeur USB avec câble USB Type-C captif ***doit*** limiter son annonce de courant et ne pas dépasser la capacité de courant du câble (jusqu'à 5 A).
- Un chargeur USB avec câble USB Type-C captif qui ne peut pas communiquer des données ***doit*** annoncer un ***courant USB Type-C*** d'au moins 1,5 A. Il ***doit*** court-circuiter ensemble D+ et D− avec une résistance inférieure à 200 Ω. Cela assure la compatibilité ascendante des destinataires existants qui ***peuvent*** utiliser l'***USB BC 1.2*** pour la détection de charge.
- La tension mesurée aux bornes de la fiche d'un chargeur USB avec câble USB Type C captif ***peut*** atteindre jusqu'à 0,75 × I/3 V (0 < I ≤ 3 A) ou 0,75 × I/5 V (0 < I ≤ 5 A) au-dessous de la plage de tolérances normalisée pour la tension choisie, où I est le courant réellement puisé.
    - Un chargeur USB qui annonce un ***courant USB Type-C*** ***doit*** fournir une tension dans la plage de 4,75 V à 5,5 V si aucun courant n'est puisé, ou dans la plage de 4,0 V à 5,5 V pour 3 A. La tension de sortie en tant que fonction de charge au ***courant USB Type-C*** annoncé (par défaut, 1,5 A et 3 A) ***doit*** rester dans la zone hachurée représentée à la Figure 4-40.

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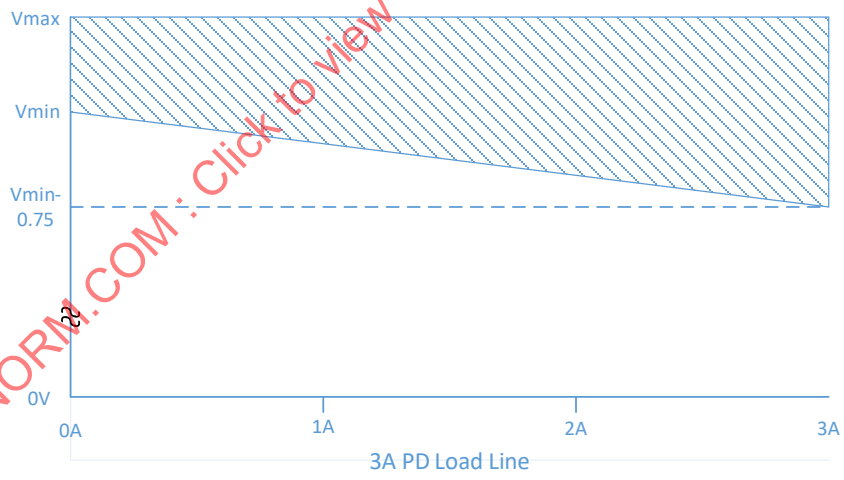
Figure 4-40 Sortie d'un câble USB Type-C en tant que fonction de charge USB Type-C non PD



Anglais	Français
Type-C Current Load Line	Ligne de charge en courant Type-C

- Un chargeur ***USB PD*** qui a négocié une tension V à une valeur ≤ 3 A ***doit*** fournir une tension dans la plage de Vmax (V + 5 %) à Vmin (V – 5 %) si aucun courant n'est puisé, ou dans la plage de Vmax à Vmin – 0,75 V pour 3 A. Pour toutes les charges, la tension de sortie ***doit*** rester dans la zone hachurée représentée à la Figure 4-41.

Figure 4-41 Sortie d'un câble USB Type-C de chargeur *USB PD* de 0 A à 3 A en tant que fonction de charge

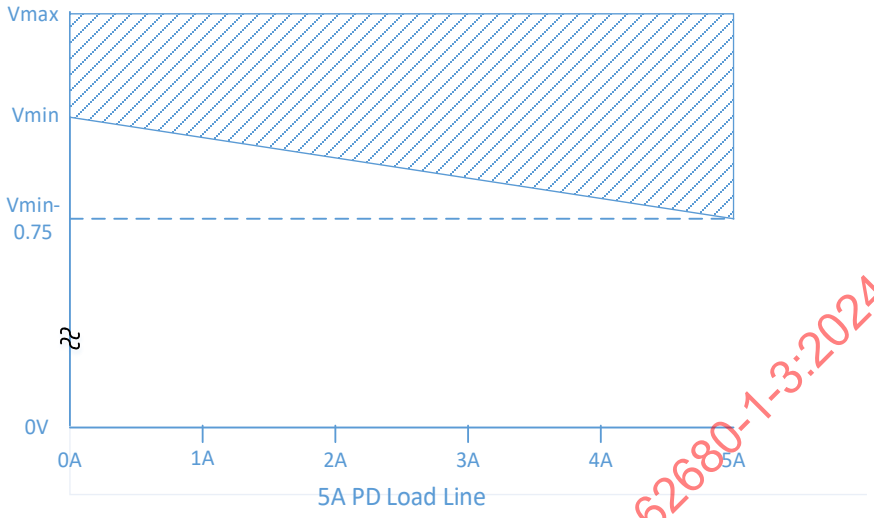


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Anglais	Français
3A PD Load Line	Ligne de charge 3A PD

- Un chargeur ***USB PD*** qui a négocié une tension V entre 3 A et 5 A ***doit*** fournir une tension dans la plage de Vmax (V + 5 %) à Vmin (V - 5 %) si aucun courant n'est puisé, ou dans la plage de Vmax à Vmin - 0,75 V pour 5 A. Pour toutes les charges, la tension de sortie ***doit*** rester dans la zone hachurée représentée à la Figure 4-42.

Figure 4-42 Sortie d'un câble USB Type-C de chargeur *USB PD* de 3 A à 5 A en tant que fonction de charge



Anglais	Français
5A PD Load Line	Ligne de charge 5A PD

- Note: La chute de tension ohmique maximale admissible pour la masse du câble est de 250 mV (voir 4.4.1). L'objet est d'assurer l'intégrité des signaux pour le fil CC, lorsqu'il est utilisé à des fins de détection de connexion et de signalisation BMC ***USB PD***.

4.8.2 Méthodes de charge non USB

Un produit (source et/ou destinataire) avec un connecteur USB Type-C ne ***doit*** utiliser que les méthodes de signalisation définies dans les spécifications USB pour négocier l'alimentation sur son ou ses connecteurs USB Type-C.

4.8.3 Hôte destinataire

Un hôte destinataire est une sous-catégorie de DRP spécifique, capable d'utiliser une alimentation, mais qui ne peut pas agir comme un dispositif USB. Par exemple, le DFP d'un hub ou d'un ordinateur portable fonctionne comme un hôte, mais pas comme un dispositif.

L'hôte destinataire ***doit*** suivre les règles applicables aux DRP (voir 4.5.1.4 et la Figure 4-15). Le DFP destinataire ***doit*** prendre en charge l'***USB PD*** et ***doit*** prendre en charge la commande ***DR_Swap***. Si l'hôte destinataire prend le rôle de données UFP après son passage à l'état ***Attached.SNK*** et après avoir établi un contrat explicite ***USB PD***, il ***doit*** accepter ou envoyer une commande ***DR_Swap*** afin d'assumer le rôle de données DFP.

4.8.4 Dispositif d'alimentation

Un dispositif d'alimentation est une sous-catégorie de DRP spécifique, capable de fournir une alimentation, mais qui ne peut pas agir comme un hôte USB. Par exemple, l'UFP d'un hub ou d'un moniteur fonctionne comme un dispositif, mais pas comme un hôte.

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Le dispositif d'alimentation ***doit*** suivre les règles applicables aux DRP (voir 4.5.1.4 et la Figure 4-15). Il ***doit*** également suivre les exigences applicables aux sources en tant que sources d'alimentation (voir 4.8.1). Le dispositif d'alimentation ***doit*** prendre en charge l'***USB PD*** et ***doit*** prendre en charge la commande ***DR_Swap***. Si le dispositif d'alimentation prend le rôle de données DFP après son passage à l'état ***Attached.SRC*** et après avoir établi un contrat explicite ***USB PD***, il ***doit*** accepter ou envoyer une commande ***DR_Swap*** afin d'assumer le rôle de données UFP.

4.8.5 Charge d'un système avec une batterie déchargée

Un système qui assume la charge par USB lorsque la batterie est déchargée ***doit*** appliquer la ***Rd*** sur les broches CC1 et CC2 et suivre l'ensemble des règles applicables aux destinataires. Lorsqu'il est connecté à une source, une DRP ou un dispositif d'alimentation, le système reçoit la VBUS par défaut. Il ***peut*** utiliser l'une des méthodes admises pour accroître la quantité d'alimentation qu'il peut utiliser pour charger sa batterie.

Uniquement dans le cas où la batterie du circuit d'application de la ***Rd*** est déchargée, il est nécessaire de garantir le maintien de la tension sur la broche CC dans la même plage que celle de la mise en œuvre du régulateur de tension de la ***Rd***, afin que la source reconnaisse le destinataire et fournisse la VBUS. Par exemple, une résistance à 20 % de la valeur ***Rd*** en série avec un TEC avec $V_{GTH}(max) < V_{CLAMP}(max)$, lorsque la porte est légèrement ramenée sur la broche CC, garantit la détection et peut être retirée lors de l'alimentation.

Lorsqu'un système avec une batterie déchargée présente une charge suffisante, il ***peut*** utiliser le message ***USB PD DR_Swap*** pour devenir un DFP.

4.8.6 Chargeurs multiports USB Type-C

Un chargeur à plusieurs ports USB Type-C est un produit qui expose plusieurs ports sources USB Type-C aux seules fins de la charge de plusieurs dispositifs connectés. Un chargeur USB Type-C conforme ***peut*** annoncer sur chacun de ses ports un ensemble d'options d'alimentation définies en 4.6.

Les chargeurs multiports se déclinent généralement en deux catégories définies ci-après:

1. chargeur à capacité assurée: chargeur multiport pour lequel la somme des capacités maximales de tous les ports exposés (indiquées à l'utilisateur) équivaut à la capacité d'alimentation totale du chargeur. Un port membre d'un groupe à capacité assurée dispose d'une quantité fixe de puissance allouée et est soit un port à capacité garantie, soit un port à capacité gérée, comme cela est défini dans la spécification ***USB PD***;
2. chargeur à capacité partagée: chargeur multiport pour lequel la somme des capacités maximales de tous les ports exposés (indiquées à l'utilisateur) est inférieure à la capacité d'alimentation totale du chargeur. Un port membre d'un groupe à capacité partagée dispose d'une quantité fixe de puissance allouée et est un port à capacité gérée, comme cela est défini dans la spécification ***USB PD***.

Un chargeur multiport ***peut*** comporter, dans un même produit, des groupements de ports de charge visuellement identifiables. Dans ce cas, chaque groupe peut annoncer indépendamment l'une des deux catégories de charge (chargeur à capacité assurée ou chargeur à capacité partagée).

Les informations suivantes définissent les exigences et les lignes directrices relatives au fonctionnement et au comportement d'un chargeur multiport USB Type-C.

4.8.6.1 Exigences générales

Les différents ports sources ***doivent*** toujours satisfaire à la négociation d'alimentation et aux règles établies par les spécifications USB Type-C et ***USB Power Delivery***, qui sont ajustées en fonction des besoins lorsque les ressources disponibles varient selon la consommation électrique des autres ports.

La capacité minimale des différents ports USB Type-C d'un chargeur multiport USB Type-C ***doit*** être de 5 V à 1,5 A, indépendamment du nombre de ports utilisés par ailleurs.

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Les règles suivantes s'appliquent aux chargeurs à capacité partagée:

- La **capacité partagée totale** est la puissance totale disponible pour un groupe de ports à capacité partagée. Il s'agit de la puissance globale disponible lorsqu'aucun des ports du groupe n'est connecté aux destinataires.
- La **puissance restante disponible** est égale à la capacité partagée totale moins la somme de la puissance allouée aux ports branchés. Pour les ports d'un contrat d'alimentation ***USB PD***, la puissance maximale offerte dans les capacités de la source ***USB PD*** est utilisée dans ce calcul, et non la puissance demandée dans le RDO.
- La **puissance disponible du port partagé** est soit:
    a) la PDP du port lorsqu'elle est inférieure ou égale à la puissance restante disponible;
    b) la puissance restante disponible lorsqu'elle est supérieure à 7,5 W et inférieure à la PDP du port; ou
    c) 7,5 W.

Lorsqu'un chargeur à capacité partagée réclame la puissance d'un ou de plusieurs ports déjà connectés pour satisfaire à l'exigence minimale de 7,5 W pour un dispositif qui vient d'être branché, le chargeur ***doit*** utiliser les méthodes de renégociation normalisées du ***courant USB Type-C*** et/ou de l'***USB PD*** et ***ne doit pas*** utiliser les états Hard Reset, ***Error Recovery*** ou ***Disabled***.

Lorsqu'un chargeur USB Type-C comporte des ports de charge équipés d'embases USB Standard-A, les exigences suivantes ***doivent*** être respectées.

- Les ports USB Standard-A ***doivent*** être mis en œuvre comme un groupe indépendant (les ports USB Standard-A ***ne doivent*** donc ***pas*** être inclus dans un groupe de ports USB Type-C en tant que chargeurs à capacité partagée). Toute modification de la charge sur un port USB Type-A ***ne doit pas*** entraîner de variation de la tension sur l'un des ports USB Type-C et inversement.
- La capacité minimale de chaque port USB Standard-A ***doit*** être de 5 V à 500 mA, indépendamment du nombre de ports utilisés.

Note de mise en œuvre: Lors de la conception d'un chargeur à capacité partagée, il convient que l'expérience utilisateur soit un facteur important dans le choix de la capacité partagée totale à prendre en charge. La PDP du port, le nombre de ports et la puissance totale disponible à partager nécessitent certains compromis, dans la mesure où ces facteurs ont une influence notable sur ce à quoi un utilisateur peut s'attendre lorsqu'il charge plusieurs dispositifs.

Le Tableau 4-23 donne des exemples comparatifs d'un chargeur à capacité partagée à 4 ports, afin de montrer l'influence de la PDP et de la capacité partagée totale sur l'expérience utilisateur à mesure qu'augmente le nombre de dispositifs branchés au chargeur. Deux politiques simplistes de partage de puissance sont représentées: une politique "du plus haut au plus faible", qui consiste à fournir la puissance la plus élevée aux ports par ordre de priorité, selon le principe du premier arrivé/premier servi; et une politique de "puissance équilibrée", qui répartit toujours équitablement la puissance entre l'ensemble des ports branchés. Dans ces exemples de politiques, il est pris pour hypothèse que le chargeur n'a pas connaissance des besoins spécifiques du dispositif autres que ce que demande le dispositif lors du choix parmi les capacités annoncées du chargeur, et que l'ordre de branchement des dispositifs va du plus haut consommateur de puissance au plus faible consommateur de puissance.

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Tableau 4-23 Exemples de chargeurs à capacité partagée à 4 ports et de politiques de partage de puissance

	PDP assignée du port	Capacité totale partagée	Du plus haut au plus faible				Équilibré				Notes
			1	2	3	4	1	2	3	4	
1	**7,5 W**	30 W	**7,5**	-	-	-	**7,5**	-	-	-	La mise en œuvre minimale équivaut sur le plan fonctionnel à un groupe de ports assurés, où la capacité totale partagée est égale à la PDP *n*, *n* étant le nombre de ports dans le groupe.
			7,5	**7,5**	-	-	**7,5**	**7,5**	-	-	
			7,5	**7,5**	**7,5**	-	**7,5**	**7,5**	**7,5**	-	
			7,5	**7,5**	**7,5**	**7,5**	**7,5**	**7,5**	**7,5**	**7,5**	
2	**30 W**	30 W	**30**	-	-	-	**30**	-	-	-	Ces exemples de mise en œuvre montrent qu'à mesure que la capacité partagée totale augmente tandis que le nombre de ports et la PDP restent constants, l'expérience utilisateur s'améliore lors de la charge de plusieurs dispositifs. En outre, à mesure que le rapport entre la capacité partagée totale et la PDP assignée du port augmente, la politique de partage du chargeur repose moins sur la récupération de puissance auprès des ports déjà branchés.
			22,5	7,5	-	-	15	15	-	-	
			15	7,5	7,5	-	10	10	10	-	
			7,5	7,5	7,5	7,5	7,5	7,5	7,5	7,5	
3	**30 W**	60 W	**30**	-	-	-	**30**	-	-	-	
			30	**30**	-	-	**30**	**30**	-	-	
			30	22,5	7,5	-	20	20	20	-	
			30	15	7,5	7,5	15	15	15	15	
4	**30 W**	100 W	**30**	-	-	-	**30**	-	-	-	
			30	**30**	-	-	**30**	**30**	-	-	
			30	**30**	**30**	-	**30**	**30**	**30**	-	
			30	**30**	**30**	10	25	25	25	25	

Des politiques plus sophistiquées pourraient être mises en œuvre pour améliorer encore l'expérience utilisateur, vraisemblablement en tenant compte des informations relatives aux capacités récupérées à partir du dispositif. Par exemple, lorsque plusieurs dispositifs sont branchés, les besoins de chaque dispositif peuvent être déterminés et la puissance être allouée pour donner la priorité aux dispositifs qui ont besoin d'une puissance supérieure. À mesure qu'un nouveau dispositif est branché, la puissance peut être rééquilibrée en tenant compte des besoins supplémentaires de chaque nouveau dispositif.

4.8.6.2 Comportements des chargeurs multiports

Chaque port source d'un chargeur à capacité assurée ***doit***, compte tenu de sa conception, se comporter de manière indépendante et ne pas être affecté par l'état ou la charge des autres ports. Une exception à ce comportement est admise si le chargeur doit effectuer une action nécessaire pour satisfaire à une exigence de sécurité fonctionnelle globale du produit, en raison d'un comportement imprévu sur l'un des ports.

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Pour les chargeurs à capacité partagée, les règles de comportement suivantes ***doivent*** s'appliquer.

- Chacun des ports sources exposés ***doit*** avoir les mêmes capacités d'alimentation. Chaque port du chargeur ***doit*** présenter les mêmes capacités minimales et maximales, et pouvoir puiser l'alimentation partagée à parts égales.
    - Les ports ***doivent*** être en mesure d'alimenter la puissance de capacité partagée disponible jusqu'à la puissance maximale du port (PDP).
        - Les ports ***peuvent*** fournir une valeur inférieure à celle-ci, mais ils ***doivent*** l'augmenter jusqu'à la valeur exigée lorsque le destinataire définit le bit de non-correspondance de capacité dans sa réponse. L'opération ***peut*** s'effectuer en plusieurs étapes, mais tous les ports du groupe de capacité partagée doivent atteindre la puissance maximale dans un délai de trois secondes.
    - Chaque fois qu'un contrat d'alimentation est conclu ou modifié sur l'un quelconque des ports, la puissance restante disponible et la puissance disponible du port partagé ***doivent*** être recalculées et la source ***doit*** envoyer des messages de capacité source mis à jour selon les besoins.
    - Les ports ne relevant pas d'un contrat ***USB PD doivent*** respecter les règles d'une source de ***courant USB Type-C*** partagé.
- Tous les ports de ***courant USB Type-C*** exposés ***doivent*** pouvoir fournir les mêmes capacités d'alimentation.
    - Tous les ports ***doivent*** initialement fournir au moins 1,5 A (par exemple, ils ***ne doivent pas*** fournir la valeur par défaut).
    - Le total des valeurs fournies sur tous les ports ne ***doit*** jamais dépasser la capacité de l'alimentation partagée.
    - Les ports qui fournissent au départ 1,5 A ***doivent*** passer à 3 A après branchement s'ils disposent d'une capacité partagée suffisante dans un délai d'une seconde.

Lorsque les ports sources sont connectés et commencent à fournir une alimentation, les ports sources restants doivent offrir les mêmes capacités d'alimentation. La capacité maximale ***peut*** être inférieure à celle des ports précédemment connectés en raison d'une capacité inutilisée inférieure à la capacité d'alimentation électrique totale du chargeur. Par exemple, si la capacité d'alimentation électrique totale d'un chargeur à deux ports USB Type-C est de 60 W avec une PDP de port de 35 W et que le premier port source connecté a établi un contrat d'alimentation de 35 W avec un destinataire connecté, le second port source peut fournir une PDP de 25 W.

Il convient que chaque port commence par fournir la capacité minimale du port, puis augmente l'alimentation fournie au destinataire au moment de la connexion. Par exemple, si la capacité maximale d'un port source USB Type-C exclusif est de 3 A, tous les ports sources exposés sont capables de fournir 3 A. ***Il convient que*** chaque port commence par fournir une alimentation inférieure à la capacité maximale (1,5 A, par exemple), puis augmente l'alimentation fournie à 3 A après un branchement. Cela se produit pour chaque port connecté jusqu'à ce que la capacité partagée inutilisée soit épuisée. À partir de ce point, aucun autre port n'augmente sa capacité à 3 A. Dans cet exemple, un destinataire reçoit une annonce de démarrage d'un ***courant USB Type-C*** de 1,5 A au moment du branchement, puis reçoit une annonce pour une augmentation du ***courant USB Type-C*** à 3 A. Autre exemple, si la capacité maximale d'un port source USB Type-C doit fournir l'***USB PD*** avec une PDP de 35 W, tous les ports sources exposés prennent également en charge l'***USB PD*** à 35 W. Chaque port doit commencer par fournir une alimentation inférieure (comme 15 W) à la connexion initiale, puis augmente l'alimentation fournie avec de nouvelles capacités sources lorsqu'il détermine que le destinataire demande une alimentation supérieure. Si le destinataire ne reçoit pas l'alimentation qu'il exige, il envoie une demande avec le bit d'incohérence de capacité indiquant à la source qu'il souhaite plus de puissance. Cela se produit pour chaque port connecté jusqu'à ce que la capacité partagée inutilisée soit épuisée. À partir de ce point, aucun autre port n'augmente la capacité d'alimentation.

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Lorsqu'il établit la capacité disponible restante, un chargeur prenant en charge le rééquilibrage d'alimentation stratégique ***peut*** inclure l'alimentation qui peut être revendiquée par les ports déjà utilisés:

1. en ajustant l'équivalent des capacités sources annoncées selon une PDP réduite sur un ou plusieurs ports déjà utilisés; ou
2. en émettant une commande ***USB PD*** GotoMin vers un ou plusieurs ports déjà utilisés.

Il convient que le rééquilibrage stratégique de l'alimentation prenne en compte l'expérience utilisateur et préserve les fonctionnalités USB nominales des dispositifs USB affectés. Les algorithmes de rééquilibrage fixes, qui n'intègrent pas la stratégie globale des systèmes USB, ***peuvent ne pas*** être adaptés à la mise en œuvre du rééquilibrage d'alimentation.

4.8.6.3 Étiquetage des ports d'un chargeur multiport

Un étiquetage des ports conçu par l'OEM et conforme aux règles ci-dessous ***doit*** être présent sur les chargeurs multiports.

- Pour les chargeurs à capacité assurée, chaque port source exposé ***doit*** être étiqueté afin d'indiquer la PDP du port. Dans ce cas, l'utilisateur peut prévoir que chaque port étiqueté soit en mesure de satisfaire aux contrats d'alimentation associés à l'étiquetage, indépendamment du nombre de ports sources utilisés.
- Pour les chargeurs à capacité partagée, chaque port source ***doit*** être étiqueté afin d'indiquer la même PDP. En outre, le chargeur ***doit*** comporter une étiquette de portée visuelle identique, qui indique la capacité partagée totale (voir 4.8.6.1) parmi l'ensemble des ports identifiés comme un groupe.

Dans le cas d'un chargeur multiport qui comporte dans un même produit des groupements de ports de charge séparés, chaque groupe ***doit*** être clairement identifié comme un groupement distinct. Chaque groupement ***doit*** être étiqueté séparément, conformément au modèle de fonctionnement du groupe, comme un chargeur à capacité assurée ou comme un chargeur à capacité partagée.

Se reporter à l'USB Implementers Forum (***USB-IF***) pour la certification des chargeurs USB Type-C ainsi qu'aux lignes directrices relatives à l'étiquetage.

4.8.6.4 Chargeurs multiports avec fonctionnalité de hub de données USB

Les chargeurs multiports qui intègrent également une fonctionnalité de hub de données USB ***doivent*** satisfaire aux mêmes exigences que les chargeurs autonomes. Ces hubs de charge ***doivent*** être autoalimentés et ***doivent*** fonctionner intégralement comme des chargeurs, indépendamment de l'état des connexions du bus de données USB.

Dans le cas de chargeurs multiports équipés de hubs et qui alimentent un port orienté en amont (vers l'hôte), ce port ***peut*** se comporter comme un port de charge à capacité assurée (et donc constituer un port de charge spécifique) ou comme un port de charge à capacité partagée (la capacité est partagée avec les ports orientés en aval). Dans ces deux cas, ***il convient*** d'étiqueter clairement le port conformément au comportement attendu et de l'identifier comme le composant d'un groupe lorsqu'il partage la capacité avec les autres ports.

Lorsque le port orienté en amont partage la capacité avec les ports orientés en aval, la PDP du port orienté en amont peut différer de celle des ports orientés en aval.

4.9 Câbles avec marquage électronique

Tous les câbles USB Type-C Complets ***doivent*** comporter un marquage électronique. Les câbles ***USB 2.0*** Type-C ***peuvent*** avoir un marquage électronique. Le marqueur électronique est un élément des câbles avec marquage électronique, qui renvoie des informations sur le câble en réponse à une commande de ***découverte d'identité*** de l'***USB PD***.

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Les câbles avec marquage électronique ***doivent*** prendre en charge la commande ***USB Power Delivery*** Structured VDM ***Discover Identity*** adressée sur SOP' (le marqueur électronique). Cela fournit une méthode de détermination des caractéristiques du câble (courant admissible, performance, identification du fournisseur, etc.). Celle-ci ***peut*** être désignée comme une fonction d'identification des câbles USB Type-C.

Avant un contrat ***USB PD*** explicite, un dispositif d'alimentation peut utiliser SOP' pour découvrir l'identité du câble. Après la négociation d'un contrat ***USB PD*** explicite, seule la source VCONN ***doit*** communiquer avec SOP' et SOP" (voir également 6.1.1).

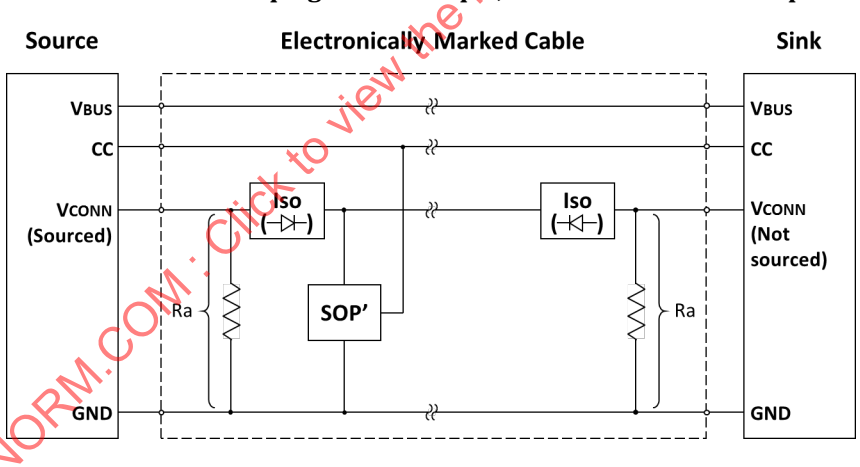
Les câbles passifs qui incluent un marqueur électronique ***doivent*** respecter le diagramme d'états des câbles défini en 4.5.2.4 et à la Figure 4-20.

Dès que la VCONN est disponible, tous les câbles avec marquage électronique ***doivent*** l'utiliser comme seule source d'alimentation. Si la VCONN est appliquée après la VBUS, tant que la VCONN n'est pas disponible, le câble ***peut*** rester non alimenté ou ***peut*** puiser la puissance dans la VBUS. Dans le délai ***tVCONNSwitch***, le câble ***doit*** basculer de la VBUS à la VCONN. Les câbles qui incluent un marqueur électronique ***doivent*** satisfaire à l'alimentation maximale définie dans le Tableau 4-6. La seule exception est un Câble actif à isolation optique (OIAC, Article 6), qui peut puiser tant de la VCONN que de la VBUS.

Voir le Tableau 4-5 pour connaître les exigences relatives aux sources d'alimentation de la VCONN. En l'absence de VCONN, un câble sous tension ***ne doit pas*** interférer avec le fonctionnement normal de la broche CC, y compris pour la détection du destinataire, l'annonce du courant et les opérations ***USB PD***.

La Figure 4-43 représente un câble avec marquage électronique classique. Les éléments d'isolation (Iso) ***doivent*** empêcher la VCONN de parcourir le câble d'une extrémité à l'autre. La ***Ra*** est exigée dans le câble pour que la source détermine si la VCONN est nécessaire.

Figure 4-43 Câble avec marquage électronique, VCONN étant connectée par le câble

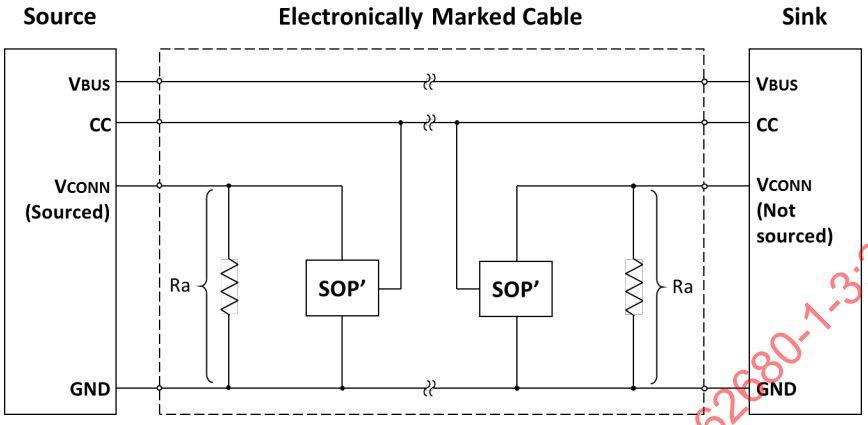


Anglais	Français
Source	Source
Electronically Marked Cable	Câble avec marquage électronique
Sink	Destinataire
(Sourced)	(Sourcée)
(Not Sourced)	(Non sourcée)

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La Figure 4-44 représente un câble avec marquage électronique, pour lequel le fil de la VCONN ne s'étend pas par le câble. Par conséquent, un élément SOP' (marqueur électronique) est exigé à chaque extrémité du câble. Dans ce cas, aucun élément d'isolation n'est nécessaire.

Figure 4-44 Câble avec marquage électronique, avec SOP' à chaque extrémité



Anglais	Français
Source	Source
Electronically Marked Cable	Câble avec marquage électronique
Sink	Destinataire
(Sourced)	(Sourcée)
(Not Sourced)	(Non sourcée)

Pour les câbles qui répondent uniquement à SOP', l'emplacement du répondeur n'est pas pertinent.

4.9.1 Valeurs de paramètres

Le Tableau 4-24 fournit les exigences de temporisation de mise sous tension pour que les marqueurs électroniques SOP' et SOP" soient prêts à communiquer.

Tableau 4-24 Temporisation SOP' et SOP"

	Valeur maximale	Description
tVCONNStable	50 ms	Délai entre l'application de la VCONN et le moment auquel SOP' et SOP" ***doivent*** être prêts à communiquer.

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4.9.2 Câbles actifs

Un câble actif est un câble avec marquage électronique qui intègre des circuits de traitement des signaux en bus de données, par exemple pour permettre la mise en œuvre de câbles plus longs. Les câbles actifs avec conditionnement des signaux en bus de données sur chaque fiche ***doivent*** mettre en œuvre SOP' et ***peuvent*** mettre en œuvre SOP". Les câbles actifs ***doivent*** satisfaire aux exigences d'alimentation définies dans le Tableau 4-6.

Les câbles actifs ***peuvent*** prendre en charge une paire TX/RX ou deux paires TX/RX. Le marqueur électronique du câble ***doit*** identifier le nombre de voies TX/RX prises en charge. Les câbles actifs ***peuvent*** ou ***peuvent ne pas*** exiger une gestion de la configuration. La gestion de la configuration des câbles actifs est définie à l'Article 6.

4.10 Accessoires alimentés par VCONN (VPA) et dispositifs USB alimentés par VCONN (VPD)

Les ***accessoires alimentés par VCONN*** et les ***dispositifs USB alimentés par VCONN*** sont des destinataires à connexion directe qui peuvent fonctionner uniquement avec la VCONN.

Ils exposent une impédance maximale de mise à la masse de ***Ra*** sur la broche VCONN et de ***Rd*** sur la broche CC.

Le retrait de la VCONN en l'absence de VBUS ***doit*** être traité comme un événement de déconnexion.

4.10.1 Accessoires alimentés par VCONN (VPA)

Un ***accessoire alimenté par VCONN*** met en œuvre un ***mode alternatif*** (voir l'Annexe E).

Les ***accessoires alimentés par VCONN*** ***doivent*** se conformer au Tableau 4-7.

Lorsqu'ils fonctionnent avec le rôle de destinataire et en l'absence de VBUS, les ***accessoires alimentés par VCONN*** ***doivent*** traiter l'application de la VCONN comme un signal de connexion et ***doivent*** répondre aux messages ***USB Power Delivery***.

Lorsqu'ils sont alimentés uniquement par la VCONN, les ***accessoires alimentés par VCONN*** ***doivent*** négocier un ***mode alternatif***. S'ils ne réussissent pas à négocier un ***mode alternatif*** dans le délai ***tAMETimeout***, leur port partenaire retire la VCONN.

Lorsque la VBUS est fournie, un ***accessoire alimenté par VCONN*** est soumis à toutes les exigences relatives aux ***modes alternatifs***, y compris la présentation d'une interface ***USB Billboard Device Class*** lorsque la négociation d'un ***mode alternatif*** échoue.

Si un ***accessoire alimenté par VCONN*** demande à fournir une fonctionnalité de charge, il doit négocier la tension et le courant de manière indépendante sur l'hôte et les ports de charge, et il doit probablement réajuster la tension de la source avant de la transmettre au destinataire. Le destinataire peut absorber l'intégralité du courant que lui a annoncé l'***accessoire alimenté par VCONN***.

4.10.2 Dispositifs alimentés par VCONN (VPD)

Un ***dispositif USB alimenté par VCONN*** ***doit*** mettre en œuvre un point d'extrémité USB UFP.

Les ***dispositifs USB alimentés par VCONN*** ***doivent*** se conformer au Tableau 4-8.

En l'absence de VBUS, les ***dispositifs USB alimentés par VCONN*** ***doivent*** traiter l'application de la VCONN comme un signal de connexion.

Un ***dispositif USB alimenté par VCONN*** ***doit*** répondre aux messages ***USB PD*** sur SOP' et ***ne doit pas*** répondre aux autres messages ***USB PD***. Un ***dispositif USB alimenté par VCONN*** ***doit*** répondre aux signaux ***USB PD*** Hard Reset et Cable Reset.

Un ***dispositif USB alimenté par VCONN*** de charge ***doit*** rejeter tous les messages ***USB PD*** pendant qu'une connexion est activée entre la broche CC du port hôte et la broche CC du port de charge.

Lorsque la VBUS est fournie par l'hôte, le ***dispositif USB alimenté par VCONN*** ***doit*** se comporter comme un destinataire UFP normal, mais ne doit répondre qu'aux messages ***USB PD*** sur SOP'. Si la VBUS est retirée par la suite et que la VCONN reste appliquée, le ***dispositif USB alimenté par VCONN*** ***doit*** rester connecté et utiliser la VCONN comme signal de déconnexion exclusif.

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Étant donné que les ***dispositifs USB alimentés par VCONN*** ne répondent pas aux messages ***USB PD*** sur SOP, ils ne peuvent pas entrer dans l'un des ***modes alternatifs***.

Un ***dispositif USB alimenté par VCONN*** ***peut*** fournir des fonctionnalités de charge par le ***VPD***. Les ***dispositifs USB alimentés par VCONN*** ***ne doivent pas*** assurer de transfert de données vers le port de charge autrement que par le fil CC.

Puisque la négociation de la puissance et du CC est transférée directement, le destinataire ***doit*** limiter son courant maximal en fonction de l'impédance supplémentaire induite par le ***dispositif USB alimenté par VCONN***.

De plus, comme l'alimentation peut uniquement passer du port de charge à l'hôte, la VCONN doit être fournie par l'hôte. Il n'y a aucune connexion de données en aval du fil CC transférée à la source connectée. Il existe des limitations concernant ce que l'hôte peut annoncer et prendre en charge par l'***USB PD***:

- l'hôte ***ne doit pas*** négocier ni accepter de ***PR_Swap*** ou de ***VCONN_Swap***;
- l'hôte ***ne doit pas*** activer de ***FR_Swap***;
- l'hôte ne ***peut*** négocier une ***DR_Swap*** que lorsqu'il utilise l'***USB PD*** Révision 2.0, et uniquement afin d'alterner le côté qui déclenche les communications PD; l'hôte reste toujours un DFP pour les données USB;
- l'hôte ***ne doit pas*** annoncer de données double fonction ni d'alimentation double fonction dans ses messages de capacité de source ou de capacité de destinataire (l'hôte modifie ses capacités annoncées en rôle UFP/destinataire uniquement);
- l'hôte ***ne doit*** négocier aucun ***mode alternatif*** qui modifie la fonction des broches sur le connecteur;
- l'hôte ***doit*** se représenter auprès de la source de charge avec l'***USB PD***, comme s'il s'agissait d'un dispositif destinataire uniquement sans données.

Tableau 4-25 Exigences relatives à l'impédance CC du VPD de charge (RccCON)

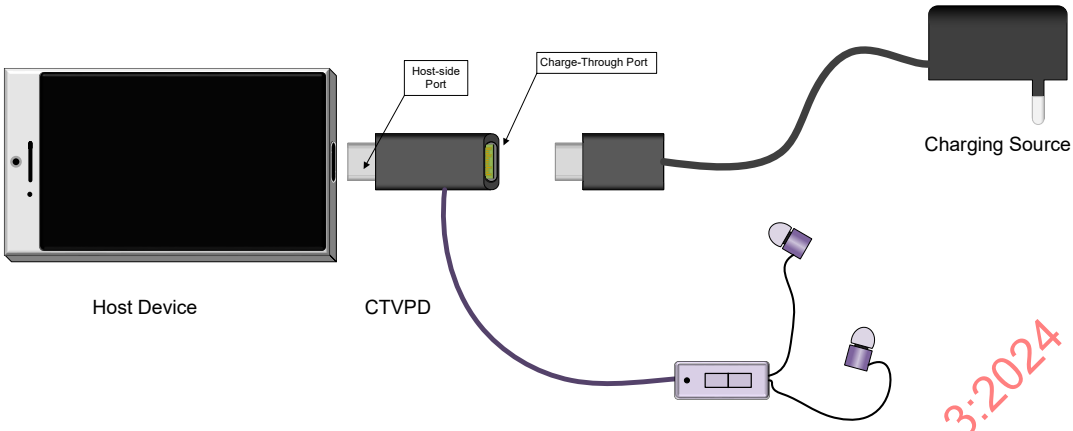
	Valeur minimale	Valeur maximale	Description
RccCON		15 Ω	Impédance dans le ***VPD*** de charge pendant qu'une connexion est activée entre la broche CC du port hôte et la broche CC du port de charge.
	zOPEN		Impédance entre la broche CC du port hôte et la broche CC de charge lorsqu'une connexion est désactivée.

Tableau 4-26 Exigences relatives au découplage de la VBUS du port de charge du CTVPD

	Valeur minimale	Valeur maximale	Description
CCTB	1 µF	10 µF	Capacité de découplage sur la connexion VBUS du port de charge pour prendre en charge ADP max CADP_THR.

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Figure 4-45 Exemple de cas d'utilisation d'un dispositif USB alimenté par VCONN de charge



Anglais	Français
Host device	Dispositif hôte
Host-side port	Port côté hôte
Charge through port	Port en charge simultanée
Charging source	Source de charge

4.11 Valeurs de paramètres

4.11.1 Paramètres de terminaison

Le Tableau 4-27 fournit les valeurs qui ***doivent*** être utilisées pour la ***Rp*** de la source, ou la source de courant. Les autres tensions de polarisation ***doivent*** être admises si elles restent inférieures à 5,5 V et respectent la plage de tensions applicables côté destinataire (voir le Tableau 4-35, le Tableau 4-36 et le Tableau 4-37). Note: Lorsque deux sources sont connectées ensemble, elles ***peuvent*** utiliser des méthodes de terminaison différentes qui peuvent entraîner un flux de courant inattendu.

Tableau 4-27 Exigences relatives aux terminaisons CC de la source (Rp)

Annonce de la source	Source de courant jusqu'à 1,7 V-5,5 V	Polarisation de la résistance jusqu'à 4,75 V – 5,5 V	Polarisation de la résistance jusqu'à 3,3 V ± 5 %
Puissance USB par défaut	80 µA ± 20 %	56 kΩ ± 20 % (Note 1)	36 kΩ ± 20 %
1,5 A à 5 V	180 µA ± 8 %	22 kΩ ± 5 %	12 kΩ ± 5 %
3,0 A à 5 V	330 µA ± 8 %	10 kΩ ± 5 %	4,7 kΩ ± 5 %

Note 1: Pour une ***Rp*** mise en œuvre dans une fiche USB Type-C sur un ensemble câble-connecteurs USB Type-C vers ***USB 3.1*** Standard-A, un ensemble câble-connecteurs USB Type-C vers ***USB 2.0*** Standard-A, un ensemble adaptateur USB Type-C vers embase ***USB 2.0*** Micro-B ou un câble USB Type-C captif connecté à un hôte USB, une valeur de 56 kΩ ± 5 % ***doit*** être utilisée afin d'assurer une tolérance sur chutes de tension ohmique sur les bornes VBUS et GND de l'ensemble câble-connecteurs.

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Le destinataire ***peut*** juger plus commode de mettre en œuvre la ***Rd*** simultanément sur plusieurs chemins (une plage ***Rd*** étendue lorsqu'il est hors tension et une plage ***Rd*** réduite lorsqu'il est sous tension). Les transitions entre les mises en œuvre de la ***Rd*** qui ne dépassent pas le délai ***tCCDebounce*** ***ne doivent pas*** être interprétées comme dépassant la plage de ***Rd*** étendue. Les transitions entre les mises en œuvre de la ***Rd*** ***ne doivent pas*** entraîner une augmentation de la tension sur la broche CC en dehors de la plage de tensions qui définit une connexion. Le Tableau 4-28 fournit les méthodes et les valeurs qui ***doivent*** être utilisées pour la mise en œuvre de la ***Rd*** du destinataire.

Tableau 4-28 Exigences relatives aux terminaisons CC du destinataire (Rd)

Mise en œuvre de la Rd	Valeur nominale	La capacité d'alimentation peut-elle être détectée?	Tension maximale sur la broche
Régulateur de tension ±20 %[1]	1,1 V	Non	1,32 V
Résistance à la masse ±20 %	5,1 kΩ	Non	2,18 V
Résistance à la masse ±10 %	5,1 kΩ	Oui	2,04 V
Note 1: La mise en œuvre du régulateur bloque la communication ***USB PD*** bien que le système puisse démarrer avec le régulateur et basculer vers la résistance dès qu'il peut exécuter l'***USB PD***.			

Le Tableau 4-29 fournit la valeur de l'impédance à la masse de la VCONN des câbles alimentés.

Tableau 4-29 Exigences relatives aux terminaisons des câbles alimentés

	Impédance minimale	Impédance maximale
Ra	800 Ω[1]	1,2 kΩ

Note:
1. L'impédance minimale ***peut*** être inférieure après l'application de la VCONN. Le courant consommé de la VCONN ***doit*** être tel qu'il est spécifié dans le Tableau 4-6, le Tableau 4-7 et le Tableau 4-8 lorsque la tension est inférieure à vVCONNValid. La tension sur la ***Ra*** connectée à une ***Rp*** valide ***doit*** être inférieure à la tension maximale du Tableau 4-39 (Tension sur les broches CC d'un destinataire (annonces de courant de plusieurs sources)) pour la ***vRa***.

Le Tableau 4-30 fournit la valeur de l'impédance à la masse minimale sur la broche CC pour qu'un dispositif (destinataire ou source) ne soit pas détecté par une source. Cela ***doit*** s'appliquer aux ports à l'état ***Disabled*** ou à l'état ***ErrorRecovery***. Cela ***doit*** également s'appliquer aux sources non alimentées (par exemple, un transformateur débranché de l'alimentation secteur en courant alternatif).

Tableau 4-30 Exigences relatives aux terminaisons CC pour les états Disabled, ErrorRecovery et Unpowered Source

	Impédance minimale à la masse	Notes
zOPEN	126 kΩ	***zOPEN doit*** uniquement être évalué sous ***vCC-Clamp***.

Le Tableau 4-31 fournit la valeur de l'impédance pour qu'une broche SBU apparaisse ouverte.

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Tableau 4-31 Exigences relatives aux terminaisons SBU

	Terminaison	Notes
zSBUTermination	≥ 950 kΩ	Fonctionnellement équivalent à un circuit ouvert

4.11.2 Paramètres de temporisation

Le Tableau 4-32 fournit les valeurs de temporisation qui ***doivent*** être respectées à des fins d'alimentation par la VBUS et la VCONN.

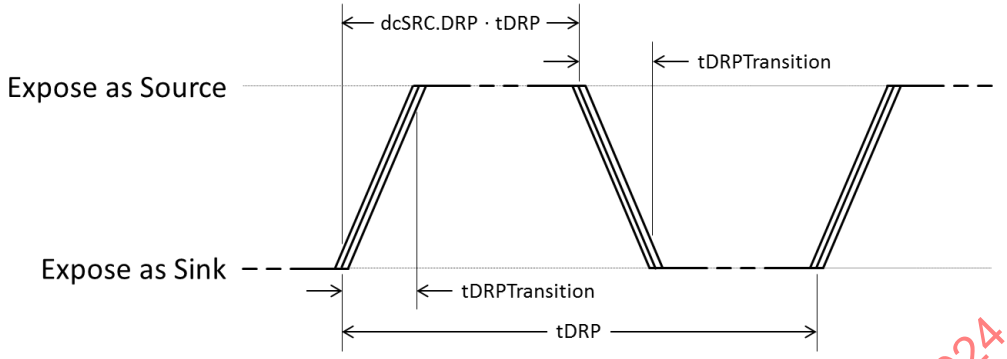
Tableau 4-32 Paramètres de temporisation de la VBUS et de la VCONN

	Valeur minimale	Valeur maximale	Description
tVBUSON	0 ms	275 ms	À compter du passage à l'état ***Attached.SRC*** et jusqu'à concurrence du seuil minimal ***vSafe5V*** pour la VBUS, mesuré sur l'embase de la source.
tVBUSOFF	0 ms	650 ms	À compter du débranchement du destinataire et jusqu'à concurrence du seuil minimal ***vSafe0V*** pour la source, qui retire la VBUS (voir l'***USB PD***).
tVsafe0V	0 ms	650 ms	Délai que peut utiliser la source pour décharger les condensateurs du destinataire afin d'atteindre ***vSafe0V*** dans le délai ***AttachWait.SRC*** et ainsi passer à l'état ***Attached.SRC***
tVCONNON	Note 1	2 ms	À compter du moment auquel la source fournit la VBUS à l'état ***Attached.SRC***. Mesuré entre ***vSafe5V*** et la tension minimale de la VCONN (voir le Tableau 4-5)
tVCONNON-PA	0 ms	100 ms	À compter du moment auquel un destinataire avec prise en charge des accessoires passe à l'état ***PoweredAccessory*** et jusqu'à ce que le destinataire fournisse la tension VCONN minimale (voir le Tableau 4-5)
tVCONNOFF	0 ms	35 ms	À compter du débranchement d'un destinataire ou, selon la demande, jusqu'à ce que l'alimentation VCONN soit déconnectée.
tSinkAdj	***tRpValueChange*** (min)	60 ms	Délai de réponse d'un destinataire pour adapter sa consommation de courant dans la plage spécifiée, en raison d'une modification d'annonce de ***courant USB Type-C***.
Note 1: La VCONN ***peut*** être appliquée avant la VBUS.			

La Figure 4-46 représente les paramètres de temporisation associés au processus d'alternance de la DRP. Le paramètre ***tDRP*** représente la période globale d'un cycle simple pendant lequel le port est exposé à la fois comme une source et comme un destinataire. Le tronçon de la période où la DRP est exposée comme une source est établi par ***dcSRC.DRP*** et le délai de transition maximal entre les états d'exposition est dicté par le délai ***tDRPTransition***.

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Figure 4-46 Temporisation des DRP



Anglais	Français
Expose as a Source	Exposé en tant que Source
Expose as a Sink	Exposé en tant que Destinataire

Le Tableau 4-33 fournit les valeurs de temporisation auxquelles les DRP ***doivent*** satisfaire. Afin de réduire le plus possible la probabilité que deux DRP échouent indéfiniment dans la résolution d'une relation source-destinataire, ***il convient que*** l'horloge utilisée pour contrôler la permutation de rôles d'une DRP ne soit pas composée d'éléments de précision (résonateurs en cristal ou céramique, etc.). De même, ***il convient que*** le pourcentage de temps qu'une DRP consacre à l'annonce de la source ne soit pas issu d'une source de temporisation de précision.

Tableau 4-33 Paramètres de temporisation des DRP

	Valeur minimale	Valeur maximale	Description
tDRP	50 ms	100 ms	Période pendant laquelle une DRP ***doit*** effectuer une annonce source destinataire et inversement
dcSRC.DRP	30 %	70 %	Pourcentage de temps qu'une DRP ***doit*** consacrer à l'annonce de la source pendant le délai ***tDRP***
tDRPTransition	0 ms	1 ms	Délai pendant lequel une DRP ***doit*** effectuer les transitions entre les rôles de source et de destinataire au cours d'une résolution de rôles
tDRPTry	75 ms	150 ms	Délai d'attente associé à l'état ***Try.SRC***
tDRPTryWait	400 ms	800 ms	Délai d'attente associé à l'état ***Try.SNK***
tTryTimeout	550 ms	1100 ms	Délai de transition de l'état ***Try.SRC*** à l'état ***TryWait.SNK***
tVPDDetach	10 ms	20 ms	Délai pendant lequel une DRP doit détecter que le dispositif USB alimenté par VCONN de charge a été débranché, lorsque la VBUS a été retirée.

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Le Tableau 4-34 fournit les exigences de temporisation associées aux comportements de connexion des broches CC.

Tableau 4-34 Paramètres de temporisation des CC

	Valeur minimale	Valeur maximale	Description
tCCDebounce	100 ms	200 ms	Délai d'attente qu'un port ***doit*** respecter avant de pouvoir déterminer qu'il est branché
tPDDebounce	10 ms	20 ms	Délai d'attente qu'un port destinataire ***doit*** respecter avant de pouvoir déterminer qu'il est débranché, en fonction du potentiel de signalisation ***USB PD*** sur la broche CC, comme cela est décrit dans les définitions d'état
tTryCCDebounce	10 ms	20 ms	Délai d'attente qu'un port ***doit*** respecter avant de pouvoir déterminer qu'il est rebranché au cours du processus tentative-attente
tErrorRecovery	25 ms		Délai pendant lequel un port autoalimenté ***doit*** rester à l'état ***ErrorRecovery***
	240 ms		Délai pendant lequel une source ***doit*** rester à l'état ***ErrorRecovery*** si elle alimentait VCONN dans l'état précédent
tRpValueChange	10 ms	20 ms	Délai d'attente qu'un port destinataire ***doit*** respecter avant de pouvoir déterminer que la ***Rp*** a fait l'objet d'une modification, selon laquelle la broche CC n'est pas à l'état BMC Idle ou le port ne peut pas détecter l'état BMC Idle
	0 ms	5 ms	Délai d'attente qu'un port destinataire ***doit*** respecter avant de pouvoir déterminer que la ***Rp*** a fait l'objet d'une modification lorsque la signalisation ***USB PD*** peut être détectée par le port et que la ligne CC est à l'état BMC Idle
tSRCDisconnect	0 ms	20 ms	Délai pendant lequel une source ***doit*** détecter l'état ***SRC.Open*** ***Il convient*** que la source détecte l'état ***SRC.Open*** le plus rapidement possible
tNoToggleConnect	0 ms	5 ms	Délai nécessaire pour détecter une connexion lorsqu'aucun des ports partenaires n'est alterné
tOnePortToggleConnect	0 ms	80 ms	Délai nécessaire pour détecter une connexion lorsqu'un port partenaire est alterné (0 ms … ***dcSRC.DRP*** max * ***tDRP*** max + 2 * ***tNoToggleConnect***)
tTwoPortToggleConnect	0 ms	510 ms	Délai nécessaire pour détecter une connexion lorsque les deux ports partenaires sont alternés (0 ms … 5 * ***tDRP*** max + 2 * ***tNoToggleConnect***)
tVPDCTDD	30 µs	5 ms	Délai nécessaire à un dispositif USB alimenté par VCONN de charge pour détecter que la source de charge a été déconnectée de la broche CC lorsque la VBUS a été retirée, passer à l'état ***CTUnattached.VPD*** et réappliquer la terminaison ***Rp*** qui annonce 3,0 A sur la broche CC du port hôte

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	Valeur minimale	Valeur maximale	Description
tVPDDisable	25 ms		Délai pendant lequel un dispositif USB alimenté par VCONN de charge ***doit*** rester à l'état ***CTDisabled.VPD***

4.11.3 Paramètres de tension

Le Tableau 4-35, le Tableau 4-36 et le Tableau 4-37 fournissent les valeurs de la tension CC qu'une source ***doit*** utiliser pour détecter qu'elle est branchée par rapport au ***courant USB Type-C*** (USB par défaut, 1,5 A à 5 V ou 3,0 A à 5 V) annoncé par la source.

Tableau 4-35 Tensions CC côté source – USB par défaut

	Tension minimale	Tension maximale	Seuil
Câble/adaptateur alimenté (vRa)	0,00 V	0,15 V	0,20 V
Destinataire (vRd)	0,25 V	1,50 V	1,60 V
Sans connexion (vOPEN)	1,65 V		

Tableau 4-36 Tensions CC côté source – 1,5 A à 5 V

	Tension minimale	Tension maximale	Seuil
Câble/adaptateur alimenté (vRa)	0,00 V	0,35 V	0,40 V
Destinataire (vRd)	0,45 V	1,50 V	1,60 V
Sans connexion (vOPEN)	1,65 V		

Tableau 4-37 Tensions CC côté source – 3,0 A à 5 V

	Tension minimale	Tension maximale	Seuil
Câble/adaptateur alimenté (vRa)	0,00 V	0,75 V	0,80 V
Destinataire (vRd)	0,85 V	2,45 V	2,60 V
Sans connexion (vOPEN)	2,75 V		

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Le Tableau 4-38 fournit les valeurs de la tension CC qui ***doivent*** être détectées par le biais de la ***Rd*** d'un destinataire qui ne prend pas en charge les annonces supérieures à celles du ***courant USB Type-C*** par défaut de la source.

Tableau 4-38 Tension sur les broches CC d'un destinataire – Courant USB Type-C par défaut uniquement

Détection	Tension minimale	Tension maximale	Seuil
vRa	–0,25 V	0,15 V	0,2 V
vRd-Connect	0,25 V	2,18 V	

Le Tableau 4-39 fournit les valeurs de la tension CC qui ***doivent*** être détectées par le biais de la ***Rd*** d'un destinataire qui met en œuvre la détection d'annonces supérieures à celles du ***courant USB Type C*** par défaut de la source. Ce tableau prend en compte l'effet de la chute de tension ohmique par la masse du câble sur la tension par la ***Rd*** du destinataire.

Tableau 4-39 Tension sur les broches CC d'un destinataire – Annonces de courant de plusieurs sources

Détection	Tension minimale	Tension maximale	Seuil
vRa	−0,25 V	0,15 V	0,2 V
vRd-Connect	0,25 V	2,04 V	
vRd-USB	0,25 V	0,61 V	0,66 V
vRd-1.5	0,70 V	1,16 V	1,23 V
vRd-3.0	1,31 V	2,04 V	

Le Tableau 4-40 donne la tension de blocage que tout port (Source, Destinataire ou DRP) ***peut*** appliquer sur sa broche CC pour la protéger. L'intégration d'un blocage ***ne doit pas*** avoir d'incidence sur la fonctionnalité lorsque la broche CC fonctionne comme une source ou un destinataire VCONN.

Tableau 4-40 Tension de blocage de la broche CC

	Tension minimale
vCC-Clamp	2,9 V

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5 Découverte et mise en service *USB4*

La découverte et la mise en service de l'***USB4*** diffèrent considérablement de celles de l'***USB 2.0*** et de l'***USB 3.2***. Le présent article définit le processus de découverte, par le biais d'une connexion USB Type-C, de la compatibilité ***USB4*** (ou non) de deux ports partenaires. Le côté DFP de la liaison doit prendre une décision concernant la mise en service (ou non) de l'***USB4*** et déterminer la manière dont cette mise en service est effectuée.

5.1 Vue d'ensemble du processus de découverte et de mise en service

Les informations ci-dessous fournissent une vue d'ensemble du processus général de découverte et de mise en service de l'***USB4***.

1. Les diagrammes d'états de connexion CC USB Type-C résolvent les rôles de source/destinataire et les rôles de données initiaux (DFP/UFP).
2. L'alimentation initiale de la VBUS et de la VCONN est fournie.
3. Le protocole ***USB Power Delivery*** est utilisé pour établir un contrat d'alimentation entre les ports partenaires.
4. Le DFP utilise le processus de ***découverte d'identité*** de l'***USB PD*** pour identifier les capacités du port partenaire (SOP).
5. Le DFP utilise le processus de ***découverte d'identité*** de l'***USB PD*** pour identifier les capacités du câble (SOP').
6. Si le câble et le port partenaire prennent en charge l'***USB4***, le DFP envoie des messages ***USB PD Enter_USB*** au câble (s'il s'agit d'un câble actif) et au port partenaire pour mettre en service l'***USB4***.
7. Si les deux ports partenaires sont compatibles DRD (données double fonction), le DFP ou l'UFP peut, ***de manière facultative***, lancer une permutation de rôles de données pour permuter les rôles d'hôte et de dispositif.

Les trois premières étapes ci-dessus sont les mêmes que celles utilisées pour toutes les connexions USB afin d'établir des relations de port et l'alimentation entre les ports partenaires. L'étape 5 au cours de laquelle le câble est interrogé sur ses capacités ***peut de manière facultative*** se produire au cours de l'étape 3. Il est possible de réaliser cette étape avant s'il est nécessaire que la source sache si le câble prend en charge un courant supérieur à 3 A.

En fonction de la relation de source d'alimentation obtenue après les premières étapes, l'utilisation du message ***USB PD DR_Swap peut*** être nécessaire pour établir le port partenaire le plus proche de l'hôte en tant que DFP de rôle de données. Par exemple, un hub alimente un hôte et ***DR_Swap*** est utilisée pour corriger les rôles de données entre le hub et l'hôte.

Lorsque les capacités du port partenaire sont identifiées par le DFP, il ***peut*** être approprié, en fonction de ce qui est découvert sur le port partenaire, d'interroger également le port partenaire avec le processus de découverte SVID ***USB PD*** en ***mode alternatif*** comme extension de l'étape 4. Dans certaines situations, un port partenaire prend en charge des ***modes alternatifs*** qui ***peuvent*** également être utilisés pendant le fonctionnement ***USB4***; cela est découvert lors de cette requête supplémentaire.

Lorsque les capacités du câble sont identifiées par le DFP, il ***peut*** être approprié, en fonction de ce qui est découvert sur le câble, d'interroger également le câble avec le processus de découverte SVID ***USB PD*** en ***mode alternatif*** comme extension de l'étape 5. Dans certaines situations, un câble prend en charge le ***mode alternatif Thunderbolt 3*** qui ***peut*** également être utilisé pendant le fonctionnement ***USB4***; cela est découvert lors de cette requête supplémentaire.

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Le fonctionnement ***USB4*** est mis en service à l'aide d'un message ***USB PD Enter_USB***. Ce message est envoyé au câble (SOP' et SOP", le cas échéant) et au port partenaire (SOP), chacun d'eux répondant par un message d'***acceptation*** afin de confirmer et d'établir lorsque le câble ou le port partenaire est prêt et opérationnel pour le fonctionnement ***USB4***. Si le câble à utiliser fonctionne en ***mode alternatif Thunderbolt 3***, il est activé avec la commande ***USB PD*** Enter Mode au lieu du message ***USB PD Enter_USB*** (voir l'Annexe F).

L'***USB4*** permet de connecter de manière fonctionnelle deux plateformes hôtes et d'établir un canal de données entre les hôtes. Cela dépend de la capacité d'au moins une de ces plateformes hôtes à effectuer des opérations de données double fonction, de sorte qu'une relation de données DFP-UFP USB Type-C appropriée puisse être établie entre elles. Dans la plupart des cas, les deux plateformes hôtes sont compatibles DRD. Après établissement du fonctionnement ***USB4***, l'une de ces plateformes hôtes peut choisir de modifier son rôle dans la relation DFP-UFP. Pour ce faire, le processus ***USB PD DR_Swap*** est utilisé à l'étape 7 ci-dessus.

5.2 Exigences fonctionnelles concernant l'*USB4*

Les exigences fonctionnelles suivantes s'appliquent aux hôtes et aux dispositifs ***USB4***.

5.2.1 Exigences fonctionnelles concernant les hôtes *USB4*

Les hôtes ***USB4 doivent*** satisfaire aux exigences fonctionnelles suivantes:

- Les hôtes ***USB4*** qui prennent en charge les données double fonction (DRD) ***doivent*** répondre à la commande de ***découverte d'identité USB PD*** avec les VDO de DFP et d'UFP.

5.2.2 Exigences fonctionnelles concernant les dispositifs USB

Les dispositifs ***USB4 doivent*** satisfaire aux exigences fonctionnelles suivantes:

- Les dispositifs ***USB4 doivent*** répondre à la commande de ***découverte d'identité*** de l'***USB PD*** avec les VDO UFP.
- Le dispositif ***USB4 doit*** fournir une interface USB exposant une classe ***USB Billboard Device Class*** lorsqu'il ne peut pas se connecter en tant que dispositif ***USB4*** et lorsqu'il ne prend pas en charge et n'affiche pas de fonctionnalité équivalente à celle d'un ***mode alternatif***, de l'***USB 3.2*** et/ou de l'***USB 2.0*** dans le délai ***tUSB4Timeout***.
- Si le dispositif ***USB4*** prend en charge les ***modes alternatifs***, il ***doit*** terminer le processus de découverte et de mise en service de l'***USB4*** (concluant ou non) avant de revenir à l'***USB 3.2*** ou à l'***USB 2.0*** et d'exposer une classe ***USB Billboard Device Class*** appropriée.

5.2.3 Prise en charge du mode alternatif *USB4*

La spécification ***USB4*** permet aux produits d'être conçus pour prendre en charge les ***modes alternatifs***, notamment le ***DisplayPort Alt Mode*** et le ***Thunderbolt 3 Alt Mode***. Contrairement aux hubs ***USB 3.2*** et ***USB 2.0***, cela inclut également la prise en charge de ***modes alternatifs*** spécifiques sur les hubs ***USB4***.

5.2.3.1 Prise en charge des modes alternatifs *USB4* sur les hôtes

Pour les hôtes ***USB4*** qui mettent en œuvre le tunneling ***DisplayPort***, le ***mode alternatif DP*** avec prise en charge multifonction (signalisation du canal DP_BR 1 associée à la prise en charge de l'***USB 3.2***), défini par la spécification ***DP Alt Mode***, ***doit*** être mis en œuvre sur tous leurs DFP USB Type-C.

L'hôte ***USB4 doit*** prendre en charge le premier écran ***DisplayPort*** connecté sur l'un de ses ports USB Type-C. La prise en charge des ***écrans connectés*** ultérieurement est ***facultative***.

Les hôtes ***USB4 peuvent***, ***de manière facultative***, mettre en œuvre la prise en charge de compatibilité ***TBT3*** définie par la spécification ***USB4*** sur leurs DFP USB Type-C.

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5.2.3.2 Prise en charge du mode alternatif *USB4* sur les hubs et les stations d'accueil *USB4*

Les hubs ***USB4*** et les stations d'accueil ***USB4 doivent*** mettre en œuvre le ***mode alternatif DP*** avec prise en charge multifonction (signalisation du canal DP_BR 1 associée à la prise en charge ***USB 3.2***), défini par la spécification ***DP Alt Mode*** sur tous leurs DFP USB Type-C.

Les hubs ***USB4 doivent*** prendre en charge le premier écran ***DisplayPort*** connecté sur l'un de leurs DFP USB Type-C. La prise en charge des ***écrans connectés*** ultérieurement est ***facultative***.

Les stations d'accueil ***USB4 doivent*** prendre en charge le premier écran connecté sur l'un de leurs DFP USB Type-C ou de leurs connecteurs d'affichage non USB (le cas échéant et de manière collective). La prise en charge des écrans connectés ultérieurement est ***facultative***.

Les hubs ***USB4 doivent*** mettre en œuvre la prise en charge de compatibilité ***TBT3*** définie par la spécification ***USB4*** sur leurs DFP USB Type-C. Les stations d'accueil ***USB4 doivent*** mettre en œuvre la prise en charge de compatibilité ***TBT3*** définie par la spécification ***USB4*** sur leurs UFP USB Type-C et sur leurs DFP USB Type-C.

Pour les hubs ***USB4***, les ports orientés en aval ***ne doivent pas*** mettre en œuvre de ***modes alternatifs*** sans ID normalisé ***USB-IF*** (SID) ni de modes accessoires.

5.3 Exigences d'alimentation *USB4*

L'***USB4*** exige que la connexion d'alimentation entre les ports partenaires soit établie et maintenue à l'aide de l'***USB PD*** avant et pendant le fonctionnement ***USB4***. Un port ***USB4***, avant d'entrer en fonctionnement ***USB4***, ***doit*** fonctionner comme un port ***USB 3.2*** en ce qui concerne l'alimentation (voir 4.6). L'***USB4*** n'utilise pas les protocoles de dispositifs USB définis dans l'***USB 2.0*** et l'***USB 3.2*** pour gérer l'alimentation des dispositifs.

5.3.1 Exigences d'alimentation de la source

Pour les ports USB Type-C qui prennent en charge le fonctionnement du bus de données ***USB4***, les exigences suivantes ***doivent*** être respectées.

- Les ports ***USB4 doivent*** pouvoir fournir au moins 7,5 W (c'est-à-dire 5 V à 1,5 A) sur la VBUS aux dispositifs ***USB4*** alimentés par VBUS.
- La capacité minimale d'alimentation des dispositifs alimentés par bus sur les ports compatibles avec les données ***doit*** être respectée indépendamment sur chaque port USB Type-C d'un hôte ou d'un hub à plusieurs ports.

5.3.2 Exigences d'alimentation du destinataire

Pour les dispositifs ***USB4*** qui dépendent de l'alimentation du bus pour fonctionner (indépendamment de tout besoin de charge), les exigences suivantes ***doivent*** être respectées.

- Les dispositifs ***USB4*** ne ***doivent*** puiser que jusqu'à 250 mA sur la VBUS lorsque la source annonce la puissance USB par défaut (voir 4.11.1) avant qu'un contrat d'alimentation ***USB PD*** ne soit conclu entre le dispositif et son port partenaire.
    - Les dispositifs ***USB4 peuvent*** puiser des niveaux de puissance plus élevés avant de conclure un contrat d'alimentation ***USB PD*** si la source annonce un ***courant USB Type-C*** de 1,5 A ou 3,0 A.
- Les dispositifs ***USB4 doivent*** être au moins capables de fonctionner avec une source qui ne fournit que jusqu'à 7,5 W (c'est-à-dire 5 V à 1,5 A).
- Les dispositifs ***USB4 ne doivent pas*** activer le fonctionnement du bus de données ***USB4*** tant qu'un contrat d'alimentation ***USB PD*** n'a pas été établi. Pendant le fonctionnement ***USB4***, le dispositif ***doit*** toujours se conformer aux exigences de comportement d'alimentation ***USB PD***, y compris en répondant de manière appropriée aux modifications des capacités de la source.

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Dans les cas où les capacités fonctionnelles complètes ou les performances les plus élevées du dispositif ***USB4*** nécessitent une puissance plus importante que celle fournie par l'hôte, le dispositif ***doit*** être au moins capable de fournir à l'utilisateur les capacités de base prévues pour le type et les fonctions répertoriées du dispositif. Cela admet un niveau de fonctionnement ou de performance plus élevé lorsqu'un niveau de puissance plus élevé est fourni (par exemple, 15 W pour la fonctionnalité complète, contre 7,5 W pour la fonctionnalité de base). Dans ce cas, le dispositif ***doit*** exposer une interface ***USB Billboard Device Class*** s'il n'est pas en mesure de fournir une fonctionnalité équivalente limitée par la puissance disponible.

5.3.3 Exigences relatives à la gestion de l'alimentation d'un dispositif

Pour l'***USB4***, la gestion de l'alimentation d'un dispositif est activée à l'aide d'une combinaison de capacités ***USB PD*** qui fonctionne conjointement avec les états de liaison ***USB4*** de la connexion UFP du dispositif.

La connexion entre l'UFP du dispositif et son port partenaire DFP peut être placée dans un état de veille en fonction de la valeur du fanion de prise en charge de la veille USB dans le message Source-Capabilities utilisé dans le contrat d'alimentation ***USB PD*** explicite.

Lorsque le fanion de prise en charge de la veille USB est défini par la source, le destinataire ***doit*** satisfaire aux exigences d'alimentation en mode veille lorsque la liaison ***USB4*** est à l'état CLd. Avant que la liaison ne passe à l'état CLd, il est attendu que l'hôte place toutes les fonctions du dispositif dans un état de veille approprié.

L'alimentation en mode veille est définie en fonction des capacités du dispositif ***USB4***.

- Dispositif ***USB4*** qui ne peut pas être réveillé à distance ou dont le réveil à distance est désactivé: 25 mW.
- Dispositif ***USB4*** qui prend en charge le réveil à distance et dont le réveil à distance est activé: 50 mW.

Si la source efface le fanion de prise en charge de la veille USB, le destinataire ***doit*** respecter les exigences d'alimentation du contrat explicite, quel que soit l'état de la liaison ***USB4***. Pour l'***USB4***, l'utilisation d'un courant ***USB PD*** négocié à zéro n'est pas une méthode d'entrée en mode veille valide, car elle n'est pas coordonnée avec le système d'exploitation hôte et les pilotes de dispositifs fonctionnels.

5.4 Exigences relatives au processus de découverte et de mise en service de l'*USB4*

Le présent paragraphe décrit les exigences relatives à la découverte et la mise en service de l'***USB4***. Les exigences supplémentaires concernant le fonctionnement ***USB4*** se trouvent dans la spécification ***USB4***.

Avant et pendant le fonctionnement ***USB4***, les exigences fonctionnelles de l'Article 4 ***doivent*** être respectées, y compris l'ensemble des exigences relatives à l'interface fonctionnelle et au canal de configuration (CC).

5.4.1 Connexion USB Type-C initiale

Pour un port compatible ***USB4***, avant d'initier une découverte de câbles et de dispositifs ***USB4***, une connexion source-destinataire valide ***doit*** exister et le port ***doit*** être à l'état ***Attached.SRC*** ou à l'état ***Attached.SNK*** dans le diagramme d'états de connexion USB Type-C.

Lorsque deux ports de données double fonction (DRD) ***USB4*** sont connectés ensemble, par exemple deux hôtes ***USB4***, le processus de connexion USB Type-C établit les rôles de données initiaux entre les ports partenaires.

Après établissement des rôles de données initiaux, le DFP ***USB4 peut*** immédiatement former la liaison pour l'***USB 3.2***. Si un UFP est compatible ***USB4***, il ***doit*** suspendre l'exposition de l'identification de vitesse ***USB 2.0*** (voir 7.1.5. de la spécification ***USB 2.0***) et les terminaisons du récepteur ***USB 3.2*** jusqu'à réception d'un message ***USB PD Enter_USB***, jusqu'à la mise en service (avec toute réaffectation éventuelle des broches) en ***mode alternatif*** ou jusqu'à l'expiration du délai ***tUSB4Timeout***.

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5.4.2 Contrat d'alimentation USB

Avant d'initier la découverte de dispositifs ***USB4***, les ports partenaires ***doivent*** négocier un contrat ***USB PD*** explicite.

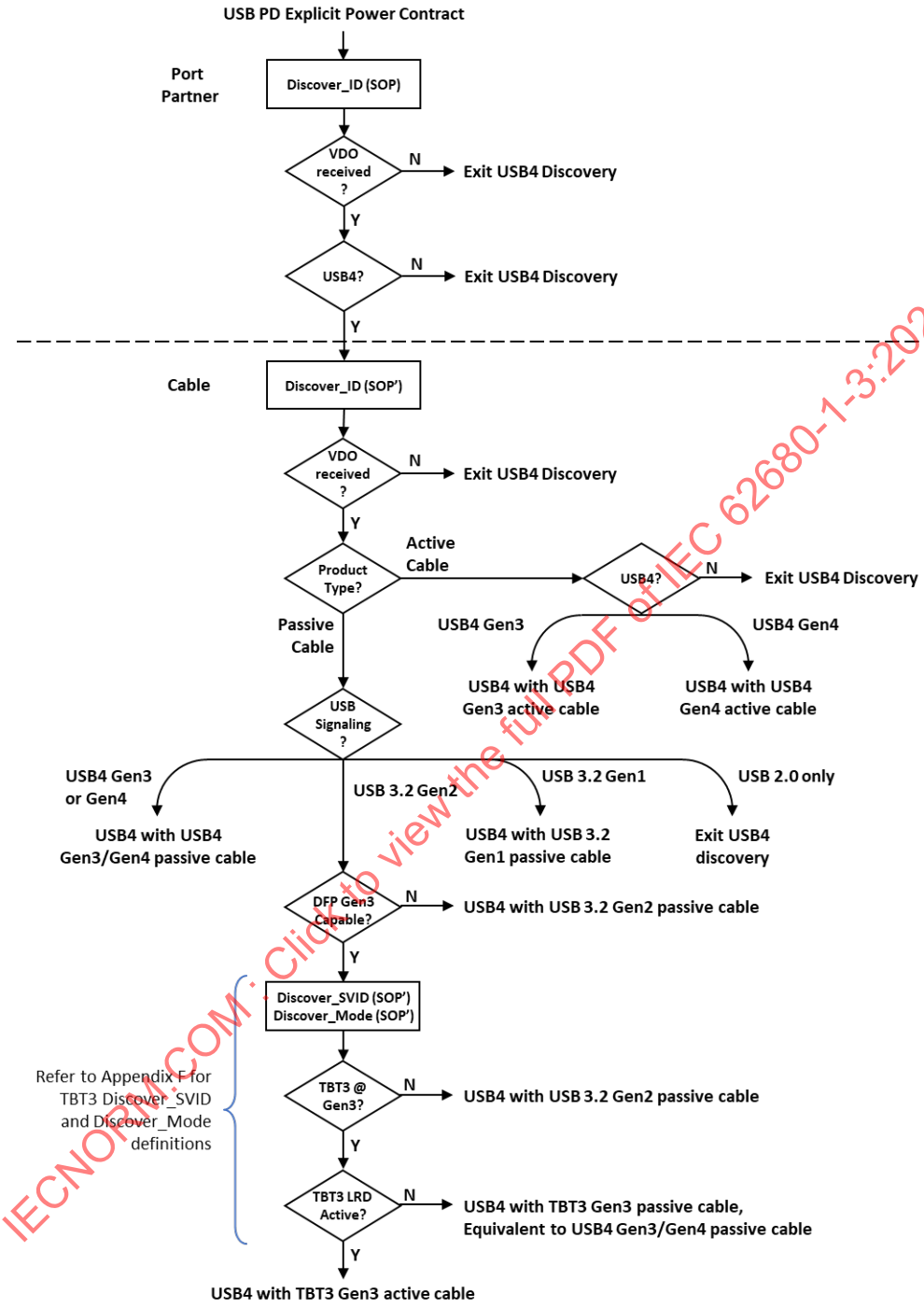
Au cours du processus d'établissement d'un contrat ***USB PD*** explicite stable, la source ou le destinataire ***peut*** avoir initié des permutations du rôle d'alimentation et de la VCONN. Avant de passer à la découverte de l'***USB4***, le rôle de données fonctionnel ***doit*** être correctement établi (par exemple, un port de hub autoalimenté orienté en amont est une DRP qui apparaît comme une source où ***DR_Swap*** est exigée pour le rôle de données approprié du hub) et le DFP ***doit*** être la source de la VCONN.

5.4.3 Processus de découverte et de mise en service de l'USB4

La Figure 5-1 représente le modèle de base du processus de découverte et de mise en service de l'***USB4***.

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Figure 5-1 Modèle du processus de découverte et de mise en service de l'*USB4*



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Anglais	Français
USB PD explicit power contract	Contrat d'alimentation explicite USB PD
Port Partner	Port partenaire
Discover_ID (SOP)	Discover_ID (SOP)
Discover_ID (SOP')	Discover_ID (SOP')

Anglais	Français
Cable	Câble
VDO received?	VDO reçues?
Exit USB4 discovery	Quitter la découverte USB4
Product type?	Type de produit?
Passive cable	Câble passif
Active cable	Câble actif
USB signaling?	Signalisation USB?
USB4 with USB4 Gen3 active cable	USB4 avec câble actif USB4 Gen3
USB4 with USB4 Gen4 active cable	USB4 avec câble actif USB4 Gen4
USB4 Gen3 or Gen4	USB4 Gen3 ou Gen4
USB 2.0 only	USB 2.0 exclusif
USB4 with USB4 Gen3/Gen4 passive cable	USB4 avec câble passif USB4 Gen3/Gen4
USB4 with USB 3.2 Gen1 passive cable	USB4 avec câble passif 3.2 Gen1
USB4 with USB 3.2 Gen2 passive cable	USB4 avec câble passif 3.2 Gen2
DFP Gen3 Capable?	Compatible DFP Gen3?
USB 2.0 only	USB 2.0 uniquement
DFP Gen3 capable?	Compatible DFP Gen3?
TBT3 LRD Active?	TBT3 LRD actif?
USB4 with TBT3 Gen3 passive cable, Equivalent to USB4 Gen3/Gen4 passive cable	USB4 avec câble passif TBT3 Gen3, Équivalent au câble passif USB4 Gen3/Gen4
Refer to Appendix F for TBT3 Discover_SVID and Discover_Mode definitions	Voir les définitions de l'Annexe F pour TBT3 Discover_SVID et Discover_Mode
N	N
Y	O

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5.4.3.1 Découverte de ports partenaires *USB4* (SOP)

La découverte de ports partenaires ***USB4*** ne ***doit*** avoir lieu qu'après avoir négocié un contrat ***USB PD*** explicite.

La découverte de ports partenaires ***USB4*** implique d'utiliser le processus de découverte d'ID ***USB PD*** entre le DFP et son port partenaire (SOP).

Le port partenaire ***USB4*** à découvrir peut être tout produit compatible avec les données qui se présente comme port partenaire de l'UFP au cours du processus de découverte. Selon le type et les capacités du port partenaire, les VDO d'UFP et de DFP ***peuvent*** être retournés en réponse à la commande ***USB PD*** Discover_ID (SOP) du DFP. Pour autant qu'au moins l'un de ces VDO est reçu, ***il convient que*** le DFP évalue la capacité de son port partenaire à prendre en charge le fonctionnement ***USB4*** en fonction du contenu des VDO reçus. Pour un VDO d'UFP reçu, cela dépend du champ Device Capability (B27...24). Pour un VDO de DFP reçu, cela dépend du champ Host Capability (B26...24).

Voir l'Annexe I pour des informations et des recommandations supplémentaires sur l'utilisation des types de produits et des VDO d'UFP et de DFP.

5.4.3.2 Découverte de câbles *USB4* (SOP')

Le DFP ***doit*** déterminer si le câble branché est compatible ***USB4*** avant d'activer le fonctionnement ***USB4***. Lorsque le dispositif ***USB4*** est directement connecté ou est équipé d'un câble captif, ce dispositif ***USB4*** doit répondre à la découverte de câbles ***USB4*** sur SOP' en tant que câble captif passif et indiquer la prise en charge de signalisation USB appropriée.

Le Tableau 5-1 récapitule les câbles destinés à prendre en charge les opérations compatibles ***USB4***. En ce qui concerne les câbles actifs, cette liste n'inclut pas les câbles actifs à isolation optique (OIAC) qui doivent être traités comme un cas particulier étant donné que ces câbles ne prennent pas en charge l'***USB 2.0*** ni l'alimentation électrique par câble (voir l'Article 6).

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Tableau 5-1 Câbles certifiés lorsqu'un fonctionnement compatible *USB4* est attendu

	Signalisation par câble	**Fonctionnement *USB4***	**Notes**
Câbles USB Type-C Complet (passifs)	***USB 3.2*** Gen1	20 Gbit/s	Ce câble indique la prise en charge de l'***USB 3.2*** Gen1 (001b) dans le champ USB Signaling de la réponse de VDO d'un câble passif. Note: Même si ce câble n'est pas explicitement soumis à l'essai, certifié ni estampillé pour le fonctionnement ***USB 3.2*** Gen2, l'***USB4*** Gen2 fonctionne généralement.
	USB 3.2 Gen2 (***USB4*** Gen2)	20 Gbit/s	Ce câble indique la prise en charge de l'***USB 3.2*** Gen2 (010b) dans le champ USB Signaling de la réponse de VDO d'un câble passif.
	USB4 Gen4 (***USB4*** Gen3)	80 Gbit/s	Ce câble indique la prise en charge de l'***USB4*** Gen3 (011b) ou de l'***USB4*** Gen4 (100b) dans le champ USB Signaling de la réponse de VDO d'un câble passif.
Câbles Thunderbolt™ 3 (passifs)	***TBT3*** Gen2 (***USB 3.2*** Gen1 ou ***USB4*** Gen2)	20 Gbit/s	Ce câble indique la prise en charge de l'***USB 3.2*** Gen1 (001b) ou de l'***USB 3.2*** Gen2 (010b) dans le champ USB Signaling de la réponse de VDO d'un câble passif.
	TBT3 Gen3 (***USB4*** Gen4)	80 Gbit/s	En plus d'indiquer la prise en charge de l'***USB 3.2*** Gen2 (010b) dans le champ USB Signaling de la réponse de VDO d'un câble passif, ce câble indique qu'il prend en charge ***TBT3*** Gen3 dans le paramètre de vitesse du câble et le câble passif dans le paramètre Active_Passive de la réponse de VDO de découverte de mode.[2]
Câbles Thunderbolt™ 3 (circuit d'amplification linéaire actif)	***TBT3*** Gen3 (***USB4*** Gen3)	40 Gbit/s	En plus d'indiquer la prise en charge de l'***USB 3.2*** Gen2 (010b) dans le champ USB Signaling de la réponse de VDO d'un câble passif, ce câble indique qu'il prend en charge ***TBT3*** Gen3 dans le paramètre de vitesse du câble et le câble actif dans le paramètre Active_Passive de la réponse de VDO de découverte de mode.[2]
Câbles USB Type-C Complet (actifs)[1]	***USB4*** Gen2	20 Gbit/s	Ce câble indique la prise en charge de l'***USB4*** Gen2 (010b) dans le champ USB Signaling de la réponse de VDO d'un câble actif.
	USB4 Gen3	40 Gbit/s	Ce câble indique la prise en charge de l'***USB4*** Gen3 (011b) dans le champ USB Signaling de la réponse de VDO d'un câble actif.
	USB4 Gen4	80 Gbit/s	Ce câble indique la prise en charge de l'***USB4*** Gen4 (100b) dans le champ USB Signaling de la réponse de VDO d'un câble actif.

Note 1: Les câbles USB SuperSpeed actifs ne prennent pas en charge le fonctionnement compatible ***USB4***.

Note 2: Voir F.2.6 et le Tableau F-11.

La détermination de la compatibilité ***USB4*** du câble lance l'utilisation du processus de découverte d'ID ***USB PD*** entre le DFP et le câble branché (SOP'). Si aucune réponse n'est reçue lorsque le DFP émet une commande de découverte d'ID ***USB PD*** sur le câble, le processus de découverte ***USB4 doit*** alors être arrêté et le DFP ***doit*** établir une connexion fonctionnelle à son port partenaire UFP d'après le processus ***USB 2.0*** traditionnel.

La prise en charge compatible ***USB4*** est généralement déterminée en fonction de la prise en charge de la signalisation USB indiquée dans les réponses de VDO d'un câble et appropriée au type de câble, passif ou actif.

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Les câbles passifs compatibles sont ceux qui indiquent une prise en charge de la signalisation USB pour Gen1 ou plus, et les câbles actifs compatibles sont ceux qui indiquent une prise en charge de la signalisation USB pour Gen2 ou plus.

Lorsqu'un câble passif est identifié comme un câble ***USB 3.2*** Gen2 et que le DFP est compatible Gen3, il est nécessaire que le DFP effectue une vérification supplémentaire en utilisant le processus ***USB PD*** en ***mode alternatif*** pour déterminer si le câble est un câble passif ***Thunderbolt 3*** prenant en charge Gen3.

Certains câbles actifs ***Thunderbolt 3 peuvent ne pas*** prendre en charge le fonctionnement ***USB4***, la découverte et l'utilisation de ces câbles étant ***facultatives***. Pour plus d'informations sur la manière de découvrir et de prendre en charge ces câbles, voir l'Annexe F.

5.4.3.2.1 Découverte de câbles passifs

La spécification ***USB PD*** définit les réponses de VDO d'un câble passif à la commande de ***découverte d'identité*** envoyée par le DFP à un câble passif compatible ***USB4***.

Si le champ USB Signaling [B2…0] de la réponse de VDO d'un câble passif est 011b (***USB4*** Gen3) ou 100b (***USB4*** Gen4), le processus de découverte ***USB4*** est terminé et le fonctionnement ***USB4*** jusqu'à 80 Gbit/s est pris en charge. À l'Article 3 de la présente spécification, ces ensembles câble-connecteurs sont ceux qui portent les références suivantes: CC4G3-3, CC4G3-5 et CC4G3-5E répertoriés dans le Tableau 3-1.

Si le champ USB Signaling [B2…0] de la réponse de VDO d'un câble passif est 000b (***USB 2.0*** exclusif), le processus de découverte ***USB4*** est terminé et le DFP ***doit*** continuer et établir une connexion fonctionnelle à son port partenaire UFP d'après le processus ***USB 2.0*** traditionnel.

Si le champ USB Signaling [B2…0] de la réponse de VDO d'un câble passif est 010b (***USB 3.2*** Gen2) ou 001b (***USB 3.2*** Gen1), le processus de découverte ***USB4*** est terminé si le DFP est limité à l'***USB4*** Gen2. À l'Article 3 de la présente spécification, ces ensembles câble-connecteurs sont ceux qui portent les références suivantes: CC3G2-3, CC3G2-5, CC3G1-3 et CC3G1-3 répertoriés dans le Tableau 3-1. Noter qu'il est attendu que les câbles ***USB 3.2*** Gen1, bien qu'ils ne soient pas soumis à l'essai ni certifiés pour le fonctionnement ***USB 3.2*** Gen2, soient adaptés au fonctionnement ***USB4*** Gen2.

Si le champ USB Signaling [B2…0] de la réponse de VDO d'un câble passif est 010b (***USB 3.2*** Gen2), mais que le DFP est capable de fonctionner avec l'***USB4*** Gen3, le DFP ***doit*** alors utiliser le processus ***USB PD*** en ***mode alternatif*** pour déterminer si le câble peut également être identifié comme un câble ***TBT3*** Gen3. Pour le processus de découverte de câbles ***TBT3***, voir 5.4.3.2.3. Si le champ Cable Speed de la réponse de VDO de découverte de mode est défini sur 011b, le processus de découverte ***USB4*** est terminé et le fonctionnement ***USB4*** jusqu'à Gen3 est pris en charge par le câble passif ***TBT3*** (voir le Tableau F-11).

5.4.3.2.2 Découverte de câbles actifs

La spécification ***USB PD*** définit les réponses de VDO d'un câble actif à la commande de ***découverte d'identité*** envoyée par le DFP à un câble actif compatible ***USB4***.

Si le champ USB Signaling Support [B2…0] de la réponse de VDO 1 d'un câble actif est 011b (***USB4*** Gen3), le processus de découverte ***USB4*** est terminé et le fonctionnement ***USB4*** jusqu'à Ge3 est pris en charge. Si le champ USB Signaling Support [B2…0] de la réponse de VDO 1 d'un câble actif est 100b (***USB4*** Gen4), le processus de découverte ***USB4*** est terminé et le fonctionnement ***USB4*** jusqu'à Gen4 est pris en charge.

De manière facultative, la découverte et l'utilisation de câbles actifs ***TBT3*** existants qui indiquent la prise en charge du fonctionnement à un débit de données arrondi sont admises si le câble actif n'est pas explicitement identifié comme compatible ***USB4***.

Tout échec de l'identification d'un câble actif connecté comme étant compatible ***USB4*** entraîne l'arrêt du processus de découverte ***USB4*** et le retour aux processus ***USB 3.2*** et ***USB 2.0*** traditionnels.

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5.4.3.2.3 Processus de découverte de câbles Thunderbolt™ 3

La spécification ***USB PD*** définit le processus de découverte des câbles activés en ***mode alternatif***. Les informations ci-dessous récapitulent le processus propre à la découverte des câbles ***Thunderbolt 3*** pour déterminer la compatibilité ***USB4***. Avant d'effectuer ces étapes, le processus de ***découverte d'identité USB PD*** a déjà été utilisé en vue d'établir si le câble est passif ou actif.

Les étapes suivantes permettent de découvrir les câbles ***Thunderbolt 3*** et leurs capacités à l'aide du processus ***USB PD*** en ***mode alternatif***.

1. Le DFP envoie la commande de découverte de SVID au SOP' du câble.
2. Si la réponse du câble à la commande de découverte de SVID indique 0x8087 (Intel/***TBT3***) comme l'un de ses SVID, passer à l'étape suivante. Sinon, le câble n'est pas un câble ***Thunderbolt 3*** (voir F.2.4).
3. Le DFP émet la commande de découverte de mode avec un SVID défini sur 0x8087 sur le SOP' du câble.
4. Si cette découverte fait partie du processus de découverte de câbles actifs compatibles ***USB4***, à partir des réponses de VDO des modes découverte du câble (voir F.2.6), extraire la valeur du champ Cable Speed pour terminer le processus. En outre, si ce câble est un câble LRD ***TBT3***, comme l'indique la réponse de VDO de découverte de mode du câble (bit 22 = 0 et bit 25 = 1), alors le DFP ***peut***, ***de manière facultative***, envoyer au câble un message ***USB PD Enter_USB*** ou une ***USB PD*** Enter Mode.
5. Si cette découverte fait partie du processus de découverte de câbles actifs compatibles ***USB4***, à partir des réponses de VDO de découverte de mode du câble (voir F.2.6), extraire la valeur du champ TBT_Rounded_Support pour terminer le processus. [Note: La découverte et l'utilisation de câbles actifs ***TBT3*** compatibles ***USB4*** est une fonctionnalité ***facultative*** qui exige d'utiliser également la commande ***USB PD*** Enter Mode afin d'activer le câble pour le fonctionnement ***USB4***.]

5.4.3.3 Mise en service de l'*USB4*

La mise en service de l'***USB4*** ne ***doit*** avoir lieu qu'après avoir établi que le câble branché, le cas échéant, et le port partenaire sont compatibles ***USB4***.

La mise en service de l'***USB4*** implique d'utiliser le processus du message ***USB PD Enter_USB*** entre le DFP et le câble branché compatible ***USB4*** ainsi que le port partenaire compatible ***USB4***. L'envoi de ce message suit un ordre spécifique: SOP' en premier, SOP'' en deuxième, le cas échéant, et SOP en troisième. Pour les câbles passifs, il n'est pas nécessaire d'envoyer le message ***USB PD Enter_USB*** à SOP' et SOP".

Lors de l'utilisation du message ***USB PD Enter_USB*** afin d'activer le fonctionnement ***USB4***, le DFP ***doit*** indiquer 010b (***USB4***) dans le champ USB Mode de l'objet de données ***USB PD Enter_USB***. Les champs restants ***doivent*** être définis de manière appropriée par le DFP en fonction des capacités du DFP et du câble branché.

5.4.4 Fonctionnement après mise en service de l'*USB4*

5.4.4.1 Pendant le fonctionnement *USB4*

En fonctionnement ***USB4***, les opérations suivantes sont admises:

- Le contrat d'alimentation ***USB PD*** explicite ***peut*** être renégocié.
- Émettre une commande ***USB PD*** Data_Reset pour modifier le mode de fonctionnement (par exemple, ***USB4*** vers ***USB 3.2*** ou un ***mode alternatif***).
- Activer les ***modes alternatifs*** qui ne reconfigurent pas l'interface des ports et fonctionnent en parallèle avec l'***USB4***.

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5.4.4.2 Sortie du fonctionnement *USB4*

Le processus ***USB PD*** Data_Reset entraîne la réinitialisation des connexions de données USB et la sortie des ***modes alternatifs***. Ce processus ne modifie pas le contrat d'alimentation et les rôles de données existants entre les ports partenaires. Le processus Data_Reset ***doit*** comprendre les étapes suivantes:

- Adresser une commande ***USB PD*** Data_Reset au port partenaire SOP pour réinitialiser le bus de données, réinitialiser le câble et quitter l'ensemble des ***modes alternatifs*** tout en conservant l'alimentation sur la VBUS.
- Les temporisateurs ***tUSB4Timeout*** et ***tAMETimeout*** de l'UFP ***doivent*** être réinitialisés lors de l'envoi ou de la réception d'une commande ***USB PD*** Data_Reset.
- Renouveler le processus de découverte et mise en service de l'***USB4*** (voir 5.4.3).

5.5 Exigences relatives à la connexion des hubs *USB4*

Le comportement des hubs ***USB4*** concernant la gestion de ses connexions DFP a des dépendances spécifiques ***USB4*** sur l'état de la connexion et les capacités de son UFP unique. De plus, les hubs ont des responsabilités ***USB4*** spécifiques pour communiquer les capacités de l'hôte ***USB4*** aux hubs ***USB4*** connectés en aval. Le présent paragraphe fournit à la fois les exigences et les recommandations relatives au comportement de connexion des ports d'un hub ***USB4***.

5.5.1 Exigences relatives à la connexion initiale des ports d'un hub *USB4*

Les exigences suivantes s'appliquent à tous les ports de hub:

1. exécuter le processus de connexion USB Type-C;
2. établir un contrat ***USB PD*** explicite initial;
3. le cas échéant, utiliser ***USB PD PR_Swap*** pour établir le rôle d'alimentation préférentiel; et
4. utiliser ***USB PD DR_Swap*** pour établir le rôle de données afin d'être cohérent avec la position du port dans l'arborescence USB si cela est nécessaire.

5.5.2 Découverte des capacités de l'hôte et de l'UFP d'un hub *USB4*

Les capacités des DFP d'un hub ***USB4*** reposent en fin de compte sur celles de son UFP (après établissement d'une connexion à l'hôte). Si l'UFP d'un hub USB4 est connecté à un hub ***USB4*** en amont, les capacités de connexion entre les deux hubs ***peuvent ne pas*** représenter au départ les capacités jusqu'à l'hôte.

Les informations ci-dessous récapitulent les principes généraux qui guident comment les capacités UFP et hôte affectent les connexions DFP.

- La connexion en aval à un dispositif ou un hub branché au DFP d'un hub ***USB4*** repose sur les capacités du hub.
- Après établissement de la connexion de l'UFP d'un hub ***USB4***, les capacités du hub sont limitées aux capacités de cette connexion à l'UFP.
- Lorsque la connexion à l'UFP d'un hub ***USB4*** indique qu'un hôte n'est pas présent, lorsque le hub est averti qu'un hôte est présent, il est nécessaire que le hub limite ses capacités en fonction de celles de l'hôte.
    - Toutes les connexions aux DFP du hub ***USB4*** qui existaient avant la présence de l'hôte sont ajustées pour s'aligner sur les variations de capacités, si cela est nécessaire.
- Lorsqu'un hôte est présent dans une arborescence ***USB4***, tous les hubs intermédiaires mettent à jour leurs connexions pour s'aligner sur les capacités de l'hôte, car l'état de présence de l'hôte est propagé vers les hubs ***USB4*** connectés en aval.

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Les capacités de l'UFP du hub reposent sur l'un des critères suivants:

- Un message ***USB PD Enter_USB*** indique le fonctionnement USB (***USB4***, ***USB 3.2*** ou ***USB 2.0***) et les caractéristiques associées prises en charge (***USB4*** PCIe, ***USB4 DP***, etc.) par le port partenaire en amont.
- Une commande ***USB PD*** Enter Mode lance un ***mode alternatif*** pris en charge (***Thunderbolt 3***, ***DisplayPort***).
- Aucun message ***USB PD Enter_USB*** n'est reçu dans le délai ***tUSB4Timeout***, ou le message ***USB PD*** Enter Mode est reçu dans le délai ***tAMETimeout*** et indique que seuls l'***USB 3.2*** et l'***USB 2.0*** sont disponibles.

Si l'UFP du hub ***USB4*** est connecté à un hub ***USB4*** en amont, les capacités signalées dans le message ***USB PD Enter_USB*** reçu ***doivent*** uniquement être interprétées comme les capacités de l'hôte si le bit Host Present est défini. Si le bit Host Present est réinitialisé, le hub ***doit*** alors attendre de recevoir un autre message ***USB PD Enter_USB*** avec le groupe de bits Host Present. Lorsque le bit Host Present est défini, les capacités représentées dans le message ***USB PD Enter_USB*** peuvent être utilisées comme capacités de l'hôte en vue d'établir les connexions finales au DFP.

Si l'UFP du hub ***USB4*** reçoit un message ***USB PD Enter_USB*** qui indique que le fonctionnement USB est l'***USB 3.2*** ou l'***USB 2.0***, le hub ***USB4 ne doit pas*** attendre la fin du délai ***tUSB4Timeout*** pour continuer et établir ses connexions à l'UFP et au DFP conformément aux exigences respectivement relatives aux hubs ***USB 3.2*** ou ***USB 2.0***.

5.5.3 Exigences relatives à la connexion au DFP d'un hub

5.5.3.1 Connexions spéculatives

Lorsqu'un dispositif est connecté au DFP d'un hub ***USB4*** avant que l'UFP du hub ne soit connecté et que les capacités de l'hôte soient connues, le hub se connecte de façon spéculative au dispositif branché en fonction des exigences suivantes.

- Utiliser la découverte d'ID ***USB PD*** et le processus ***USB PD*** en ***mode alternatif*** pour déterminer l'intégralité des capacités du câble et du dispositif branchés.
- À partir des capacités découvertes, établir la connexion la plus performante en fonction des capacités du DFP du hub ***USB4*** selon l'ordre de priorité suivant:
    1. ***USB4***
    2. ***mode alternatif Thunderbolt 3;***
    3. ***mode alternatif DP;***
    4. ***USB 3.2***
    5. ***USB 2.0***
- Interdire les notifications d'état des ports et les chemins de données en amont des DFP du hub ***USB4*** en attendant que la connexion à l'UFP du hub ***USB4*** soit établie.

5.5.3.2 Connexions fonctionnelles

Lorsque la connexion à l'UFP du hub ***USB4*** a été établie et que les capacités de l'hôte sont déterminées (voir 5.5.2), le hub ***doit*** évaluer chaque connexion au DFP existante en fonction des capacités associées à la connexion à l'UFP du hub et effectuer l'une des actions suivantes:

- Si la connexion au DFP s'aligne correctement sur les capacités de la connexion à l'UFP, activer les notifications d'état et le chemin de données pour ce port.

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- Si la connexion au DFP ne s'aligne pas correctement sur les capacités de la connexion à l'UFP, la connexion au DFP ***doit*** effectuer l'une des opérations suivantes:
    - si l'UFP reste en ***USB4*** et que la connexion au DFP s'effectue avec un hub ***USB4*** en aval, envoyer un message ***USB PD Enter_USB*** révisé avec le groupe de bits Host Present;
    - si l'UFP passe en ***USB 3.2*** ou en ***USB 2.0*** et que la connexion au DFP s'effectue avec un hub ***USB4*** en aval, le DFP ***doit*** réinitialiser la connexion avec l'***USB PD*** Data Reset, puis envoyer un message ***USB PD Enter_USB*** qui indique ***USB 3.2*** ou ***USB 2.0*** et le groupe de bits Host Present;
    - à défaut, le DFP ***doit*** passer à l'état ***ErrorRecovery*** pour réinitialiser la connexion et établir une nouvelle connexion qui s'aligne sur les capacités de l'UFP du hub.

5.5.4 Exemples de processus de comportement de connexion des ports d'un hub

Le présent paragraphe représente plusieurs exemples de connexions qui prennent pour hypothèse que la connexion au DFP du hub est établie avant la connexion à l'UFP du hub. Dans ces cas, les capacités de l'hôte sont inconnues au moment où le DFP du hub se connecte au dispositif branché. Compte tenu de ces éléments, la connexion initiale établie par le DFP du hub repose uniquement, de façon spéculative, sur les capacités du hub et du dispositif. Elle ***peut*** devoir être révisée dès que les capacités de l'hôte sont connues, en cas d'incohérence fonctionnelle. Lorsque la connexion à l'UFP du hub est pleinement établie avant que les dispositifs n'apparaissent sur le DFP du hub, la connexion peut être établie en parfaite connaissance des capacités de l'hôte (les processus associés à cette relation ne sont pas représentés).

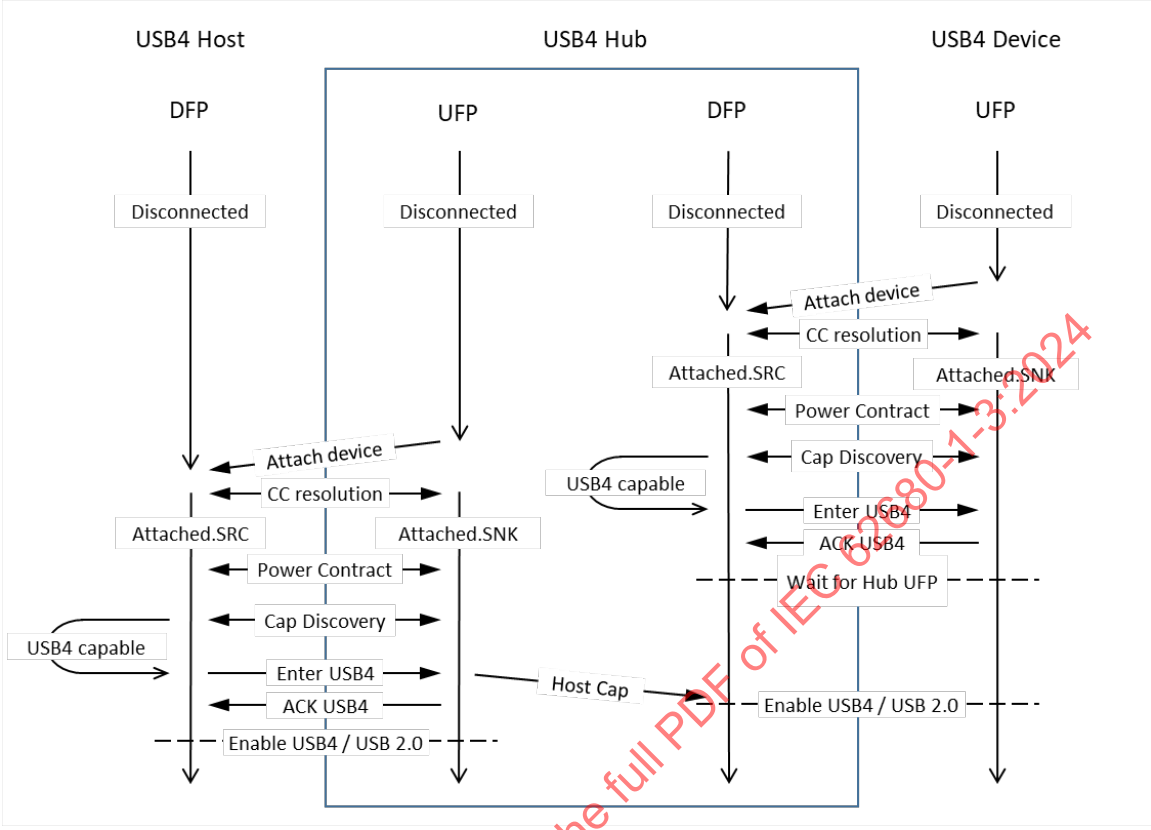
Pour les exemples de processus décrits dans le présent paragraphe, les rôles d'alimentation source/destinataire restent tels qu'initialement résolus par le diagramme d'états de connexion CC, sans activité ***PR_Swap*** ou ***DR_Swap***.

Tous ces exemples de processus visent à réduire le plus possible le délai total de connexion pour activer la fonctionnalité du dispositif connecté au DFP du hub. Pour ce faire, il faut établir la connexion la plus fonctionnelle par rapport aux capacités mutuelles entre le hub et le dispositif, même si les capacités de l'UFP du hub sont inconnues ou qu'elles ne sont pas prêtes. Si la connexion établie de façon spéculative s'avère valide lorsque les capacités de l'UFP du hub ont été établies, la connexion au DFP est activée en l'état. Si la connexion établie de façon spéculative s'avère invalide, la connexion au DFP doit être réinitialisée et une connexion qui s'aligne sur les capacités de l'UFP du hub ***doit*** être établie.

La Figure 5-2 représente un processus de connexion aligné pour la combinaison hôte-hub-dispositif ***USB4***. Le résultat attendu est l'activation concluante du fonctionnement ***USB4*** de bout en bout.

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Figure 5-2 Alignement du processus de connexion d'un hub *USB4* sur un hôte et un dispositif *USB4*



Anglais	Français
USB4 host	Hôte USB4
USB4 hub	Hub USB4
USB4 device	Dispositif USB4
Disconnected	Déconnecté
USB4 capable	Compatible USB4
Attach device	Branchement dispositif
CC resolution	Résolution CC
Power contract	Contrat d'alimentation
Cap discovery	Découverte des capacités
Host cap	Capacité hôte
Wait for hub UFB	Attente hub UFP
Enter USB4	Entrée USB4
Enable USB4/USB 2.0	Activer USB4/USB 2.0

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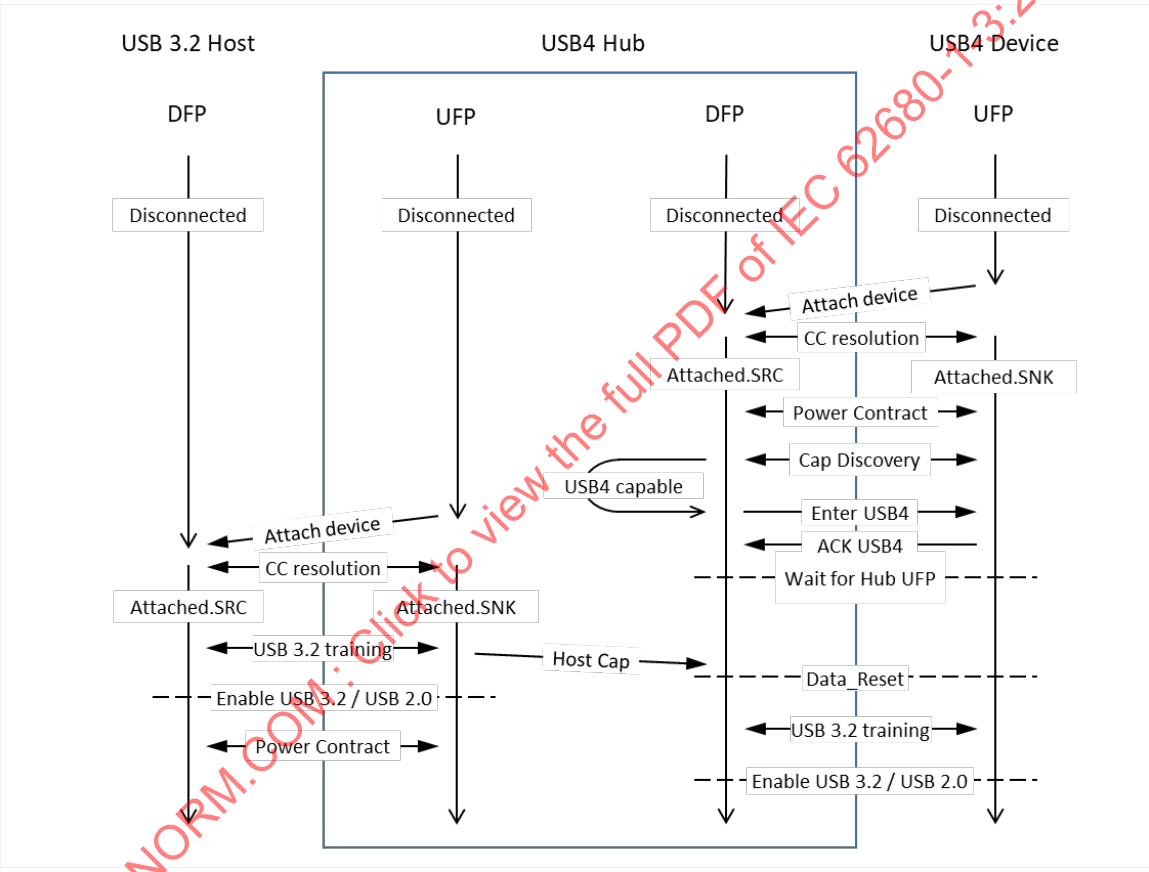
Dans le processus représenté, la découverte de capacités inclut toutes les permutations de messages ***USB PD*** nécessaires entre le DFP et son port partenaire UFP pour découvrir les capacités USB de l'UFP ainsi que les capacités de compatibilité ***TBT3*** et du ***mode alternatif DP***. Pour le DFP du hub ***USB4***, la découverte de capacités s'effectue de façon spéculative chaque fois qu'il ne connaît pas déjà les capacités de l'hôte à terme connecté par l'UFP du hub.

À l'issue du processus de découverte des capacités entre le DFP du hub et son port partenaire UFP, le DFP du hub établit la connexion la plus fonctionnelle qui soit, puis attend que l'UFP du hub achève sa connexion. Après établissement de la connexion à l'UFP du hub, les capacités disponibles de l'hôte sont utilisées pour déterminer ce qu'***il convient de*** faire pour achever la connexion du DFP du hub au port partenaire UFP.

Les capacités de l'hôte reposent sur la configuration obtenue (par exemple, le protocole et la vitesse du bus de données) de l'UFP du hub ***USB4*** et sur les informations relatives aux capacités de l'hôte reçues dans le message ***USB PD Enter_USB*** de son port partenaire DFP (voir 5.5.2). Le hub ***USB4*** utilise les capacités de l'hôte pour définir les capacités disponibles des DFP du hub.

La Figure 5-3 représente le modèle de processus de connexion aligné pour la combinaison hôte ***USB 3.2***-hub ***USB4***-dispositif ***USB4***.

Figure 5-3 Processus de connexion d'un hub *USB4* avec un hôte *USB 3.2*et un dispositif *USB4*



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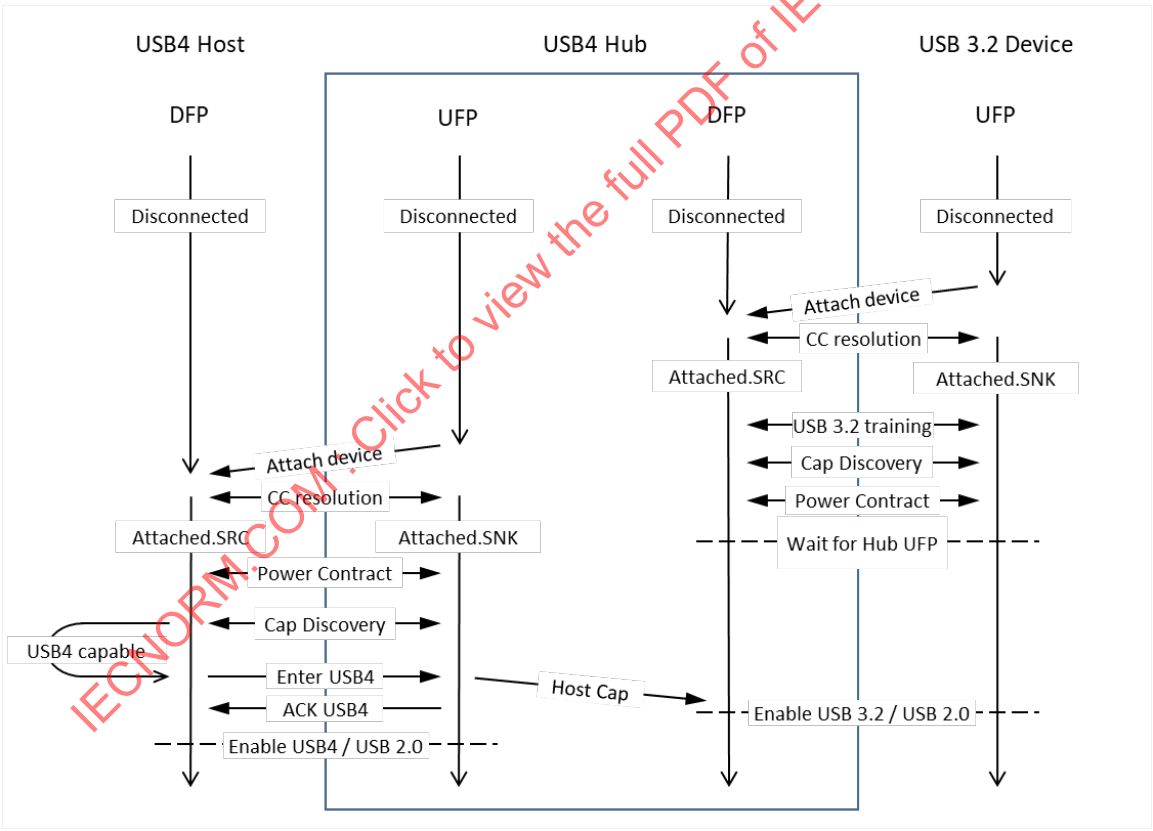
Anglais	Français
USB 3.2 host	Hôte USB 3.2
USB4 hub	Hub USB4
USB4 device	Dispositif USB4
Disconnected	Déconnecté
USB4 capable	Compatible USB4
Attach device	Branchement dispositif
CC resolution	Résolution CC
Power contract	Contrat d'alimentation

Anglais	Français
Cap discovery	Découverte des capacités
Host cap	Capacité hôte
Wait for hub UFP	Attente hub UFP
USB 3.2 training	Formation USB 3.2
Enter USB4	Entrée USB4
Enable USB 3.2/USB 2.0	Activer USB 3.2/USB 2.0

Dans le processus ci-dessus, après connexion à un hôte ***USB 3.2***, les capacités de l'hôte indiquent que le hub ne peut prendre en charge que l'***USB 3.2*** sur ses DFP et que la connexion ***USB4*** établie de façon spéculative sur les DFP est arrêtée; le hub ***USB4*** fonctionne alors comme un hub ***USB 3.2*** traditionnel.

La Figure 5-4 représente le modèle de processus de connexion aligné pour la combinaison hub ***USB4***-hôte ***USB4***-dispositif ***USB 3.2***.

Figure 5-4 Alignement du processus de connexion d'un hub *USB4* sur un hôte *USB4* et un dispositif *USB 3.2*



Anglais	Français
USB4 host	Hôte USB4
USB4 hub	Hub USB4
USB 3.2 device	Dispositif USB 3.2
Disconnected	Déconnecté

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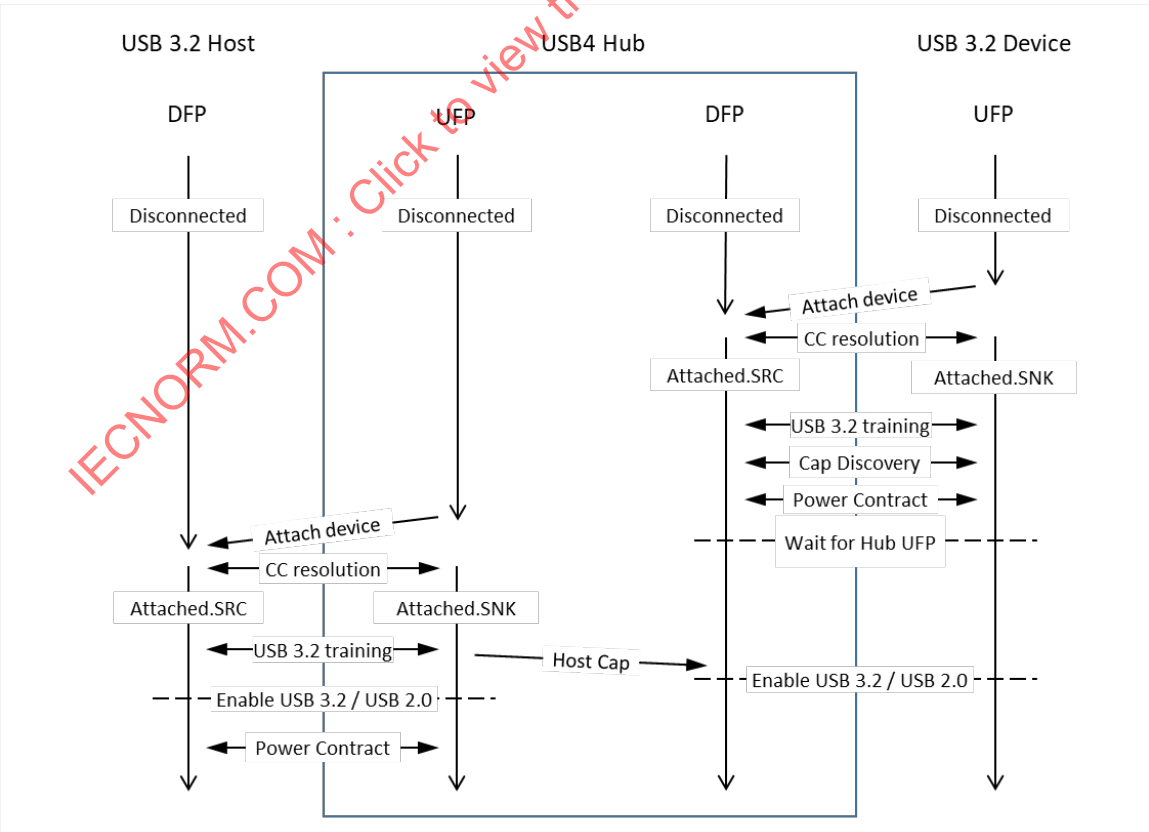
Anglais	Français
USB4 capable	Compatible USB4
Attach device	Branchement dispositif
CC resolution	Résolution CC
Power contract	Contrat d'alimentation
Cap discovery	Découverte des capacités
Host cap	Capacité hôte
Wait for hub UFP	Attente hub UFP
Enter USB4	Entrée USB4
ACK USB4	ACK USB4
Enable USB4 / USB 2.0	Activer USB4/USB 2.0
Enable USB3.2 / USB 2.0	Activer USB3.2/USB 2.0

Même si les dispositifs ***USB 3.2*** ne répondent pas nécessairement à la découverte d'ID (SOP), le DFP du hub ***USB4*** tente de découvrir les capacités du dispositif branché.

Dans le processus ci-dessus, après établissement de la connexion ***USB4*** à l'UFP du hub, la connexion au DFP reste valide, le chemin de données ***USB 3.2*** du DFP étant desservi par le tunnel ***USB4*** Enhanced SuperSpeed.

La Figure 5-5 représente le modèle de processus de connexion aligné pour la combinaison hub ***USB4***-hôte ***USB 3.2***-dispositif.

Figure 5-5 Processus de connexion d'un hub *USB4* avec un hôte et un dispositif *USB 3.2*



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Anglais	Français
USB 3.2 host	Hôte USB 3.2
USB4 hub	Hub USB4
USB 3.2 device	Dispositif USB 3.2
Disconnected	Déconnecté
Attach device	Branchement dispositif
CC resolution	Résolution CC
USB 3.2 training	Formation USB 3.2
Cap discovery	Découverte des capacités
Power contract	Contrat d'alimentation
Wait for hub UFP	Attente hub UFP
USB 3.2 training	Formation USB 3.2
Host cap	Capacité hôte
Enable USB 3.2/USB 2.0	Activer USB 3.2/USB 2.0

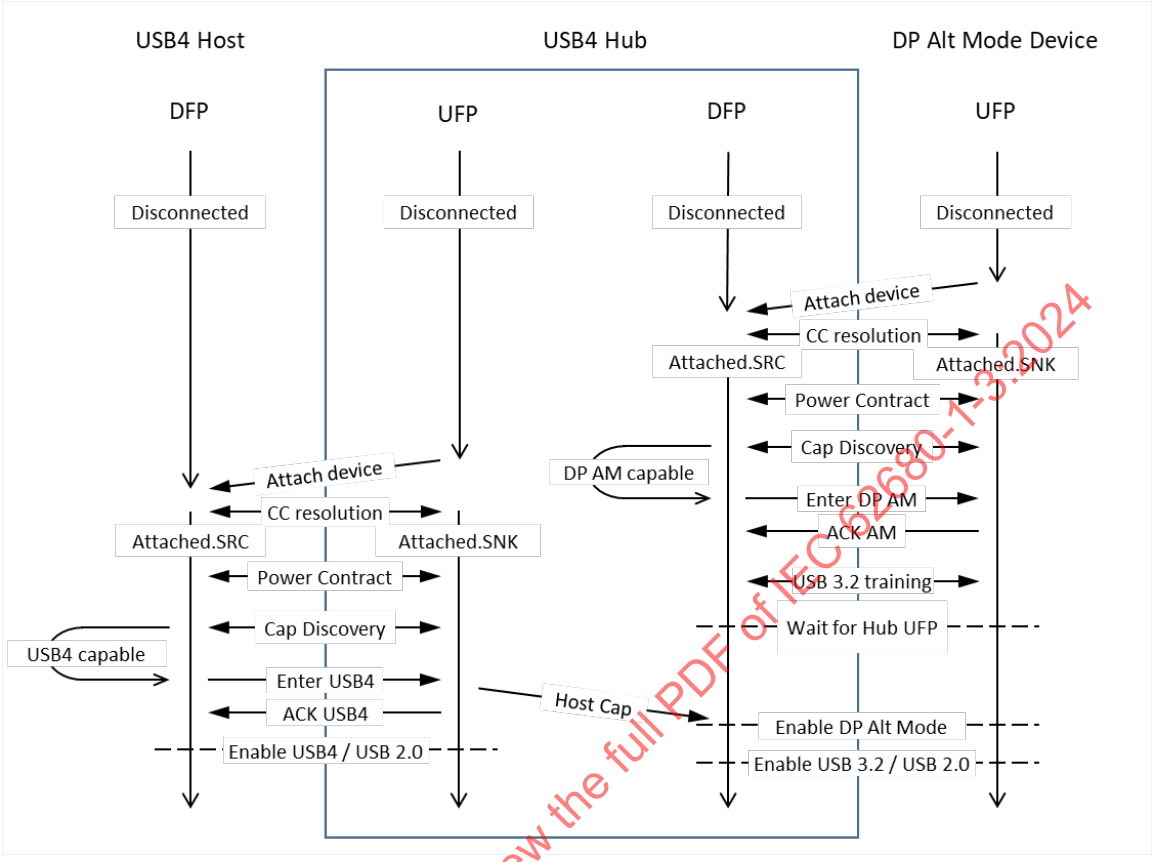
Même si les dispositifs ***USB 3.2*** ne répondent pas nécessairement à la découverte d'ID (SOP), le DFP du hub ***USB4*** tente de découvrir les capacités du dispositif branché.

Dans le processus ci-dessus, après établissement de la connexion ***USB 3.2*** à l'UFP du hub, la connexion au DFP reste valide; le hub ***USB4*** fonctionne alors comme un hub ***USB 3.2*** traditionnel.

La Figure 5-6 représente le modèle de processus de connexion aligné pour la combinaison hôte ***USB4***-hub ***USB4***-dispositif en ***mode alternatif DP*** (mode multifonction). Dans ce cas, le résultat attendu est l'activation du ***mode alternatif DP***, ponté à partir du tunneling ***USB4 DisplayPort***.

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Figure 5-6 Processus de connexion d'un hub *USB4* avec un hôte *USB4* et un dispositif en mode alternatif DP



Anglais	Français
USB4 host	Hôte USB4
USB4 hub	Hub USB4
DP alt mode device	Dispositif mode alt DP
Disconnected	Déconnecté
USB4 capable	Compatible USB4
DP AM capable	Compatible DP AM
Attach device	Branchement dispositif
CC resolution	Résolution CC
Power contract	Contrat d'alimentation
Cap discovery	Découverte des capacités
Host cap	Capacité hôte
Enter USB4	Entrée USB4
ACK USB4	ACK USB4
Enter DP AM	Entrée DP AM
Enable DP Alt mode	Activer mode alt DP
Wait for hub UFP	Attente hub UFP
Enable USB4/USB 2.0	Activer USB4/USB 2.0

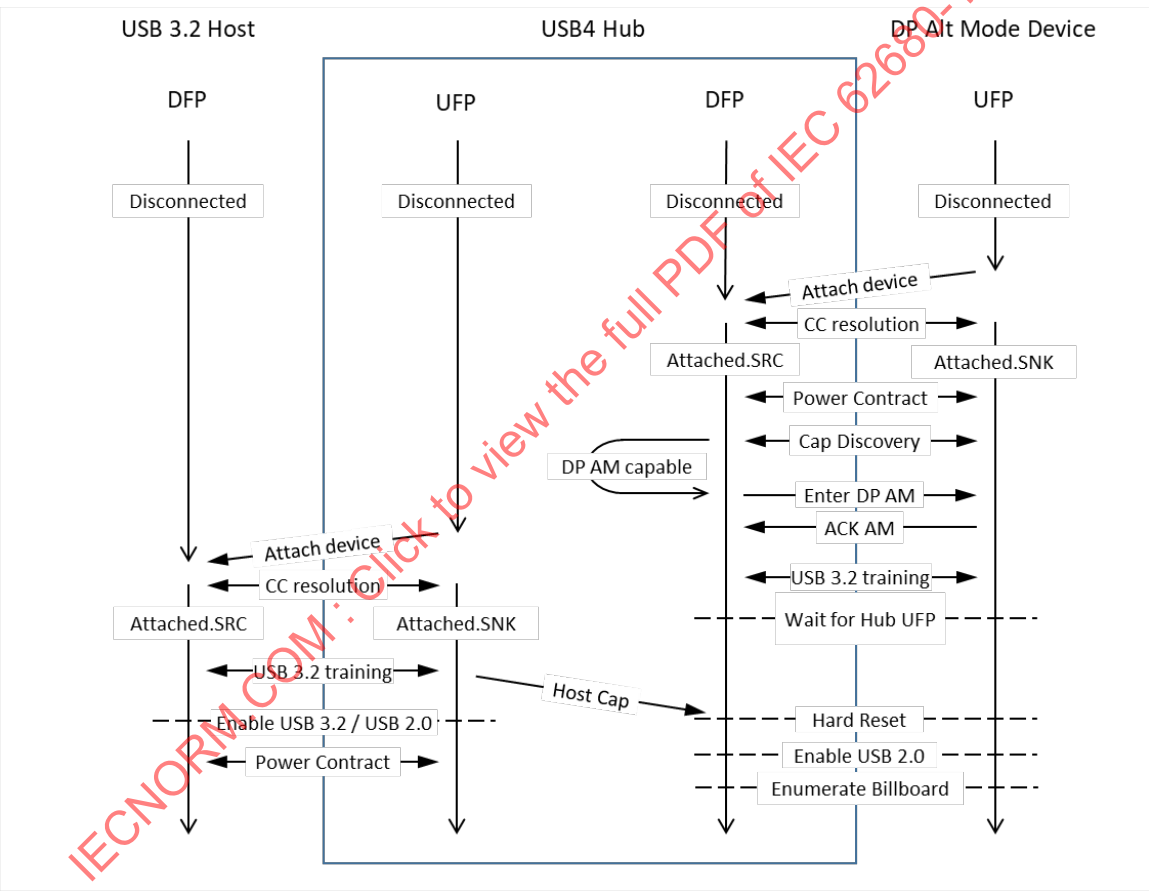
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Anglais	Français
Enable USB 3.2/USB 2.0	Activer USB 3.2/USB 2.0

Dans le processus ci-dessus, après établissement de la connexion ***USB4*** à l'UFP du hub, la connexion au DFP reste valide, les chemins de données ***DisplayPort*** et ***USB 3.2*** du DFP étant desservis par les tunnels ***USB4 DisplayPort*** et Enhanced SuperSpeed.

La Figure 5-7 représente le modèle de processus de connexion aligné pour la combinaison hôte ***USB 3.2***-hub ***USB4***-dispositif en ***mode alternatif DP*** (mode multifonction). Dans ce cas, le résultat attendu est que le ***mode alternatif DP*** n'est pas activé et qu'une interface ***USB Billboard Device Class*** est exposée par le dispositif puisque l'hôte ne prend pas en charge l'***USB4***.

Figure 5-7 Processus de connexion d'un hub *USB4* avec un hôte *USB 3.2* et un dispositif en mode alternatif DP



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Anglais	Français
USB 3.2 host	Hôte USB 3.2
USB4 hub	Hub USB4
DP alt mode device	Dispositif mode alt DP
Disconnected	Déconnecté
DP AM capable	Compatible DP AM
Attach device	Branchement dispositif

Anglais	Français
CC resolution	Résolution CC
Power contract	Contrat d'alimentation
Cap discovery	Découverte des capacités
Host cap	Capacité hôte
Enter DP AM	Entrée DP AM
Enable USB 3.2 / USB 2.0	Activer USB 3.2/USB 2.0
Wait for hub UFP	Attente hub UFP
USB 3.2 training	Formation USB 3.2
Hard reset	Réinitialisation matérielle
Enumerate billboard	Énumérer billboard

Dans le processus ci-dessus, après établissement de la connexion ***USB 3.2*** à l'UFP du hub, la connexion au DFP n'est plus valide; le hub ***USB4*** fonctionne alors comme un hub ***USB 3.2*** traditionnel. Le DFP du hub doit alors réinitialiser le port, ce qui se traduit par une connexion ***USB 2.0*** et une exposition de la ***USB Billboard Device Class***.

5.5.5 Connexion aux hubs *USB4* en aval

Lorsqu'un hub ***USB4*** est branché sur son DFP à l'UFP d'un autre hub ***USB4***, ce hub ***USB4 doit*** utiliser le bit Host Present du message ***USB PD Enter_USB*** pour indiquer au hub en aval si les capacités ***USB4*** répertoriées dans le message reflètent (ou non) les capacités de l'hôte. Si une connexion initiale est établie avec le hub en aval et inclut la réinitialisation du bit Host Present dans le message ***USB PD Enter_USB***, le hub ***USB4 doit*** ensuite envoyer un message ***USB PD Enter_USB*** révisé avec le bit Host Present défini après l'établissement complet de son UFP (voir 5.5.2).

5.5.6 Exigences fonctionnelles concernant le repli des hubs *USB4*

Lorsque l'UFP d'un hub ***USB4*** est branché à un DFP non ***USB4***, le hub ***USB4 doit*** basculer en mode de repli en toute fluidité et satisfaire aux exigences d'un hub ***USB 3.2***.

5.6 Exigences relatives à la connexion des dispositifs *USB4*

5.6.1 Mise en correspondance de repli des fonctions périphériques *USB4* vers les types de classes de dispositifs USB

Les dispositifs périphériques ***USB4*** fournissent des fonctions qui reposent sur les données transférées sur un ou plusieurs tunnels de protocole de l'***USB4***: ***Enhanced SuperSpeed USB***, ***DisplayPort*** et ***PCI Express***. Pour toutes les fonctions périphériques qui utilisent le tunnel de protocole USB Enhanced SuperSpeed, la mise en correspondance de ces fonctions vers les spécifications de classe de dispositifs USB est claire. Toutefois, pour celles qui reposent sur les autres protocoles en tunnel, cette mise en correspondance ne s'applique pas, puisque ces fonctions ne dépendent pas des pilotes de classe de dispositifs USB pour fonctionner.

Chaque fonction d'un dispositif ***USB4 doit*** être mise en correspondance vers une classe de dispositifs USB équivalente, lorsque cela est possible. Les dispositifs ***USB4*** qui contiennent des fonctions de classe de dispositifs USB mises en correspondance ***doivent*** prendre en charge le fonctionnement ***USB 3.2*** ou ***USB 2.0*** lorsqu'ils sont connectés à des hôtes non ***USB4***. Cette exigence ne s'applique pas aux fonctions qui utilisent des tunnels ***DisplayPort*** ou ***PCIe*** pour le transfert de données ***USB4*** qui ne sont pas raisonnablement mises en correspondance vers une classe de dispositifs USB existante, par exemple un adaptateur graphique PCIe.

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Il est attendu que les performances d'une fonction, lorsqu'elle est mappée vers une connexion à vitesse inférieure, s'adaptent de manière appropriée tout en fournissant l'équivalent fonctionnel des capacités primaires de la fonction périphérique.

Le Tableau 5-2 répertorie les types de classes de dispositifs USB et les exigences de mise en correspondance pour les fonctions périphériques des dispositifs ***USB4*** en ce qui concerne le repli lors du fonctionnement ***USB 3.2*** ou ***USB 2.0***.

Tableau 5-2 Mise en correspondance de repli des fonctions périphériques USB4 vers les types de classes de dispositifs USB

Catégorie de classe de dispositif	Mise en correspondance des fonctions périphériques *USB4*	Notes
Audio	***Exigé***	
Vidéo	***Exigé***	
Stockage de masse	***Exigé***	
Communication/Gestion réseau	***Exigé***	
Impression	***Exigé***	
HID	***Exigé***	Uniquement exigé lorsque l'utilisation de sous-classes ou de rapports HID est définie de façon équivalente.
Protocole de transport multimédia	***Exigé***	
Carte à puce	***Exigé***	
Capture d'images fixes	***Exigé***	
Dispositif de surveillance	***Exigé***	Uniquement exigé en conjonction avec la fourniture d'applications d'affichage associées.

Pour toutes les fonctions périphériques ***USB4*** qui reposent sur le tunneling de protocole ***DisplayPort*** et ***PCIe*** et qui ne sont pas mises en correspondance vers des équivalents de classe de dispositifs USB en fonctionnement ***USB 3.2*** ou ***USB 2.0***, une interface ***USB Billboard Device Class*** appropriée ***doit*** être exposée pour activer les notifications utilisateur par le système d'exploitation de la plateforme hôte.

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5.7 Valeurs de paramètres

5.7.1 Paramètres de temporisation

Le Tableau 5-3 fournit une exigence d'expiration pour qu'un dispositif qui prend en charge l'***USB4*** active une interface ***USB Billboard Device Class*** lorsqu'il ne peut pas se connecter en tant que dispositif ***USB4*** pendant le processus de découverte et de mise en service (voir 5.4).

Tableau 5-3 Disponibilité USB Billboard Device Class à l'issue d'un échec de mise en service d'un dispositif *USB4*

	Valeur maximale	Description
tUSB4Timeout	1 000 ms	Le délai de (1) connexion d'un destinataire ou de (2) connexion de données est rétabli lors du processus ***USB PD*** Data Reset, jusqu'à ce que l'interface ***USB Billboard Device Class*** soit exposée lorsque la mise en service du dispositif ***USB4*** échoue.

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6 Câbles actifs

Les câbles actifs ***doivent*** au moins prendre en charge ***USB 3.2*** Gen 2x2. Les câbles actifs ***USB4 doivent*** prendre en charge l'***USB4*** en plus de toutes les vitesses ***USB 3.2***. Les câbles actifs ***doivent*** prendre en charge les marqueurs électroniques ***USB PD*** et ***peuvent*** prendre en charge les ***modes alternatifs*** et les annoncer comme cela est défini en 6.1.1.

Tous les câbles actifs ***USB4 doivent*** être interopérables avec ***Thunderbolt 3*** comme cela est défini dans la spécification ***USB4*** (Article 13) et la présente spécification (6.1.1 et Annexes E et F).

Les câbles actifs qui prennent en charge des longueurs allant jusqu'à 5 m ***doivent*** fonctionner dans les deux sens, et ***il convient*** qu'ils fonctionnent comme des câbles passifs du point de vue de l'utilisateur.

Les câbles actifs optiques hybrides utilisent le cuivre pour l'alimentation et les données ***USB 2.0***, et la fibre optique pour la signalisation des données à grande vitesse (TX/RX). Sur le plan fonctionnel, ils sont identiques aux câbles actifs cuivre et ***doivent*** fonctionner comme des câbles passifs du point de vue de l'utilisateur.

Les câbles actifs à isolation optique (OIAC) constituent un cas particulier de câbles actifs, avec des exigences et des limitations propres aux OIAC. Les OIAC prennent en charge des longueurs plus longues, jusqu'à 50 m, et assurent l'isolation électrique entre les deux extrémités du câble. Les câbles OIAC sont destinés à des applications industrielles et médicales, de vision par ordinateur, de télédétection et de vidéo professionnelle. Les câbles OIAC ne fonctionnent pas "simplement" comme des câbles normaux. Voir 6.3 pour plus d'informations sur les exigences et les limitations relatives aux câbles OIAC.

6.1 Spécifications générales applicables à tous les câbles actifs

6.1.1 Découverte des caractéristiques d'un câble actif

La commande ***USB PD*** Discover_Identity permet de découvrir les caractéristiques du câble actif. Cette commande ne ***doit*** être envoyée qu'à SOP'. Tous les câbles actifs ***doivent*** répondre à la commande Discover_Identity, par l'intermédiaire des VDO des câbles actifs qui renvoient des informations sur le câble. Noter qu'***il convient que*** le câble actif réponde avec l'***USB PD*** Révision 3, mais qu'il ***peut*** répondre avec l'***USB PD*** Révision 2 suivant les règles d'interopérabilité ***USB PD***.

Le Tableau 6-1 récapitule les câbles ***USB4*** en ce qui concerne les valeurs d'identité essentielles qui sont renvoyées aux commandes Discover_Identity de l'***USB PD*** Révision 3.

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Tableau 6-1 Récapitulatif de l'identité de câble *USB4*

USB4 **Câble**	**Fonction**				**Configuration SOP' (*USB PD* Révision 3)**					
					VDO d'en-tête d'ID	**VDO de câble passif**	**VDO de câble actif 1**	**VDO de câble actif 2**		
	USB2	**USB3**	***TBT3***	**DP**	**Fiche de câble passif/ actif B29…27**	**Type de terminaison de câble B12…11**	**Type de terminaison de câble B12…11**	**Connexion physique B10**	**Élément actif B9**	**Câble actif à isolation optique B2**
Passif[1]	Oui	Oui	Oui	Oui	011b	00b/01b	n/a	n/a	n/a	n/a
Circuit d'amplification linéaire *TBT3*[1]	Oui	Oui	Oui	Fac.	011b	01b[2]	n/a	n/a	n/a	n/a
Circuit d'amplification linéaire (Gen4)[1]	Oui	Oui	Oui	Fac.	100b[4]	n/a	10b/11b	0b	0b	0b
					011b[4]	01b[2]	n/a	n/a	n/a	n/a
Circuit de retemporisation[1]	Oui	Oui	Oui	Fac.	100b	n/a	10b/11b	0b	1b	0b
Optique hybride [1, 3]	Oui	Oui	Oui	Fac.	100b	n/a	11b	1b	0b/1b	0b
À isolation optique	Non	Oui	Fac.	Non	100b	n/a	11b	1b	0b/1b	1b

Notes:

1. Il est exigé que les câbles ***USB4***, à l'exception des câbles à isolation optique, prennent en charge la compatibilité ***Thunderbolt 3***. Les exigences d'identité spécifiques à ***TBT3*** sont définies à l'Annexe F.
2. Le câble actif du circuit d'amplification linéaire ***TBT3*** représente uniquement un câble passif qui est découvert selon la Figure 5-1.
3. Un câble actif optique hybride est défini comme utilisant une ligne de transmission optique intermédiaire pour le chemin de signalisation à grande vitesse (TX/RX) tout en conservant une solution en cuivre pour le reste des interfaces définies.
4. Le câble actif fondé sur le circuit d'amplification linéaire ***USB4*** Gen4 s'identifie comme un câble actif comme ou un câble passif (pour la rétrocompatibilité), en fonction du numéro de version (B14…11) indiqué dans le message ***USB PD*** Structured VDM ***Discover Identity***, comme suit: pour B14…11 = 0101b, le câble s'identifie comme actif, et pour B14…11 = 0100b, le câble s'identifie comme passif.

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Note: Comme cela est indiqué dans le Tableau 6-1, il est exigé que les câbles passifs ***USB4*** prennent en charge la compatibilité ***Thunderbolt 3***. Cette exigence implique que les câbles passifs ***USB4*** Gen3 répondent correctement aux commandes de découverte d'identité de câble passif ***TBT3*** avec les VDO (voir le Tableau F-1 et le Tableau F-3 du F.2.1) afin de les utiliser dans une connexion ***TBT3*** aux vitesses Gen3. ***Il convient que*** les câbles ***USB4*** Gen2 ne mettent ***pas*** en œuvre les VDO d'identité de câble passif ***TBT3***.

Tableau 6-2 Caractéristiques d'un câble actif

Type de câble	Longueur	*USB PD*	VBUS	Fil VCONN	CC	*USB 2.0*	*USB 3.2* (tous sont exigés)	*USB4*	Modes alternatifs	SBU
USB 3.2 actif	< 5 m	SOP' ***exigé*** (SOP" ***facultatif***)	3 A ou 5 A	Identique au câble passif	Identique au câble passif	Identique au câble passif	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	***N/A***	***Facultatif***	Note 2 Note 3
USB4 actif	< 5 m	SOP' ***exigé*** (SOP" ***facultatif***)	3 A ou 5 A	Identique au câble passif	Identique au câble passif	Identique au câble passif	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	Gen 2 Gen3 Gen4	***TBT3*** Note 1	Note 2 Note 4
USB4 actif hybride	< 5 m	SOP' ***exigé*** (SOP" ***facultatif***)	3 A ou 5 A	Identique au câble passif	Identique au câble passif	Identique au câble passif	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	Gen 2 Gen3 Gen4	***TBT3*** Note 1	Note 2 Note 4

Notes:
1. Prise en charge du ***mode alternatif Thunderbolt 3*** exigée comme cela est défini dans l'Annexe F.
2. Une connexion passive en mode ***USB 3.2*** est exigée.
3. La prise en charge de la SBU est ***normative facultative*** en ***modes alternatifs***.
4. La prise en charge de la SBU pour ***USB4*** peut être passive ou active dans le cas d'un câble actif fondé sur le circuit d'amplification, ou actif dans le cas d'un câble actif fondé sur le circuit de retemporisation.

Tous les câbles actifs, quelle que soit leur longueur, ***doivent*** respecter la présente spécification, l'***USB 3.2*** (Annexe E notamment) et le CTS de câble actif ***USB 3.2***.

6.1.2 Exigences électriques

6.1.2.1 Exigence concernant l'efficacité de l'écrantage

Tous les câbles actifs ***doivent*** satisfaire à l'exigence concernant l'efficacité de l'écrantage, définie en 3.7.7 et représentée à la Figure 3-65.

6.1.2.2 Exigence concernant les signaux à basse vitesse

6.1.2.2.1 Exigences relatives aux canaux CC

Les câbles actifs ***doivent*** satisfaire aux exigences relatives aux signaux à basse vitesse du 3.7.2.6.

6.1.2.2.2 Exigences relatives à la SBU

Les SBU désignent une paire de connexions électriques de bout en bout dans le câble. Ces connexions ne sont pas utilisées avec l'***USB 3.2***, mais elles sont utilisées pour les ***modes alternatifs*** tels que ***DisplayPort***. L'***USB4*** utilise également ces connexions, mais les a renommées SBTX et SBRX. Les exigences électriques sont les mêmes dans les deux cas.

Les fils SBU des câbles actifs ***doivent*** satisfaire aux exigences définies dans le Tableau 6-3. Ils ***doivent*** aussi satisfaire aux exigences relatives à la paradiaphonie et à la télédiaphonie entre les signaux à basse vitesse définies en 3.7.2.6.

Les broches SBU n'offrent aucune garantie de performance lorsque la VCONN n'est pas fournie au câble. L'hôte ou le dispositif ***ne doit pas*** fournir de signal supérieur à celui indiqué dans le Tableau 6-3, lorsque la VCONN n'a pas été fournie.

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Tableau 6-3 Exigences relatives aux SBU des câbles actifs

Nom	Description	Valeur minimale	Maximale	Unités
zCable_SBU	Impédance caractéristique du câble sur les fils SBU	32	53	Ω
tCableDelay_SBU	Délai de propagation sur le fil SBU dans le câble		26	ns
rCable_SBU	Résistance en courant continu des fils SBU dans le câble en USB		40	Ω
vCable_SBU	Oscillation de la tension sur les fils SBU dans le câble	−0,3	4,0	V
Perte d'insertion[1]	Perte d'insertion du câble		5 dB à 0,5 MHz 7 dB à 1 MHz 12 dB à 10 MHz 13 dB à 25 MHz 15 dB à 50 MHz 16 dB à 100 MHz	dB
iCableSBU	Courant maximal de bout en bout	−25	25	mA
Note 1: Mesurage faisant référence à 50 Ω.				

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6.1.2.3 *USB 2.0*

Les câbles actifs ***doivent*** satisfaire aux exigences de l'***USB 2.0*** définies en 3.7.2.6 et 3.7.2.7.

Note: Les câbles actifs supérieurs à 5 m indiquent le nombre de sauts de hub consommés dans les VDO d'un câble actif.

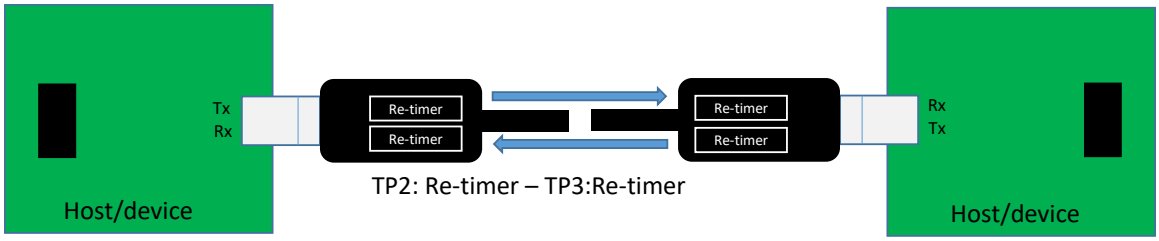
6.1.2.4 *USB 3.2*

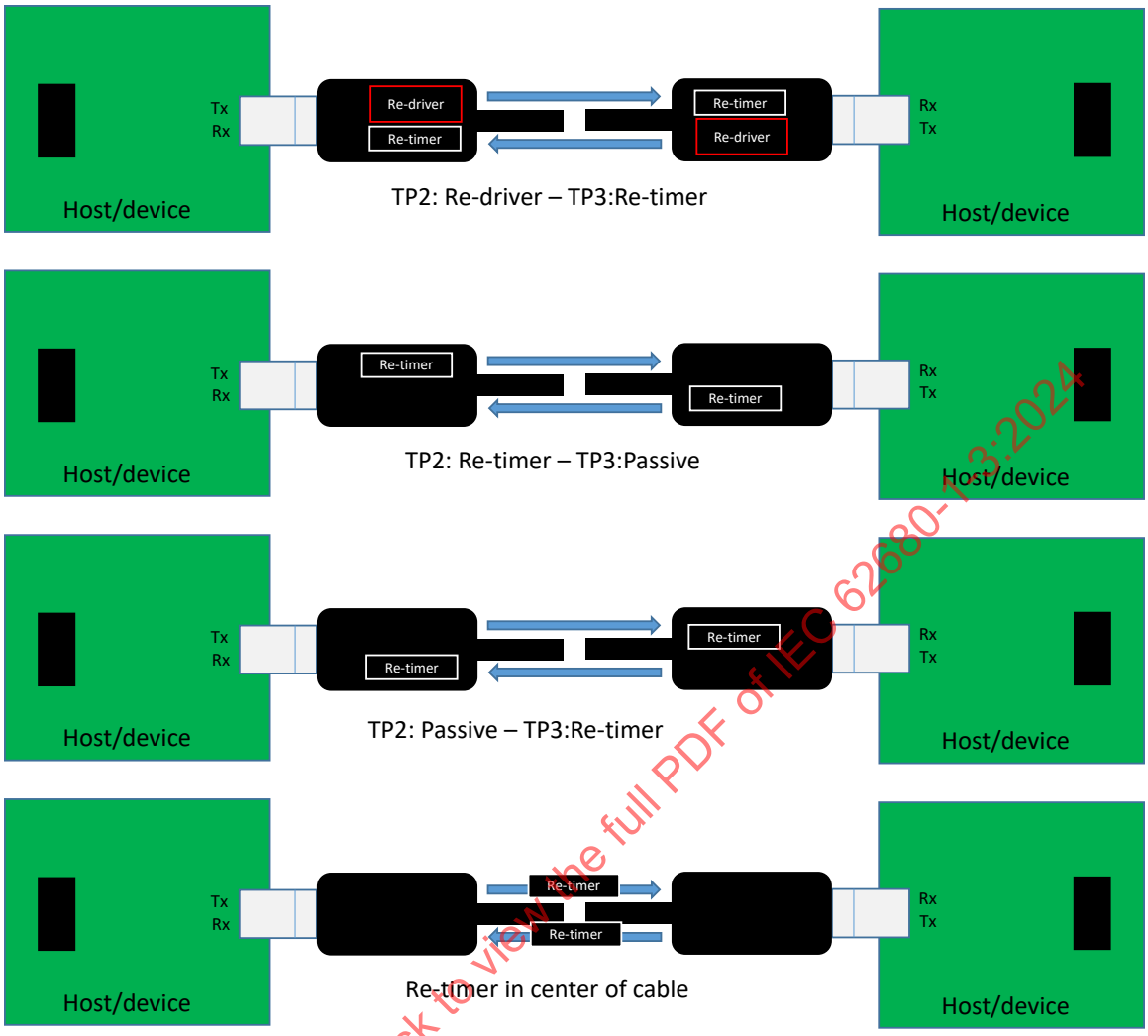
Les câbles actifs ***doivent*** intégrer un couplage en courant alternatif entre la fiche et le répéteur sur les signaux ***USB 3.2*** TX et RX. Les câbles actifs ***doivent*** fournir une voie de décharge qui permet de décharger les condensateurs de couplage en courant alternatif du câble, lors d'une déconnexion selon l'***USB 3.2***.

6.1.2.4.1 Architectures des câbles actifs *USB 3.2*

Les câbles actifs ***peuvent*** fournir des combinaisons de circuits de retemporisation et de circuits d'amplification, comme cela est représenté à la Figure 6-1. Les câbles actifs sans au moins un circuit de retemporisation ne relèvent pas du présent domaine d'application. Les câbles actifs sans au moins un circuit de retemporisation connecté à TP3 ne relèvent pas du présent domaine d'application. Les câbles actifs ***doivent*** prendre en charge les fonctionnalités définies dans le Tableau 6-2.

Figure 6-1 Topologies des câbles actifs





Anglais	Français
Host/Device	Hôte/Dispositif
Re-timer	Circuit de retemporisation
TP2: Re-timer – TP3:Re-timer	TP2: Circuit de retemporisation – TP3: Circuit de retemporisation
Re-driver	Circuit d'amplification
TP2: Re-driver – TP3:Re-timer	TP2: Circuit d'amplification – TP3: Circuit de retemporisation
TP2: Re-timer – TP3:Passive	TP2: Circuit de retemporisation – TP3: Passif
TP2: Re-Passive – TP3:Re-timer	TP2: Circuit passif – Circuit de retemporisation TP3
Re-timer in center of cable	Circuit de retemporisation au centre du câble

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6.1.2.4.2 Mise sous tension *USB 3.2* et Rx.Detect

Les câbles actifs ***doivent*** présenter une impédance de mise à la masse élevée de $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ lorsqu'ils ne sont pas alimentés. Les câbles actifs ***doivent*** présenter une impédance de mise à la masse élevée de $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ à la mise sous tension initiale. Le câble actif ***doit*** effectuer une détection des terminaisons du récepteur d'extrémité aux deux extrémités du câble à la réception de la VCONN. Lors de la détection d'une terminaison de récepteur d'extrémité à faible impédance ($R_{RX\text{-}DC}$), le câble actif ***doit*** permettre à sa terminaison de récepteur à faible impédance ($R_{RX\text{-}DC}$) de mettre en miroir la présence de l'hôte/du dispositif. Le câble actif ***doit*** permettre la détection des terminaisons du récepteur d'extrémité pour les répéteurs selon l'***USB 3.2***, y compris dans les états de faible puissance U2/U3.

Un câble actif ***doit*** permettre la mise sous tension et la détection des terminaisons du récepteur d'extrémité par le câble dans le délai $t_{FWD_RX.DETECT}$.

Tableau 6-4 Exigences relatives à la mise sous tension des câbles actifs

Nom	Valeur minimale	Valeur maximale	Unités
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$	Par l ***USB 3.2***	Par l ***USB 3.2***	
$R_{RX\text{-}DC}$	Par l ***USB 3.2***	Par l ***USB 3.2***	
$t_{FWD_RX.DETECT}$		42[1]	ms
Note 1: 84 ms – (2 · 12 ms + 18 ms) dans le cas le plus défavorable.			

Les câbles actifs, y compris les câbles OIAC, ***doivent*** refléter les terminaisons du récepteur sur le câble pour reproduire le comportement d'un câble passif.

6.1.2.4.3 Délai *USB 3.2* U0

Tous les câbles actifs ***doivent*** satisfaire au délai ***USB 3.2*** défini dans le Tableau 6-5.

Tableau 6-5 Délai *USB 3.2* U0 maximal pour un câble OIAC

Génération *USB 3.2*	Délai U0 maximal du câble	Notes
Gen 1	3 000 ns	Les câbles actifs qui présentent une latence ***USB 3.2*** Gen1 supérieure à 125 ns ***peuvent ne pas*** fonctionner correctement lorsqu'ils sont utilisés conjointement avec les hôtes, dispositifs et hubs qui ne prennent pas en charge ***USB 3.2***.
Gen2	3 000 ns	Les câbles actifs qui présentent une latence ***USB 3.2*** Gen2 supérieure à 305 ns ***peuvent ne pas*** fonctionner correctement lorsqu'ils sont utilisés conjointement avec les hôtes, dispositifs et hubs qui ne prennent pas en charge ***USB 3.2***.

6.1.2.4.4 Exigences d'alimentation des états U de l'*USB 3.2*

Les câbles actifs ***doivent*** satisfaire aux exigences d'alimentation de la VCONN pour le fonctionnement ***USB 3.2*** données dans le Tableau 6-6. Ces exigences s'appliquent à l'ensemble du câble et non aux seules fiches de câbles.

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Tableau 6-6 Exigences relatives aux états U de l'*USB 3.2*

État	Consommation électrique VCONN maximale	Notes relatives à la consommation électrique
U0	1,0 W à voie unique 1,5 W à double voie	S'applique aux états POLLING.LFPS, TRAINING et RECOVERY.
U1	≤ à la puissance U0	Le transfert de la LFPS est exigé.
U2	≤ à la puissance U1	Le transfert de la LFPS est exigé.
U3	20 mW	Puissance en régime permanent. Marqueur électronique en veille.
Rx.Detect	20 mW	La période Rx.Detect ***peut*** être prolongée lorsqu'aucune terminaison ***USB 3.2*** n'a été détectée.
eSS.Disabled	20 mW	***USB 3.2*** est désactivée. Marqueur électronique en veille.

6.1.2.4.5 Latence de sortie des états U de l'*USB 3.2*

Les câbles actifs ***doivent*** satisfaire à la latence de sortie des états U définie dans l'Annexe E de l'***USB 3.2***.

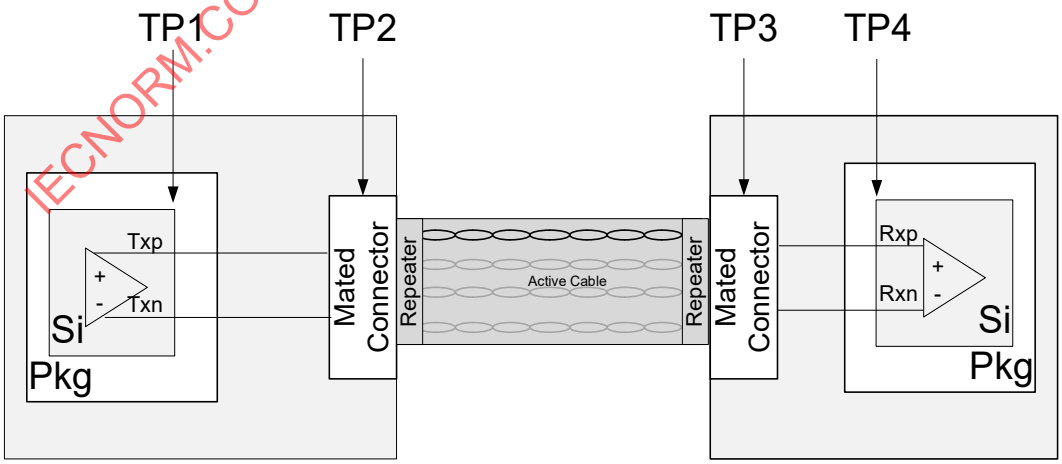
6.1.2.4.6 Oscillation du signal *USB 3.2*

Un émetteur de câble actif ne doit générer qu'une perte d'insertion de 8,5 dB à 5 GHz sur le récepteur du contrôleur d'hôte/de dispositif pour l'***USB 3.2*** Gen2, si l'émetteur est situé dans la fiche de câble, à côté du port de réception.

Un émetteur de contrôleur d'hôte/de dispositif doit générer une perte totale de 23 dB à 5 GHz sur l'extrémité pour l'***USB 3.2*** Gen2. La différence dans le bilan des pertes admet la réduction de l'oscillation de l'émetteur d'un câble actif. Le récepteur d'un câble actif peut prendre pour hypothèse une oscillation de récepteur plus importante que celle de l'hôte/du dispositif pour une même raison.

La Figure 6-2 définit les points d'essai électrique SuperSpeed. Elle est reprise de la spécification ***USB 3.2***. La Figure 6-3 indique les points d'essai et les connexions d'équipement d'essai.

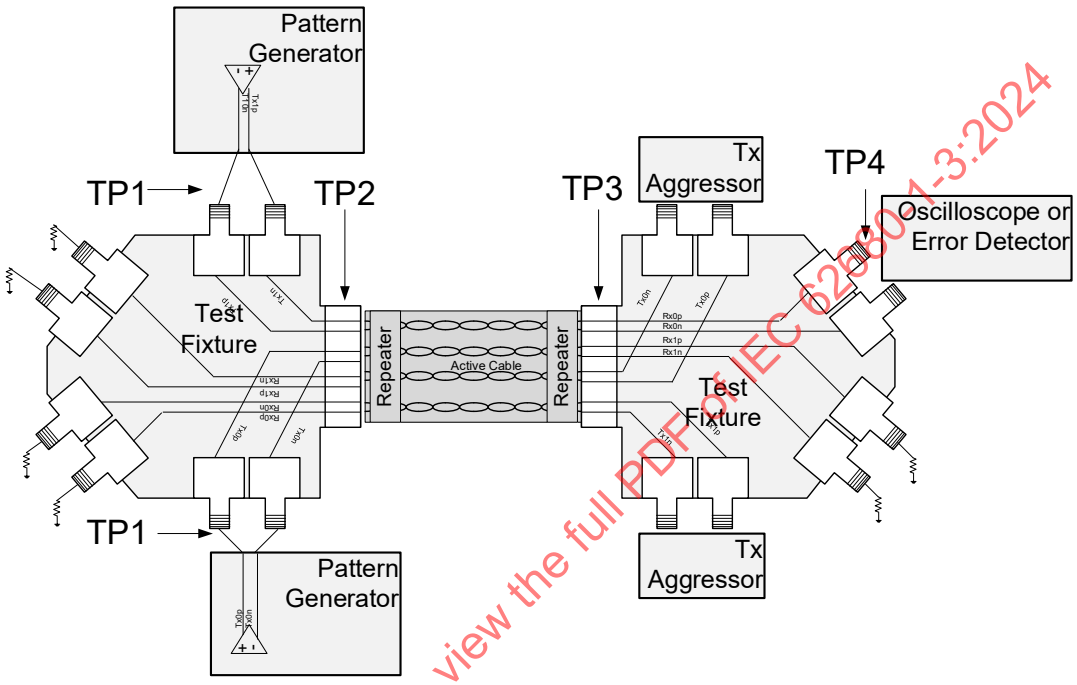
Figure 6-2 Points d'essai électrique USB SuperSpeed



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Anglais	Français
Mated Connector	Connecteur couplé
Repeater	Répéteur
Active Cable	Câble actif

Figure 6-3 Montage d'essai de conformité USB SuperSpeed



Anglais	Français
Pattern Generator	Mire électronique
Test Fixture	Montage d'essai
Repeater	Répéteur
Active Cable	Câble actif
TX Aggressor	Agresseur TX
Oscilloscope or Error Detector	Oscilloscope ou détecteur d'erreurs

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6.1.2.4.6.1 TP1 – Source contrainte d'entrée de câble actif

La source contrainte d'entrée de câble actif est générée au niveau de TP1 conformément au Tableau 6-7 pour l'amplitude et au Tableau 6-8 pour la gigue. Le SSC ***doit*** être présent dans le signal contraint au niveau de TP1. Le Tableau 6-7 est un sous-ensemble du Tableau 6-18 de l'***USB 3.2***. Le Tableau 6-8 est un sous-ensemble du Tableau 6-28 de l'***USB 3.2***. S'il existe une divergence entre la présente spécification et la spécification ***USB 3.2***, la spécification ***USB 3.2 doit*** prévaloir.

L'oscillation maximale avec la valeur de désaccentuation et de prédépassement maximale ***doit*** être soumise à l'essai avec carte d'essai de complaisance de perte minimale. L'oscillation minimale avec la valeur de désaccentuation et de prédépassement minimale ***doit*** être soumise à l'essai avec carte d'essai de complaisance de perte maximale. La composition de la gigue d'entrée est la même pour les sources contraintes d'oscillation minimale et maximale.

Le câble actif ***doit*** fonctionner sur la plage de paramètres du Tableau 6-7 et du Tableau 6-17 ***USB 3.2***.

Tableau 6-7 Oscillation de la source contrainte *USB 3.2* d'un câble actif, TP1

Symbole	Paramètre	Gen 1 (5,0 GT/s)	Gen 2 (10 GT/s)	Unités	Commentaires
$V_{TX-DIFF-PP}$	Oscillation de la tension TX p-p différentielle	0,8 (au minimum) 1,2 (au maximum)	0,8 (au minimum) 1,2 (au maximum)	V	La valeur nominale est de 1 V p-p.
$V_{TX-DE-RATIO}$	Désaccentuation TX	Tableau 6-17 de l'**USB 3.2**	−3,1 ± 1,0	dB	La valeur nominale est de 3,5 dB pour le fonctionnement Gen 1. Les exigences relatives à l'égalisation d'un émetteur Gen2 sont décrites dans l'***USB 3.2***, 6.7.5.2.
$V_{PRESHOOT}$	Prédépassement TX	Tableau 6-17 de l'**USB 3.2**	2,2 ± 1,0	dB	Les exigences relatives à l'égalisation d'un émetteur Gen2 sont décrites dans l'***USB 3.2***, 6.7.5.2.

Tableau 6-8 Gigue de la source contrainte *USB 3.2* d'un câble actif, TP1

Symbole	Paramètre	Gen 1 (5,0 GT/s)	Gen 2 (10 GT/s)	Unités	Notes
f1	Angle de tolérance	4,9	7,5	MHz	
J_{Rj}	Gigue aléatoire	0,0 121	0,0 100	UI eff.	1
J_{Rj_p-p}	Gigue aléatoire crête à crête à 10^{-12}	0,17	0,14	UI p-p	1,4
J_{Pj_500kHZ}	Gigue sinusoïdale	2	4,76	UI p-p	1, 2, 3
J_{Pj_1Mhz}	Gigue sinusoïdale	1	2,03	UI p-p	1, 2, 3
J_{Pj_2MHz}	Gigue sinusoïdale	0,5	0,87	UI p-p	1, 2, 3
J_{Pj_4MHz}	Gigue sinusoïdale	***N/A***	0,37	UI p-p	1, 2, 3
J_{Pj_f1}	Gigue sinusoïdale	0,2	0,17	UI p-p	1, 2, 3
J_{Pj_50MHz}	Gigue sinusoïdale	0,2	0,17	UI p-p	1, 2, 3
J_{Pj_100MHz}	Gigue sinusoïdale	***N/A***	0,17	UI p-p	1, 2, 3

Notes:

1. Tous les paramètres sont mesurés au niveau du TP1. Le point d'essai est représenté à la Figure 6-2 et à la Figure 6-3.
2. En raison des limitations de temps lors des essais de conformité, seul un sous-ensemble de fréquences peut être soumis à l'essai. Cependant, le RX doit tolérer Pj à toutes les fréquences entre les points d'essai de conformité.
3. Pendant l'essai de tolérance RX, le SSC est généré par l'équipement d'essai et est toujours présent. Chaque source JPj est ensuite ajoutée et soumise à l'essai à la limite de la spécification, l'une après l'autre.
4. La gigue aléatoire est également présente pendant l'essai de tolérance RX.
5. Les spécifications JTOL pour Gen2 comprennent l'écrêtage de la gigue avec circuits de retemporisation dans le système et fournissent une pente de 25 dB/dizaine.

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6.1.2.4.6.2 TP2 – Entrée de câble actif (*informative*)

Les valeurs du Tableau 6-9 indiquent les oscillations ***informatives*** des signaux d'entrée au niveau du TP2 pour un câble actif. Le Tableau 6-9 répertorie les recommandations plus strictes par rapport aux exigences ***normatives*** fournies dans le Tableau 6-7 et le Tableau 6-8. Un câble actif peut être pleinement conforme aux exigences ***normatives*** de la présente spécification et ne pas satisfaire à toutes les valeurs du Tableau 6-9. De même, il n'est pas garanti qu'un câble actif qui satisfait à toutes les valeurs du Tableau 6-9 soit pleinement conforme à la partie ***normative*** de la présente spécification.

Tableau 6-9 Oscillation de l'entrée *USB 3.2* d'un câble actif au niveau du TP2 (*informative*)

Symbole	Paramètre	Gen 1 (5,0 GT/s)	Gen 2 (10 GT/s)	Unités	Commentaires
$V_{TX-DIFF-PP}$	Oscillation de la tension TX p-p différentielle	250 (au minimum) 1 000 (au maximum)	250 (au minimum) 850 (au maximum)	mV	La valeur nominale est de 550 mV p-p.
$V_{TX-DE-RATIO}$	Désaccentuation TX	0 (au minimum) 4,0 (au maximum)	2,1 (au minimum) 4,1 (au maximum)	dB	La désaccentuation pour Gen 1 n'est soumise à aucune exigence.
$V_{PRESHOOT}$	Prédépassement TX	NA	1,2 (au minimum) 3,2 (au maximum)	dB	Uniquement applicable au fonctionnement ***USB 3.2*** Gen2.

6.1.2.4.6.3 TP3 – Sortie de câble actif (*informative*)

Les valeurs du Tableau 6-10 indiquent les oscillations ***informatives*** des signaux de sortie au niveau du TP3 pour un câble actif. Le Tableau 6-10 répertorie les recommandations plus strictes par rapport aux exigences ***normatives*** fournies dans le Tableau 6-7 et le Tableau 6-8. Un câble actif peut être pleinement conforme aux exigences ***normatives*** de la présente spécification et ne pas satisfaire à toutes les valeurs du Tableau 6-10. De même, il n'est pas garanti qu'un câble actif qui satisfait à toutes les valeurs du Tableau 6-10 soit pleinement conforme à la partie ***normative*** de la présente spécification.

Tableau 6-10 Oscillation de la sortie *USB 3.2* d'un câble actif au niveau du TP3 (*informative*)

Symbole	Paramètre	Gen 1 (5,0 GT/s)	Gen 2 (10 GT/s)	Unités	Commentaires
$V_{TX-DIFF-PP}$	Tension RX crête à crête différentielle	300 (au minimum) 850 (au maximum)	300 (au minimum) 850 (au maximum)	mV	Mesuré après la fonction RX EQ. La valeur nominale est de 0,5 V p-p.
$V_{TX-DE-RATIO-GEN1}$	Désaccentuation TX	0 (au minimum) 4,0 (au maximum)	NA	dB	Aucun prédépassement admis.

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Symbole	Paramètre	Gen 1 (5,0 GT/s)	Gen 2 (10 GT/s)	Unités	Commentaires
$V_{TX\text{-}DE\text{-}RATIO}$ + $V_{PRESHOOT\text{-}GEN2}$	Désaccentuation TX + Prédépassement TX	NA	0 (au minimum) 3,0 (au maximum)	dB	Somme de la désaccentuation et du prédépassement. La désaccentuation et le prédépassement ne sont soumis à aucune exigence.

6.1.2.4.6.4 TP4 – Sortie de câble actif

La sortie de l'émetteur d'un câble actif est définie au niveau du TP4 pour les canaux à faible perte et à perte élevée. Les exigences relatives au TP4 sont définies dans le Tableau 6-20 de la spécification ***USB 3.2***. Le signal d'entrée de l'essai ***doit*** être appliqué au niveau du TP1, comme cela est décrit dans spécification ***USB 3.2***.

La carte d'essai à faible perte ***doit*** être utilisée pour soumettre à l'essai l'oscillation de sortie maximale. La carte d'essai à perte maximale ***doit*** être utilisée pour soumettre à l'essai l'oscillation de sortie minimale. La gigue doit être respectée avec ces deux cartes.

Le taux d'erreur binaire d'un câble actif ***doit*** être soumis à l'essai au niveau du TP4 et atteindre ou dépasser un BER de 10^{-12}. Le détecteur d'erreur utilisé ***doit*** être capable de retirer les ensembles ordonnés SKP.

6.1.2.5 *USB4*

Le présent paragraphe décrit les exigences électriques et les essais de conformité des câbles actifs ***USB4***. L'essai de conformité est défini pour assurer l'interopérabilité en matière d'intégrité des données et de spécifications électriques, permettant au câble actif, en toute fiabilité, de recevoir un signal d'entrée et d'émettre un signal valide à son autre extrémité.

Les types de câbles actifs ***USB4*** sont les suivants:

1. les câbles actifs de type circuit de retemporisation (le présent paragraphe couvre les câbles actifs circuits de retemporisation pour ***USB4*** uniquement, le câble de retemporisation ***USB 3.2*** étant défini en 6.1.2.4);

2. les câbles actifs circuits d'amplification (fondés sur LRD) (***USB 3.2*** et ***USB4***; ou

3. les câbles actifs optiques linéaires (les exigences électriques LRD du 6.1.2.5.4 s'appliquent généralement à un OIAC ***USB4***).

6.1.2.5.1 Exigences électriques applicables à tous les câbles actifs

6.1.2.5.1.1 Définition des points d'essai de conformité du système

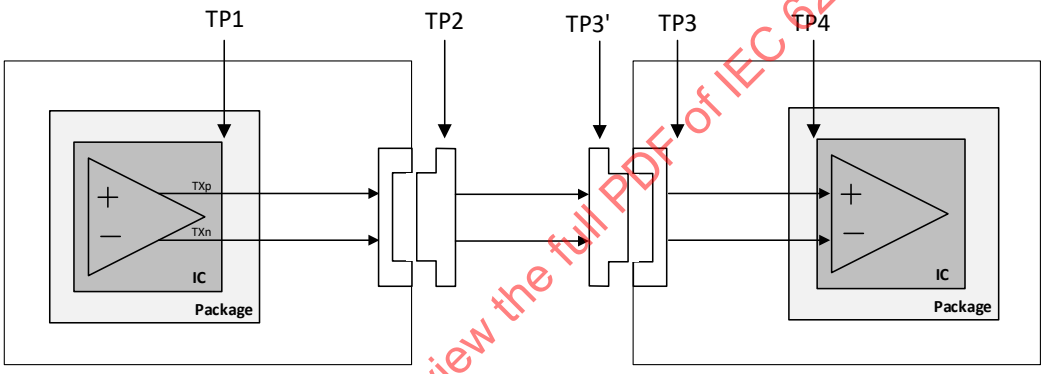
Tous les mesurages ***doivent*** être référencés selon les points de conformité suivants. Un étalonnage ***doit*** être appliqué dans les cas où un mesurage direct n'est pas possible.

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Tableau 6-11 Définition des points de conformité

Point d'essai	Description	Commentaires
TP1	Sortie IC de l'émetteur	Non utilisée pour les essais électriques
TP2	Sortie du connecteur de port de l'émetteur	Mesurée côté fiche du connecteur
TP3	Sortie du connecteur de port du récepteur	Mesuré côté embase du connecteur. Tous les mesurages à ce point ***doivent*** être effectués en appliquant la fonction d'égalisation de référence.
TP3'	Entrée du connecteur de port du récepteur	Mesurée côté fiche du connecteur
TP4	Entrée IC du récepteur	Non utilisée pour les essais électriques

Figure 6-4 Définition des points de conformité



Anglais	Français
Package	Paquet

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6.1.2.5.1.2 Cartes d'essai de l'embase de conformité

Le montage d'essai à grande vitesse USB Type-C ***doit*** être utilisé pour procéder aux essais de conformité du câble. Le montage ***doit*** être composé d'une embase USB Type-C et d'une courte piste CCI qui ***peut*** être connectée à un câble coaxial avec un connecteur SMA/SMP à son extrémité. Les points de référence TP2 et TP3' qui se trouvent sur la fiche USB Type-C, la perte et la distorsion du montage d'embase ***doivent*** être étalonnées de sorte que toutes les valeurs mesurées correspondent aux points de référence normalisés. Le point de référence TP3 est défini de sorte que la perte d'insertion entre les plaques de connecteur et le point de conformité soit de 0,5 dB ± 0,25 dB à 5 GHz et de 1 dB ± 0,25 dB à 10 GHz. Les éléments de perte et de distorsion supplémentaires ***doivent*** être compensés par des moyens physiques et/ou mathématiques.

L'impédance cible du montage ***doit*** être de 85 Ω. Les condensateurs de couplage en courant alternatif ***doivent*** être placés sur le montage d'essai de l'embase selon les exigences d'assemblage de routeur indiquées dans la spécification ***USB4*** et le CTS.

6.1.2.5.1.3 Condensateur de couplage en courant alternatif

Les câbles actifs ***doivent*** inclure une capacité de couplage en courant alternatif comprise entre 135 nF et 265 nF à l'intérieur de leurs fiches placés au niveau du chemin d'émission en sortie, et entre 300 nF et 363 nF au niveau du chemin de réception en entrée. Les résistances de décharge entre 200 KΩ et 242 KΩ ***doivent*** être placées au niveau du chemin de réception en entrée. Voir la Figure 3-3 de la spécification ***USB4*** pour un diagramme des condensateurs de couplage en courant alternatif et des résistances de décharge.

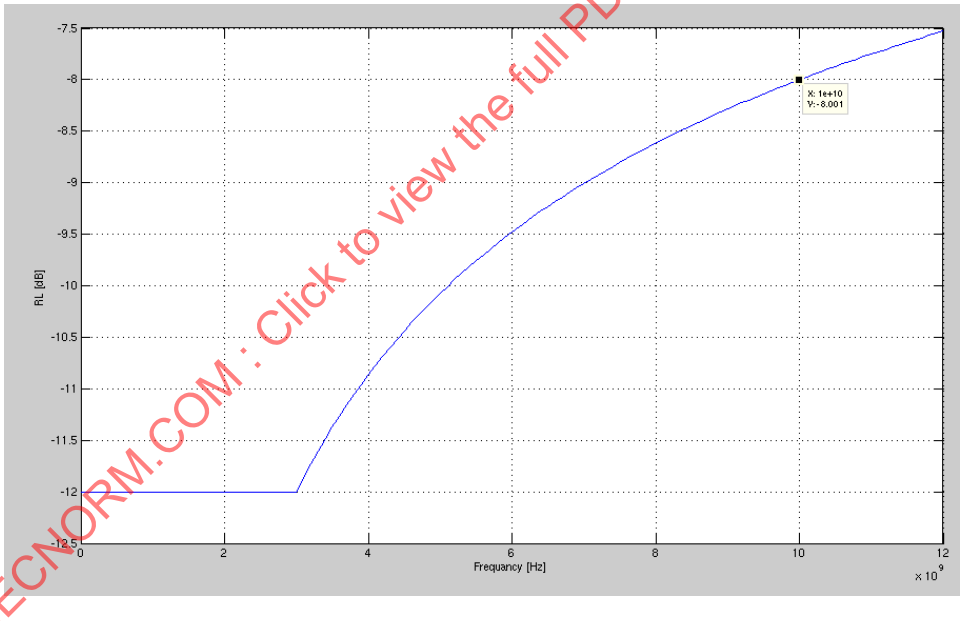
Il est nécessaire que les conceptions de câble actif prennent en compte le fait qu'une variation de la consommation de courant par VBUS, telle que le permet ***USB Power Delivery***, peut ajouter un décalage en mode commun considérable qui ***peut ne pas*** être traité par le couplage en courant alternatif de la présente spécification.

6.1.2.5.1.4 Masque de facteur d'adaptation différentiel (*informative*)

Les mesurages du facteur d'adaptation d'entrée et de sortie du circuit de retemporisation et du circuit d'amplification ***doivent*** être référencés à une impédance différentielle de 85 Ω. Lorsque le mesurage est réalisé au niveau de TP3' et de TP1 (respectivement), il est recommandé que le facteur d'adaptation en mode différentiel ne dépasse pas les limites indiquées dans l'équation suivante:

$$SDD22(f), SDD11(f) = \begin{cases} -12 \; 0.05 < f_{GHz} \leq 3 \\ -7.5 + 7.5 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) 3 < f_{GHz} \leq 12 \end{cases}$$

Figure 6-5 Masque de facteur d'adaptation différentiel RX



Anglais	Français
-12.5	-12,5
Frequency [Hz]	Fréquence [Hz]
X: 1e+10 Y: -8.001	X: 1e+10 Y: -8,001

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6.1.2.5.2 Exigences d'alimentation *USB4* à l'état CL pour les câbles actifs

Les câbles actifs ***doivent*** prendre en charge tous les états CL et satisfaire aux exigences d'alimentation VCONN pour le fonctionnement ***USB4*** conformément au Tableau 6-12. Ces exigences s'appliquent à l'ensemble du câble et non aux seules fiches de câbles.

Tableau 6-12 Exigences d'alimentation *USB4* à l'état CL pour les câbles actifs

État	Consommation électrique VCONN maximale	Notes relatives à la consommation électrique
CL0	1,5 W	S'applique aux états de formation et à CL0.
CL0s	≤ à la puissance CL0	
CL1	≤ à la puissance CL0	
CL2	≤ à la puissance CL1	
CLd	20 mW	Puissance en régime permanent.
Note: Les exigences d'alimentation à l'état CL des OIAC sont indiquées en 6.3.6.5.2.		

6.1.2.5.3 Exigences électriques du câble actif fondé sur le circuit de retemporisation

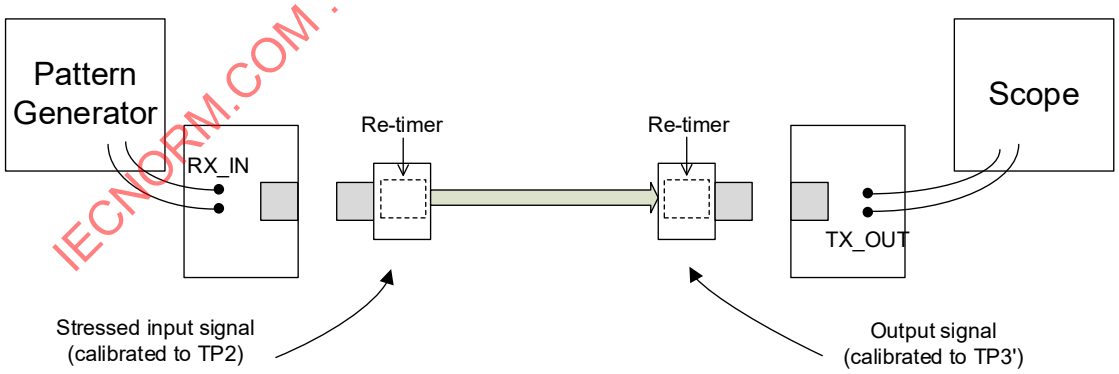
Le présent paragraphe décrit les exigences électriques et les essais de conformité des câbles actifs fondés sur le circuit de retemporisation ***USB4***.

6.1.2.5.3.1 Égalisation de sortie

Un câble actif ***USB4 doit*** mettre en œuvre une égalisation à réponse impulsionnelle finie (FIR) à 3 bandes réglable au niveau de sa sortie. L'égalisation d'émission ***doit*** prendre en charge 16 configurations prédéfinies avec différents réglages de désaccentuation et de prédépassement (voir la spécification ***USB4***) et ***doit*** être mesurée au niveau de TP3'.

6.1.2.5.3.2 Montage d'essai de conformité du câble actif fondé sur le circuit de retemporisation

Figure 6-6 Montage d'essai de conformité du câble actif fondé sur le circuit de retemporisation



Anglais	Français
Pattern Generator	Mire électronique
Stressed input signal (calibrated to TP2)	Signal d'entrée contraint (étalonné sur TP2)
Re-timer	Circuit de retemporisation

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