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First edition
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Helical-scan compressed digital video cassette system using 6,35 mm magnetic tape – Format D-12 –

Part 2: Compression format

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

HELICAL-SCAN COMPRESSED DIGITAL VIDEO CASSETTE SYSTEM USING 6,35 mm MAGNETIC TAPE – FORMAT D-12 –

Part 2: Compression format

FOREWORD

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International Standard IEC 62247-2 has been prepared by IEC technical committee 100: Audio, video and multimedia systems and equipment.

The text of this standard is based on the following documents:

CDV	Report on voting
100/1092/CDV	100/1187/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The list of all the parts of the IEC 62247 series, under the general title *Helical-scan compressed digital video cassette system using 6,35 mm magnetic tape – Format D-12,* can be found on the IEC website.

This part 2 describes the specifications for encoding process and data format for 1080i, 1080p and 720p systems.

Part 1 describes the VTR specifications which are tape, magnetization, helical recording, modulation method and basic system data for video compressed data.

Part 3 describes the specifications for transmission of DV-based compressed video and audio data stream over 360 Mb/s serial digital interface.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

HELICAL-SCAN COMPRESSED DIGITAL VIDEO CASSETTE SYSTEM USING 6,35 mm MAGNETIC TAPE – FORMAT D-12 –

Part 2: Compression format

1 Scope

This part of IEC 62247 defines the data structure for the interface of DV-based digital audio, subcode data, and compressed video at 100 Mb/s. This standard defines the processes required to decode the DV-based data structure into eight channels of AES-3 digital audio at 48 kHz, subcode data, and high-definition video at 1080/60i, 1080/50i, and 720/60p.

The following high-definition video parameters are used in this standard:

1080/60i system

Input video format: 1920 × 1080 image sampling structure, 59,94 Hz field rate, interlace format. Compressed video data rate: 100 Mb/s

1080/50i system

Input video format: 1920 × 1080 image sampling structure, 50 Hz field rate, interlace format. Compressed video data rate: 100 Mb/s

720/60p system

Input video format: 1280 × 720 image sampling structure, 59,94 Hz frame rate, progressive format. Compressed video data rate: 100 Mb/s

In this standard, the 60 Hz system nomenclature refers to both 1080/60i and 720/60p systems; whereas the 50 Hz system refers only to the 1080/50i system. The nomenclature 1080-line system refers to both 1080/60i and 1080/50i systems, while the 720-line system refers only to the 720/60p system.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

SMPTE 12M:1999, *Television, Audio and Film – Time and Control Code*

SMPTE 274M:1998, *Television, 1920 x 1080 Scanning and Analog and Parallel Digital Interfaces for Multiple Picture Rates*

SMPTE 260M:1999, *Television, 1125/60 High-Definition Production System – Digital Representation and Bit Parallel Interface*

SMPTE 296M:1997, *Television, 1280 x 720 Scanning, Analog and Digital Representation and Analog Interface*

AES3:1992, *Serial Transmission Format for Two-Channel Linearly Represented Digital Audio Data*

3 Abbreviations and acronyms

AAUX	Audio auxiliary data
AP1	Audio application ID
AP2	Video application ID
AP3	Subcode application ID
APT	Track application ID
Arb	Arbitrary
AS	AAUX source pack
ASC	AAUX source control pack
CGMS	Copy generation management system
CM	Compressed macro block
DBN	DIF block number
DCT	Discrete cosine transform
DIF	Digital interface
DRF	Direction flag
Dseq	DIF sequence number
DSF	DIF sequence flag
EFC	Emphasis audio channel flag
EOB	End of block
LF	Locked mode flag
QNO	Quantization number
QU	Quantization
Res	Reserved for future use
SCT	Section type
SMP	Sampling frequency
SSYB	Subcode sync block
STA	Status of the compressed macro block
STYPE	Signal type
Syb	Subcode sync block number
TF	Transmitting flag
VAUX	Video auxiliary data
VLC	Variable length coding
VS	VAUX source pack
VSC	VAUX source control pack

4 Data processing

4.1 General

As shown in Figure 1, processed audio, video and subcode data are output for recording on a D-xx recorder. Additionally, these data are output in DIF format data for a different application through a digital interface port. Details of this process are shown in Figure 1 and described in Clauses 3 and 4. Dotted lines are related to the data flow described in the VTR document.

Annex A shows the block diagram of D-xx recorder. Figure A.1 of this standard shows the part defined by this compression format document.

4.1.1 Video encoding parameter

The source component signal to be processed shall comply with the video parameters as defined by SMPTE 274M and SMPTE 296M.

4.1.2 Audio encoding parameter

The audio signal is sampled at 48 kHz with 16-bit quantization defined by AES3.

4.1.3 Subcode data

The time code format in the subcode area complies with SMPTE 12M.

4.1.4 Frame structure

In 1080/60i and 1080/50i systems, video frame data, audio frame data, and subcode data are processed in each frame. The audio frame in this standard is defined as an audio-processing unit.

In the 720/60p system, data in two video frames are processed within one frame duration of the 1080/60i system. Consequently, audio data and subcode data are processed in the same way as the 1080/60i system.

Each frame of time code shows a frame number that corresponds to each video frame in the 1080-line system, and two video frames each in 720/60p system. Therefore, time codes of the 1080/60i and 720/60p systems are the same.

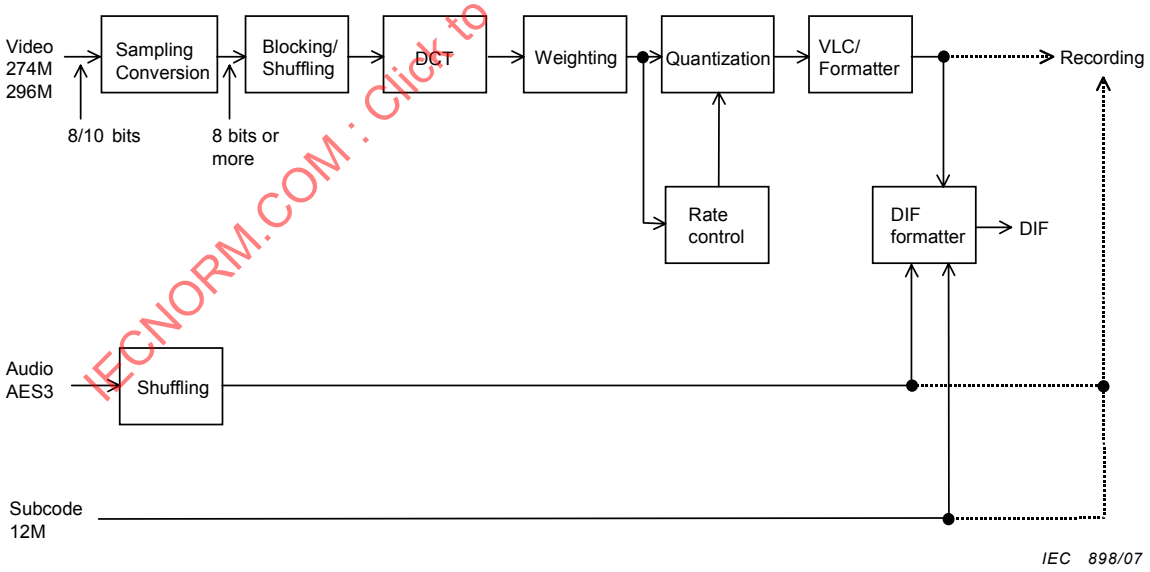


Figure 1 – Data processing block diagram

4.2 Data structure

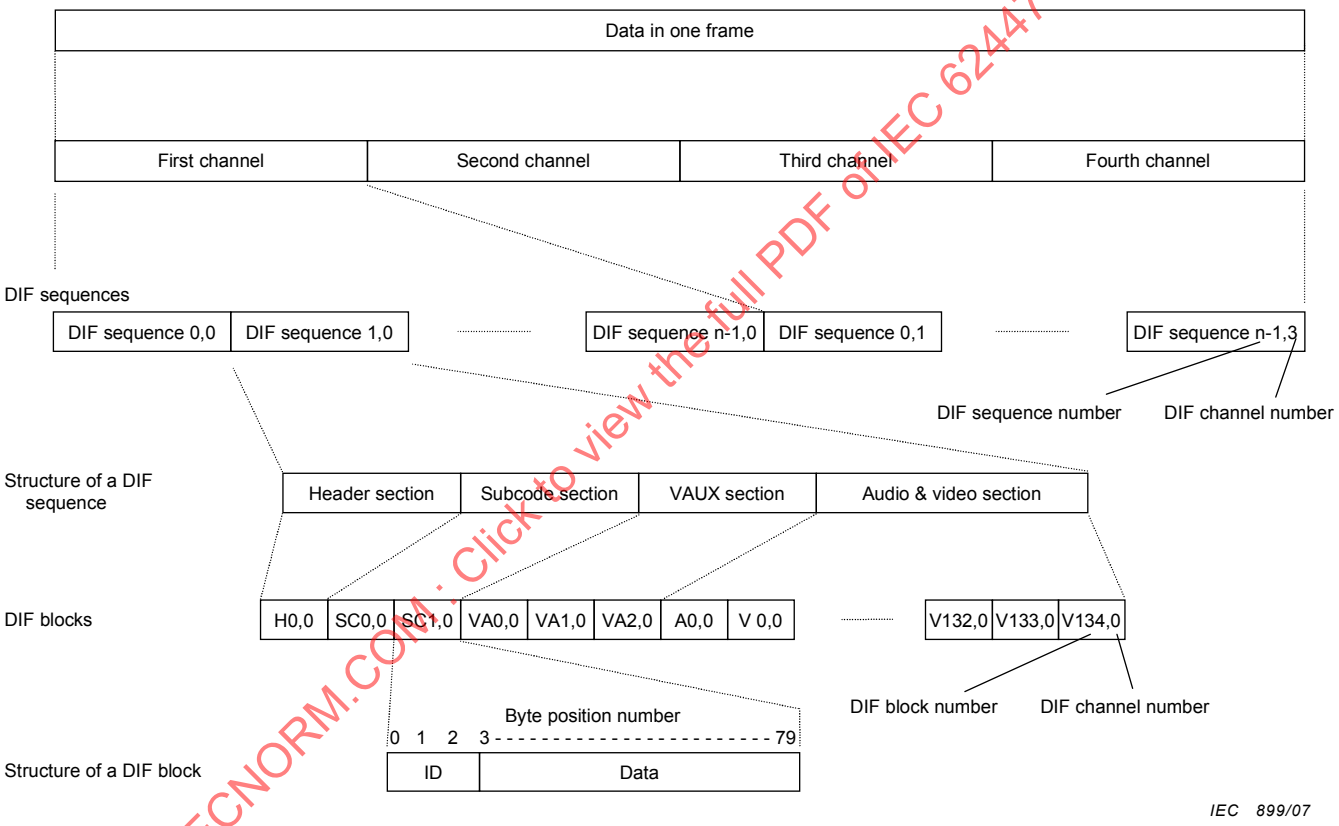
The data structure of the compressed stream at the digital interface is shown in Figure 2. The data of each frame are divided into four DIF channels.

Each DIF channel is divided into 10 DIF sequences for the 60 Hz system and 12 DIF sequences for the 50 Hz system.

Each DIF sequence consists of a header section, subcode section, VAUX section, audio section, and video section with the following DIF blocks respectively.

Header section:	1 DIF block
Subcode section:	2 DIF blocks
VAUX section:	3 DIF blocks
Audio section:	9 DIF blocks
Video section:	135 DIF blocks

As shown in Figure 2, each DIF block consists of a 3-byte ID and 77 bytes of data. DIF data bytes are numbered 0 to 79. Figure 3 shows the data structure of a DIF sequence.

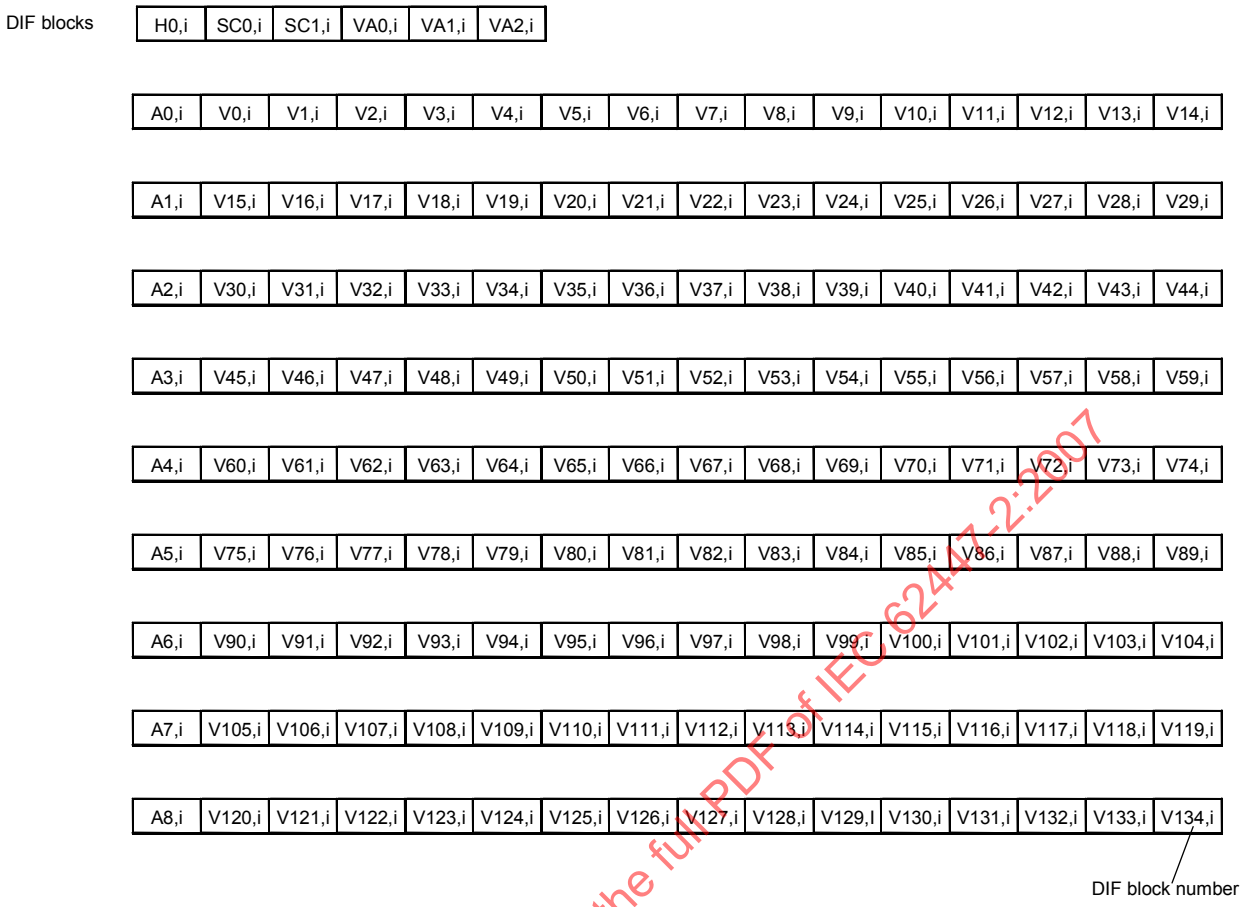


where

n = 10 for the 60 Hz system;

n = 12 for the 50 Hz system.

Figure 2 – Data structure



where

I is the DIF channel number;

i = 0,1,2,3;

H0,I is the DIF block in the header section;

SC0,i to SC1,I are the DIF blocks in the subcode section;

VA0,i to VA2,I are the DIF blocks in the VAUX section;

A0,i to A8,I are the DIF blocks in the audio section;

V0,i to V134,I are the DIF blocks in the video section.

Figure 3 – Data structure of a DIF sequence

4.3 Header section

4.3.1 ID

The ID part of each DIF block in the header section shown in Figure 2 consists of 3 bytes (ID0, ID1, ID2). Table 1 shows the ID content of a DIF block.

Table 1 – ID data of a DIF block

	Byte position number		
	Byte 0 (ID0)	Byte 1 (ID1)	Byte 2 (ID2)
MSB	SCT2	Dseq3	DBN7
	SCT1	Dseq2	DBN6
	SCT0	Dseq1	DBN5
	Res	Dseq0	DBN4
	Arb	FSC	DBN3
	Arb	FSP	DBN2
	Arb	Res	DBN1
LSB	Arb	Res	DBN0

The ID contains the following.

SCT: Section type (see Table 2)

Dseq: DIF sequence number (see Table 3 and 4)

FSC, FSP: Channel identification of a DIF block (see Table 5)

NOTE The FSP bit is reserved in SMPTE 314M.

DBN: DIF block number (see Table 6)

Arb: Arbitrary bit

Res: Reserved bit for future use

Default value shall be set to 1

Table 2 – Section type

Section type bit			Section type
SCT2	SCT1	SCT0	
0	0	0	Header
0	0	1	Subcode
0	1	0	VAUX
0	1	1	Audio
1	0	0	Video
1	0	1	Reserved
1	1	0	
1	1	1	

Table 3 – DIF sequence number for the 60 Hz system

DIF sequence number bit				DIF sequence number
Dseq3	Dseq2	Dseq1	Dseq0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	Not used
1	0	1	1	Not used
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	Not used

Table 4 – DIF sequence number for the 50 Hz system

DIF sequence number bit				DIF sequence number
Dseq3	Dseq2	Dseq1	Dseq0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	Not used

Table 5 – DIF channel number

FSC	FSP	DIF channel number
0	1	0: first channel
1	1	1: second channel
0	0	2: third channel
1	0	3: fourth channel

Table 6 – DIF block number

DIF block number bit								DIF block number
DBN7	DBN6	DBN5	DBN4	DBN3	DBN2	DBN1	DBN0	
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	0	0	0	0	1	1	0	134
1	0	0	0	0	1	1	1	Not used
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	Not used

4.3.2 Data

The data part (payload) of each DIF block in the header section is shown in Table 7. Bytes 3 to 7 are active and bytes 8 to 79 are reserved.

Table 7 – Data (payload) in the header section

	Byte position number of Header DIF block							
	3	4	5	6	7	8	-------	79
MSB	DSF	Res	TF1	TF2	TF3	Res	-------	Res
	0	Res	Res	Res	Res	Res	-------	Res
	Res	Res	Res	Res	Res	Res	-------	Res
	Res	Res	Res	Res	Res	Res	-------	Res
	Res	Res	Res	Res	Res	Res	-------	Res
	Res	APT2	AP12	AP22	AP32	Res	-------	Res
	Res	APT1	AP11	AP21	AP31	Res	-------	Res
LSB	Res	APT0	AP10	AP20	AP30	Res	-------	Res

DSF: DIF sequence flag

0 = 10 DIF sequences included in a DIF channel (60 Hz system)

1 = 12 DIF sequences included in a DIF channel (50 Hz system)

APTn, AP1n, AP2n, and AP3n data shall be identical to the track application IDs (APTn = 001, AP1n = 001, AP2n = 001, AP3n = 001), if the source signal comes from the DV-based digital VCR. If the signal source is unknown, all bits for this data shall be set to 1.

T F: Transmitting flag

TF1: Transmitting flag of audio DIF blocks

TF2: Transmitting flag of VAUX and video DIF blocks

TF3: Transmitting flag of subcode DIF blocks

0 = Valid data

1 = Invalid data.

Res: Reserved bit for future use

Default value shall be set to 1.

4.4 Subcode section

4.4.1 ID

The ID part of each DIF block in the subcode section is the same as that described in 4.3.1. The section type shall be 001.

4.4.2 Data

The data part (payload) of each DIF block in the subcode section is shown in Figure 4. The subcode data consists of 6 SSYBs, each 48 bytes long, and a reserved area of 29 bytes in each DIF block. SSYBs in a DIF sequence are numbered 0 to 11. Each SSYB is composed of an SSYB ID equal to 2 bytes, an FFh, and an SSYB data payload of 5 bytes.

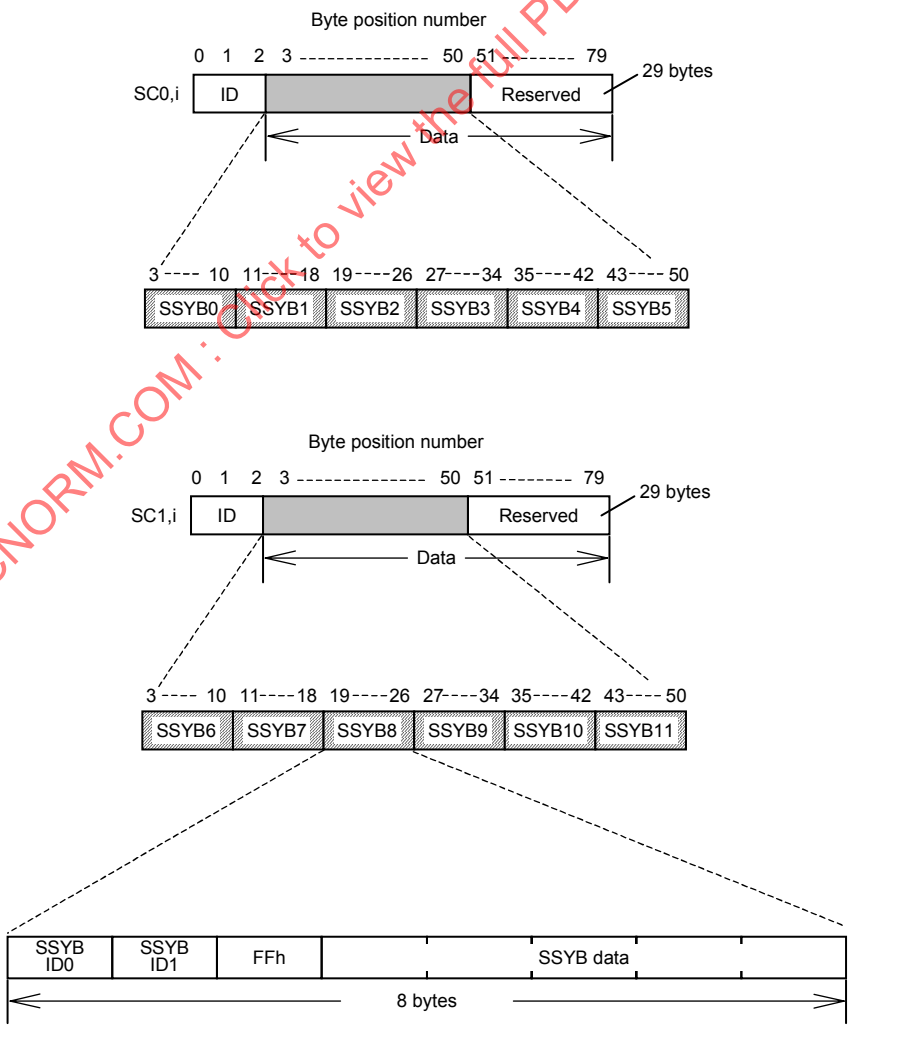


Figure 4 – Data in the subcode section

4.4.2.1 SSYB ID

Table 8 shows the parts of SSYB ID (ID0, ID1). It contains FR ID, application ID ($AP3_2$, $AP3_1$, $AP3_0$), (APT_2, APT_1, APT_0), and SSYB number (Syb_3, Syb_2, Syb_1, Syb_0).

Table 8 – SSYB ID

Bit position	SSYB number 0 and 6		SSYB number 1 to 5 and 7 to 10		SSYB number 11	
	ID0	ID1	ID0	ID1	ID0	ID1
b7	FR	Arb	FR	Arb	FR	Arb
b6	AP32	Arb	Res	Arb	APT2	Arb
b5	AP31	Arb	Res	Arb	APT1	Arb
b4	AP30	Arb	Res	Arb	APT0	Arb
b3	Arb	Syb3	Arb	Syb3	Arb	Syb3
b2	Arb	Syb2	Arb	Syb2	Arb	Syb2
b1	Arb	Syb1	Arb	Syb1	Arb	Syb1
b0	Arb	Syb0	Arb	Syb0	Arb	Syb0
NOTE Arb = arbitrary bit						

FR: The identification for the first half or second half of each DIF channel.

1 = the first half of each DIF channel

0 = the second half of each DIF channel

The first half of each DIF channel

DIF sequence number 0, 1, 2, 3, 4 for 60 Hz system

DIF sequence number 0, 1, 2, 3, 4, 5 for 50 Hz system

The second half of each DIF channel

DIF sequence number 5, 6, 7, 8, 9 for 60 Hz system

DIF sequence number 6, 7, 8, 9, 10, 11 for 50 Hz system

If information is not available, all bits shall be set to 1.

4.4.2.2 SSYB data

Each SSYB data payload consists of a pack of 5 bytes as shown in Figure 5. Table 9 shows the pack header table (PC0 byte organization). Table 10 shows the pack arrangement in SSYB data for each DIF channel.

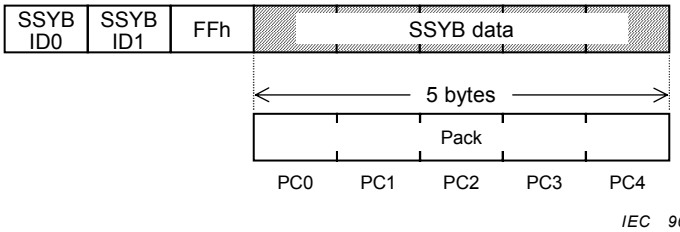


Figure 5 – Pack in SSYB

Table 9 – Pack header table

UPPER / LOWER	0000	0001	0010	0011	0100	0101	0110	0111	-----	1111
0000						AUDIO SOURCE	VIDEO SOURCE			
0001						AUDIO SOURCE CONTROL	VIDEO SOURCE CONTROL			
0010										
0011		TIME CODE								
0100		BINARY GROUP								
0101										
⋮										
1111										NO INFO

Table 10 – Mapping of packets in SSYB data

SSYB number	The first half of each DIF channel	The second half of each DIF channel
0	Reserved	Reserved
1	Reserved	Reserved
2	Reserved	Reserved
3	TC	TC
4	BG	Reserved
5	TC	Reserved
6	Reserved	Reserved
7	Reserved	Reserved
8	Reserved	Reserved
9	TC	TC
10	BG	Reserved
11	TC	Reserved

NOTE 1 TC is the time code pack.

NOTE 2 BG is the binary group pack.

NOTE 3 Reserved: the default value of all bits should be set to 1.

NOTE 4 TC and BG data are the same within each frame. The time code data are an LCT type

4.4.2.2.1 Time code pack (TC)

Table 11 shows a mapping of the time code pack. The time code data mapped to the time code packs are the same within each frame.

Table 11 – Mapping of time code pack

60 Hz system

	MSB							LSB
PC0	0	0	0	1	0	0	1	1
PC1	CF	DF	TENS of FRAMES		UNITS of FRAMES			
PC2	PC	TENS of SECONDS			UNITS of SECONDS			
PC3	BGF0	TENS of MINUTES			UNITS of MINUTES			
PC4	BGF2	BGF1	TENS of HOURS		UNITS of HOURS			

50 Hz system

	MSB							LSB
PC0	0	0	0	1	0	0	1	1
PC1	CF	Arb	TENS of FRAMES		UNITS of FRAMES			
PC2	BGF0	TENS of SECONDS			UNITS of SECONDS			
PC3	BGF2	TENS of MINUTES			UNITS of MINUTES			
PC4	PC	BGF1	TENS of HOURS		UNITS of HOURS			

NOTE Detailed information is given in ANSI/SMPTE 12M.

CF: Colour frame

0 = unsynchronized mode

1 = synchronized mode

DF: Drop frame flag

0 = Non-drop frame time code

1 = Drop frame time code

PC: Biphase mark polarity correction

0 = Even

1 = Odd

BGF: Binary group flag

Arb: Arbitrary bit

4.4.2.2.2 Binary group pack (BG)

Table 12 shows the mapping of binary group pack. Binary group data mapped to the binary group packs are the same within each frame.

Table 12 – Mapping of binary group pack

	MSB							LSB
PC0	0	0	0	1	0	1	0	0
PC1	BINARY GROUP2				BINARY GROUP1			
PC2	BINARY GROUP4				BINARY GROUP3			
PC3	BINARY GROUP6				BINARY GROUP5			
PC4	BINARY GROUP8				BINARY GROUP7			

4.5 VAUX section

4.5.1 ID

The ID part of each DIF block in the VAUX section is the same as that described in 4.3.1. The section type shall be 010.

4.5.2 Data

The data part (payload) of each DIF block in the VAUX section is shown in Figure 6. This figure shows the VAUX pack arrangement for each DIF sequence.

There are 15 packs, each 5 bytes long, and two reserved bytes in each VAUX DIF block payload. A default value for the reserved byte is set to FFh.

Therefore, there are 45 packs in a DIF sequence. VAUX packs of the DIF blocks are sequentially numbered 0 to 44. This number is called a video pack number.

Table 13 shows the mapping of the VAUX packs of the VAUX DIF blocks. A VAUX source pack (VS) and a VAUX source control pack (VSC) must exist in each frame. The remaining VAUX packs of the DIF blocks in a DIF sequence are reserved and the value of all reserved words is set to FFh.

If VAUX data are not transmitted, a NO INFO pack, which is filled with FFh, shall be transmitted.

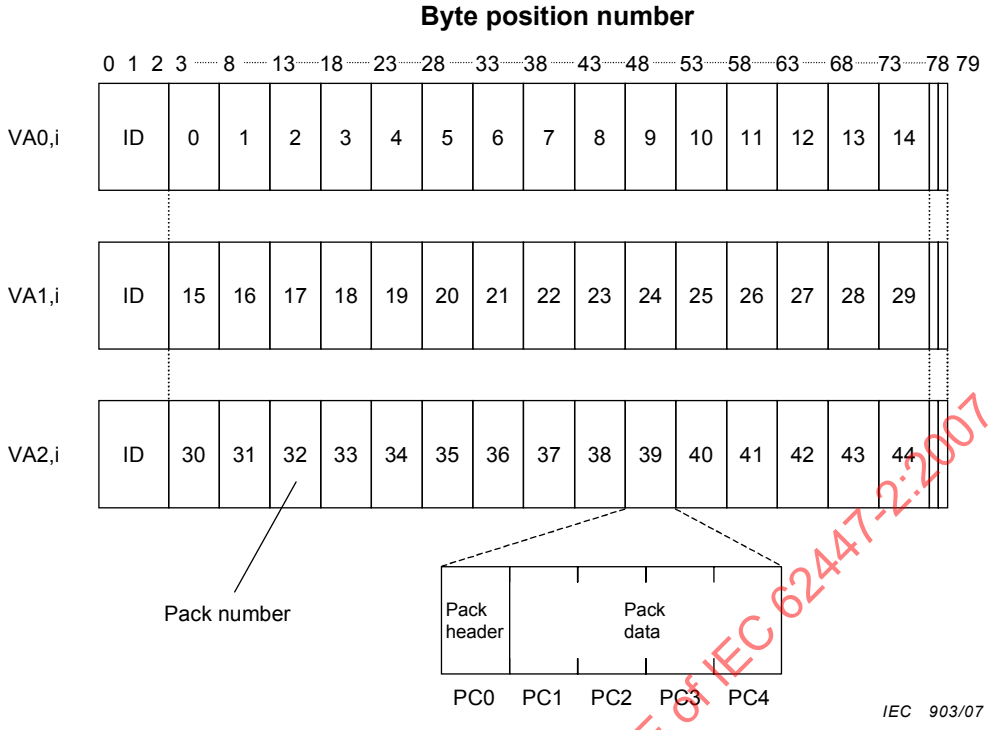


Figure 6 – Data in the VAUX section

Table 13 – Mapping of VAUX pack in a DIF sequence

Pack Number		Pack data
Even DIF sequence	Odd DIF sequence	
39	0	VS
40	1	VSC

Even DIF sequence:

DIF sequence number 0, 2, 4, 6, 8 for 60 Hz system

DIF sequence number 0, 2, 4, 6, 8, 10 for 50 Hz system

Odd DIF sequence:

DIF sequence number 1, 3, 5, 7, 9 for 60 Hz system

DIF sequence number 1, 3, 5, 7, 9, 11 for 50 Hz system

4.5.2.1 VAUX source pack (VS)

Table 14 shows the mapping of a VAUX source pack.

Table 14 – Mapping of VAUX source pack

	MSB							LSB
PC0	0	1	1	0	0	0	0	0
PC1	Res	Res	Res	Res	Res	Res	Res	Res
PC2	Res	Res	Res	Res	Res	Res	Res	Res
PC3	Res	Res	50/60	STYPE				
PC4	0	Res	Res	Res	Res	Res	Res	Res

50/60:

0 = 60 Hz system

1 = 50 Hz system

STYPE: Video signal type

For 60 Hz system

0 0 0 0 0 b = 4:1:1 compression (D-7, 25 Mb/s)

0 0 1 0 0 b = 4:2:2 compression (D-7, 50 Mb/s)

1 0 1 0 0 b = 1080/60i compression, active line 1080 (D-12,100 Mb/s)

1 0 1 0 1 b = 1080/60i compression, active line 1035 (D-12,100 Mb/s)

1 1 0 0 0 b = 720/60p compression (D-12, 100 Mb/s)

Other = Reserved

For 50 Hz system

0 0 0 0 0 b = 4:1:1 compression (D-7, 25 Mb/s)

0 0 1 0 0 b = 4:2:2 compression (D-7, 50 Mb/s)

1 0 1 0 0 b = 1080/50i compression (D-12,100 Mb/s)

Other = Reserved

Res: Reserved bit for future use

The default value shall be set to 1.

4.5.2.2 VAUX source control pack

Table 15 shows mapping of VAUX source control pack.

Table 15 – Mapping of VAUX source control pack

	MSB							LSB
PC0	0	1	1	0	0	0	0	1
PC1	CGMS		Res	Res	Res	Res	Res	Res
PC2	Res	Res	0	0	Res	DISP		
PC3	FF	FS	FC	Res	Res	Res	0	0
PC4	Res	Res	Res	Res	Res	Res	Res	Res

CGMS: Copy generation management system

0 0 b = Copy free

Other = Reserved

DISP: Display select mode

0 1 0 b = 16:9

Other = Reserved

FF: Frame/Field flag

For the 1080-line system (see Table 16)

FF indicates whether two consecutive fields are delivered or one field is repeated twice during one video frame period (see Table 16).

0 = Only one of the two fields is delivered twice

1 = Both fields are delivered in order

For the 720-line system (see Table 17)

FF indicates whether two consecutive video frames are delivered or one video frame is repeated twice during the two video frames period.

0 = Only one of the two video frames is delivered twice

1 = Both video frames are delivered in order

FS: First/second field flag

For the 1080-line system (see Table 16)

FS indicates a field which is delivered during the field one period (see Table 16)

0 = Field 2 is delivered

1 = Field 1 is delivered

For the 720-line system (see Table 17)

FS indicates a video frame which is delivered during the video frame one period.

0 = Video frame 2 is delivered

1 = Video frame 1 is delivered

Table 16 – FF/FS for the 1080-line system

FF	FS	Output field
1	1	Field 1 and field 2 are output in this order (1,2 sequence)
1	0	Field 2 and field 1 are output in this order (2,1 sequence)
0	1	Field 1 is output twice
0	0	Field 2 is output twice

Table 17 – FF/FS for the 720-line system

FF	FS	Output video frame
1	1	Video frame 1 and video frame 2 are output in this order (1,2 sequence)
1	0	Video frame 2 and video frame 1 are output in this order (2,1 sequence)
0	1	Video frame 1 is output twice
0	0	Video frame 2 is output twice

FC: Frame change flag

For the 1080-line system

FC indicates whether the picture of the current video frame is repeated based on immediate previous video frame.

0 = Same picture as the previous video frame

1 = Different picture than the previous video frame

For the 720-line system

FC indicates whether the picture of the current two video frames is repeated based on immediate previous two video frames

0 = Same picture as the previous two video frames

1 = Different picture than the previous two video frames

Res: Reserved bit for future use

The default value shall be set to 1.

4.6 Audio section

4.6.1 ID

The ID part of each DIF block in the audio section is the same as described in 3.3.1. The section type shall be 011.

4.6.2 Data

The data part (payload) of each DIF block in the audio section is shown in Figure 7. The data of a DIF block in the audio section are composed of 5 bytes of audio auxiliary data (AAUX) and 72 bytes of audio data which is encoded and shuffled by the process as described in 3.6.2.1 and 3.6.2.2.

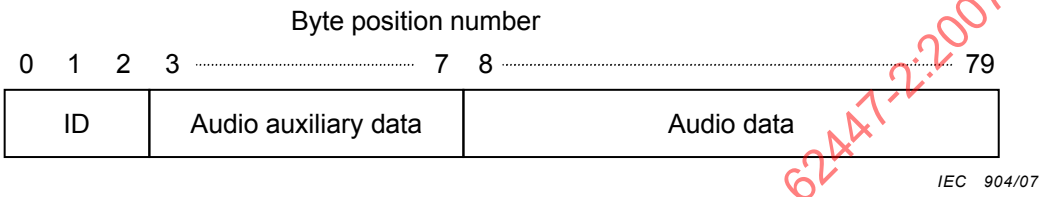


Figure 7 – Data in the audio section

4.6.2.1 Audio encoding

4.6.2.1.1 Source coding

Each audio input signal is sampled at 48 kHz with 16-bit quantization. The system provides eight audio channels. Audio data for each audio channel are located in each respective audio block.

4.6.2.1.2 Emphasis

The audio encoding is carried out with the first order pre-emphasis of 50/15 µs. For the analogue input recording, emphasis shall be off in the default state.

4.6.2.1.3 Audio error code

In the encoded audio data, 8000 h shall be assigned as an audio error code to indicate an invalid audio sample. This code corresponds to negative full scale value in ordinary twos complement representation. When the encoded data includes 8000 h, it shall be converted to 8001 h.

4.6.2.1.4 Relative audio-video timing

1080-line system

An audio frame begins with an audio sample acquired within the duration of minus 50 samples relative to zero samples from the start of line number 1.

720-line system

An audio frame begins with an audio sample acquired within the duration of minus 50 samples relative to zero samples from the start of line number 1 of video frame 1.

4.6.2.1.5 Audio frame processing

The audio data is processed in each audio frame. Each audio frame contains 1602 or 1600 audio samples for the 60 Hz system or 1920 audio samples for the 50 Hz system for an audio channel with associated status, user, and validity data. For the 60 Hz system, the number of audio samples per audio frame shall follow the five-frame sequence as shown below:

1600, 1602, 1602, 1602, 1602 samples.

One audio frame shall be capable of 1620 samples for the 60 Hz system or 1944 samples for the 50 Hz system. The unused space at the end of each audio frame is filled with arbitrary values.

4.6.2.2 Audio shuffling

The 16-bit audio data word is divided into two bytes. The upper byte contains MSB, and the lower byte contains LSB, as shown in Figure 8. Audio data shall be shuffled over DIF sequences and DIF blocks within an audio frame. The data bytes are defined as D_n (n = 0, 1, 2,.....) which is sampled in the n-th order within an audio frame and shuffled by each D_n unit.

The data shall be shuffled through a process as expressed by the following equations.

60 Hz system:

DIF channel number
- i = 0: Audio CH1,CH2
- i = 1: Audio CH3,CH4
- i = 2: Audio CH5,CH6
- i = 3: Audio CH7,CH8

DIF Sequence number:

(INT (n/3) + 2 × (n mod 3)) mod 5 for Audio CH1,CH3,CH5,CH7

(INT (n/3) + 2 × (n mod 3)) mod 5 + 5 for Audio CH2,CH4,CH6,CH8

Audio DIF block number: 3 x (n mod 3) + INT ((n mod 45)/15)

Byte position number:
- 8 + 2 × INT(n/45) for the most significant byte
- 9 + 2 × INT(n/45) for the least significant byte

where n = 0 to 1619

50-Hz system:

DIF channel number
- i = 0: Audio CH1,CH2
- i = 1: Audio CH3,CH4
- i = 2: Audio CH5,CH6
- i = 3: Audio CH7,CH8

DIF Sequence number:

(INT (n/3) + 2 × (n mod 3)) mod 6 for Audio CH1,CH3,CH5,CH7

(INT (n/3) + 2 × (n mod 3)) mod 6 + 6 for Audio CH2,CH4,CH6,CH8

Audio DIF block number: 3 x (n mod 3) + INT ((n mod 54)/18)

Byte position number:
- 8 + 2 × INT(n/54) for the most significant byte
- 9 + 2 × INT(n/54) for the least significant byte

where n = 0 to 1943

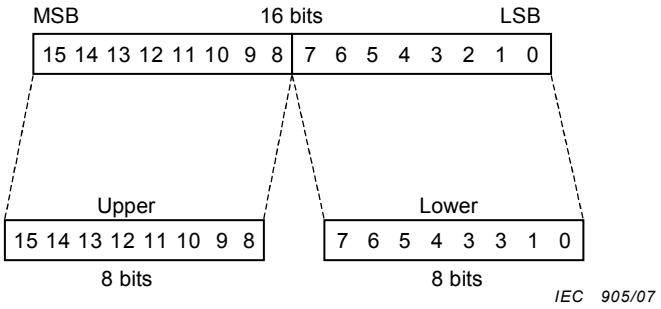


Figure 8 – Conversion of audio sample to audio data bytes

4.6.2.3 Audio auxiliary data (AAUX)

AAUX shall be added to the shuffled audio data as shown in Figures 7 and 9. The AAUX pack shall include an AAUX pack header and data (AAUX payload). The length of the AAUX pack shall be 5 bytes as shown in Figure 9, which depicts the AAUX pack arrangement. Packs are numbered 0 to 8 as shown in Figure 9. This number is called an audio pack number.

Table 18 shows the mapping of an AAUX pack. An AAUX source pack (AS) and an AAUX source control pack (ASC) shall be included in the compressed stream.

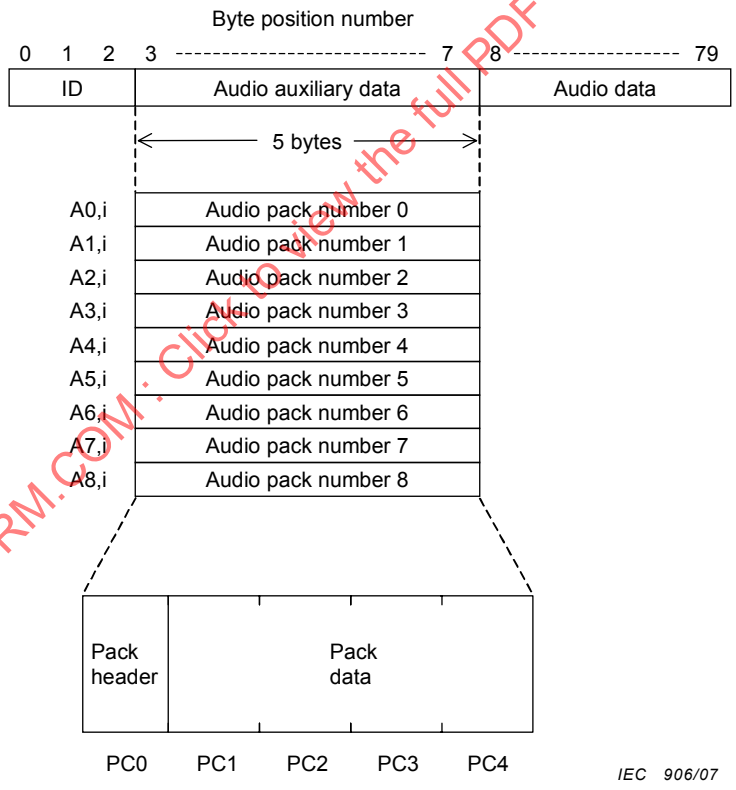


Figure 9 – Arrangement of AAUX packs in audio auxiliary data

Table 18 – Mapping of AAUX pack in a DIF sequence

Audio pack Number		
Even DIF sequence	Odd DIF sequence	Pack data
3	0	AS
4	1	ASC

Even DIF sequence:

DIF sequence number 0, 2, 4, 6, 8 for 60 Hz system

DIF sequence number 0, 2, 4, 6, 8, 10 for 50 Hz system

Odd DIF sequence:

DIF sequence number 1, 3, 5, 7, 9 for 60 Hz system

DIF sequence number 1, 3, 5, 7, 9, 11 for 50 Hz system

4.6.2.3.1 AAUX source pack (AS)

The AAUX Source pack is configured as shown in Table 19.

Table 19 – Mapping of AAUX source pack

	MSB							LSB
PC0	0	1	0	1	0	0	0	0
PC1	LF	Res	AF SIZE					
PC2	0	CHN		Res	AUDIO MODE			
PC3	Res	Res	50/60	STYPE				
PC4	Res	Res	SMP		QU			

LF: Locked mode flag

Locking condition of audio sampling frequency with video signal.

0 = Locked mode

1 = Reserved

AF SIZE: The number of audio samples per frame

0 1 0 1 0 0 b = 1600 samples/frame (60 Hz system)

0 1 0 1 1 0 b = 1602 samples/frame (60 Hz system)

0 1 1 0 0 0 b = 1920 samples/frame (50 Hz system)

Other = Reserved

CHN: The number of audio channels within an audio block

0 0 b = One audio channel per an audio block

Other = Reserved

An audio block consists of 45 DIF blocks (9 DIF blocks x 5 DIF sequences) for the 60 Hz system and 54 DIF blocks (9 DIF blocks x 6 DIF sequences) for the 50 Hz system.

AUDIO MODE: The contents of the audio signal on each audio channel

0 0 0 0 b = Audio CH1,CH3,CH5,CH7

0 0 0 1 b = Audio CH2,CH4,CH6,CH8

1 1 1 1 b = Invalid audio data

Other = Reserved

50/60:

0 = 60 Hz system

1 = 50 Hz system

STYPE: Audio blocks for each frame

0 0 0 0 0 b = 2 audio blocks

0 0 0 1 0 b = 4 audio blocks

0 0 0 1 1 b = 8 audio blocks

Other = Reserved

SMP: Sampling frequency

0 0 0 b = 48 kHz

Other = Reserved

QU: Quantization

0 0 0 b = 16 bits linear

Other = Reserved

Res: Reserved bit for future use

The default value shall be set to 1.

4.6.2.3.2 AAUX source control pack (ASC)

The AAUX source control pack is configured as shown in Table 20.

Table 20 – Mapping of AAUX source control pack

	MSB							LSB
PC0	0	1	0	1	0	0	0	1
PC1	CGMS		Res	Res	Res	Res	EFC	
PC2	REC ST	REC END	FADE ST	FADE END	Res	Res	Res	Res
PC3	DRF	SPEED						
PC4	Res	Res	Res	Res	Res	Res	Res	Res

CGMS: Copy generation management system

0 0 b = Copy free

Other = Reserved

EFC: Emphasis audio channel flag

0 0 b = Emphasis off

0 1 b = Emphasis on

Other = Reserved

EFC shall be set for each audio block.

REC ST: Recording start point

0 = Recording start point

1 = Not recording start point

At a recording start frame, REC ST 0 lasts for a duration of one audio block which is equal to 5 or 6 DIF sequences for each audio channel.

REC END: Recording end point

0 = Recording end point

1 = Not recording end point

At a recording end frame, REC END 0 is lasting for a duration of one audio block which is equal to 5 or 6 DIF sequences for each audio channel.

FADE ST: Fading of recording start point

0 = Fading off

1 = Fading on

The FADE ST information is only effective at the recording start frame (REC ST = 0).If FADE ST is 1 at the recording start frame, the output audio signal should be faded in

from the first sampling signal of the frame. If FADE ST is 0 at the recording start frame, the output audio signal should not be faded.

FADE END: Fading of recording end point

0 = Fading off

1 = Fading on

The FADE END information is only effective at the recording end frame (REC END = 0). If FADE END is 1 at the recording end frame, the output audio signal should be faded out to the last sampling signal of the frame. If FADE END is 0 at the recording end frame, the output audio signal should not be faded.

DRF: Direction flag

0 = Reverse direction

1 = Forward direction

SPEED: shuttle speed of VTR (see Table 21)

Table 21 – SPEED code definition

Codeword MSB LSB	Shuttle speed of VTR	
	60 Hz system	50 Hz system
0000000	0/120 (=0)	0/100 (=0)
0000001	1/120	1/100
:	:	:
1100100	100/120	100/100 (=1)
:	:	Reserved
1111000	120/120 (=1)	Reserved
:	Reserved	Reserved
1111110	Reserved	Reserved
1111111	Data invalid	Data invalid

Res: Reserved bit for future use

Default value shall be set to 1.

4.7 Video section

4.7.1 ID

The ID part of each DIF block in the video section is the same as described in 4.3.1. The section type shall be 100.

4.7.2 Data

The data part (payload) of each DIF block in the video section consists of 77 bytes of video data which shall be sampled, shuffled and encoded. The video data of every frame is processed as described in Clause 5.

This 77 byte data are called a compressed macro block.

4.7.2.1 DIF block and compressed macro block

Correspondence between video DIF blocks and video compressed macro blocks CM h,i,j,k is shown in Table 22 for the 60 Hz system and Table 23 for the 50 Hz system.

The rule defining the correspondence between video DIF blocks and compressed macro blocks is shown below:

60 Hz system

```
for(h=0; h<4; h++){
   for(s=0; s<2; s++){
      for(k=0; k<27; k++){
         for(t=0; t<5; t++){
            a = (4h + s + 2t + 2) mod 10;
            b = (4h + s + 2t + 6) mod 10;
            c = (4h + s + 2t + 8) mod 10;
            d = (4h + s + 2t + 0) mod 10;
            e = (4h + s + 2t + 4) mod 10;
             DBNq = (5t + 25k) mod 135;
             DSNp = INT((5t + 25k + 675s)/135);

            V DBNq, h       of DSNp = CM h,a,2,k
            V (DBNq + 1), h of DSNp = CM h,b,1,k
            V (DBNq + 2), h of DSNp = CM h,c,3,k
            V (DBNq + 3), h of DSNp = CM h,d,0,k
            V (DBNq + 4), h of DSNp = CM h,e,4,k
         }
      }
   }
}
```

where

DBNq: DIF block number
DSNp: DIF sequence number
h: Divided block
s, t: Vertical order of super block
k: Macro block order in super block

50 Hz system

```
for(h=0; h<4; h++){
   for(k=0; k<27; k++){
      for(i=0; i<11; i++){
            a = (4h + i + 2) mod 11;
            b = (4h + i + 6) mod 11;
            c = (4h + i + 8) mod 11;
            d = (4h + i + 0) mod 11;
            e = (4h + i + 4) mod 11;
             DBNq = (5i + 55k) mod 135;
              DSNp = INT((5i + 55k)/135);

            V DBNq, h       of DSNp = CM h,a,2,k
            V (DBNq + 1), h of DSNp = CM h,b,1,k
            V (DBNq + 2), h of DSNp = CM h,c,3,k
            V (DBNq + 3), h of DSNp = CM h,d,0,k
            V (DBNq + 4), h of DSNp = CM h,e,4,k
      }
   }
}
for(k=0; k<27; k++){
             DBNq = 5k;
             DSNp = 11;

            V DBNq, 0       of DSNp = CM 0,11,0,k
            V (DBNq + 1), 0 of DSNp = CM 0,11,1,k
```

V (DBNq + 2), 0 of DSNp = CM 0,11,2,k
V (DBNq + 3), 0 of DSNp = CM 0,11,3,k
V (DBNq + 4), 0 of DSNp = CM 0,11,4,k
}

where

DBNq is the DIF block number;
DSNp is the DIF sequence number;
H is the divided block;
I is the vertical order of the super block;
K is the macro block order in the super block.

Table 22 – Video DIF blocks and compressed macro blocks for the 60 Hz system

DIF channel number	DIF sequence number	DIF block	Compressed macro block
0	0	V 0,0	CM 0,2,2,0
		V 1,0	CM 0,6,1,0
		V 2,0	CM 0,8,3,0
		V 3,0	CM 0,0,0,0
		V 4,0	CM 0,4,4,0
		:	:
	:	:	:
	9	:	:
		V 134,0	CM 0,3,4,26
1	0	V 0,1	CM 1,6,2,0
		V 1,1	CM 1,0,1,0
		V 2,1	CM 1,2,3,0
		V 3,1	CM 1,4,0,0
		V 4,1	CM 1,8,4,0
		:	:
	:	:	:
	9	:	:
		V 134,1	CM 1,7,4,26
:	:	:	:
3	0	V 0,3	CM 3,4,2,0
		V 1,3	CM 3,8,1,0
		V 2,3	CM 3,0,3,0
		V 3,3	CM 3,2,0,0
		V 4,3	CM 3,6,4,0
		:	:
	:	:	:
	9	:	:
		V 134,3	CM 3,5,4,26

Table 23 – Video DIF blocks and compressed macro blocks for the 50 Hz system

DIF channel number	DIF sequence number	DIF block	Compressed macro block
0	0	V 0,0	CM 0,2,2,0
		V 1,0	CM 0,6,1,0
		V 2,0	CM 0,8,3,0
		V 3,0	CM 0,0,0,0
		V 4,0	CM 0,4,4,0
		:	:
	:	:	:
	10	:	:
		V 134,0	CM 0,3,4,26
	11	V 0,0	CM 0,11,0,0
		V 1,0	CM 0,11,1,0
		:	:
		V 134,0	CM 0,11,4,26
1	0	V 0,1	CM 1,6,2,0
		V 1,1	CM 1,10,1,0
		V 2,1	CM 1,1,3,0
		V 3,1	CM 1,4,0,0
		V 4,1	CM 1,8,4,0
		:	:
	:	:	:
	10	:	:
		V 134,1	CM 1,7,4,26
	11	V 0,1	—
		:	:
		V 134,1	—
:	:	:	:
3	0	V 0,3	CM 3,3,2,0
		V 1,3	CM 3,7,1,0
		V 2,3	CM 3,9,3,0
		V 3,3	CM 3,1,0,0
		V 4,3	CM 3,5,4,0
		:	:
	:	:	:
	10	:	:
		V 134,3	CM 3,4,4,26
	11	V 0,3	—
		:	:
		V 134,3	—

5 Video compression

This clause includes video compression processing for the 1080/60i system, the 1080/50i system, and the 720/60p system.

5.1 Video structure

5.1.1 Video sampling structure

The video sampling structure is defined by SMPTE 274M for the 1080-line system, and SMPTE 296M for the 720-line system. The construction of luminance (Y) and two colour-difference signals (CR, CB) is described in Table 24. A sample conversion from 10-bit input video to 8bits or more is provided by the resampling process (the first processing block of Figure 1).

5.1.1.1 Video frame pixel structure

5.1.1.1.1 1080/60i system

The sampling starting point of the Y signal shall be 192T from the horizontal sync timing reference:

where T = 1,001/(74,25 × 10^6) s

1920 pixels of luminance and 960 pixels of each colour-difference signal per line shall be transmitted as shown in Figure 10. The sampling starting point in the active period of the CR and CB signals shall be the same as the sampling starting point in the active period of the Y signal. Each pixel shall be converted to the code of twos complement (–508 to 507) by inverting the MSB of the input video signal.

5.1.1.1.2 1080/50i system

The sampling starting point of the Y signal shall be 192T from the horizontal sync timing reference:

where T = 1/(74,25 × 10^6) s

1920 pixels of luminance and 960 pixels of each colour-difference signal per line shall be transmitted as shown in Figure 11. The sampling starting point in the active period of the CR and CB signals shall be the same as the sampling starting point in the active period of the Y signal. Each pixel shall be converted to the code of twos complement (-508 to 507) by inverting the MSB of the input video signal.

5.1.1.1.3 720/60p system

The sampling starting point of the Y signal shall be 260T from the horizontal sync timing reference:

where T = 1,001/(74,25 × 10^6) s

1280 pixels of luminance and 640 pixels of each colour-difference signal per line shall be transmitted as shown in Figure 12. The sampling starting point in the active period of the CR and CB signals shall be the same as the sampling starting point in the active period of the Y signal. Each pixel shall be converted to the code of twos complement (-508 to 507) by inverting the MSB of the input video signal.

5.1.1.2 Video frame line structure

5.1.1.2.1 1080-line system

540 lines for the Y, CR, and CB signals from each field shall be transmitted. The transmitted lines in each two fields are described in Table 24.

5.1.1.2.2 720-line system

720-lines for the Y, CR, and CB signals from each video frame shall be transmitted. The transmitted lines in each video frame are described in Table 24.

5.1.1.3 Horizontal resampling

5.1.1.3.1 1080/60i system

1920 horizontally sampled Y signals shall be resampled to 1280 pixels. The 960 horizontally sampled CR and CB signals shall be resampled to 640 pixels. The output signal of the resampler shall have a sample resolution equal to 8 bits or more (see Annex B).

5.1.1.3.2 1 080/50i system

1920 horizontally sampled Y signals shall be resampled to 1440 pixels. The 960 horizontally sampled CR and CB signals shall be resampled to 720 pixels. The output signal of the resampler shall have a sample resolution equal to 8 bits or more (see Annex B).

5.1.1.3.3 720/60p system

1280 horizontally sampled Y signals shall be resampled to 960 pixels. The 640 horizontally sampled CR and CB signals shall be resampled to 480 pixels. The output signal of the resampler shall have a sample resolution equal to 8 bits or more (see Annex B).

Table 24 – Construction of input video

		1080/60i system	1080/50i system	720/60p system
Sampling frequency	Y	74,25/1,001 MHz	74,25 MHz	74,25/1,001 MHz
	CR, CB	37,125/1,001 MHz	37,125 MHz	37,125/1,001 MHz
Total number of pixels per line	Y	2200		1650
	CR, CB	1100		825
The number of active pixels per line	Y	1920		1280
	CR, CB	960		640
Total number of lines per video frame		1125		750
The number of active lines per video frame		1080		720
The active line numbers		Field 1	21 to 560	26 to 745
		Field 2	584 to 1 123	
Quantization		Each sample is linearly quantized to 10 bits for Y, CR and CB.		
Relation between video signal level and quantized level	Scale	4 to 1 019		
	Y	Video signal level of white: 940 Video signal level of black: 64		Quantized level 877
	CR, CB	Video signal level of gray: 512		Quantized level 897

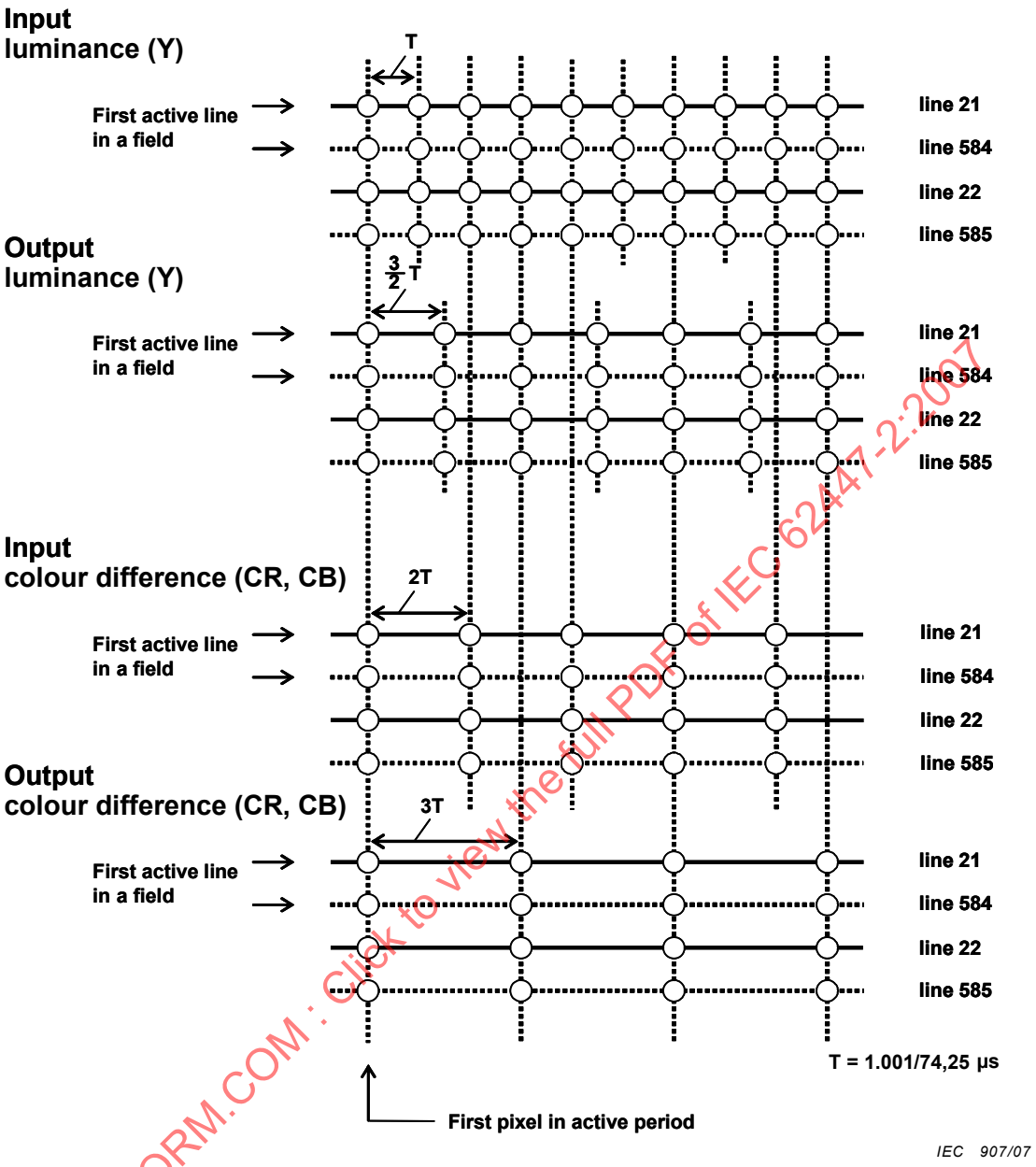


Figure 10 – Sampling structure for the 1080/60i system

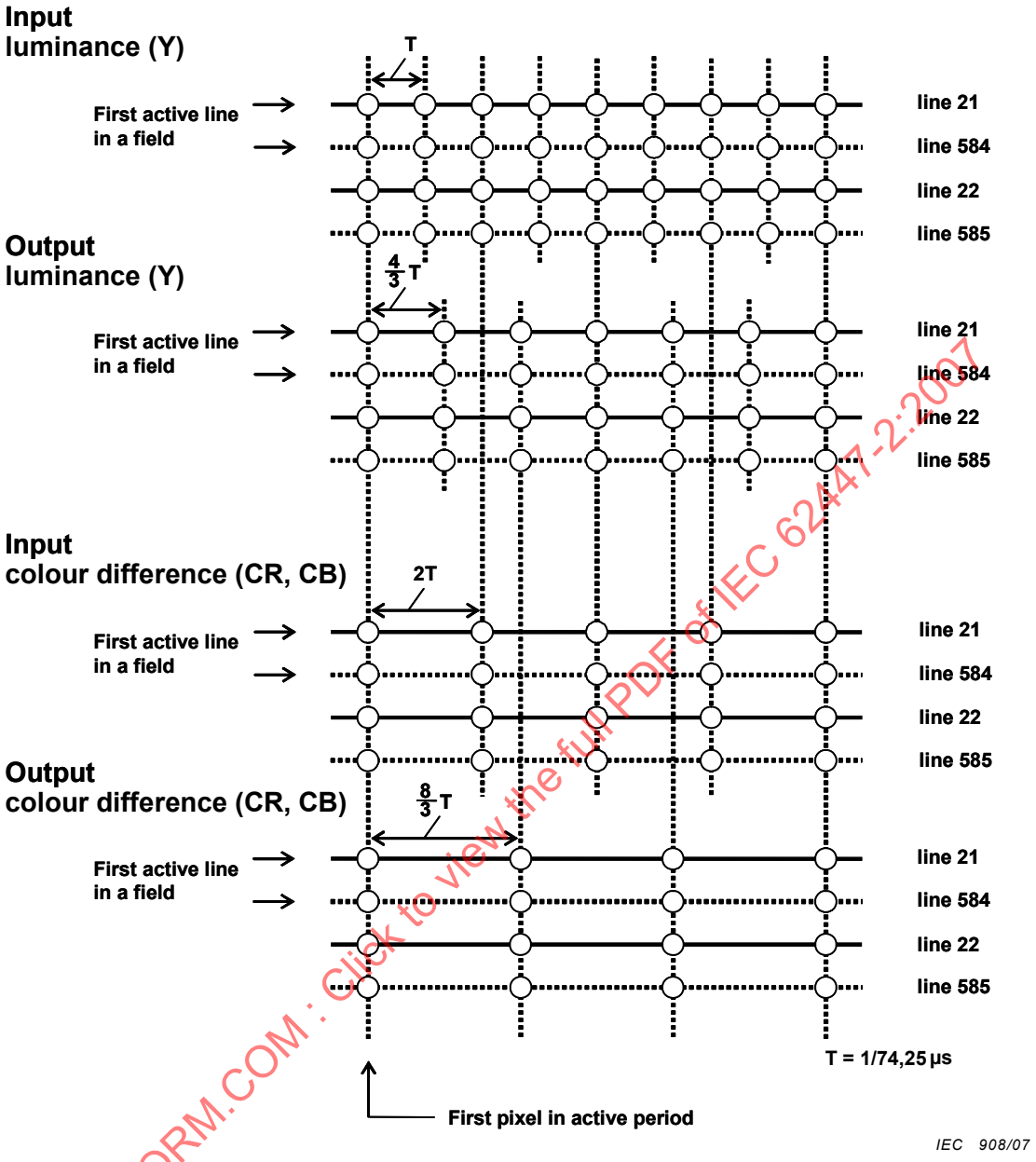


Figure 11 – Sampling structure for the 1080/50i system

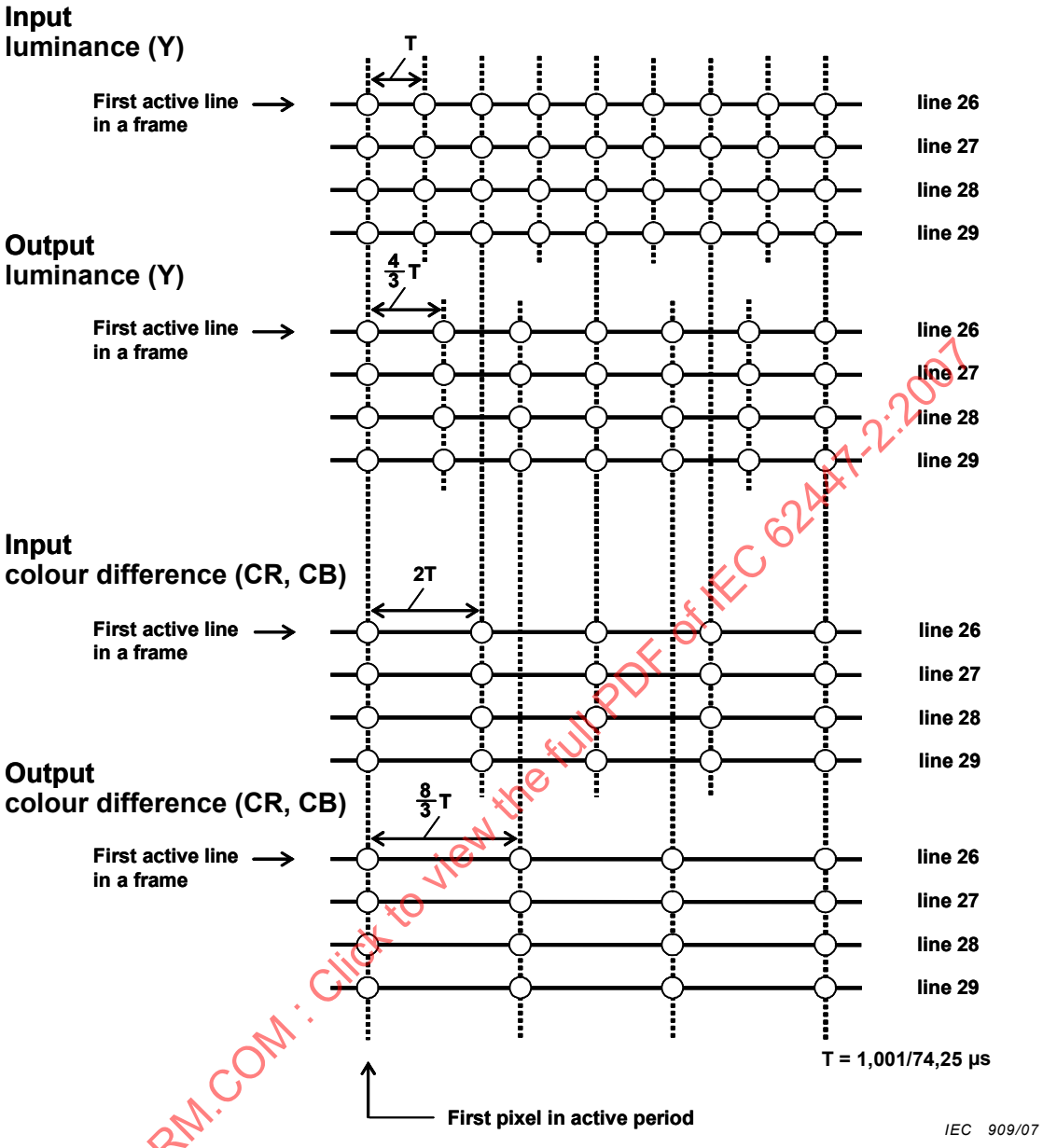


Figure 12 – Sampling structure for the 720/60p system

5.1.2 DCT block

The Y, CR, and CB pixels in each video frame shall be divided into DCT blocks as shown in Figure 13 for the 1080-line system and Figure 14 for the 720-line system. DCT blocks are structured with a rectangular area of eight vertical pixels and eight horizontal pixels in a video frame. The value of x shows the horizontal coordinate from the left and the value of y shows the vertical coordinate from the top.

For the 1080-line system, even lines of y = 0, 2, 4, 6 are the horizontal lines of field one, and odd lines of y = 1, 3, 5, 7 are those of field two.

The DCT block arrangement in each video frame follows.

5.1.2.1 1080/60i system

The arrangement of horizontal DCT blocks in each video frame is shown in Figure 15. The same horizontal arrangement is repeated to 135 DCT blocks in the vertical direction. Pixels in one video frame are divided into 43200 DCT blocks.

Y: 135 Vertical DCT blocks x 160 horizontal DCT blocks = 21600 DCT blocks
CR: 135 vertical DCT blocks x 80 horizontal DCT blocks = 10800 DCT blocks
CR: 135 vertical DCT blocks x 80 horizontal DCT blocks = 10800 DCT blocks

5.1.2.2 1080/50i system

The arrangement of horizontal DCT blocks in each video frame is shown in Figure 16. The same horizontal arrangement is repeated to 135 DCT blocks in the vertical direction. Pixels in one video frame are divided into 48600 DCT blocks.

Y: 135 Vertical DCT blocks x 180 horizontal DCT blocks = 24300 DCT blocks
CR: 135 vertical DCT blocks x 90 horizontal DCT blocks = 12150 DCT blocks
CR: 135 vertical DCT blocks x 90 horizontal DCT blocks = 12150 DCT blocks

5.1.2.3 720/60p system

The arrangement of horizontal DCT blocks in each video frame is shown in Figure 17. The same horizontal arrangement is repeated to 90 DCT blocks in the vertical direction. Pixels in one video frame are divided into 21600 DCT blocks.

Y: 90 vertical DCT blocks x 120 horizontal DCT blocks = 10800 DCT blocks
CR: 90 vertical DCT blocks x 60 horizontal DCT blocks = 5400 DCT blocks
CR: 90 vertical DCT blocks x 60 horizontal DCT blocks = 5400 DCT blocks

5.1.3 Macro block

Each macro block consists of eight DCT blocks. Figure 18 for the 1080-line system and Figure 19 for the 720-line system show the relationship between macro block and DCT blocks.

5.1.3.1 Arrangement of macro block

5.1.3.1.1 1080/60i system

The macro block arrangement in each video frame has two steps.

Step1: Arranging macro blocks

The pixels in each video frame are divided into 5400 macro blocks as shown in Figure 20.

Each macro block except the bottom macro blocks consists of four DCT blocks of Y which are horizontally and vertically adjacent, two vertically adjacent DCT blocks of CR and two vertically adjacent DCT blocks of CB on a TV screen

where 67 vertical macro blocks × 80 horizontal macro blocks = 5360 macro blocks.

Each bottom macro block consists of four horizontally adjacent DCT blocks of Y, two horizontally adjacent DCT blocks of CR and two horizontally adjacent DCT blocks of CB on a TV screen

where 1 vertical macro block × 40 horizontal macro blocks = 40 macro blocks.

Step2: Rearranging macro blocks

Sets consisting of 40 macro blocks which are named A0 to A7 and sets consisting of 30 macro blocks which are named A8 to A15 are arranged as shown in Figure 20.

40 macro blocks in A16 are arranged into 4 vertical macro blocks × 10 horizontal macro blocks in B16 respectively as shown in Figure 20

where 60 vertical macro blocks × 90 horizontal macro blocks = 5400 macro blocks

5.1.3.1.2 1080/50i system

The macro block arrangement in each video frame has two steps.

Step1: Arranging macro blocks

The pixels in each video frame are divided into 6 075 macro blocks as shown in Figure 21.

Each macro block except the bottom macro blocks consists of four DCT blocks of Y which are horizontally and vertically adjacent, two vertically adjacent DCT blocks of CR and two vertically adjacent DCT blocks of CB on a TV screen

where 67 vertical macro blocks × 90 horizontal macro blocks = 6030 macro blocks.

Each bottom macro block consists of four horizontally adjacent DCT blocks of Y, two horizontally adjacent DCT blocks of CR and two horizontally adjacent DCT blocks of CB on a TV screen

where 1 vertical macro block × 45 horizontal macro blocks = 45 macro blocks.

Step2: Rearranging macro blocks

The macro blocks are divided into a main unit and an edge unit. The edge unit contains top macro blocks in A0 and bottom macro blocks in A1 as shown in Figure 21. The main unit contains the remaining blocks

where

main unit: 66 vertical macro blocks × 90 horizontal macro blocks = 5940 macro blocks;

edge unit: 1 vertical macro blocks × 135 horizontal macro blocks = 135 macro blocks.

5.1.3.1.3 720/60p system

The pixels in each video frame are divided into 2700 macro blocks as shown in Figure 22

where 45 vertical macro blocks × 60 horizontal macro blocks = 2700 macro blocks

5.1.3.2 Divided blocks

5.1.3.2.1 1080/60i system

The macro blocks in each video frame are divided into halfway blocks as shown in Figure 23. Each halfway block H consists of nine macro blocks horizontally and one macro block vertically.

Halfway blocks H are distributed into divided blocks as follows.

Divided blocks:

h = 0: H 2m,2n

h = 1: H 2m,2n+1

h = 2: H 2m+1,2n

h = 3: H 2m+1,2n+1

where

m = 0,1,2,...,29;

n = 0,1,2,3,4.

As a result, one video frame is divided into four divided blocks. Each divided block consists of 30 vertical macro blocks × 45 horizontal macro blocks.

5.1.3.2.2 1080/50i system

Macro blocks in the main unit are divided into halfway blocks as shown in Figure 24. Each halfway block H consists of nine horizontally adjacent macro blocks.

Halfway blocks H are distributed into divided blocks as follows.

Divided blocks:

h = 0: H 2m,2n

h = 1: H 2m,2n+1

h = 2: H 2m+1,2n

h = 3: H 2m+1,2n+1

where

m = 0,1,2,...,32;

n = 0,1,2,3,4.

As a result, the main unit is divided into four divided blocks. Each divided block is consists of 33 vertical macro blocks x 45 horizontal macro blocks.

5.1.3.2.3 720/60p system

The macro blocks in each video frame are divided into halfway blocks as shown in Figure 25. Each halfway block H consists of six macro blocks horizontally and one macro block vertically.

Halfway blocks H are distributed into divided blocks as follows.

Divided blocks:

h = 0: H m, 2n

h = 1: H m, 2n+1

h = 2: H m+45, 2n

h = 3: H m+45, 2n+1

where

m = 0,1,2,...,44;

n = 0,1,2,3,4.

As a result, each two video frames are divided into four divided blocks. Each divided block consists of 45 vertical macro blocks × 30 horizontal macro blocks.

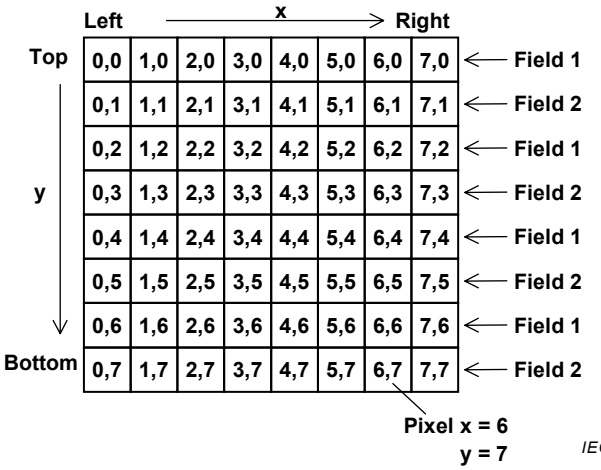


Figure 13 – DCT block and the pixel coordinates for the 1080-line system

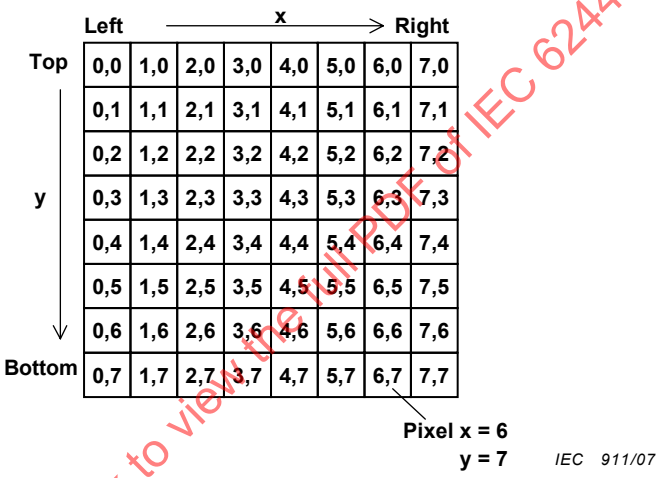


Figure 14 – DCT block and the pixel coordinates for the 720-line system

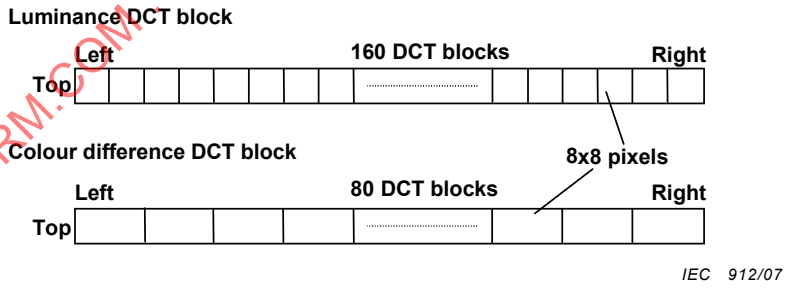


Figure 15 – DCT block arrangement for the 1080/60i system

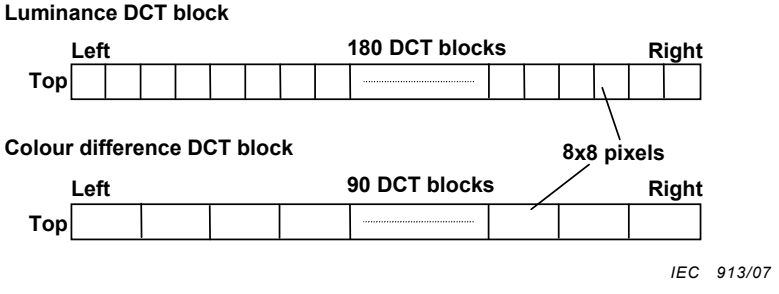


Figure 16 – DCT block arrangement for the 1080/50i system

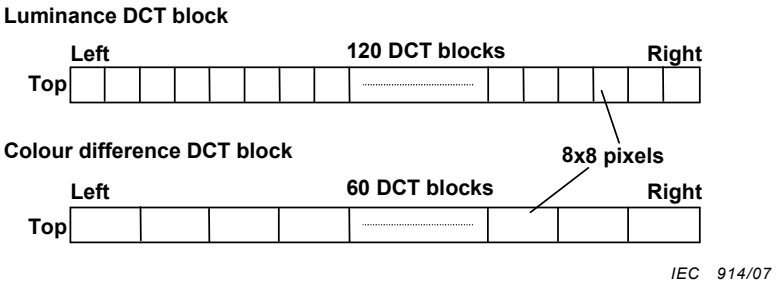


Figure 17 – DCT block arrangement for the 720/60p system

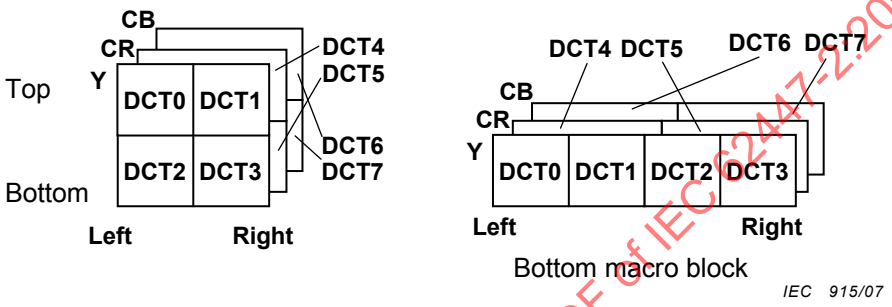


Figure 18 – Macro block and DCT blocks for the 1080-line system

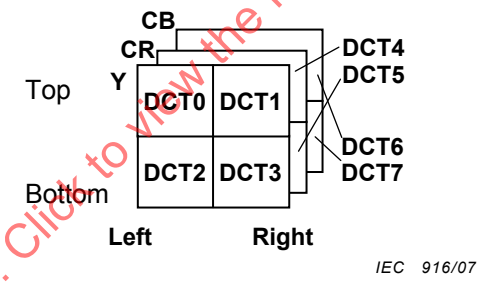


Figure 19 – Macro block and DCT blocks for the 720-line system

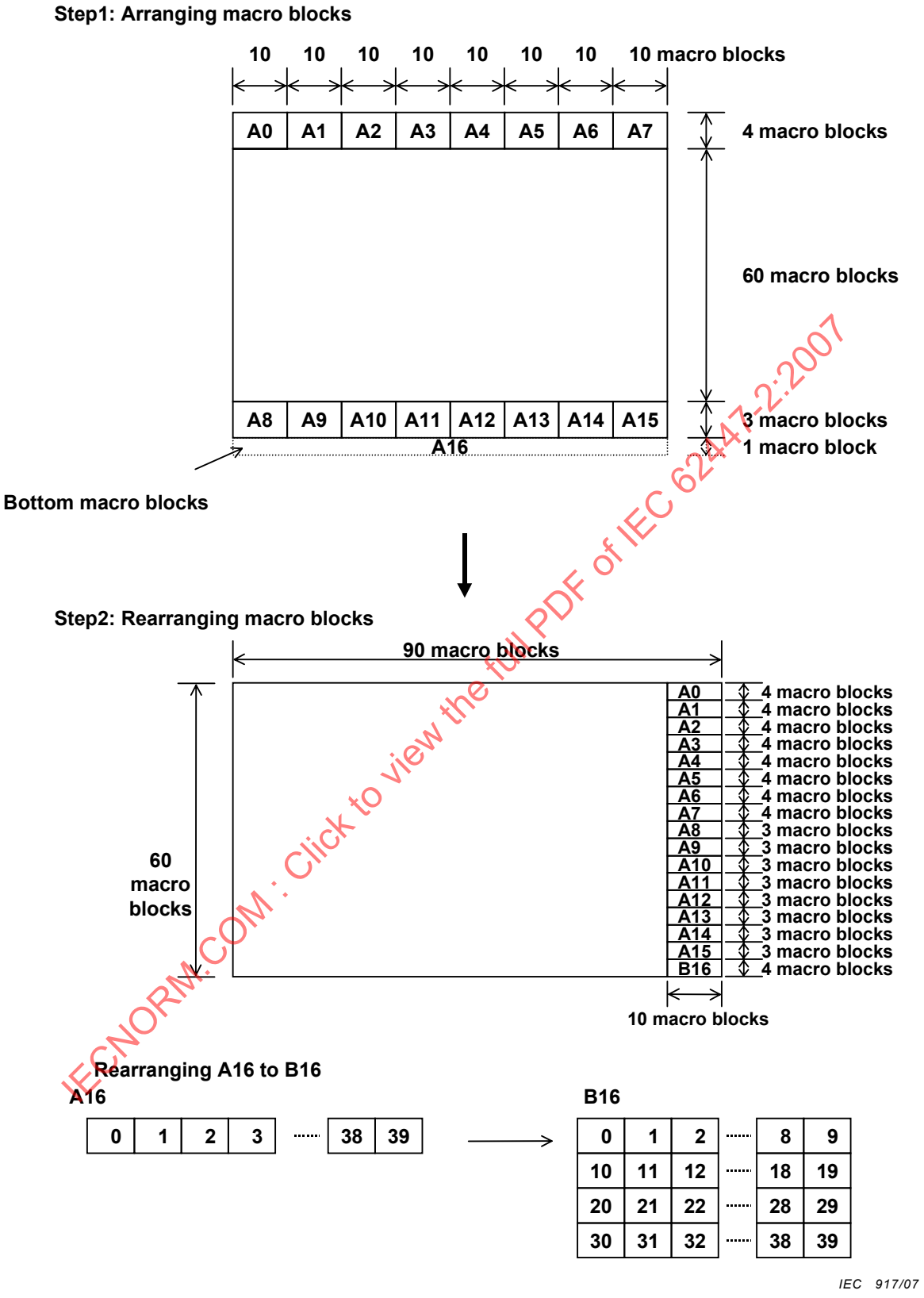


Figure 20 – Arrangement of macro blocks for the 1080/60i system

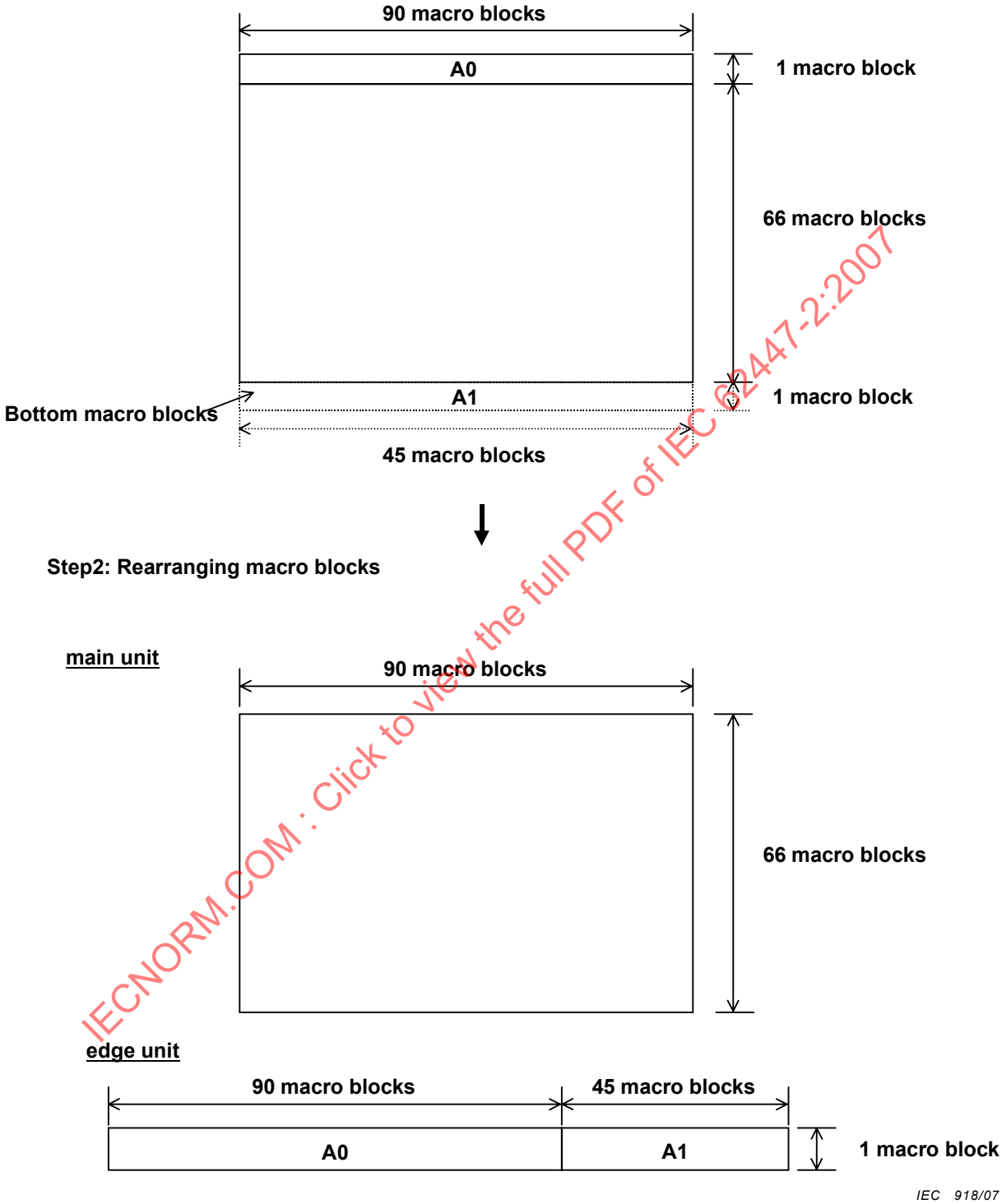


Figure 21 – Arrangement of macro blocks for the 1080/50i system

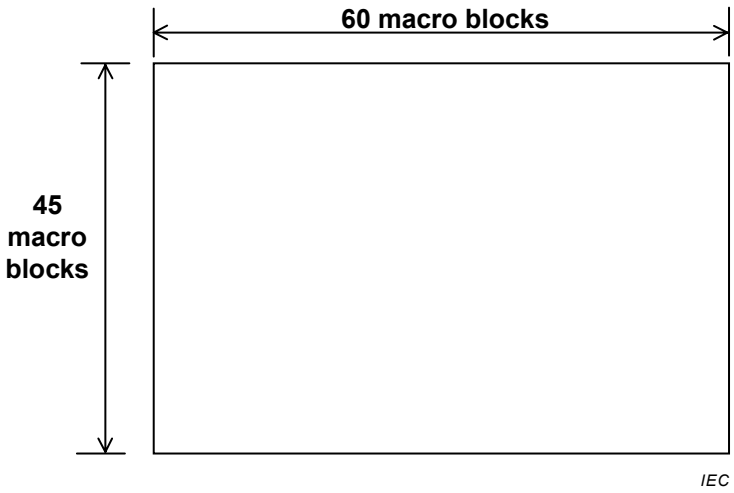


Figure 22 – Arrangement of macro blocks for the 720/60p system

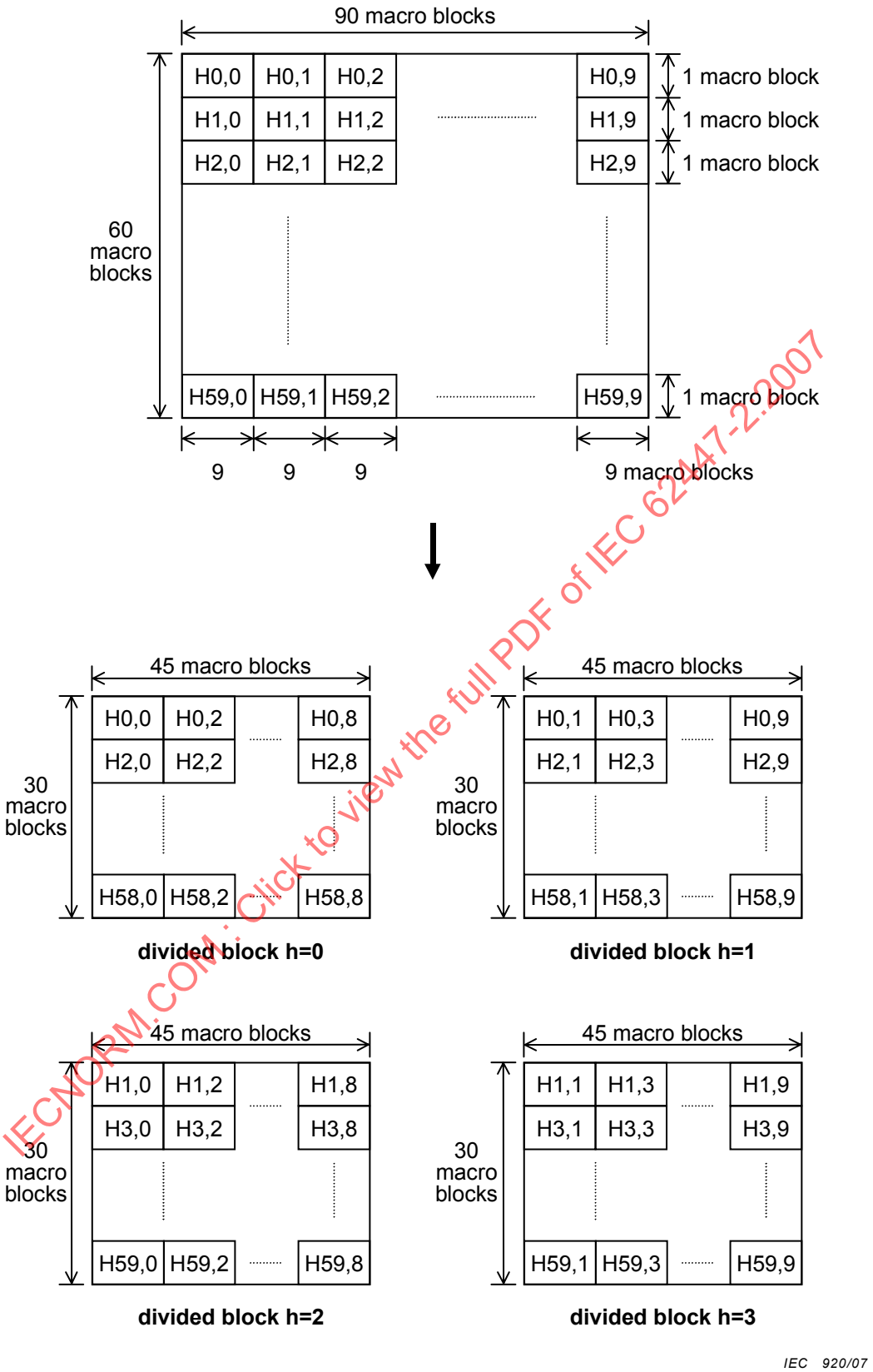


Figure 23 – Divided blocks for the 1080/60i system

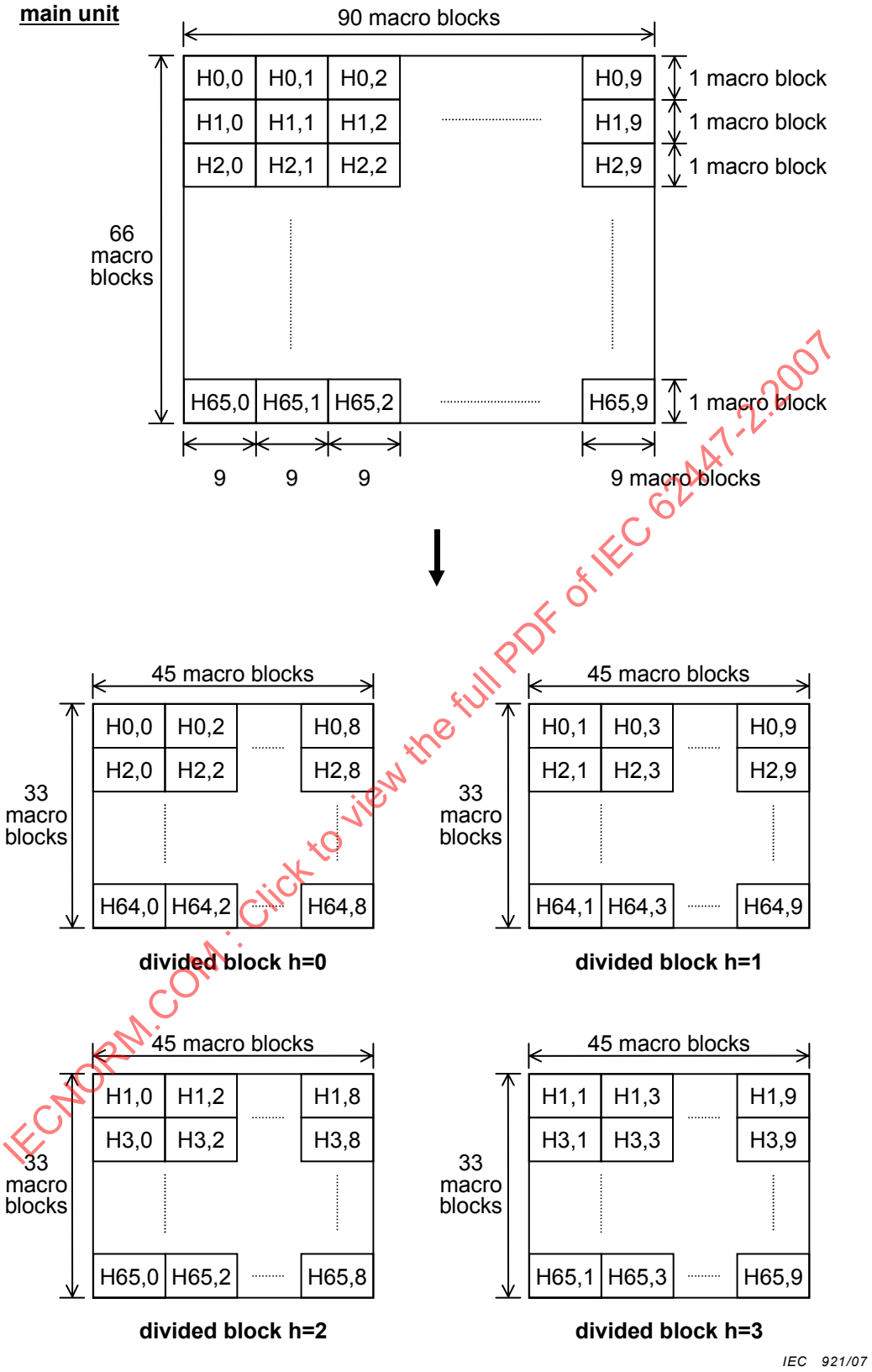


Figure 24 – Divided blocks for the 1080/50i system

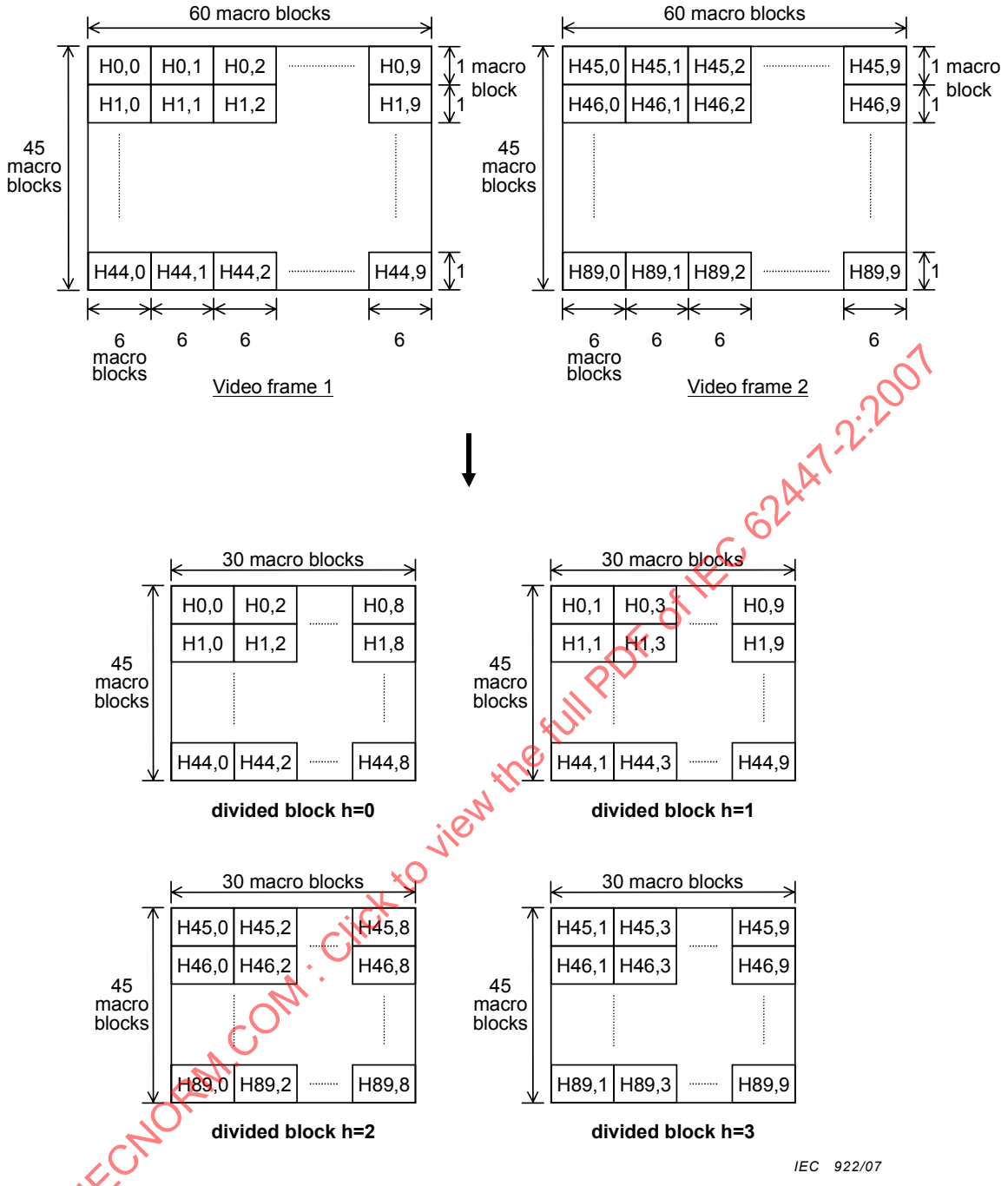


Figure 25 – Divided blocks for the 720/60p system

5.1.4 Super block

Each super block consists of 27 macro blocks.

5.1.4.1 1080/60i system

The arrangement of super blocks in a divided block is shown in Figure 26. The pixels in a divided block are divided into 50 super blocks.

10 vertical super blocks × 5 horizontal super blocks = 50 super blocks.

5.1.4.2 1080/50i system

The arrangement of super blocks in a divided block is shown in Figure 28. The pixels in a divided block are divided into 55 super blocks.

11 vertical super blocks × 5 horizontal super blocks = 55 super blocks.

The pixels in the edge unit are divided into 5 super blocks.

1 vertical super blocks × 5 horizontal super blocks = 5 super blocks.

5.1.4.3 720/60p system

The arrangement of super blocks in a divided block is shown in Figure 30. The pixels in a divided block are divided into 50 super blocks.

10 vertical super blocks × 5 horizontal super blocks = 50 super blocks.

5.1.5 Definition of super block number, macro block number and value of the pixel

5.1.5.1 Super block number

The super block number is expressed as S h,i,j shown in Figures 26, 28, and 30.

S h,i,j

where

h is the divided block	h = 0, …, 3;	
I is the vertical order of the super block	i = 0, …, 9	for 60 Hz system;
	i = 0, …,11	for 50 Hz system;
j is the horizontal order of the super block	j = 0, …, 4.	

5.1.5.2 Macro block number

The macro block number is expressed as M h,i,j,k. The symbol k is the macro block order in the super block shown in Figure 27 for the 1080/60i system, Figure 29 for the 1080/50i system, and Figure 31 for the 720/60p system. The small rectangle in these figures shows a macro block, and a number in the small rectangle expresses k.

M h,i,j,k

where

h,i, j are the super block numbers;

k is the macro block order in the super block k = 0, …,26.

5.1.5.3 Pixel location

The pixel location is expressed as P h,i,j,k,l(x,y). The pixel is indicated as the suffix of h, i, j, k, l (x, y). The symbol l is the DCT block order in a macro block shown in Figures 18 and 19. The rectangle in the figure shows a DCT block, and a DCT number in the rectangle expresses l. The symbol x and y are the pixel coordinates in the DCT block as described in 4.1.2.

P h,i,j,k,l(x,y)

where

h,i, j, k are the macro block numbers;

l is the DCT block order in the macro block;

(x, y) are the pixel coordinates in the DCT block x = 0, …, 7;

y = 0, …, 7.

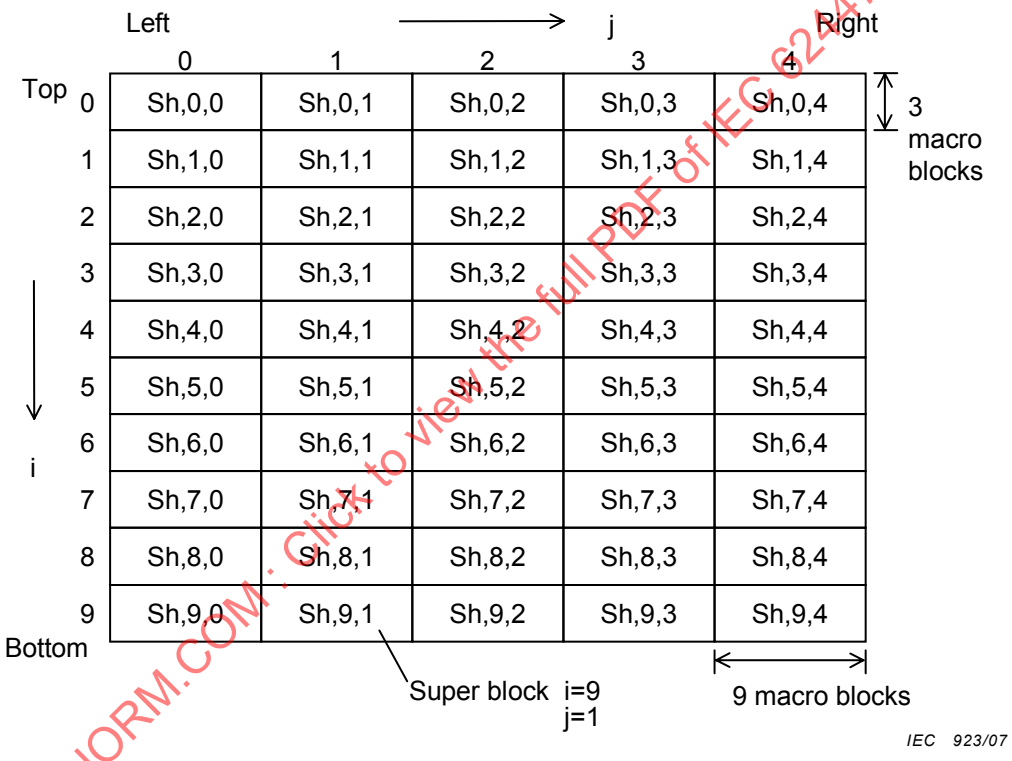


Figure 26 – Super blocks and macro blocks in a divided block for the 1080/60i system

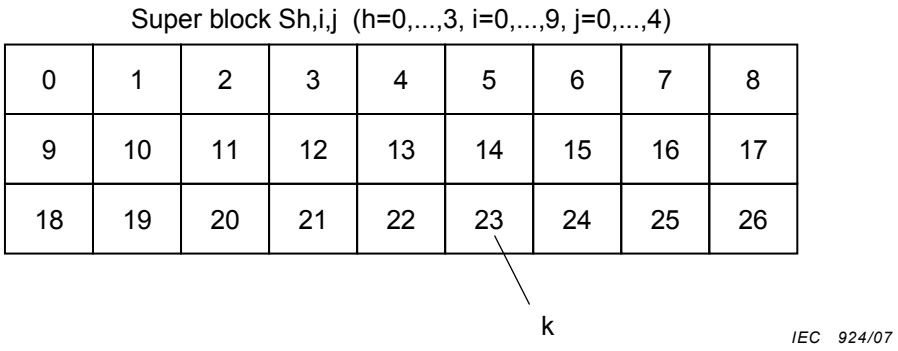


Figure 27 – Macro block order in a super block for the 1080/60i system

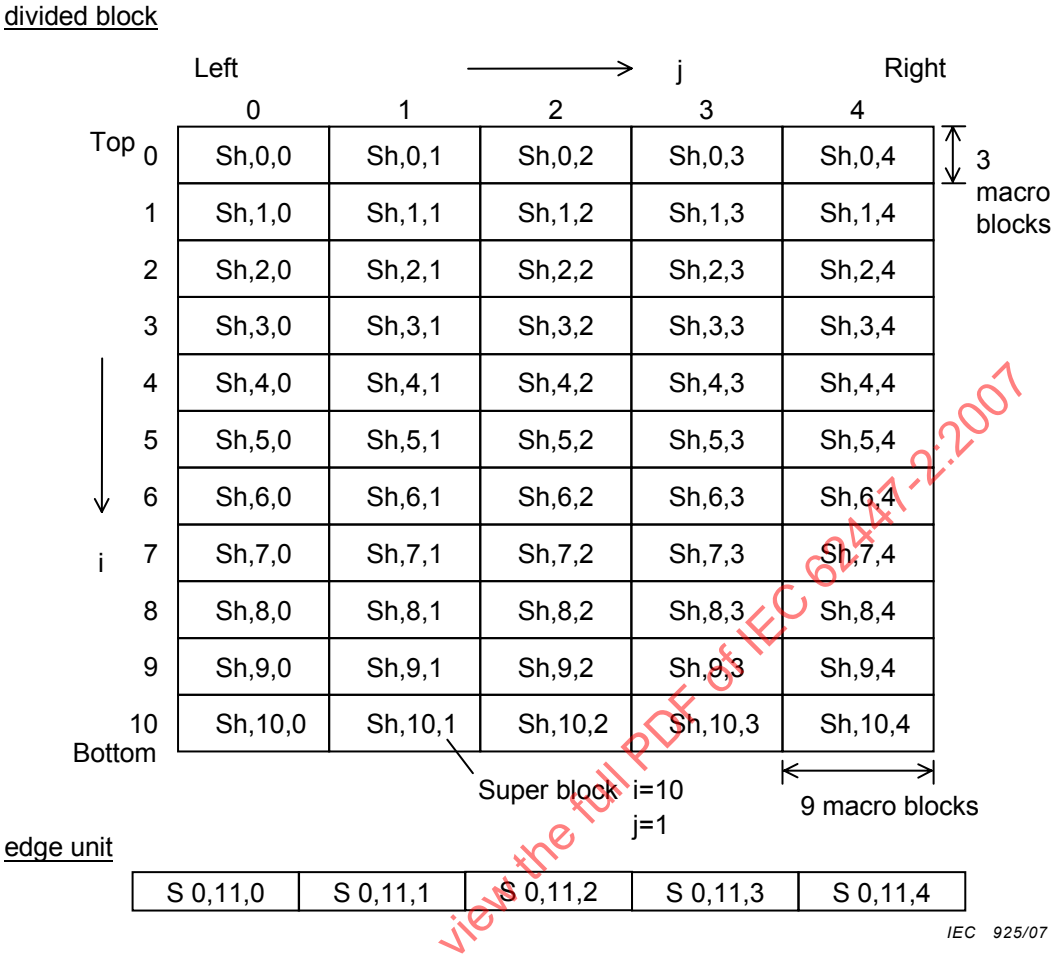


Figure 28 – Super blocks and macro blocks for the 1080/50i system

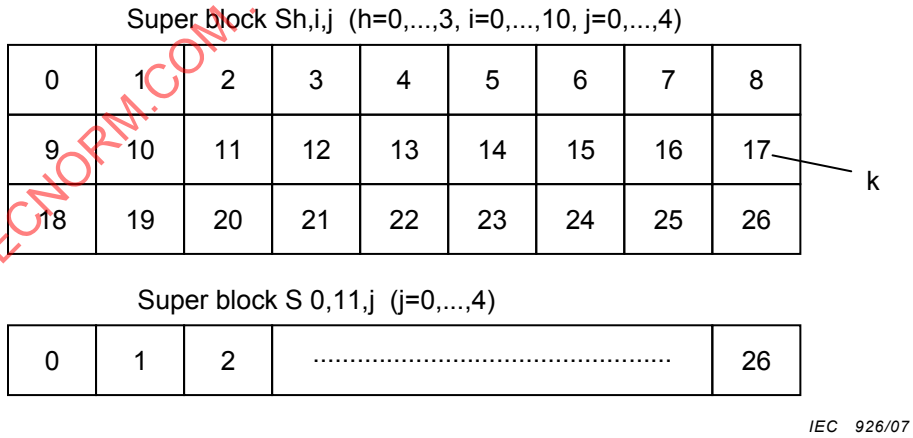


Figure 29 – Macro block order in a super block for the 1080/50i system

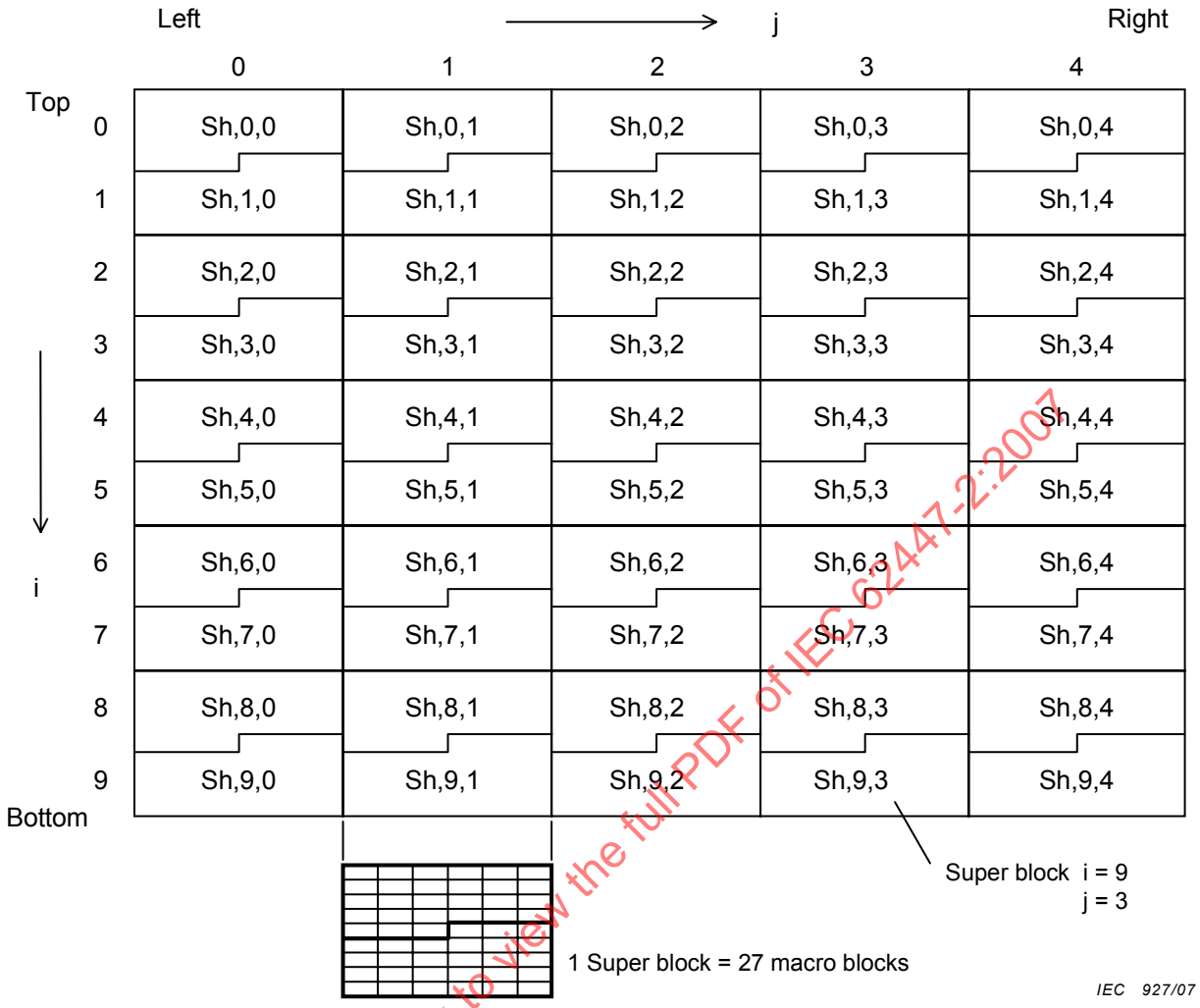


Figure 30 – Super blocks and macro blocks in a divided block for the 720/60p system

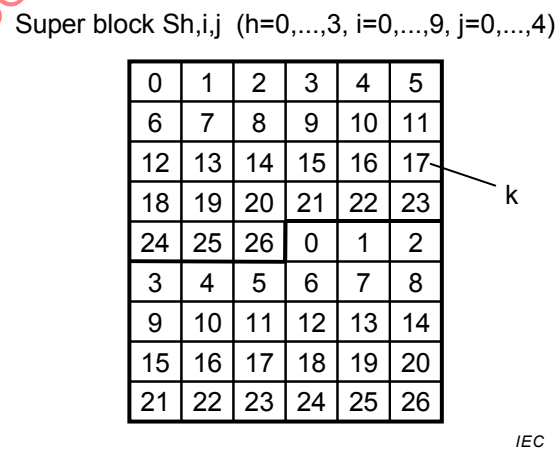


Figure 31 – Macro block order in a super block for the 720/60p system

5.1.6 Definition of video segment and compressed macro block

A video segment consists of five macro blocks which are assembled from various areas within the video frame.

a) 60 Hz system

M h,a,p,k where a = (i + 2) mod 10, p = 2
M h,b,q,k where b = (i + 6) mod 10, q = 1
M h,c,r,k where c = (i + 8) mod 10, r = 3
M h,d,s,k where d = (i + 0) mod 10, s = 0
M h,e,t,k where e = (i + 4) mod 10, t = 4

where

h is the divided block h = 0, …, 3;
i is the vertical order of the super block i = 0, …, 9;
k is the macro block order in the super block k = 0, …, 26.

b) 50 Hz system

1) divided block

M h,a,p,k where a = (i + 2) mod 11, p = 2
M h,b,q,k where b = (i + 6) mod 11, q = 1
M h,c,r,k where c = (i + 8) mod 11, r = 3
M h,d,s,k where d = (i + 0) mod 11, s = 0
M h,e,t,k where e = (i + 4) mod 11, t = 4

where

h is the divided block h = 0, …, 3;
i is the vertical order of the super block i = 0, …, 10;
k is the macro block order in the super block k = 0, …, 26

2) edge unit

M h,a,p,k where h = 0, a = 11, p = 0
M h,b,q,k where h = 0, b = 11, q = 1
M h,c,r,k where h = 0, c = 11, r = 2
M h,d,s,k where h = 0, d = 11, s = 3
M h,e,t,k where h = 0, e = 11, t = 4

where

k is the macro block order in the super block k = 0, …, 26.

Each video segment before the bit rate reduction is expressed as V h,i,k which consists of M h,a,p,k; M h,b,q,k; M h,c,r,k; M h,d,s,k; and M h,e,t,k.

The bit-rate reduction process is operated sequentially from M h,a,p,k to M h,e,t,k. The data in a video segment are compressed and transformed to a 385-byte data stream. A set of compressed video data consists of five compressed macro blocks. Each compressed macro block consists of 77 bytes and is expressed as CM. Each video segment after the bit-rate reduction is expressed as CV h,i,k which consists of CM h,a,p,k; CM h,b,q,k; CM h,c,r,k; CM h,d,s,k; and CM h,e,t,k as shown below:

CM h,a,p,k:

This block includes all parts or most parts of the compressed data from macro block M h,a,p,k and may include the compressed data of macro block M h,b,q,k; or M h,c,r,k; or M h,d,s,k; or M h,e,t,k.

CM h,b,q,k:

This block includes all parts or most parts of the compressed data from macro block M h,b,q,k and may include the compressed data of macro block M h,a,p,k; or M h,c,r,k; or M h,d,s,k; or M h,e,t,k.

CM h,c,r,k:

This block includes all parts or most parts of the compressed data from macro block M h,c,r,k and may include the compressed data of macro block M h,a,p,k; or M h,b,q,k; or M h,d,s,k; or M h,e,t,k.

CM h,d,s,k:

This block includes all parts or most parts of the compressed data from macro block M h,d,s,k and may include the compressed data of macro block M h,a,p,k; or M h,b,q,k; or M h,c,r,k; or M h,e,t,k.

CM h,e,t,k:

This block includes all parts or most parts of the compressed data from macro block M h,e,t,k and may include the compressed data of macro block M h,a,p,k; or M h,b,q,k; or M h,c,r,k; or M h,d,s,k.

5.2 DCT processing

Four rows of eight horizontal pixels from each field of a video frame form a DCT block in the 1080-line system. Eight rows of eight horizontal pixels from a video frame form a DCT block in the 720-line system.

The DCT transformation from 64 pixels in a DCT block whose numbers are h, i, j, k, l (x, y) to 64 coefficients whose numbers are h, i, j, k, l (u, v) is described as follows.

P h,i,j,k,l(x,y) is the value of the pixel and C h,i,j,k,l(u,v) is the value of the coefficient.

For u = 0 and v = 0, the coefficient is called the DC coefficient.

All other coefficients are called AC coefficients.

5.2.1 DCT mode

For the 1080-line system, two DCT modes are used for the purpose of improving the quality of the picture after bit-rate reduction. These modes are called the 8-8-frame-DCT mode and the 8-8-field-DCT mode.

The 8-8-frame-DCT mode should be selected when the difference between two fields in a video frame is small. The 8-8-field-DCT mode should be selected when the difference between two fields in a video frame is large.

For the 720-line system, the 8-8-frame-DCT mode should be selected.

The same DCT mode is applied to the DCT blocks in a macro block.

As shown in Figure 32, if the 8-8-field-DCT mode is selected, pixels in the two vertical adjacent DCT blocks are rearranged to form re-arranged DCT blocks that contain pixels from the same field.

The following DCT paragraph shows the algorithm that is applied to both DCT modes, the 8-8-frame-DCT and the 8-8-field-DCT modes.

DCT:

$$C\,h,i,j,k,l(u,v) = C(v)\,C(u) \sum_{y=0}^{7} \sum_{x=0}^{7} (P\,h,i,j,k,l(x,y)\,\mathrm{COS}(\pi v(2y+1)/16)\,\mathrm{COS}(\pi u(2x+1)/16))$$

Inverse DCT:

$$P\,h,i,j,k,l(x,y) = \sum_{v=0}^{7} \sum_{u=0}^{7} (C(v)\,C(u)\,C\,h,i,j,k,l(u,v)\,\mathrm{COS}(\pi v(2y+1)/16)\,\mathrm{COS}(\pi u(2x+1)/16))$$

where

$C(u) = 0{,}5/\sqrt{2}$ for u = 0;

C(u) = 0,5 for u = 1 to 7;

$C(v) = 0{,}5/\sqrt{2}$ for v = 0;

C(v) = 0,5 for v = 1 to 7.

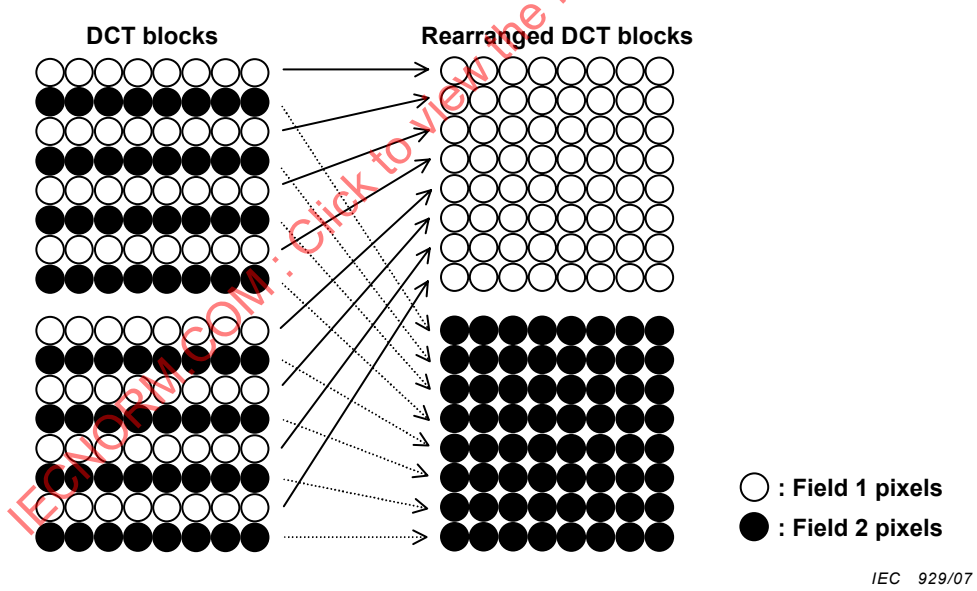


Figure 32 – Rearrangement of pixels in the 8-8-field-DCT mode

5.2.2 Weighting

The DCT coefficients C h,i,j,k,l(u,v) shall be weighted by quantizer matrix. Different quantizer matrices can be set for luminance signals and colour-difference signals as shown in Figure 33 for the 1080/60i system, Figure 34 for the 1080/50i system, and Figure 35 for the 720/60p system.

5.2.3 Output order

Figure 36 shows the output order of the weighted coefficients.

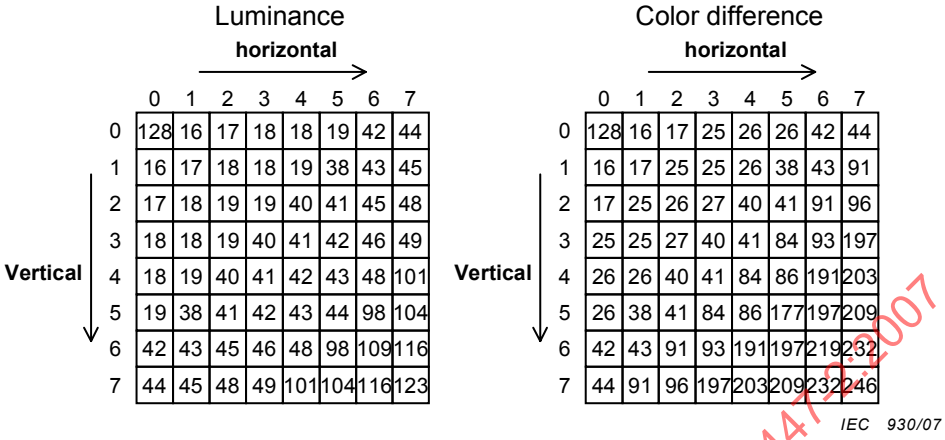


Figure 33 – Quantizer matrix for the 1080/60i system

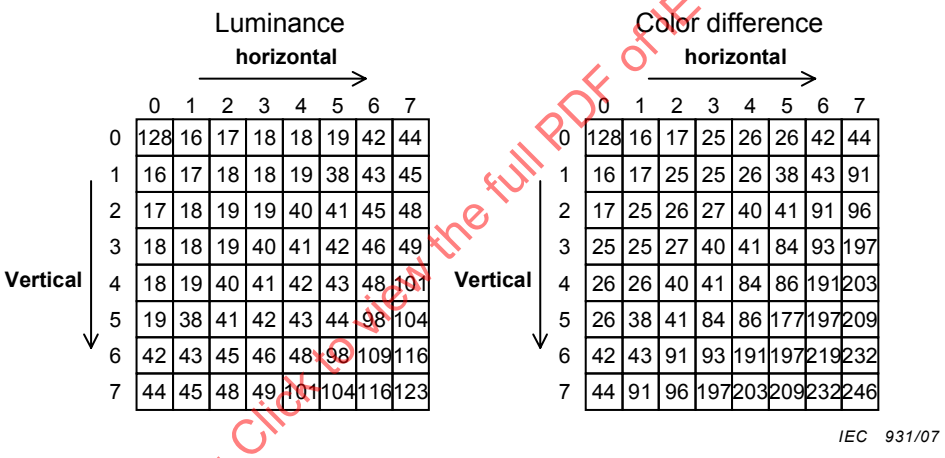


Figure 34 – Quantizer matrix for the 1080/50i system

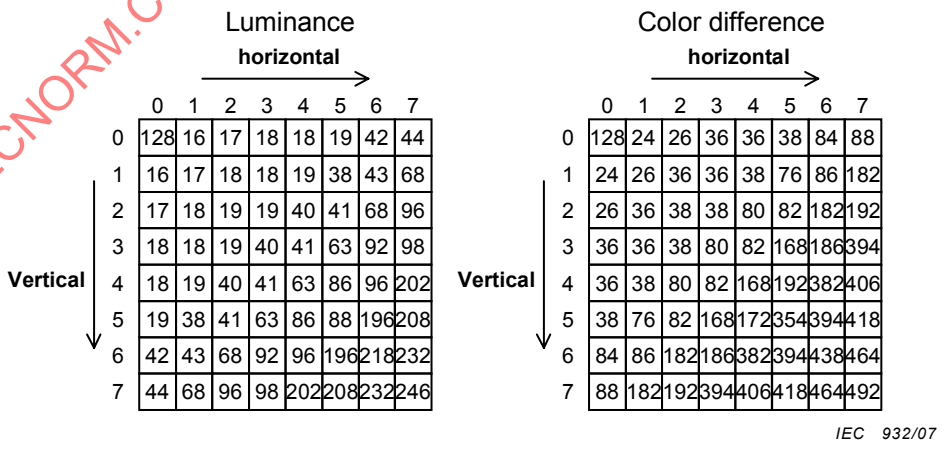


Figure 35 – Quantizer matrix for the 720/60p system

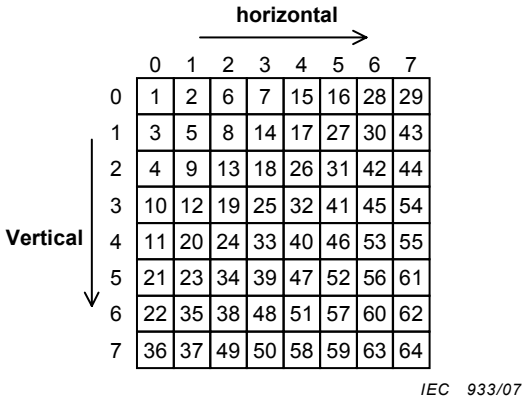


Figure 36 – The output order of a weighted DCT block

5.3 Quantization

5.3.1 Introduction

Weighted DCT coefficients are divided by quantization steps in order to limit the amount of data in one video segment to five compressed macro blocks and transformed 9 bits.

5.3.2 Bit assignment for quantization

Weighted DCT coefficients are represented as follows:

DC coefficient value (9 bits): b8 b7 b6 b5 b4 b3 b2 b1 b0
twos complement (–255 to 255)

AC coefficient value (12 bits): s b10 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0
1 sign bit + 11 bits of absolute value (-2 047 to 2 047)

5.3.3 Quantization step

The quantization step (Q-step) is selected in order to limit the amount of data in each five compressed macro blocks which are generated from a single video segment. The Q-step shall be decided by the quantization number (QNO) and class number as specified in Table 25. The QNO shall be applied to every macro block. The class number shall be applied to every DCT block.

Data reduction consists of two procedures. First, the AC coefficient is divided by the Q-step. If the bit length of the quantized AC coefficient obtained is more than 9, then the second procedure is performed. In the second procedure, the AC coefficient is divided again by a larger Q-step according to increasing class numbers in order to make the bit length of the quantized AC coefficient 9 or less.