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2005-08

Semiconductor die products –

Part 1:
Requirements for procurement and use

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International Electrotechnical Commission, 3, rue de Varembé, PO Box 131, CH-1211 Geneva 20, Switzerland
Telephone: +41 22 919 02 11 Telefax: +41 22 919 03 00 E-mail: inmail@iec.ch Web: www.iec.ch

Commission Electrotechnique Internationale
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CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DIE PRODUCTS –

Part 1: Requirements for procurement and use

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 62258-1 has been prepared by IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47/1820/FDIS	47/1832/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

IEC 62258, as currently conceived, consists of the following parts, under the general title *Semiconductor die products:*

Part 1: Requirements for procurement and use

Part 2: Exchange data formats [1]

Part 3: Recommendations for good practice in handling, packing and storage (Technical Report) [1]

Part 4: Questionnaire for die users and suppliers (Technical Report) [2]

Part 5: Requirements for information concerning electrical simulation [2]

Part 6: Requirements for information concerning thermal simulation [2]

Further parts may be added as required.

A bilingual version of this publication may be issued at a later date.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

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1 To be published.

2 In preparation.

INTRODUCTION

This International Standard is based on the work carried out in the ESPRIT 4th Framework project GOOD-DIE which resulted in the publication of the ES59008 series of European specifications. Organizations that helped prepare this standard include the ESPRIT GOOD-DIE project, The Die Products Consortium, JEITA, JEDEC and ZVEI.

SEMICONDUCTOR DIE PRODUCTS –

Part 1: Requirements for procurement and use

1 Scope

This part of IEC 62258 has been developed to facilitate the production, supply and use of semiconductor die products, including

– wafers,
– singulated bare die,
– die and wafers with attached connection structures,
– minimally or partially encapsulated die and wafers.

This standard defines the minimum requirements for the data which are needed to describe such die products and is intended as an aid in the design of and procurement of assemblies incorporating die products. It covers the requirements for data, including

– product identity,
– product data,
– die mechanical information,
– test, quality, assembly and reliability information,
– handling, shipping and storage information.

This standard covers the specific requirements for data needed to describe the geometrical properties of die, their physical properties and the means of connection necessary for their use in the development and manufacture of products. It also contains, in Annexes A and B, terminology and a list of common acronyms, respectively.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60191-4:1999, *Mechanical standardization of semiconductor devices – Part 4: Coding system and classification into forms of package outlines for semiconductor device packages*
Amendment 1 (2001)
Amendment 2 (2002)

IEC 61360-1:2002, *Standard data element types with associated classification scheme for electric components – Part 1: Definitions – Principles and methods*

IEC 62258-2, *Semiconductor die products – Part 2: Exchange data formats* [3]

ISO 14644-1:1999, *Cleanrooms and associated controlled environments – Part 1: Classification of air cleanliness*

3 To be published.

3 Terms and definitions

For the purposes of this document, the following terms apply.

NOTE 1 All terms defined here are in addition to relevant terms defined in IEC 60050: International Electrotechnical Vocabulary.

NOTE 2 Additional terms and acronyms are given for information in Annexes A and B.

3.1 Basic definitions

3.1.1
die (singular or plural)
separated piece(s) of semiconductor wafer that constitute(s) a discrete semiconductor or whole integrated circuit

3.1.2
wafer
slice or flat disc, either of semiconductor material or of such a material deposited on a substrate, in which devices or circuits are simultaneously processed and which may be subsequently separated into die

3.1.3
singulated die
individual and distinct die which have been separated from the wafer

3.1.4
bare die
unpackaged discrete semiconductor or integrated circuit with pads on the upper surface suitable for interconnection to the substrate or package

3.1.5
bare die with connection structures
unpackaged die that have had added bumps, lead frames or other terminations to interconnect for electrical attachment

NOTE Typically these can be die that have had solder or other metallic bumps added to the metallized pads on the die in the form of peripheral bumps or arrays (also known as flip-chip) or die that have had fine leads attached to the metallized pads on the die known as TAB.

3.1.6
minimally packaged die
MPD
die that have had some exterior packaging medium and interconnection structure added for protection and ease of handling

NOTE This definition includes such packaging technologies as chip scale packages (CSP) in which the area of the package is not significantly greater than the area of the bare die.

3.1.7
die device
bare die, with or without connection structures, or a minimally packaged die

3.2 General terminology

3.2.1
chip
common parlance for die

3.2.2
chip scale package
chip size package
CSP
generic term for packaging technologies that result in a packaged part that is only marginally larger than the internal die

3.2.3
discrete (semiconductor)
single two-, three- or four-terminal semiconductor device

NOTE Discrete semiconductors include such devices as individual diodes, transistors and thyristors.

3.2.4
hybrid (circuit)
module or encapsulated sub-assembly that comprises semiconductor die and printed or otherwise attached passive components

NOTE Also see multi-chip module and multi-chip package.

3.2.5
known good die
KGD
qualification of a semiconductor die which indicates that the die has been tested to a specified or determined level of quality or "goodness"

NOTE A commonly accepted definition of KGD is a die that has been tested and/or screened to quality levels that are of the same order as those applicable to the equivalent packaged parts.

3.2.6
package
total assembly which protects one or more electronic components from mechanical, environmental and electrical damage throughout its operational life and which provides means of interconnection

3.2.7
packaging
process of assembling one or more electronic components into a package

NOTE The use of "packaging" as a participle (e.g. "When packaging ICs into dual-in-line packages …") is deprecated.

3.2.8
packing
material which is used to protect electronic items from mechanical, environmental and electrical damage during transportation or storage and which is discarded prior to the incorporation of the item into its end application

3.2.9
multi-chip module
MCM
module that contains two or more die and/or minimally packaged die

NOTE Also see hybrid and multi-chip package.

3.2.10
multi-chip package
MCP
package that contains two or more die and/or minimally packaged die

NOTE Also see hybrid and multi-chip module.

3.2.11
system in a package
SiP
multi-chip package (MCP) that performs a complete system function

3.2.12
multi-device sub-assembly
MDS
sub-system which consists of multiple electronic devices including at least one integrated circuit

NOTE This is a generic term which includes, amongst others, hybrid, MCM, MCP and SiP.

3.2.13
pad
conducting feature on a die device forming a terminal to which external electrical connections are made

NOTE For bare die without external connections, the pad acts as the terminal itself. For bumped die the terminal is in the form of additional conducting material placed on a pad, whilst for die with attached lead frame the terminal is in the form of a conductor connected to the pad and extending from the die.

3.3 Semiconductor manufacturing and interconnection terminology

3.3.1
mask
a) optical overlay used in photo-etching during the process of semiconductor fabrication

b) general term to refer to the major individual patterning stages that are used within the fabrication process

3.3.2
layer
loose topological term used in describing the process of semiconductor fabrication

NOTE A layer consists of a specific material and a semiconductor device consists of many layers.

3.3.3
passivation
top or final processing and covering on a die, usually of semiconductor oxide or nitride, that protects and seals the active areas of the die from further external chemical or mechanical contamination

NOTE Bond pads require an opening in this passivation to allow electrical contact.

3.3.4
scribe line
scribe lane
area surrounding the die that is set aside on the wafer for the purposes of scribing and sawing the die from the wafer

NOTE This feature may be covered by many other terms such as scribe street, saw lane, dicing lane, etc.

3.3.5
die separation
dicing
sawing
means by which individual die are cut from the wafer

NOTE Die separation is commonly performed by using a fine circular saw.

3.3.6
wire bonding
process of attaching interconnection wire or ribbon to a die

3.3.7
bond pads
metallized areas on the die that are used for temporary or permanent electrical connection (bonding)

3.3.8
bumps
raised metallized areas on the die that are used for temporary or permanent electrical connection

3.3.9
lead frame
supporting structure upon which a die is mounted and which also includes the connection structure to which the die is bonded

3.3.10
die attach
method and materials used to attach a die to a substrate

3.3.11
flip-chip
semiconductor die which is electrically and/or mechanically connected to an interconnection structure in such a way that the active area faces the interconnection structure

3.3.12
interposer
material placed between two surfaces giving electrical insulation, mechanical strength and/or controlled mechanical separation between the two surfaces

NOTE An interposer may be used as a means for redistributing electrical connections and/or allowing for different thermal expansions between adjacent surfaces.

3.3.13
redistribution
process of moving terminals on die to more convenient positions by additional connectivity layers or by the use of an interposer

4 General requirements

4.1 General

Suppliers of die devices shall furnish information which is necessary and sufficient for users of the devices at all stages of design, procurement, manufacture and test of products containing them. Details of the requirements are given below and in other parts of this standard. The form in which the information may be supplied is covered in IEC 62258-2.

Whilst it is expected that much of the information supplied in conformance with this standard will be in the public domain and available from sources such as manufacturers' data sheets, this specification does not place an obligation on a supplier to make information public. Any information that a supplier considers to be proprietary or commercially sensitive may be supplied under the terms of a non-disclosure agreement.

For further details of requirements, refer to Clauses 6, 7, 8, 9, 10 and 11.

4.2 Identity

All die devices shall have an identifier, consisting of one or more type designators, which shall distinguish each die device from all other die devices and from equivalent packaged parts. Such identifiers shall ensure the ability to distinguish among different versions of die which are intended to perform the same or different functions.

4.3 Source

The source of supply for die devices shall be given with sufficient information for the customer to communicate adequately with the supplier. If the die manufacturer is different from the supplier, the identity of the manufacturer shall also be given.

4.4 Function

A description of the electrical function and performance variants of all die devices shall be given.

4.5 Electrical and physical characteristics

Electrical characteristics covering limiting conditions of use and normal operating conditions shall be given for all die devices. Technology of manufacture, including the materials used, shall be given where necessary.

4.6 Geometry

All physical dimensions needed for layout and assembly of a product containing die devices shall be given. These shall include dimensions of the die and the size, shape and position of all terminals.

4.7 Connectivity

The electrical function of all terminals shall be given in such a way that the relationships between electrical function and geometric position of the terminals are fully defined. Any requirement for connection to the die substrate shall also be given.

4.8 Documentation

Data sheets containing all the information prescribed herein shall be provided. These may be supplied as hard copy or in electronic form.

4.9 Test and quality

An indication of the expected quality level and information on device reliability shall be given.

4.10 Handling

Information necessary for handling of the die shall be provided, including, as appropriate, details of the form in which the die are supplied and of the form of packing for shipment and recommendations for ESD protection.

4.11 Assembly

Information and recommendations for assembly of the die shall be provided.

4.12 Thermal data

Thermal properties needed for thermal modelling of the die device shall be given.

4.13 Models

The availability of any models for simulation or test of the die device shall be stated.

5 Data exchange

It is recommended that data intended for exchange by electronic means should be formatted in accordance with the provisions of IEC 62258-2 and IEC 61360-1.

6 Requirements for bare die with and without connection structures

6.1 Form of supply

The physical form in which the die or wafers are supplied shall be stated, whether as singulated die, sawn or unsawn wafers and with or without connection structures or minimal packaging.

6.2 Die name

The name given by the manufacturer to identify the die shall be the one used.

6.3 Die version

The revision or step code to identify the mask version or revision used in production of the die shall be given.

6.4 Manufacturer

The identity of the firm responsible for manufacture of the die or wafer shall be given.

6.5 Type number

The type number or device name given by the manufacturer to identify the finished die as supplied to the customer shall be given.

6.6 Function

A basic description of the electrical function performed by the device shall be provided.

6.7 Information source

The identity of the organization or individual responsible for creating the data set shall be given.

6.8 Data version

The version and/or date of creation of the data set shall be given.

6.9 Units of measurement

The units in which die and pad dimensions are given shall be stated. For data exchange using IEC 61360-1, all dimensions shall be given in metres.

6.10 Geometric view

A statement shall be made as to whether the die is viewed from the top (active side upwards) or bottom (active side downwards). The preferred view is from the top.

6.11 Die size

The maximum length and width of the die shall be given:

a) for bare die these are the maximum dimensions after sawing;

NOTE If these are not available, the step-and-repeat dimensions shall be given.

b) for wafers these are the step-and-repeat dimensions.

6.12 Die thickness

The maximum thickness of the finished die shall be given.

6.13 Geometric origin

The coordinates of a reference position on the die with respect to the geometric centre of the die surface shall be given. This forms the origin of the coordinate system with respect to which the position of die features, such as pad positions, are referenced.

6.14 Dimension tolerances

Tolerances for die size, die thickness, pad dimensions and pad positions should be given.

6.15 Pad count

The number of separate pads on the die shall be stated.

6.16 Pad information

For each pad on the die, the following information shall be given:

a) **position** – the coordinates of the geometric centre of the pad with respect to the geometric origin;

b) **shape** – the shape and associated dimensions of the pad at that position;

c) **orientation** – the orientation of the pad with respect to a reference direction on the die;

d) **signal name** – the name of the signal or supply connection made to the pad.

6.17 Signal type

The type of signal, power supply or other connection to each pad (input, output, supply voltage, no connect, etc.) shall be stated.

6.18 Technology

The technology of manufacture of the semiconductor device, for example CMOS, BiCMOS, bipolar etc., shall be stated

6.19 Semiconductor material

The type of active semiconductor material used in fabricating the die should be stated.

6.20 Substrate material

Where the die is fabricated using a different material as substrate to support the active semiconductor material, the type of this material should be stated.

6.21 Substrate connection

Any requirements for connection to the substrate of the die to ensure that the material is correctly biased shall be given and it shall be made clear whether a substrate connection is obligatory, optional or forbidden.

6.22 Passivation material

The material used in the final passivation layer on the surface of the die for protection and insulation should be stated.

6.23 Pad metallization

The material used for the metallization on the die over that part of the surface which includes the bonding pads should be stated.

6.24 Backside finish

For a die intended for wire bonding, details of any surface finish and plating applied to a die on the surface where it is attached to the mounting surface shall be given.

6.25 Wafer size

If the die are supplied in wafer form, the diameter of the wafer shall be given.

6.26 Wafer thickness

If the die are supplied in wafer form, the thickness of the wafer shall be given.

6.27 Wafer map

If the die are supplied in the form of a tested wafer, information shall be supplied to enable the user to identify individual good and reject die devices or grades of device.

6.28 Power dissipation

Either the power dissipation within the die or the operating supply current at nominal operating voltage under stated normal operating conditions shall be provided.

NOTE If figures for both typical and maximum power dissipation are available, both should be given.

6.29 Operating temperature

The range of operating temperatures of the die over which the device will operate according to its published specifications shall be given.

6.30 Packing

Information on the packing used to protect the die or wafers during handling, shipment and storage shall be given.

6.31 Supplier

The identity of the supplier of the die when this is different from the die manufacturer shall be stated.

6.32 Bump material

For bumped die, the material used in forming the bumps shall be stated.

6.33 Bump size

For bumped die, the height perpendicular to the die surface shall be given. In addition, shapes of the bumps and their dimensions parallel to the die surface should also be given.

6.34 Bump height tolerance

For bumped die, the tolerance on the height of the bumps should be given.

6.35 Connection material

For die with attached connection structures (other than bumped die), the material from which the connection structures are made should be stated.

6.36 Die picture

A drawing or photograph of the die which shows the relative positions of the pads, bumps or lead frame connections should be supplied.

NOTE Die pictures may be supplied as files in a suitable graphic format.

6.37 Die fiducials

Information should be given on identifying marks on the die that serve to assist in its differentiation from other die and in orientation for mounting.

7 Minimally packaged devices

7.1 General

The information described in the following subclauses is required in addition to any relevant information as defined in Clause 6. Where appropriate, reference should be made to standard package outline styles in IEC 60191-4 or in corresponding national standards.

7.2 Terminal position

Information shall be given which will allow the user to determine the position of all terminals on the device.

Where the terminals are not in a regular rectangular array, the information shall be in the form of a list of the coordinates of the geometric centres of all terminals with respect to the geometric origin.

Where information is not given in this form and where terminals are in a regular rectangular array, the information shall be given in such a form that there is sufficient information to deduce the geometric position of every terminal in the array:

a) terminal pitch – the distance between the centres of adjacent terminals. If the pitch is different for the length and width directions, both values shall be given;

b) terminal pattern – the pattern of occupied terminal positions shall be given either by an associated diagram or other representation.

7.3 Terminal size

The following information shall be given:

a) for ball- or column-grid arrays, the nominal diameter of the terminals;

b) for non-leaded packages, the dimensions of the effective footprint area on the mounting surface.

7.4 Number of terminals

The number of terminal positions and the number of actual terminals shall be given. Where terminals are disposed over a rectangular array, or along the edges of a rectangular package, the numbers of terminal positions in each of the length and width directions shall also be given.

7.5 Package size

The maximum length and width of the package shall be given.

7.6 Seated height

The maximum seated height of the packaged device when mounted shall be given.

7.7 Encapsulation material

The type of material used for the outer coating or encapsulation of the device shall be stated.

7.8 Terminal material

The type of material and/or finish used for the terminals shall be stated.

7.9 Package style code

The package style code in accordance with IEC 60191-4 shall be given.

8 Test, quality and reliability

8.1 General

Test, quality and reliability information, if deemed sensitive, may be subject to a non-disclosure agreement (NDA) between supplier and vendor.

8.2 Outgoing quality level

8.2.1 General

Information shall be given on the outgoing quality level of the die product. This may, for example, be expressed as defects per million (dpm), acceptable quality level (AQL) or other metric.

8.2.2 Outgoing quality level description

The manufacturer or supplier shall provide a description of the method, parameters and associated values used to calculate the outgoing quality level as stated in 8.2.1.

8.3 Electrical parameters specified

The manufacturer or supplier shall state the conditions for which the electrical parameters are specified, but it is the responsibility of the customer to review all data supplied for suitability within his module design requirements and end application.

8.4 Compliance to standards

The compliance of the die device to any specific standards shall be stated.

8.5 Additional device screening

The existence of additional screening specifically for die products, employed by the manufacturer or supplier, for the purposes of standards compliance, or for enhancing outgoing reliability, should be stated.

8.6 Reliability

8.6.1 General

A reliability estimate for the die product type shall be stated by the die supplier and the corresponding reliability value shall be supplied as a FIT rate, MTTF or other metric.

NOTE Final module reliability is a combination of the individual die type reliability, quantity of die in the module, substrate signal routing, thermal dissipation properties and many other variables. Any reliability data so provided by the manufacturer or supplier shall be treated for an individual die device type only, and only as "*as received*", not as "*as assembled*".

8.6.2 Reliability calculation

The die supplier shall state the method, parameters and data upon which the estimate of reliability is based.

8.7 Product status

The manufacturer shall make available, upon request, information stating the availability and status of the product, for instance, an impending electrical/mechanical change to the die device, such as a die shrink.

9 Requirements for handling and shipping

9.1 General

All shipping and handling methods shall provide a system for coding and maintaining traceability of each die to its wafer lot.

Information specified in this clause shall either be on the die device, primary or secondary packing, or on accompanying documentation including, where appropriate, invoices.

The user should be aware that, unless each die is uniquely identified, additional procedures and documentation will be required to maintain traceability once the die device has been removed from the primary packing.

All shipping methods shall provide protection from mechanical damage, electrostatic discharge (ESD) and contamination, whilst allowing recovery of die. If multiple units are shipped in the same package, means such as a waffle pack or a wafer boat shall be provided to prevent any intermingling that could cause physical damage.

Each shipping method should also provide a means to prevent excessive movement or rotation of product such as may cause damage to or prevent the automated handling of the product.

a) Customer part number

   The part number designated and required by the customer shall be stated where this is different from the type number or the manufacturer's part number.

b) Type number

   The type number or device name given by the manufacturer to identify the finished die as supplied to the customer shall be the one provided.

c) Supplier

The name of the supplier shall be stated.

d) Manufacturer

The name of the manufacturer, if different from the supplier, shall be stated.

e) Traceability

The supplier lot number, or any other information necessary to uniquely link the die device, or batch of devices, to the corresponding documentation from the wafer fabrication lot and/or test lot shall be stated.

f) Quantity

The total quantity of die in the shipment and the breakdown of quantities in each packing unit such as waffle pack, reel or wafer shall be stated. In the case of wafers, this quantity may be the number of good die on the wafer.

g) Form of supply

The physical form in which the die or wafers are supplied shall be stated.

h) Requirements for environmental protection

The supplier shall make a declaration that national or regional legal requirements have been met detailing appropriate measures taken to protect the environment.

NOTE Consideration should also be given to the recycling of packing materials, re-use of packing materials and the control of toxic materials.

9.2 Specific requirements for bare die or wafers - Die version

The revision or step code to identify the mask version shall be given.

9.3 Specific requirements for wafers - Product grading

Where die are provided in the form of a tested wafer, information shall be supplied to enable the user to identify good and reject die products, or grades of die products. This information may be supplied in the form of a wafer map showing the results from the test and uniquely identifying selected die on the wafer. A wafer map may be supplied in printed or electronic form. Alternatively, the wafer itself may be physically marked, for example by marking reject or secondary grade die using an ink dot, in which case a corresponding statement shall be made as to the meaning of the marks.

9.4 Special item requirements

9.4.1 General

If there are special requirements for unpacking and handling the product, appropriate labelling of primary and secondary packing shall provide warnings to persons handling the container.

9.4.2 Special protection requirements

A description of any unique materials or exposed surfaces that may require special protection during handling shall be given. For example, some die devices must not be touched on the top surface or some die devices must not be exposed to UV light.

9.4.3 Unencapsulated die warning label

When the primary package contains unencapsulated die or wafers, information shall be given to indicate that a container is to be opened in a controlled environment as classified by ISO 14644-1. This information shall be in the form of a warning label affixed to the primary packing.

9.4.4 Toxic material warning

When the package contains toxic material, adequate warning information shall be given in accordance with legal requirements and regulations applicable throughout the supply chain.

9.4.5 Fragile components warning

When the package contains fragile components that could be damaged when the container is opened, an appropriate warning shall be included on the primary packing.

9.4.6 ESD sensitivity warning

When the package contains ESD-sensitive components that could be damaged when the product is handled, an appropriate warning shall be included on the primary packing.

10 Requirements for storage

10.1 General

Die products are normally moisture- and oxygen-sensitive and any environment used to store die should be designed to reduce the risk of contamination whilst ensuring that the product degradation is minimized.

Bare die and wafers are also placed into long-term storage, known as wafer banking, as a solution to the component obsolescence problem. Whilst it is accepted that bare die and wafers can be stored for long periods of time, the storage conditions and packing materials need to ensure minimum product degradation during storage.

10.2 Storage duration and conditions

The maximum duration of storage shall be stated together with the conditions under which this storage period is valid.

10.3 Long-term storage

Where a product has been intentionally stored for an extended duration, the long-term storage conditions shall be given and traceability of the product stored shall have been maintained.

11 Information related to assembly

11.1 General

Whilst it is accepted that the semiconductor manufacturer or supplier has no control nor liability over the assembly methods used by the assembler of die products, there may be specific instances where additional information is required for correct assembly or operation of the die. This may be of particular importance for the assembly of MEMS products.

Items related to assembly that are essential to the correct use of the product are detailed in this clause.

11.2 Attach methods and materials

Information on special or abnormal attach methods and materials, including pre-conditioning, shall be given where required for proper assembly of the product.

11.3 Bonding method and materials

Information on special bonding methods to be used shall be given together with information on suitable bonding materials where these methods and/or materials are required for correct operation of the die.

Annex A
(informative)

Terminology

NOTE All trade marks are acknowledged.

A.1 Assembly terminology

A.1.1
Chip-On-Board (COB)
mounting and attach technology where the die is mounted onto a substrate, often a printed-circuit board

A.1.2
MCM-C
MCM using interconnections on a ceramic substrate

A.1.3
MCM-D
MCM using interconnections on a dielectric substrate

A.1.4
MCM-L
MCM using interconnections on a laminated substrate

A.1.5
Surface Mount Technology (SMT)
assembly and PCB technology requiring the components to be mounted on the surface of a PCB, without the need of holes to align and connect to the component pins

A.1.6
pin-in-hole
common term used to express an assembly and PCB technology whereby components are attached by and connected to pins or leads that are mounted through holes in the PCB

A.2 Test terminology

A.2.1
absolute maximum ratings
range of voltages, currents, temperatures, etc., beyond which a device may suffer degradation in performance or reliability, may cease functioning or may suffer irreversible damage

A.2.2
bond pull
test involving the pulling of the bond wires to destruction to determine the strength of the bonds

A.2.3
burn-in
time/temperature/voltage related process intended to uncover potential failures

A.2.4
defect level (DL)
number of undetected defects in a lot
device under test (DUT)
actual semiconductor device that is currently undergoing electrical or environmental test

A.2.5
ESD protected area
EPA
area or workplace that has protection against ESD

A.2.6
electro-static discharge sensitive device
ESDS
device with known sensitivity or susceptibility to ESD

A.2.7
lot accept number
maximum number of devices which may fail a sample test without causing rejection of the lot

A.2.8
lot reject number
for a sample test, number of failed devices which will cause lot rejection

A.2.9
lot tolerance percent defective
LTPD
single lot sampling concept that statistically ensures rejection of 90 % of all lots having a greater per cent defective than the specified LTPD

A.2.10
prober
machine intended to permit electrical connection to individual die on a wafer (q.v.)

A.2.11
resistance to solvents
test which requires immersion of sample devices in solvents such as trichlorotrifluoroethane and methylene chloride, followed by brushing to determine the durability of unit marking

A.2.12
sampling plan
statistically derived set of sample sizes, accept numbers, and/or reject number which will confirm that a given lot of materials meets established AQLs or LTPDs

A.2.13
stabilization bake
placement of devices in a chamber at elevated temperature without electrical bias

A.2.14
temporary carrier
system of contacts, used to hold die during electrical test, which does not make permanent contact to the die, and which possibly can be re-used

A.2.15
testability
measure of whether an IC can be electrically tested economically in production

A.2.16
tester
generic term generally relating to an electronic apparatus designed and used for the purposes of testing and analysing electronic components, including integrated circuits

A.2.17
test vectors
series of test stimuli and expected responses applied to and received by either a simulator to a device model, or a tester to an actual device

A.3 Semiconductor terminology

A.3.1
metal
metallic conducting layer, usually but not specifically aluminium

A.3.2
via
void or hole in a non-conducting layer in order to allow two or more conducting layers to be connected

A.3.3
thermal via
via included for the express purpose of assisting thermal conductivity

A.3.4
poly
layer consisting of poly-crystalline silicon

A.3.5
passivation step
change in thickness of the passivation for metal-to-metal or metal-to-semiconductor interconnection by design, where passivation layers have been removed as a result of normal device processing

A.3.6
glassivation
top layer(s) of transparent insulating material which covers the active circuit area including metallisation, except bond pads

NOTE See also passivation.

A.3.7
crazing
minute cracks in the glassivation

A.3.8
glob top
encapsulation performed by depositing an epoxy resin or similar material over a bonded or attached die

A.3.9
contact window
opening that has been etched in the semiconductor oxide, nitride or other insulating layer, grown or deposited directly onto the die, so as to allow ohmic contact to the underlying semiconductor material

A.3.10
flat
missing segment of a circular wafer used for orientation purposes

A.3.11
under-bump metallization
metallic layer placed on a pad to provide a good connection between a bump and the pad

A.3.12
wafer-level packaging
technique of partial encapsulation and protection of die whilst still on the wafer and before the wafer is sawn or divided into singulated die

A.3.13
reflow
technique for connection of components to a substrate by reheating and melting solder

A.3.14
thickness reduction
process of reducing the thickness of die or wafer for a specific application

A.3.15
bipolar (technology)
fabrication technology, resulting in the creation of bipolar devices

A.3.16
metal oxide semiconductor
MOS
fabrication technology, resulting in the creation of FET devices

A.3.17
N-type metal oxide semiconductor
NMOS
fabrication technology that results in the creation of NMOS FET devices

A.3.18
P-type metal oxide semiconductor
PMOS
fabrication technology that results in the creation of PMOS FET devices

A.3.19
complementary metal oxide semiconductor
CMOS
fabrication technology that results in the creation of both NMOS and PMOS FET devices

A.3.20
bipolar and CMOS devices
BiCMOS
transistor fabrication technology, resulting in the creation of both bipolar and CMOS devices

A.3.21
Gallium Arsenide (GaAs) technology
GaAs
semiconductor material having higher performance speeds than silicon

A.3.22
micron
unit of length, 10^{-6} m, commonly used to describe the geometry of a process; the smallest viable dimension sustainable and practicable in that process

A.3.23
mil
unit of length, 10^{-3} in; non-preferred unit commonly used in describing the dimensions of a die

A.3.24
multi-project wafer
MPW
means of processing prototypes or low volume runs of different ASICs on the same wafer

A.3.25
silicon on insulator
SOI
general term describing a fabrication technology that uses an insulating material as the bulk material instead of silicon, which may be sapphire (SOS)

NOTE It is generally implied that an SOI technology is also a CMOS technology.

A.3.26
silicon on sapphire
SOS
specific fabrication technology that uses sapphire, a variety of corundum (Al2O3), as the bulk material instead of silicon

NOTE It is generally implied that an SOS technology is also a CMOS technology.

A.4 Semiconductor assembly technology

A.4.1
ball bond
capillary-formed impact bond of ball shape, using thermosonic or thermocompression action to create the electrical bond joint

A.4.2
wedge bond
bond joint created by ultrasonic action

A.4.3
laser bond
bond joint created using laser technology

A.4.4
eutectic attach
die attach method relying on a gold-silicon eutectic joint being formed at the Si-Au eutectic temperature of 483 °C

A.4.5
silver-glass attach
die attach method using a glass paste loaded with silver particles for thermal and/or electrical conductivity

A.4.6
polyimide attach
die attach method using a thermally cured organic compound (polyimide), optionally containing a conductive or thermo-conductive additive

A.4.7
polymer attach
die attach method using a thermally cured or thermo-plastic organic compound, optionally containing a conductive or thermo-conductive additive

A.4.8
epoxy attach
die attach method using a thermally cured organic compound (an epoxy resin), optionally containing a conductive or thermo-conductive additive

A.4.9
θ_{JC}
thermal resistance between a die junction and the external surface of a package containing it

A.4.10
metallization run
batch of wafers metallized at the same time

NOTE Since the number of wafers accommodated by the evaporation (i.e. metallization) chamber is frequently less than the number of wafers accommodated by a diffusion chamber, it is possible to have several metallization runs which come from the same wafer run.

A.4.11
traces
tracks
term used to describe the pattern of electrical interconnects on a substrate (term generally used in PCB engineering)

A.4.12
thermal relief
void or series of voids in a thermally conductive layer intended to relieve mechanical stress caused by thermal expansion and contraction

A.5 Design and simulation terminology

A.5.1
workstation
computer system, usually multi-user and multi-tasking, with powerful graphics facilities

A.5.2
netlist
software file containing interconnection and instance information pertinent to a specific design

A.5.3
model
mathematical, software or textual representation describing the behaviour of a circuit or device

A.5.4
library
suite of data representing a semiconductor technology

A.5.5
simulation package for integrated circuit electronics
SPICE
generic term describing a range of commercial analogue simulators, having common ancestry in the original Berkeley SPICE2 electrical simulation program

NOTE The majority of modern SPICE simulators maintain a common compliance level for SPICE modelling.

A.5.6
VITAL
timing compliant library for use with VHDL simulators

A.5.7
Verilog
simulation and synthesis language, overseen by the Open Verilog Institute (OVI), and defined in IEEE 1364

NOTE Verilog® is a registered trademark of Cadence Design Systems, Inc.

A.5.8
register transfer level
RTL
level of logic design abstraction used to simplify the visualization of a design

A.5.9
layout versus schematic
LVS
process to verify a semiconductor IC or MCM layout matches the intended device schematic (or netlist)

A.5.10
design rules check
DRC
process to verify that mechanical or topological design rules have not been infringed, specifically applicable for a semiconductor IC or MCM layout

A.5.11
electrical rules check
ERC
process to verify that electrical and electromechanical design rules have not been infringed, specifically applicable for a semiconductor IC or MCM layout and schematic

A.5.12
synthesis
automatic way of carrying out logic design

A.5.13
layout
representation of the geometric implementation of an electronic design

A.5.14
pad layout
drawing, photograph or reproduction of the die metallization pattern, giving sufficient information as to the placement of the connection or bond pads

A.5.15
extraction
term given to the mechanism of obtaining electrical and/or netlist data from a physical/ mechanical layout

A.5.16
data pack
collection of information, often including design documentation and test results, which identify and document all aspects of the qualification process for a given design or a given lot of die

A.5.17
deck
common expression for a file or files containing either checking rules, e.g. for LVS, DRC and ERC, or variable parameters for simulation, e.g. SPICE

A.5.18
joint test action group
JTAG
international group that resulted in the creation of a test specification and definition relating to the interconnection of ICs and their testability as IEEE 1149.1

A.5.19
quality test action group
QTAG
international technical group making research into test techniques

A.5.20
Boundary Scan Definition Language
BSDL
software language (model) specification for use with and defined in the IEEE 1149.1 for boundary scan testing

A.5.21
Die Information Exchange
DIE
software language and file format specification used for the transfer of pertinent die data

A.5.22
Electronic Design Interchange Format
EDIF
specification for the transfer of electronic CAD data

NOTE Current versions are EDIF 2 0 0 and EDIF 3 0 0, whilst EDIF 4 0 0 supports the description of MCMs.

A.5.23
Initial Graphics Exchange Specification
IGES
specification for the interchange of geometric data

A.5.24
standards for the exchange of product data
STEP
ISO 10303 series of standards

A.5.25
Graphical Display System
GDSII
software language and file format specification used in the transfer of semiconductor physical layout design data

NOTE GDSII is a registered trademark of Cadence Design Systems.

A.5.26
stream format
alternative name often given to GDSII data

A.5.27
Caltech Intermediate Format
CIF
software language and file format specification used in the transfer of semiconductor physical layout design data, defined and specified by the California Institute of Technology

A.5.28
Drawing eXchange Format
DXF
software language and file format specification used to transfer mechanical drawing data

NOTE DXF is a registered trademark of Autodesk Inc.

A.5.29
Comma Separated Variable
CSV
common data format, where discrete data fields are separated by commas

A.6 Packing and delivery terminology

NOTE Refer to IEC 61540 for the Basic Specification on the Protection of Electrostatic Sensitive Devices.

A.6.1
date code
three or four digit number identifying the date of assembly of a lot; the first one or two digits commonly identifying the year, the last two the week

A.6.2
wafer box
wafer pot
container in which wafers may be housed for storage and transport

A.6.3
waffle tray
waffle pack, die tray
compartmentalized shallow tray in which the die may be housed for storage and transport

A.6.4
dry pack
container that maintains the moisture content of the packages of die devices within specified limits

A.6.5
GEL-PAK™
proprietary name for a container similar to a waffle pack (q.v.) used for die storage and transportation which uses a low-tack insert gel in place of compartments to hold the die in a specific position

A.6.6
wafer foil carrier
plastic foil membrane or film stretched across a frame and having one side slightly adhesive, which holds a wafer in position for sawing and subsequent processing