IEC 62150-6

Edition 1.0 2022-01

INTERNATIONAL STANDARD

colour inside

Fibre optic active components and devices – Test and measurement procedures –
Part 6: Universal mezzanine boards for test and measurement of photonic devices

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FIBRE OPTIC ACTIVE COMPONENTS AND DEVICES – TEST AND MEASUREMENT PROCEDURES –

Part 6: Universal mezzanine boards for test and measurement of photonic devices

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IEC 62150-6 has been prepared by subcommittee SC 86C: Fibre optic systems and active devices of IEC technical committee 86: Fibre optics. It is an International Standard.

The text of this International Standard is based on the following documents:

Draft	Report on voting
86C/1721/CDV	86C/1752/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

A list of all parts in the IEC 62150 series, published under the general title *Fibre optic active components and devices – Test and measurement procedures*, can be found on the IEC website.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

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- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

This document defines a generic electro-optic mezzanine board for the test and measurement of micro-optical and micro-photonic devices, including a wide diversity of photonic integrated circuit (PIC) technologies including, but not limited to, transceivers, switches, sensors, neuromorphic networks, LiDAR and quantum integrated circuits. The board size and shape would allow two mezzanine boards to be mounted, side-by-side, on a larger Eurocard form factor daughtercard, which itself can be docked into and powered from a backplane system. Alternatively, each mezzanine board can be operated alone, for example on a lab bench powered from a bench supply.

The purpose of this generic mezzanine board concept is to allow like-for-like comparative characterisation of devices under test (DUTs) with respect to one another and to measure the performance of DUTs within larger test environments, relevant to their targeted application, such as data centre systems, high performance computers, automotive or 5G cabinets. The mezzanine board PCB will be designed to accommodate very high-speed electronic signals and a high-speed electronic signal interface to allow external test equipment such as test pattern generators, bit error rate testers and communication signal analysers to drive the device under test (DUT).

This approach will be instrumental in accelerating commercial adoption of micro-photonic devices as they will provide a common benchmark, against which to evaluate the true performance of a DUT. For example, power consumption is an increasingly important figure of merit for optical micro-transceivers in ICT systems; however, the declared values of power consumption as interpreted by the developer often do not reflect the true power consumption of a device under test in operation. The mezzanine board will therefore include provision for a smaller detachable power distribution and sensor mezzanine board allowing multiple tuneable voltages to be provided to the device under test and real-time current or power measurement for each voltage.

Variants of these mezzanine boards have been successfully developed and adopted within the European research and development projects European FP7 project PhoxTrot [1][1], European H2020 Nephele [2] and European H2020 COSMICC [3]. Annex A provides an introduction to these projects.

[1] Numbers in square brackets refer to the Bibliography.

FIBRE OPTIC ACTIVE COMPONENTS AND DEVICES – TEST AND MEASUREMENT PROCEDURES –

Part 6: Universal mezzanine boards for test and measurement of photonic devices

1 Scope

This part of IEC 62150 specifies a generic mezzanine board system to support test and measurement of devices based on micro-optical and micro-photonic technologies, including but not limited to photonic integrated circuit (PIC) devices.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050-731, *International Electrotechnical Vocabulary – Part 731: Optical fibre communication* (available at www.electropedia.org)

IEC 62150-1, *Fibre optic active components and devices – Test and measurement procedures – Part 1: General and guidance*

IEC TR 63072-1, *Photonic integrated circuits – Part 1: Introduction and roadmap for standardization*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60050-731, IEC 62150-1, IEC TR 63072-1 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
mezzanine board
electronic, optical, or electro-optical printed circuit board designed to be docked onto a larger board such that the surfaces of the mezzanine board and larger board are parallel

3.2
photonic integrated circuit
PIC
integrated circuit that contains optical structures to guide and process optical signals

Note 1 to entry: See IEC TR 63072-1.

3.3
device under test
DUT
single component or combination of components as defined to be tested

4 Mezzanine board requirements

4.1 Functional description

This document specifies three categories of mezzanine boards:

- half-width mezzanine test board 1 (M1);
- full-width mezzanine test board 2 (M2);
- power distribution and sensor board (PDS).

Figure 1 shows the outline shapes of these three mezzanine boards with electric power and other low-speed electric connectors on the top and bottom surfaces.

This document defines the outline boundary of the three boards, as shown by the solid thick line in Figure 1, but the designer is free to adopt any shape within the defined boundary, as long as it does not interfere with the positions of the power and low-speed connectors on the top and/or bottom surfaces. M2 is shown with optional example cut-outs along the edges. The purpose of such cut-outs typically is to allow the user to access components on the underlying host board over which the mezzanine board is attached. For example, during operation, the user may require transient access to connectors on the underlying host board for low-speed diagnostic read-outs from the PDS.

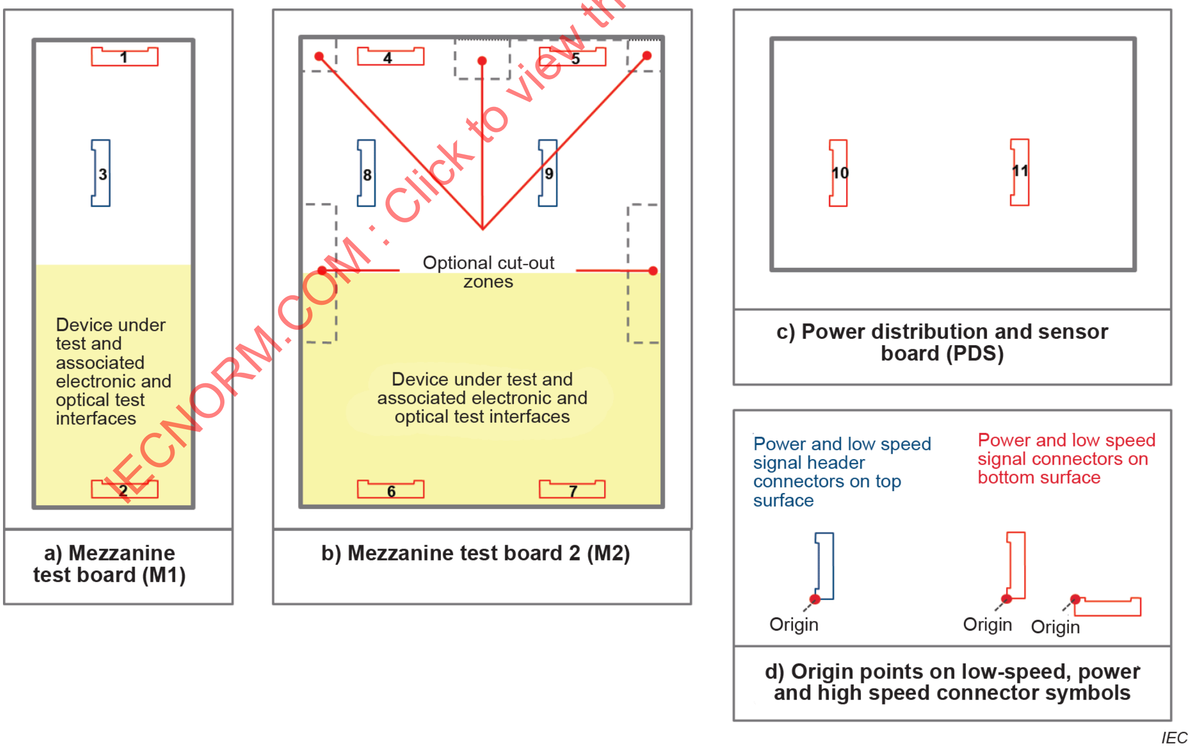

Figure 1 – Outlines of mezzanine test boards

M1 and M2 are mezzanine test boards with areas assigned for micro-optical or micro-photonic devices under test (DUTs) and the associated electronic and optical test interfaces.

For example, the DUT on a mezzanine test board (M1 or M2) could be an experimental photonic integrated circuit (PIC) optical transceiver. The associated electronic test interface could be a high RF electronic signal header connector array through which high-speed test signals generated from an external electronic signal pattern generator could be conveyed to the optical transmit section of the transceiver DUT and through which electronic high-speed signals generated from the optical receiver section of the transceiver DUT could be conveyed off the mezzanine test board to an external electronic communications signal analyser or bit error rate tester. The associated optical test interface could be an optical array connector attached by an optical fibre ribbon to the optical transceiver DUT through which high-speed optical signals from an external optical signal pattern generator could be conveyed to the optical receiver section of the transceiver DUT and through which optical high-speed optical signals generated from the optical transmit section of the transceiver DUT could be conveyed off the mezzanine test board to an external optical communications signal analyser or optical bit error rate tester.

The PDS is a power distribution and sensor board that attaches onto a full width mezzanine card (M1) or across one or two half-width mezzanine test boards (M1) and provides the requisite voltage or separate voltages to the device under test on its host mezzanine test board or boards. In addition, the PDS provides a current sensor for each voltage provided to the mezzanine test board(s), allowing the power consumption of the corresponding DUT to be measured. Typically, the current sensor will communicate the readings of current in real-time across a low-speed signal interface, for example a serial wire interface such as I2C. Figure 2 shows a PDS attaching to an M2 board.

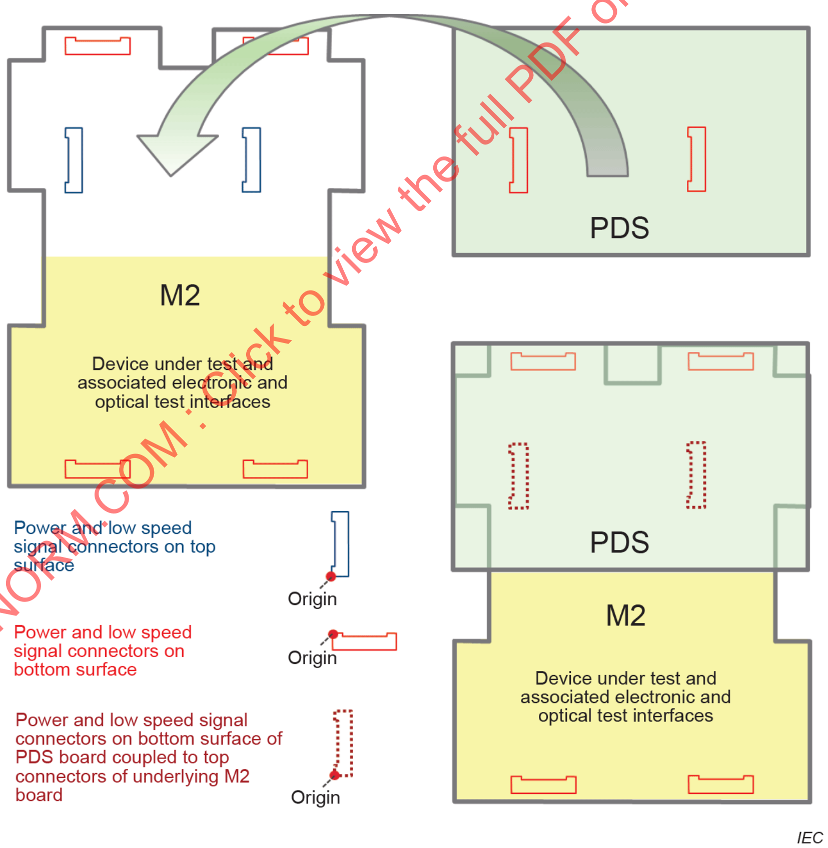

Figure 2 – Attachment of PDS onto M2 board

4.2 Critical dimensions

This document defines the outline board dimensions and the relative positions of the origin points of the power and low-speed signal connectors on the top and bottom surfaces with respect to one another and the board origin points. The connector origin points are always defined by the centre position of pin 1. In Figure 2, as well as in Figure 3 to Figure 10, the connector origin points are represented by a corner of the package shape itself, but as connectors may vary, the package sizes may also vary.

Figure 3 shows the relative positions of the origin points of the power and low-speed signal connectors on top and bottom surfaces and the mezzanine board origin point on M1.

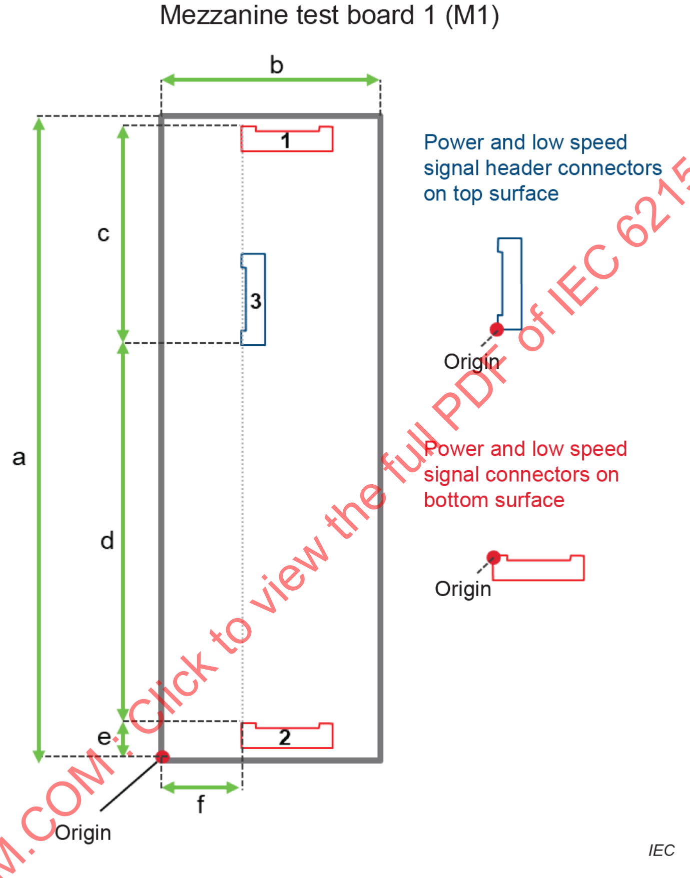

Figure 3 – Mezzanine board 1 (M1) – Relative positions of power and low speed signal connectors on top and bottom surfaces and mezzanine board origin

Figure 4 shows the relative positions of the origin points of the power and low-speed signal connectors on top and bottom surfaces and the mezzanine board origin point on M2.

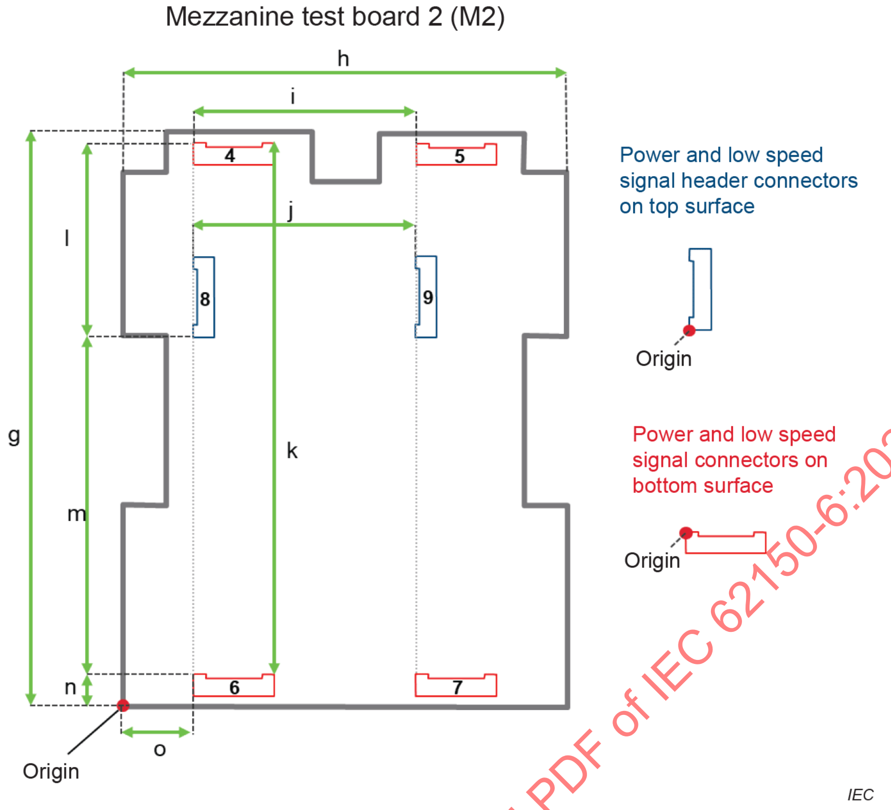

Figure 4 – Mezzanine board 2 (M2) – Relative positions of power and low speed signal connectors on top and bottom surfaces and mezzanine board origin

Figure 5 shows the relative positions of power and low-speed signal header connectors on bottom surfaces and the mezzanine board origin point on the PDS.

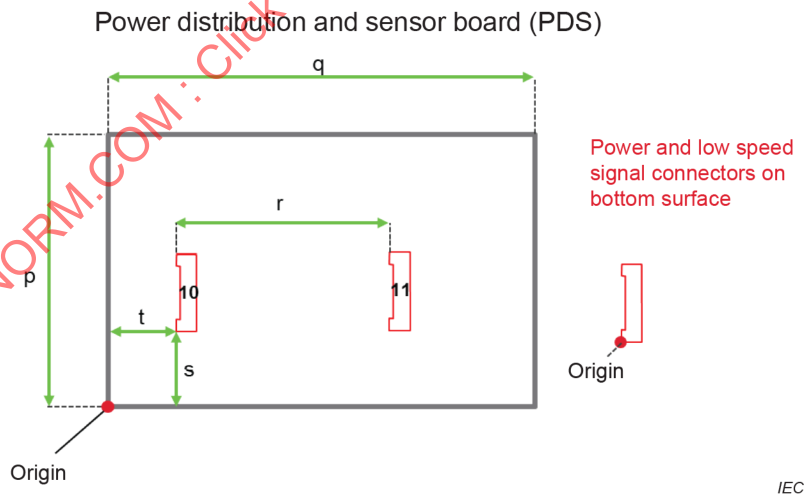

Figure 5 – Power distribution and sensor board (PDS) – Relative positions of power and low speed signal connectors on bottom surfaces and mezzanine board origin

Table 1 shows the values of the critical relative dimensions of the board outline and relative positions of the power and low-speed signal connectors on the top and bottom surfaces with respect to one another and the board origin points.

Table 1 – Critical relative dimensions

Designation	Description	Value mm
Mezzanine board 1 (M1)		
a	Length of M1	145
b	Width of M1	Maximum 53
c	Vertical distance between bottom connector 1 and top connector 3	48
d	Vertical distance between top connector 3 and bottom connector 2	86,35
e	Vertical distance between bottom connector 2 and board origin point	8,25
f	Horizontal distance between bottom connector 2 and board origin point	15
Mezzanine board 2 (M2)		
g	Length of M2	145
h	Width of M2	Maximum 112
i	Horizontal distance between bottom connectors 4 and 5	70
j	Horizontal distance between top connectors 8 and 9	70
k	Vertical distance between bottom connectors 4 and 6	134
l	Vertical distance between bottom connector 4 and top connector 8	48
m	Vertical distance between top connector 8 and bottom connector 6	86,35
n	Vertical distance between bottom connector 6 and board origin point	8,25
o	Horizontal distance between bottom connector 6 and board origin point	15
Power distribution and sensor board (PDS)		
p	Length of PDS	112
q	Width of PDS	Maximum 145
r	Horizontal distance between bottom connectors 10 and 11	70
s	Vertical distance between bottom connector 10 and board origin point	14,75
t	Horizontal distance between bottom connector 10 and board origin point	16,5

4.3 Daughtercard and extended system

The M1 and M2 boards populated with PDS can be used stand-alone, for example on a lab bench powered by an external power supply.

Alternatively, the M1 and M2 boards can be incorporated into a wider rack-scale test system, whereby they are mounted onto a test daughtercard, and the test daughtercard, in turn, could be electro-optically plugged into the backplane of the test enclosure.

The M1 and M2 board dimensions were designed to allow either four M1 or two M2 boards to be populated onto a daughtercard with "extended double Eurocard form factor", which is a common industrial form factor appropriate for deployment in rack-scale enclosures.

Figure 6 shows the outline dimensions of an extended double Eurocard form factor daughtercard with example electrical edge connectors and example cut-outs to accommodate optical backplane connectors.

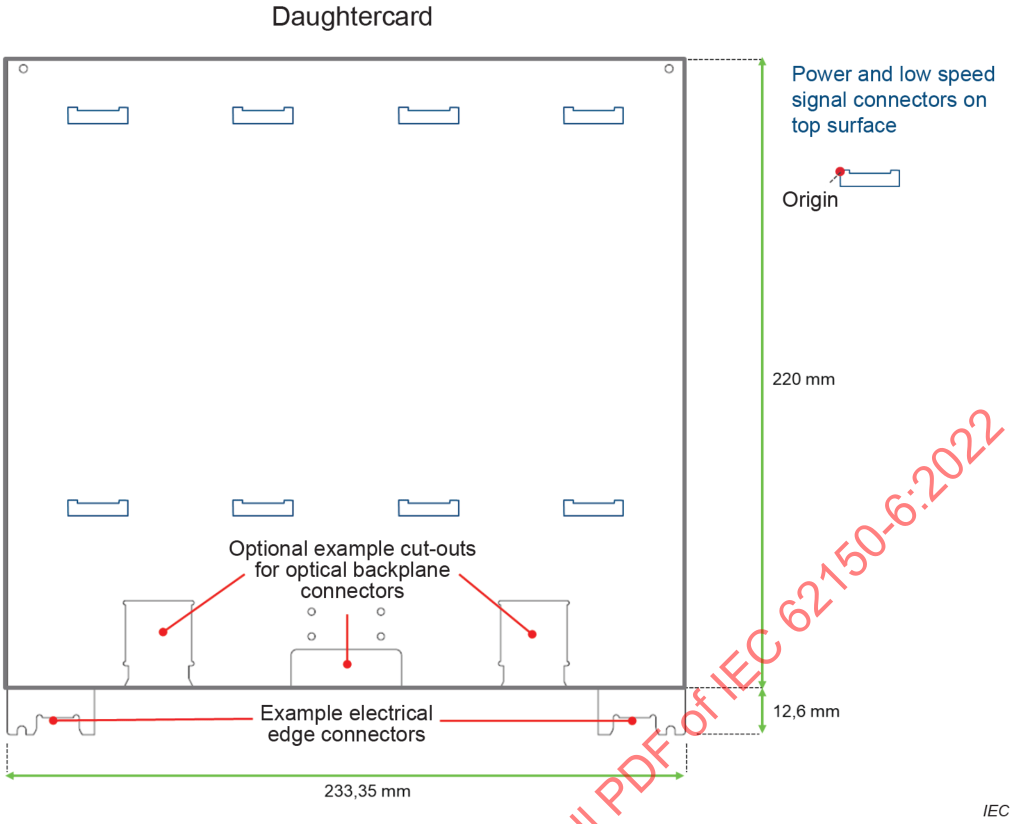

Figure 6 – Outline dimensions of extended double Eurocard form factor daughtercard with electrical edge connectors and cut-outs to accommodate optical backplane connectors

Figure 7 shows two M2 boards being attached to a test daughtercard.

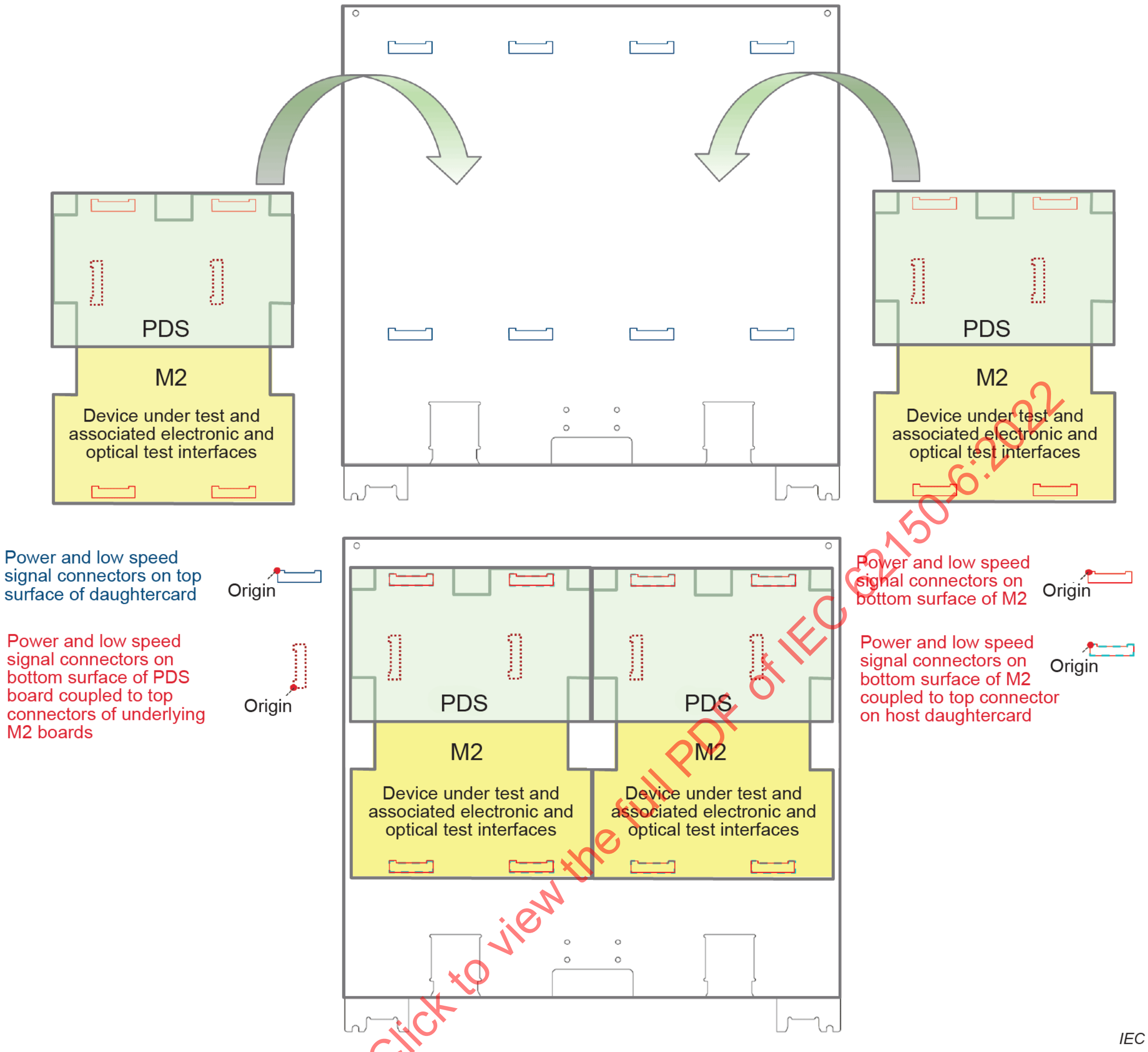

Figure 7 – Attachment of M2 boards onto daughtercard

Figure 8 shows two M2 boards populated with PDS boards attached to a test daughtercard.

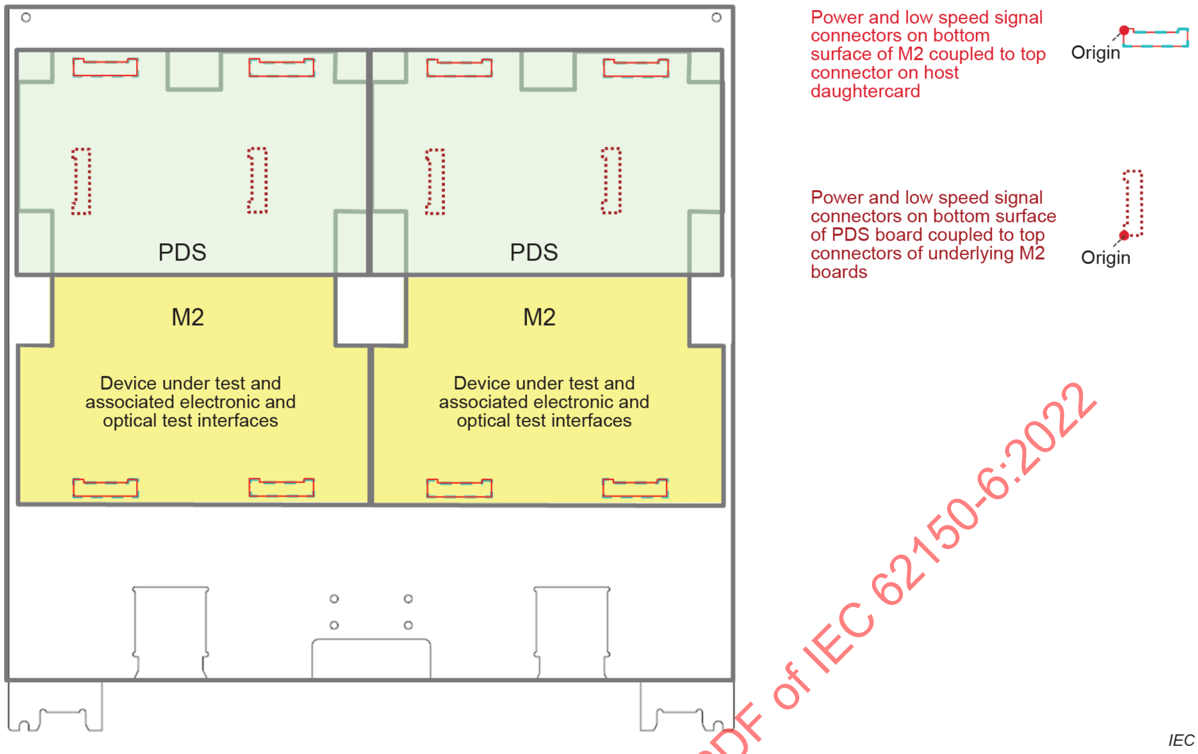

Figure 8 – Extended double Eurocard form factor daughtercard with two M2 boards attached

Figure 9 shows four M1 boards attached to a test daughtercard. Two PDS boards are connected across two adjacent pairs of M1 boards.

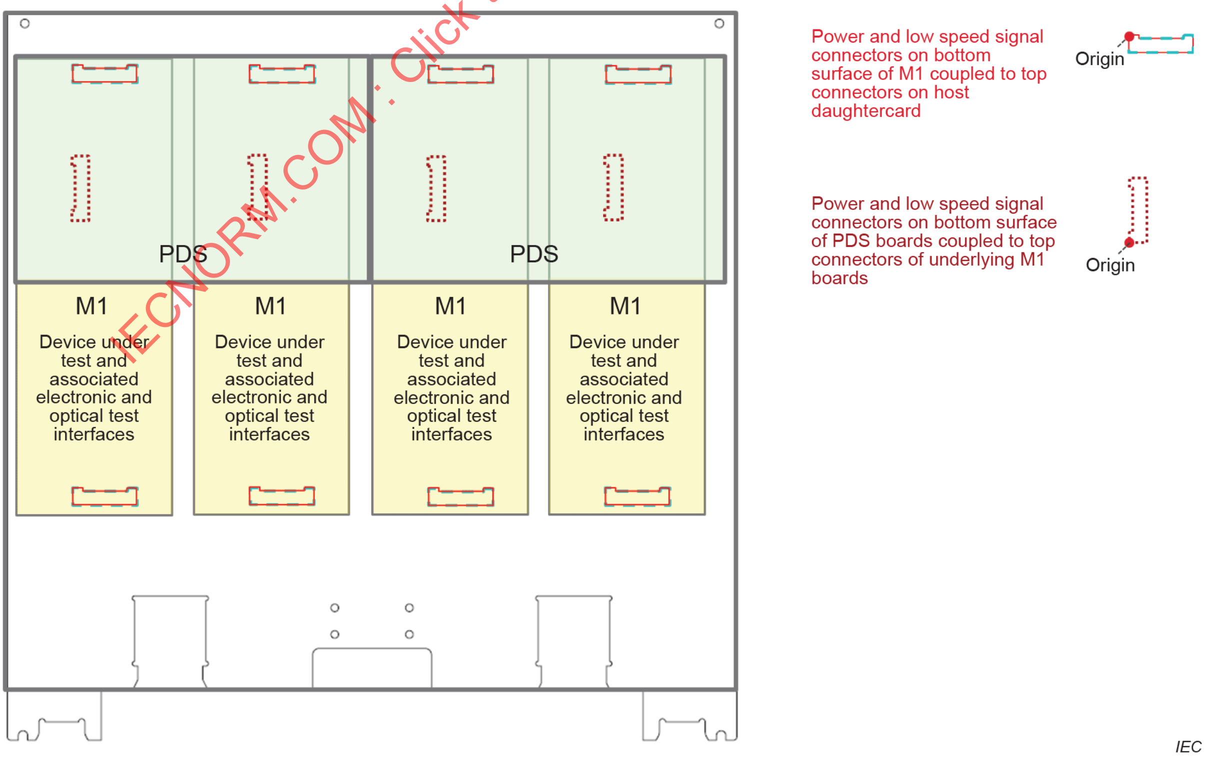

Figure 9 – Extended double Eurocard form factor daughtercard with four M1 boards attached

Figure 10 shows two M1 boards and one M2 board on a test daughtercard. A PDS board is connected across the two M1 boards. Another PDS is connected onto the M2 board.

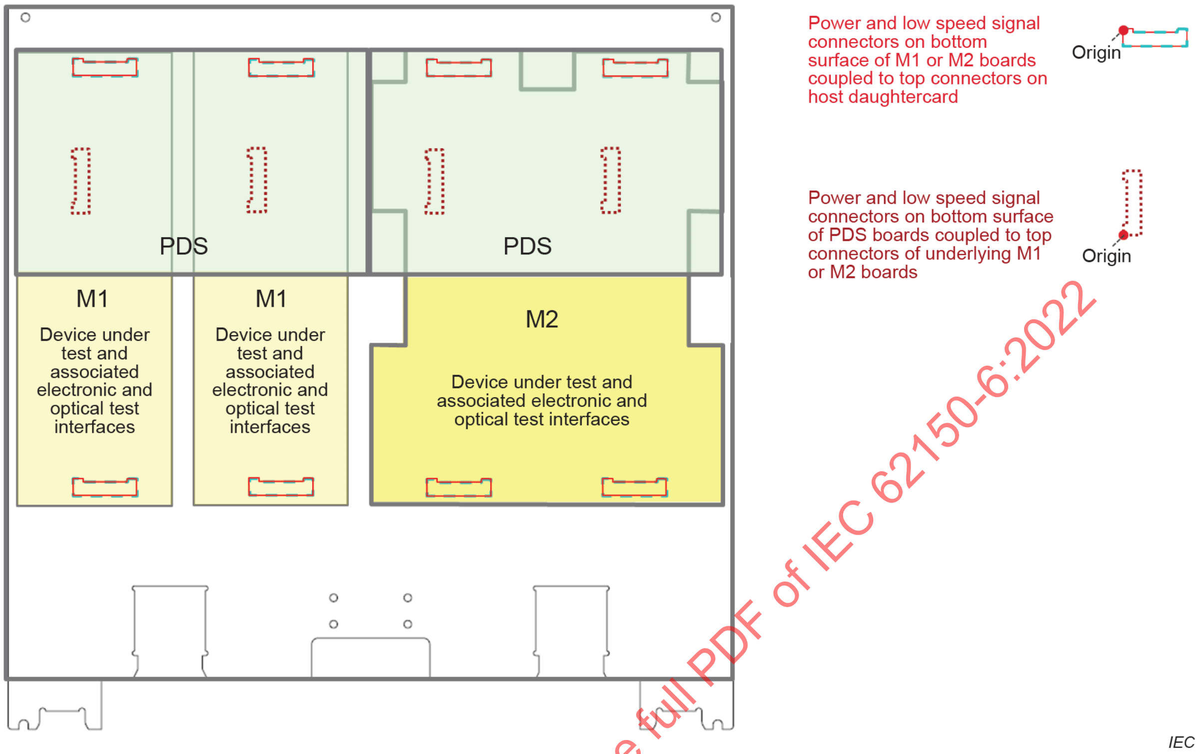

Figure 10 – Extended double Eurocard form factor daughtercard with two M1 boards and one M2 board attached

4.4 Power and signal flows

Figure 11 shows the flow of the master and slave voltages and low-speed signals, and Table 2 lists the corresponding voltage and low-power signal designations.

Up to six separate master voltages (A to F) can be conveyed to the PDS mounted on a mezzanine test card M1 or M2. The master voltages can either be conveyed directly to the PDS from an external power supply via a standard power connector header on the PDS, or they can be conveyed via the test daughtercard on which the mezzanine test card is mounted, from the system backplane into which the daughtercard is plugged.

Typically, only one master voltage is required, but provision also includes multiple grounds as master voltages. The master voltages are conveyed to voltage regulators on the PDS, which convert the master voltage(s) into slave voltages, which are passed to the device under test mounted on the underlying mezzanine test card. Taking into account the size of the PDS and the typical size of drop-down regulators, up to eight slave voltages can be generated. If the PDS straddles two M1 boards, then the slave voltages would need to be divided across the DUTs on those M1 boards.

The PDS will also include a current sensor associated with each voltage regulator to allow the power consumption to be accurately determined on each slave voltage line. This can be a powerful characterisation tool and collectively will yield an accurate measurement of whole device power consumption. The sensors will convey the sensor read-outs from the PDS to the host mezzanine board. Preferably, as there will be a large number of such low-speed signals (for e.g. device diagnostics), they can be passed to a signal aggregator, such as an I2C multiplexer. The multiplexer can be polled directly from the mezzanine card or conveyed to the system backplane to be gathered and processed by the test system.

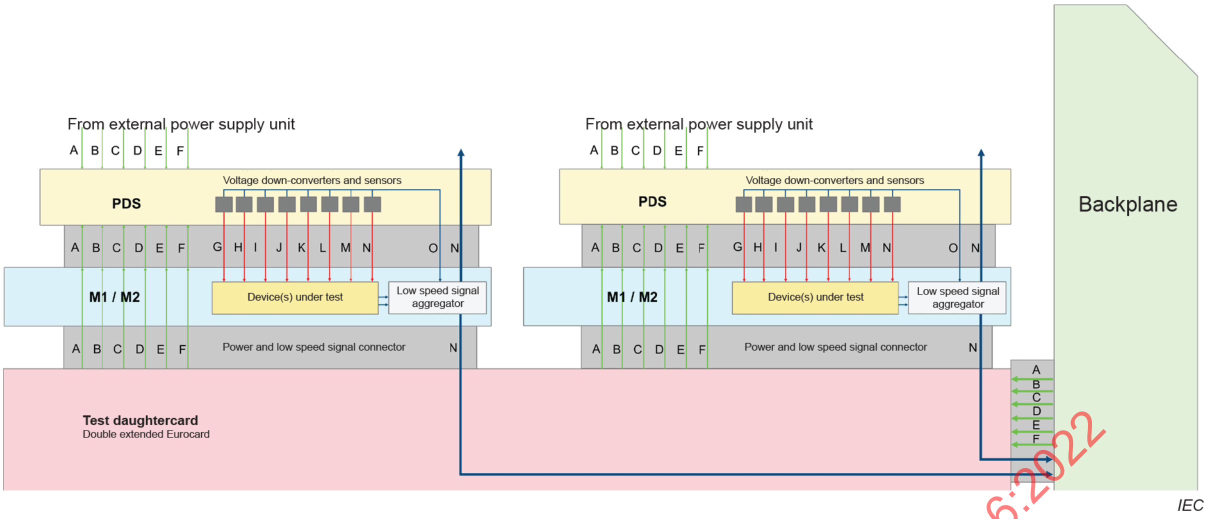

Figure 11 – Functional diagram showing power and low speed signal distribution between PDS, M1/M2, daughtercard and backplane

Table 2 – Voltages and low-power signal designations

Designation	Type	Description
A, B, C, D, E, F	Voltage	Master voltages including ground provided to the PDS board(s) either directly from an external power supply unit or from the backplane via the mezzanine board (M1 or M2) and test daughtercard.
G, H, I, J, K, L, M, N	Voltage	Up to eight slave voltages derived from one or more of the master voltages and generated on the PDS and fed to the underlying M1/M2 board. The slave voltages can be generated by, for example, linear drop-down or switching voltage regulators on the PDS. The voltage regulators are preferably tuneable.
O	Low speed signal	Real-time sensor read-out of current (and thus power) drawn on each slave voltage. Sensor read-out signal is passed from the PDS to the underlying M1/M2 for redirection either to a signal access port on M1/M2 itself (for stand-alone testing), or to the larger test system via the daughtercard and backplane (for in-system testing). Sensor read-out signal could be via a serial wire interface such as I2C. Preferably, the sensor read-out signal is passed to a low-speed signal aggregator on M1/M2 (e.g. an I2C multiplexer), which will allow multiple low-speed signals, including status read-out signals from the device under test, to be aggregated and redirected to a signal access port on M1/M2 itself (for stand-alone testing), or to the larger test system via the daughtercard and backplane (for in-system testing).
N	Low speed signal	Redirected low-speed sensor signals from PDS and M1/M2 via a signal aggregator (e.g. an I2C multiplexer).

Figure 12 shows multiple populated daughtercards being plugged into a system backplane.

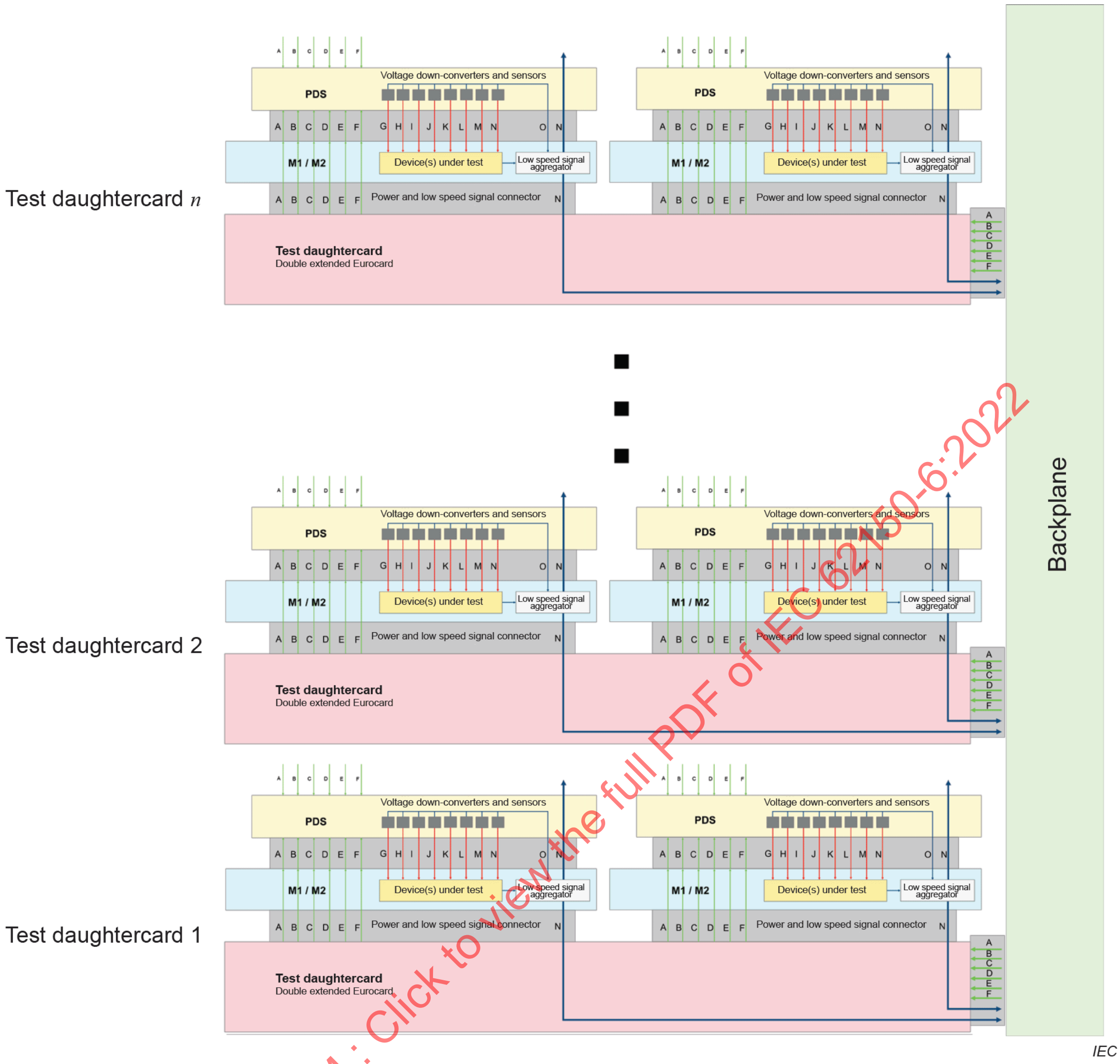

Figure 12 – Multiple daughtercards populated with M1/M2 and PDS in multiple slots on a system backplane

Annex A
(informative)

International collaborative research and development

A.1 Overview

Global research and development into the incorporation of optical and photonic interconnects into information communication technology (ICT) systems is yielding a diverse eco-system of contender technologies. This eco-system includes

1) micro-optical or micro-photonic devices, such as photonic integrated circuit (PIC) based transceivers, switches, sensors,
2) fibre, polymer and glass waveguide based electro-optical circuit boards, and
3) optical connectors.

System embedded optical and photonic interconnects have been a strong area of focus in the USA, APAC, and, in particular, the European funding programmes for collaborative research and technological development over the past 15 years. This is particularly evident in projects from the Sixth Framework Programme (FP6) [4], which ran from 2002 to 2006, the Seventh Framework Programme (FP7) [5], which ran from 2007 to 2013, and the Horizon2020 programme [6], which ran from 2014 to 2021.

Figure A.1 a), b) and c) shows an example of the deployment of these mezzanine cards in European collaborative projects.

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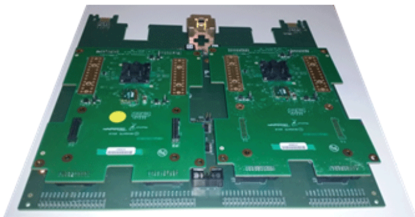
a) European cross-project Aurora system



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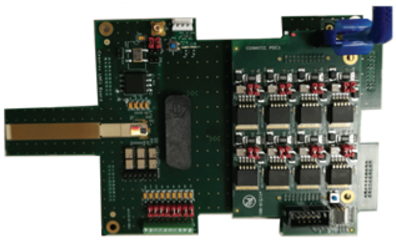
b) Test daughtercard



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c) Mezzanine card from H2020 COSMICC

Figure A.1 – Example of cross-project deployment of mezzanine test card [3]