INTERNATIONAL STANDARD

IEC 62026-6

First edition
2001-11

**Low-voltage switchgear and controlgear –
Controller-device interfaces (CDIs) –**

**Part 6:
Seriplex (Serial Multiplexed Control Bus)**

*Appareillage à basse tension –
Interfaces appareil de commande-appareil (CDI) –*

*Partie 6:
Seriplex (Serial Multiplexed Control Bus)*

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Reference number
IEC 62026-6:2001(E)

Publication numbering

As from 1 January 1997 all IEC publications are issued with a designation in the 60000 series. For example, IEC 34-1 is now referred to as IEC 60034-1.

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Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия

PRICE CODE XC

For price, see current catalogue

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

LOW-VOLTAGE SWITCHGEAR AND CONTROLGEAR – CONTROLLER-DEVICE INTERFACES (CDIs) –

Part 6: Seriplex (Serial Multiplexed Control Bus)

FOREWORD

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International Standard IEC 62026-6 has been prepared by subcommittee 17B: Low-voltage switchgear and controlgear, of IEC technical committee 17: Switchgear and controlgear.

The text of this standard is based on the following documents:

FDIS	Report on voting
17B/1162/FDIS	17B/1174/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

The committee has decided that the contents of this publication will remain unchanged until 2004. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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INTRODUCTION

The general rules in IEC 62026-1 are applicable to this International Standard, where specifically called for. All such rules, clauses and subclauses, together with tables, figures and annexes, are identified by reference to part 1, for example 7.2.4.1 of IEC 62026-1.

Seriplex (Serial Multiplexed Control Bus) is a controller-device interface which provides a deterministic means of exchanging simple data among control and sensing devices. All devices are connected together by a single shielded four-conductor cable.

Any device which fully conforms to this part of IEC 62026 will be able to perform at least elementary data exchange with other compliant devices through the Seriplex controller-device interface.

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LOW-VOLTAGE SWITCHGEAR AND CONTROLGEAR – CONTROLLER-DEVICE INTERFACES (CDIs) –

Part 6: Seriplex (Serial Multiplexed Control Bus)

1 Scope

This part of IEC 62026 specifies an interface system between single or multiple controllers, and control circuit devices or switching elements. The interface system uses two twisted conductor pairs within one cable – one of these pairs provides a communication medium and the other pair provides power to the devices. It also establishes requirements for the interchangeability of components with such interfaces.

This standard specifies the physical and operating characteristics of the Seriplex controller-device interface, including:

– requirements for interfaces between controllers and switching elements;
– normal service conditions for devices;
– constructional and performance requirements;
– tests to verify conformance to requirements.

These particular requirements apply in addition to the general requirements of IEC 62026-1.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 62026. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of IEC 62026 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 60068-2-6:1995, *Environmental testing – Part 2: Tests – Test Fc: Vibration (sinusoidal)*

IEC 60068-2-27:1987, *Basic environmental test procedures – Part 2: Tests – Test Ea and guidance: Shock*

IEC 60664-1:1992, *Insulation coordination for equipment within low voltage systems – Part 1: Principles, requirements, and tests*

IEC 60947-1:1999, *Low-voltage switchgear and controlgear – Part 1: General rules*

IEC 61000-4-2:1995, *Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 2: Electrostatic discharge immunity test.* Basic EMC Publication

IEC 61000-4-3:1995, *Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 3: Radiated, radio-frequency, electromagnetic field immunity test*

IEC 61000-4-4:1995, *Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 4: Electrical fast transient/burst immunity test.* Basic EMC Publication

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IEC 61000-4-5:1995 *Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 5: Surge immunity test*

IEC 61000-4-6:1996, *Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 6: Immunity to conducted disturbances induced by radio-frequency fields*

IEC 62026-1:2000, *Low-voltage switchgear and controlgear – Controller-device interfaces (CDIs) – Part 1: General rules*

CISPR 11:1997, *Industrial, scientific and medical (ISM) radio-frequency equipment – Electromagnetic disturbance characteristics – Limits and methods of measurement*

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purpose of this of this part of IEC 62026, clause 3 of IEC 62026-1, together with the following additions, apply.

3.1.1
address multiplexing
means of extending the data capacity of a Seriplex controller-device interface by assigning signals to one of 16 multiplex channels and broadcasting the multiplex channel number at the start of each data frame

3.1.2
address sharing
practice of assigning two or more signals to the same address

NOTE In the peer-to-peer mode, all addresses used are typically shared by one input signal and one output signal.

3.1.3
analogue input device
device which converts an external analogue signal to a numeric signal to be transmitted to the controller-device interface as input data

3.1.4
analogue output device
device which converts a Seriplex numeric output signal to an external analogue signal

3.1.5
Bus Fault Detect (BFD) pulse
negative-going (logic high-to-low-to-high) pulse on the data line during the sync period, produced by the clock source, and used by the clock source and I/O devices to evaluate the condition of the Seriplex controller-device interface

3.1.6
bus halt
intentional condition in which generation of the Seriplex clock signal is suspended, so that no data signals are transmitted through the controller-device interface, and all output devices assume their default states

NOTE A bus halt is essentially the same as a clock loss condition; bus halt is usually used to indicate that the condition is normal and intentionally induced by the clock source.

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3.1.7
clock
Seriplex signal which is used to synchronize data exchange among connected devices

3.1.8
clock loss
condition in which the Seriplex clock signal is not operating due to a fault condition, so that no data signals are transmitted through the controller-device interface, and all output devices assume their default states

3.1.9, t_{closs}
clock loss detection period
time without a transition of the Seriplex clock signal (low-to-high or high-to-low) after which a device detects a clock loss condition

NOTE Typically, output devices will assume their default states after the clock loss detection period has elapsed.

3.1.10
clock module
dedicated device which performs clock source functions for a Seriplex CDI operating in peer-to-peer mode

3.1.11
clock pulse
sequence of logic level transitions on the Seriplex clock line, beginning with a positive (logic low-to-high) transition and including a negative (high-to-low) transition

3.1.12
clock rate
repetition frequency of the Seriplex clock signal during the data-transmission portion of a data frame

NOTE This rate is the reciprocal of the clock period.

3.1.13
clock source
Seriplex device which generates the clock signal, provides the current source for the data line, and transmits the Bus Fault Detect pulse

NOTE Usually the clock source is incorporated within an interface to a controller, but for peer-to-peer mode operation this may be a clock module instead.

3.1.14
control software
software which monitors Seriplex input signals and controls Seriplex output signals

NOTE This software might be C or Basic or other code within a computer, ladder logic within a PLC, or embedded firmware within a dedicated control device. Typically this software performs controller-device interface start/stop functions and interface card initialization as well as signal monitoring and control.

3.1.15
daisy-chain
method of connecting Seriplex devices by cable segments connected end-to-end

3.1.16
data echo
feature of Seriplex devices whereby the device receives a signal then retransmits that signal to the controller-device interface

NOTE This feature may be used to indicate to a data-transmission device that a data signal has been properly received by another device.

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3.1.17
data frame
sequence of clock pulses on the clock line, bounded at its beginning and end by a sync period

3.1.18
data line capacitance
capacitance of the data line to all the other conductors

3.1.19
data pass-through
interface feature used in master/slave mode, which takes controller-device interface input signals and retransmits them as controller-device interface output signals at the same signal addresses, without the intervention of control software

NOTE This feature mimics peer-to-peer mode operation in that input devices may directly control output devices at the same address without control programming.

3.1.20
default state
state of Seriplex I/O device output signals under initial power-up, clock loss, and bus fault conditions

NOTE Usually this state is the “off” or inactive state, and corresponds to an output signal value of 0.

3.1.21
digital debounce
optional feature of Seriplex devices whereby multiple identical values of a particular discrete controller-device interface output signal are detected in successive data frames in order to cause the Seriplex device to change the logic state of its external output signals

3.1.22
discrete signal
data signal consisting of exactly one bit of information

NOTE Such a signal may assume one of only two states or values–logic high or low, 0 or 1. Both Seriplex input and output data signals and a device's external input and output signals may be discrete signals.

3.1.23
drop
relatively short length of Seriplex cable which is connected to a longer "trunk" cable

NOTE Typically branch lines are 16 m or less, while trunk lines may be hundreds or thousands of metres long.

3.1.24
excess time constant
bleedover

effect which occurs when the data line cannot recharge to a high logic state within one-half clock period after being released from a logic low state

NOTE This effect may result in signals with an intended value of 0 being incorrectly interpreted as having a value of 1.

3.1.25
frame length
number of signal addresses transmitted within a single Seriplex data frame

3.1.26
frame period, t_f
time consumed by one data frame, that is, the elapsed time between the end of successive sync periods during normal operation

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3.1.27
host interface
electronic hardware device which allows control software running on a controller to monitor and control I/O devices through a Seriplex controller-device interface by some means such as a backplane interface or controller-device interface gateway

NOTE A host interface typically also provides Seriplex clock source functions.

3.1.28
input propagation delay
elapsed time between an external input signal event and that signal's availability within a Seriplex input device for transmission to the controller-device interface

3.1.29
input response time, t_{ir}
a) in **peer-to-peer mode**, elapsed time between an external input signal event and that signal's appearance on the controller-device interface communications medium

b) in **master/slave mode**, the elapsed time between an external input signal event and that signal's availability to a master's internal logic processor

3.1.30
input signal
signal received by a Seriplex device other than a controller, and reported to the Seriplex controller-device interface

3.1.31
I/O module
device that converts between Seriplex signals and external signals from control circuit devices

3.1.32
master
Seriplex device which executes control logic, incorporates the clock source function, has exclusive access to input data, and is the only device which transmits output data

3.1.33
master/slave mode
mode 2

operating mode comprising a master and one or more slaves

NOTE In this mode, two clock pulses are transmitted per address – one for input data and the other for output data.

3.1.34
multiplex channel number
integer between 0 and 15 which serves as an extension of the signal address of devices which support address multiplexing

NOTE Each multiplexed signal is assigned to a single multiplex channel, and is transmitted through the Seriplex controller-device interface during data frames in which the multiplex channel number broadcast by the clock source at the beginning of the data frame matches its assigned channel number.

3.1.35
node
logically active connection to the controller-device interface

NOTE 1 Typical nodes consist of a clock source or I/O devices.

NOTE 2 Passive connections such as T-junctions are not nodes.

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3.1.36
numeric signal
group of consecutive input or output data bits which together represent a single number or quantity

NOTE The allowable range of a numeric signal value is determined by the number of bits assigned to that signal, typically 8, 12, or 16, and usually assigned a starting signal address which is a multiple of 16 (0, 16, 32, ..., 240).

3.1.37
output propagation delay, t_{op}
time between a change in the logic state of an output signal within a Seriplex device and the corresponding change in state of its external output signal

3.1.38
output response time, t_{or}
a) in **peer-to-peer mode**, time between a signal's appearance on the controller-device interface and the corresponding change in state of an external output signal

b) in **master/slave mode**, elapsed time between a signal's assertion by the controller's internal logic processor (usually into an interface card's memory) and the corresponding change in state of an external output signal

3.1.39
output signal
signal which is received through the controller-device interface by a device other than a controller

3.1.40
peer-to-peer mode
mode 1

operating mode in which one device can control signals to any other device directly, without the intervention of a controller

NOTE In this mode, one clock pulse is transmitted per address, and input and output data are sampled at the same time.

3.1.41
Seriplex device
control or sensing apparatus which is electrically connected to the controller-device interface, including both clock sources and I/O devices

NOTE The term "device" refers collectively to the controller-device interface communications circuitry, to any other circuitry within the device, to any mechanical and/or electromechanical actuators which interface with the device circuitry and to the device's physical housing and electrical connectors.

3.1.42
Seriplex power supply
device which produces the d.c. voltage applied to the controller-device interface circuitry of Seriplex devices

NOTE Typically this power source is electrically isolated from any power sources used to activate control devices or sensors.

3.1.43
signal address
address
integer between 0 and 255 which identifies a single bit of Seriplex input or output data

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3.1.44
signal update time, t_u
time between successive transmissions of a particular signal through the Seriplex controller-device interface

NOTE For non-multiplexed signals, the signal update time is equal to the frame period. For multiplexed signals, the signal update time is equal to the frame period multiplied by the number of multiplex channels scanned by the clock source.

3.1.45
slave
Seriplex device that does not generate the controller-device interface clock signal

3.1.46
sync period, t_{sync}
pause in the Seriplex clock signal at the end of each data frame, causing all I/O devices to reset their address counters, and therefore synchronizing data transmission among devices

3.1.47
system response time, t_{sr}
elapsed time between an external input signal event and a resulting change in state of an external output signal

NOTE It includes input response time, output response time, controller processing time and I/O device propagation delays.

3.1.48
word
group of 16 bits of Seriplex input or output data assigned to consecutive signal addresses, with the starting address being an integer multiple of 16 (0, 16, 32, ..., 240)

3.2 Symbols and abbreviations

BFD	Bus Fault Detect
CDR	Complementary Data Retransmission
EUT	Equipment Under Test
N_{ch}	Number of multiplex channels scanned by the clock source
t_{bd}	BFD pulse delay
t_{bfd}	BFD pulse duration
t_{br}	BFD pulse recovery time
t_{ch}	Data line charge time
t_{clock}	Clock period
t_{closs}	Clock loss detection period
t_{dis}	Data line discharge time
t_{eof}	End of frame delay
t_f	Frame period
t_{hip}	Host interface input propagation delay
t_{hold}	Hold time after data sampling
t_{hop}	Host interface output propagation delay
t_{hr}	Controller response time
t_{ip}	Input device propagation delay
t_{ir}	Input response time

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t_{op}	Output device propagation delay
t_{or}	Output response time
t_{poff}	Data off propagation delay
t_{pon}	Data on propagation delay
t_{setup}	Set-up time before data sampling
t_{sr}	System response time
t_{u}	Signal update time
V_{h}	High level of the square wave data signal
V_{l}	Low level of the square wave data signal

4 Classification

4.1 General

Seriplex is usually applied at the lowest level in a multi-level automation hierarchy. Seriplex concentrates on the typical requirements to connect binary elements to a controller.

Seriplex can be used as an interface physically integrated into field devices, e.g. actuators, sensors, or other devices, allowing design of "intelligent" binary actuators, sensors or other devices and elements. Alternatively, Seriplex may be used in separate modules, each providing interfaces for conventional actuators, sensors or other devices and elements.

The Seriplex concept is independent of the specific field devices.

Connected devices may include:

– sensors (photoelectric switches, proximity sensors, and pushbuttons);
– actuators (valves and contactors);
– universal input/output modules;
– controllers (PLCs and personal computers);
– clock modules.

Cable topology may be of any type. Recommended topologies are daisy chain or trunk and drop, since their performance is the most predictable and easily characterized. Each drop length in a trunk and drop or loop system should be limited to less than 10 m.

The Seriplex cable consists of four or six individually insulated conductors surrounded by a foil shield, and housed within a single overall insulating jacket. The conductors of the four-core cable correspond to the power, common, clock, and data lines. In the six-core cable the two additional conductors (I/O+ and I/O–) are located outside the shield but within the outer jacket.

Both master/slave and peer-to-peer configurations are possible in Seriplex systems.

Clock rates may be up to 200 kHz.

Seriplex signal update time depends on the length of the data frame (from 16 to 256 addresses), the clock rate (10 kHz to 200 kHz), and the number of multiplex channels scanned (1 to 16).

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4.2 Frame period, t_f

A frame period is defined as the elapsed time between the end of successive sync periods while a Seriplex bus system is operating normally. Within a given system, the frame period is fixed and is determined by the designated frame length, clock rate, and sync period (t_{sync}).

For clock rates up to 100 kHz, assuming the sync period is eight clock periods in duration, the frame period can be calculated as

$$t_f = [(\text{mode} \times \text{frame length}) + 8]/\text{clock rate}$$

where

mode = 1 for peer-to-peer operation;

mode = 2 for master/slave operation.

For clock rates above 100 kHz, the sync period is normally 16 clock periods in duration, so the frame period is calculated as

$$t_f = [(\text{mode} \times \text{frame length}) + 16]/\text{clock rate}$$

As the formula indicates, the frame period can be reduced either by shortening the frame length or by increasing the clock rate.

4.3 Signal update time, t_u

Signal update time is defined as the elapsed time between successive transmissions of a particular signal through the Seriplex CDI. The longest signal update time for any signal within a given system also defines the time required to update all the CDI data within that system. For non-multiplexed signals, the signal update time equals the frame period:

$$t_u = t_f$$

For multiplexed signals when no priority channels are designated, the signal update time equals the frame period times the number of multiplex channels scanned by the clock source (N_{ch}):

$$t_u = t_f \times N_{ch}$$

If a multiplexed priority channel is designated, the calculations are modified as follows.

For a priority channel:

$$t_u = t_f \times 2$$

For non-priority channels:

$$t_u = t_f \times 2 \times (N_{ch} - 1)$$

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4.4 Input response time, t_{ir}

In peer-to-peer mode, input response time is defined as the elapsed time between an external input signal event and that signal's appearance on the Seriplex CDI. Since the timing of the input event need not be synchronized with the operation of the Seriplex CDI, the maximum input response time for a given signal is primarily determined by the signal update time. The propagation delay (t_{ip}) of the input device also affects the input response time, although this factor is usually negligible compared to the signal update time:

$$t_{ir} = t_u + t_{ip}$$

This formula is true for both multiplexed and non-multiplexed signals.

In master/slave mode, input response time is defined as the elapsed time between an external input signal event and that signal's availability to a controller's internal logic processor. In the case of a typical backplane interface, this would be the time from the input event until new input data is posted in the interface's dual-port memory for use by application software. Master/slave input response time is determined by the propagation delay (t_{ip}) of the input device, the signal update time (t_u), the propagation delay (t_{hip}) of the host interface, and whether input data is posted immediately when received or withheld until completion of bus fault detection (BFD) checks.

The input response time formula for immediately posted data is

$$t_{ir} = t_{ip} + t_u + t_{hip}$$

Since input propagation delay can usually be disregarded, and the propagation delay for typical CPU interface cards is approximately 32 clock periods in master/slave mode, the complete calculation for input response time is usually performed as follows:

$$t_{ir} = [(2 \times \text{frame length} + 8) \times N_{ch} + 32]/\text{clock rate}$$

NOTE 1 For clock rates >100 kHz, the factor of 8 in the above formula changes to 16 or to some other value specified by the interface manufacturer.

NOTE 2 For non-multiplexed signals, $N_{ch} = 1$.

If data posting is withheld until BFD checks are completed, an extra delay (t_{eof}) from the time the signal is reported on the Seriplex bus until the end of the following sync period is introduced. This end-of-frame delay is determined by the frame length and the signal's address (input_addr):

$$t_{eof} = [(2 \times \text{frame length} + 8) - (2 \times \text{input\_addr})]/\text{clock rate}$$

Therefore the complete input response time formula becomes:

$$t_{ir} = t_{ip} + t_u + t_{hip} + t_{eof}$$

Under the assumptions given above, this would be calculated as

$$t_{ir} = [(2 \times \text{frame length} + 8) \times N_{ch} + 32 + (2 \times \text{frame length} + 8) - (2 \times \text{input\_addr})]/\text{clock rate}$$

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which can be simplified to

$$t_{ir} = [(2 \times \text{frame length} + 8) \times (N_{ch} + 1) + 32 - (2 \times \text{input\_addr})]/\text{clock rate}$$

NOTE 3 For clock rates > 100 kHz, the factor of 8 in the above formula changes to 16 or to some other value specified by the interface manufacturer.

NOTE 4 For non-multiplexed signals, $N_{ch} = 1$.

If digital debounce is used, input response time can still be calculated by the same formula. In this case, the selected number of data samples (2 or 3) should be substituted for the number of multiplex channels (N_{ch}).

Digital debounce and address multiplexing shall not be used simultaneously for the same signal.

4.5 Output response time, t_{or}

In peer-to-peer mode, output response time is defined as the elapsed time between a signal's appearance on the Seriplex CDI and the corresponding change in state of an output device's external output signal.

Since Seriplex output devices hold output data until a valid BFD check is made before passing the data on to the physical outputs, the primary component of peer-to-peer output response time is the end-of-frame delay (t_{eof}) from the time the signal is reported on the Seriplex CDI until the end of the following sync period. The propagation delay (t_{op}) of the output device also affects the output response time, although this factor is usually negligible compared to the end-of-frame delay:

$$t_{or} = t_{eof} + t_{op}$$

where

$$t_{eof} = (\text{frame length} + 8 - \text{output\_addr})/\text{clock rate}$$

NOTE 1 For clock rates >100 kHz, the factor of 8 in the above formula changes to 16 or to some other value specified by the interface manufacturer.

NOTE 2 This formula applies to both multiplexed and non-multiplexed signals.

If digital debounce is used, output response time becomes:

$$t_{or} = t_{eof} + t_{op} + (\text{deb\_lgth} \times t_u)$$

where deb_lgth is the selected debounce length for the signal; the number of identical data samples (2 or 3) required before the corresponding output changes state.

Digital debounce and address multiplexing shall not be used simultaneously for the same signal.

In master/slave mode, output response time is defined as the elapsed time between a signal's assertion by the controller's internal logic processor (usually into a backplane interface's dual-port memory) and the corresponding change in state of an external output signal.

Since the writing of output data into a backplane interface's dual-port memory is not synchronized with the operation of the Seriplex CDI, the maximum output response time for a given signal is primarily determined by the signal update time. There is also an end of frame delay (t_{eof}) as described for peer-to-peer output response time. Finally, the propagation delays of both the host interface (t_{hop}) and the output device itself (t_{op}) contribute to the total output response time.

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The complete output response time formula is

$$t_{or} = t_u + t_{hop} + t_{eof} + t_{op}$$

Since output propagation delay can usually be disregarded, and the host propagation delay for typical CPU interface cards is approximately 32 clock periods in master/slave mode, the complete calculation for output response time is usually performed as follows:

$$t_{or} = [(2 \times \text{frame length} + 8) \times N_{ch} + 32 + (2 \times \text{frame length} + 8) - (2 \times \text{output\_addr})]/\text{clock rate}$$

which can be simplified to

$$t_{or} = [(2 \times \text{frame length} + 8) \times (N_{ch} + 1) + 32 - (2 \times \text{output\_addr})]/\text{clock rate}$$

NOTE 3 For clock rates > 100 kHz, the factor of 8 in the above formula can change to 16 or to some other value specified by the interface manufacturer.

NOTE 4 For non-multiplexed signals, $N_{ch} = 1$.

If digital debounce is used, output response time can be calculated using the same formula. In this case, the debounce length (deb_lgth) of 2 or 3 data samples should be substituted for the number of multiplexed channels (N_{ch}).

Digital debounce and address multiplexing shall not be used simultaneously on the same signal.

4.6 System response time, t_{sr}

Seriplex CDI system response time is defined as the elapsed time between an external input signal event and a resulting change in state of an external output signal.

For the Seriplex CDI peer-to-peer mode, system response time is simply the sum of input response time and output response time:

$$t_{sr} = t_{ir} + t_{or}$$

This formula can be expanded to

$$t_{sr} = t_{ip} + t_u + t_{eof} + t_{op}$$

Disregarding input and output propagation delays as before, this formula is typically calculated using the formula:

$$t_{sr} = [(\text{frame length} + 8) \times N_{ch} + (\text{frame length} + 8) - \text{output\_addr}]/\text{clock rate}$$

which can be simplified to

$$t_{sr} = [(\text{frame length} + 8) \times (N_{ch} + 1) - \text{output\_addr}]/\text{clock rate}$$

NOTE 1 For clock rates > 100 kHz, the factor of 8 in the above formula changes to 16 or to some other value specified by the clock source manufacturer.

NOTE 2 For non-multiplexed systems, $N_{ch} = 1$.

If digital debounce is used, system response time can still be calculated by the same formula. In this case, the debounce length (deb_lgth) of 2 or 3 data samples should be substituted for the number of multiplexed channels (N_{ch}).

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Digital debounce and address multiplexing shall not be used simultaneously on the same signal.

For Seriplex master/slave mode systems, system response time factors include controller processing time t_{hr} as well as input response time t_{ir} and output response time t_{or}:

$$t_{sr} = t_{ir} + t_{hr} + t_{or}$$

Disregarding input and output propagation delays, this formula is calculated as:

$$t_{sr} = [2 \times (2 \times \text{frame length} + 8) \times (N_{ch} + 1) + 64 - (2 \times \text{input\_addr}) - (2 \times \text{output\_addr})]/\text{clock rate} + t_{hr}$$

If digital debounce is used, system response time can still be calculated by the same formula. In this case, the debounce length (deb_lgth) of 2 or 3 data samples should be substituted for the number of multiplexed channels (N_{ch}).

Digital debounce and address multiplexing shall not be used simultaneously on the same signal.

Controller processing time is outside the scope of this standard, and is dependent on a wide variety of factors including processor type and speed, control program type and size, and data polling methods.

5 Characteristics

5.1 System overview

A Seriplex system consists of the following elements, as shown in figure 1:

– controller-device interface cable;
– clock source;
– input and output (I/O) devices;
– Seriplex power supply(ies);
– control power supply(ies);
– controller (optional).

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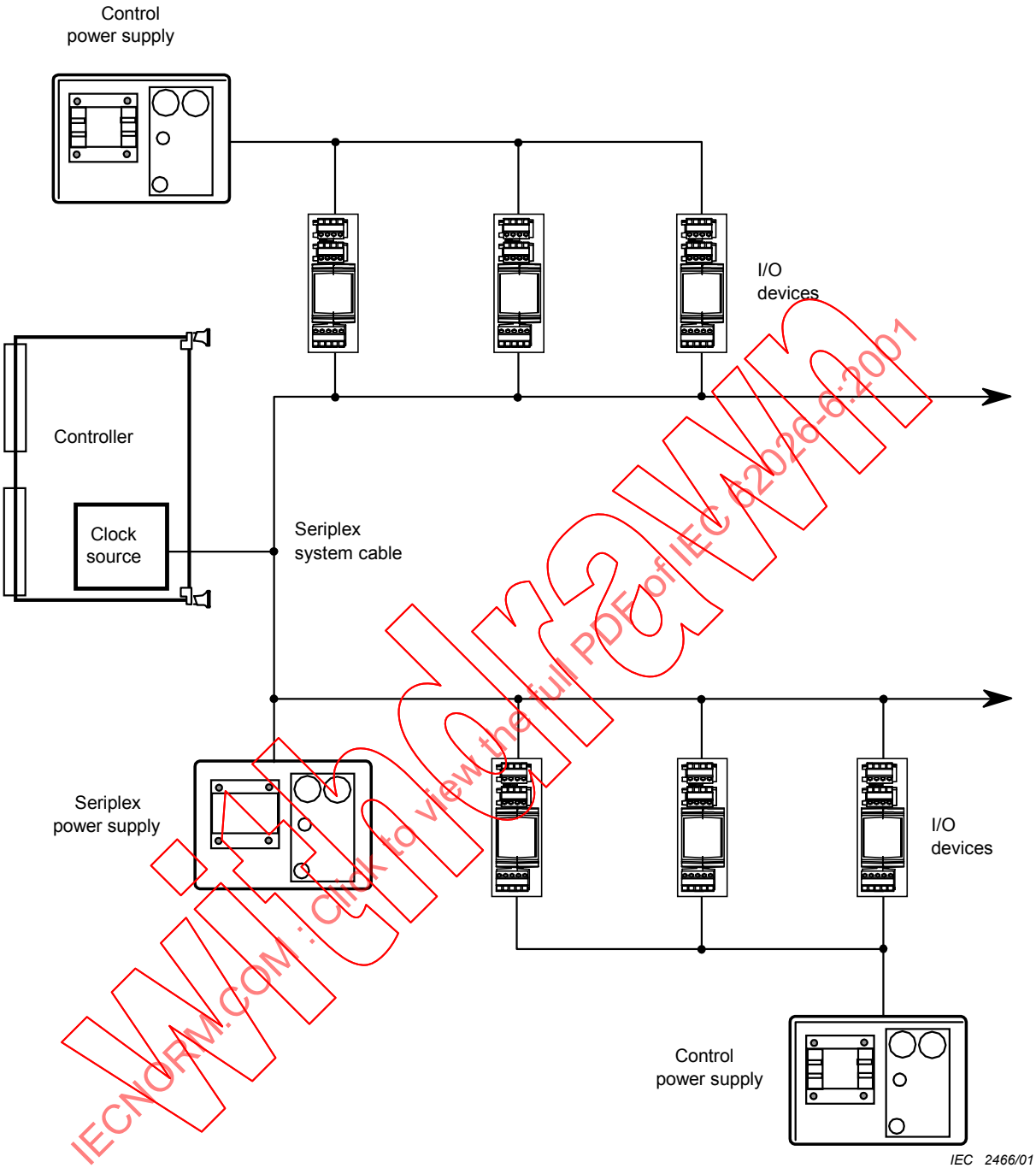

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Figure 1 – Seriplex controller-device interface system diagram

The controller-device interface cable conducts Seriplex power and signals among the various system elements. It consists of four insulated conductors, surrounded by a shield and an outer insulating jacket. Two of the wires conduct Seriplex power, while the other two conduct a clock and a data signal which are used to transmit data among system devices. A six-core cable can be used in which the two additional conductors (I/O+ and I/O–) are located outside the shield but within the outer jacket.

The clock source generates the controller-device interface clock signal which is used to synchronize data transfer among system devices. It also provides a current source for the data signal, so that this signal assumes a normally-high logic state. The clock source periodically transmits a Bus Fault Detect (BFD) pulse which is used by input and output devices to validate the operational status of the controller-device interface; the clock source also makes use of this pulse to monitor and report fault conditions. The clock source may either be a "passive" device providing controller-device interface arbitration, or it may be a master or controller providing centralized control and reporting of all controller-device interface data.

I/O devices carry out the physical activities of a control system. They may be simple devices such as switches and lamps, or complex such as operator interface terminals and motion controllers. Input devices sense external conditions and report them to the controller-device interface, while output devices perform some action based on controller-device interface data.

The Seriplex power supply provides power for the controller-device interface itself; that is, for the controller-device interface circuitry within each device. The Seriplex power supply provides a 24 V d.c. source for the controller-device interface. Multiple Seriplex power supplies may be used within a single system.

NOTE 1 In general, the Seriplex power supply does not provide power to monitoring and control devices, so that an I/O fault would not cause a controller-device interface supply failure and in turn halt the operation of the controller-device interface.

NOTE 2 Control power supplies provide power for I/O circuitry such as sensors and actuators. Although this type of power supply may also connect directly to Seriplex I/O devices, in general such supplies are electrically isolated from the Seriplex power supply. This is so that control faults such as a short-circuit load do not affect the operation of the controller-device interface itself, although they may trip circuit breakers or otherwise remove power from the control devices.

NOTE 3 A controller typically consists of a combination of hardware and software, such as a personal computer or programmable controller, and provides centralized reporting and control of data. A controller usually operates a controller-device interface in the master/slave mode, meaning that all input data is reported exclusively to the controller, and that the controller has exclusive control over the states of all output signals.

Controller-device interface data is transmitted through the clock and data signals. Each data transmission frame is defined by a series of pulses on the clock line, bounded by a sync period during which the clock line remains inactive for a defined period of time. Each device on the controller-device interface counts the clock pulses, and the state of the data line during a particular clock period defines the value of a corresponding data signal bit (see figure 2).

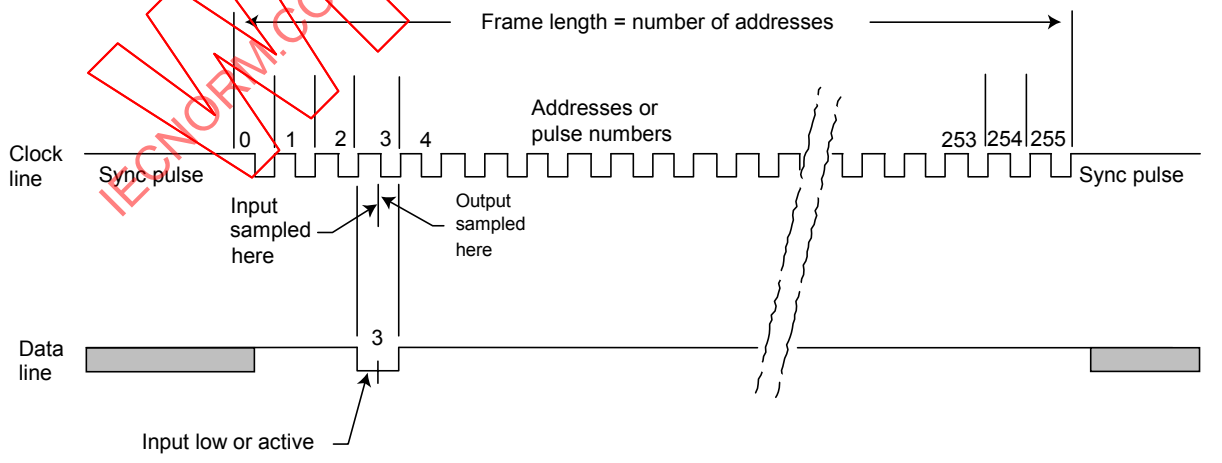

Figure 2 – Peer-to-peer timing diagram

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Each discrete I/O device on the controller-device interface is assigned an address. In the peer-to-peer mode, this signal address corresponds directly to the sequence of the clock pulses. For example, input device 17 asserts its signal value on the data line during clock pulse 17. Correspondingly, output device 17 monitors the data line during clock pulse 17 to determine whether it should be on or off until the next time its signal is presented to the controller-device interface. In this way, input devices directly control output devices without intervention by a host controller such as a computer or programmable logic controller (PLC).

Devices may be assigned multiple signal addresses in order to form a multi-bit signal value. For example, 16 consecutive bits could be assigned to an analogue input device such as a flow meter; these bits would then represent a 16-bit binary number which could be read and used by another device.

In the master/slave mode, there are two clock pulses per signal address instead of one as in the peer-to-peer mode (see figure 3). During the first clock pulse for each address, input data is transmitted from a device to a controller such as a computer or PLC. During the second clock pulse, the controller transmits output data to devices. This logically separates input signals from output signals at the same address, and allows the host controller to make all control decisions and to have exclusive control over the state of all output signals.

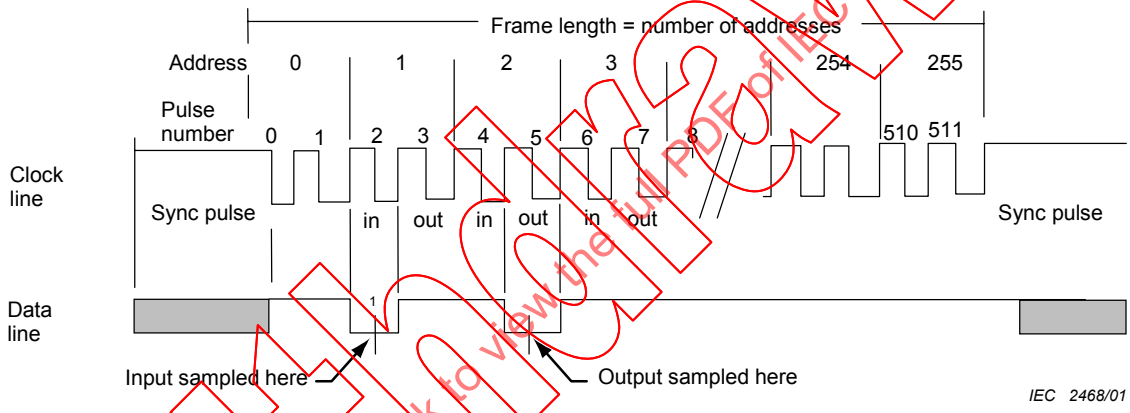

Figure 3 – Master/slave timing diagram

The maximum number of signal bits which may be transmitted within a single data frame is 255 in peer-to-peer mode and 510 in master/slave mode (address 0 is not used). However, the peer-to-peer mode still supports 510 I/O devices because each signal acts as both an input and an output signal. Signal capacity may be increased by address multiplexing in which multiplexed devices are assigned the same signal addresses. This is accomplished by using output signals 1 through 4 as a binary number which indicates a "multiplex channel" between 0 and 15 (see figure 4). A single multiplex channel is scanned in each data frame. Remote I/O devices may be assigned to an individual multiplex channel. These devices monitor the multiplex channel indication to determine whether to assert or receive their signals within a particular data frame.

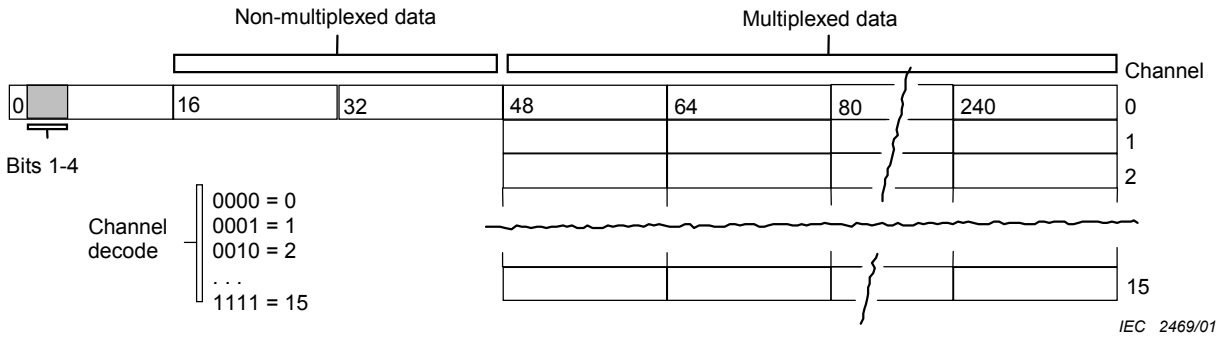

Figure 4 – Example of address multiplexing

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Seriplex signal update time depends on the length of the data frame (from 16 to 256 addresses), the clock rate (10 kHz to 200 kHz), and the number of multiplex channels scanned (1 to 16).

The Seriplex clock and data signal amplitude is 12 V d.c. nominal. The data signal is low-true, meaning that a low logic level corresponds to a value of 1, with high corresponding to 0. In its “resting” state, the data line is pulled high by the clock source. Any device asserts its input signals by either pulling the data line low during the proper clock pulse to indicate a 1, or by leaving the data line high to indicate a 0. With this method, "wire-OR" logic may be used; that is, multiple devices may be assigned to a given input signal and any of them may assert a 1 to override the 0s asserted by the other devices. Similarly, multiple output devices may be assigned to the same address, and will respond to the same output signal value. In this way the I/O capacity of the controller-device interface may increase to more than 510 devices per data frame.

5.2 Frequency, cable length and node count

The relationship between clock rate, node count, and cable length is governed by two limiting factors; voltage drop through the cable, and cable transmission effects. The two primary transmission effects are propagation delay and bulk capacitance of both the cable and the connected devices.

Table 1 and table 2 both show the maximum allowable operating frequency for a given bus node count and cable length, under different conditions. In both cases the following assumptions are made:

– cable type = 1622P16;

– I/O device capacitance = 75 pF;

– I/O device current consumption = 17 mA;

– ambient temperature = 25 °C.

Table 1 assumes that the clock source and a single bus power supply are located at the same end of the bus cable, and that all nodes are connected directly to the trunk cable (drop length = 0) and distributed evenly along the length of the cable. In this case the voltage drop in the cable is the primary limiting factor.

Table 1 – Maximum available clock frequency for valid networks (single power supply)

Cable length	Number of nodes							
M	5	10	20	50	100	200	500	1 000
25	150 kHz	125 kHz	75 kHz	50 kHz	20 kHz	—	—	—
50	125 kHz	100 kHz	64 kHz	—	—	—	—	—
100	75 kHz	64 kHz	32 kHz	—	—	—	—	—
200	64 kHz	32 kHz	—	—	—	—	—	—
500	25 kHz	—	—	—	—	—	—	—
1 000	—	—	—	—	—	—	—	—
2 000	—	—	—	—	—	—	—	—
3 000	—	—	—	—	—	—	—	—

Table 2 assumes that the clock source is at one end of the bus cable, that all nodes are connected directly to the trunk cable (drop length = 0) and that multiple power supplies are distributed throughout the bus as necessary to ensure that the cable voltage drop is limited to that caused by the 30 mA data line current. In this case, cable transmission effects limit the operating frequency.

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Table 2 – Maximum available clock frequency for valid networks (multiple power supplies)

Cable length	Number of nodes							
m	5	10	20	50	100	200	500	1 000
25	192 kHz	167 kHz	167 kHz	125 kHz	75 kHz	50 kHz	25 kHz	16 kHz
50	167 kHz	150 kHz	150 kHz	100 kHz	75 kHz	50 kHz	25 kHz	16 kHz
100	150 kHz	125 kHz	125 kHz	100 kHz	75 kHz	50 kHz	25 kHz	16 kHz
200	100 kHz	100 kHz	100 kHz	75 kHz	64 kHz	50 kHz	25 kHz	10 kHz
500	64 kHz	64 kHz	64 kHz	50 kHz	50 kHz	32 kHz	20 kHz	10 kHz
1 000	32 kHz	32 kHz	32 kHz	32 kHz	32 kHz	32 kHz	20 kHz	10 kHz
2 000	25 kHz	20 kHz	20 kHz	20 kHz	20 kHz	20 kHz	10 kHz	10 kHz
2 810	16 kHz	16 kHz	16 kHz	16 kHz	16 kHz	10 kHz	10 kHz	—

The capacity of most applications will fall somewhere between the values given in these tables. The values given in these tables can be increased or decreased by altering the cable topology (for example, placing the clock source in the middle of the trunk) or the parameters of the cable and devices.

5.3 Data transmission

5.3.1 General

The controller-device interface may operate in either of two modes; master/slave or peer-to-peer. In the master/slave mode, data is exclusively controlled by a "master" device; that is, all input data is reported exclusively to the master, and the master has exclusive control over the states of all output signals, with all I/O devices acting as "slaves". In the peer-to-peer mode, input and output data is shared directly among devices. Although a controller may be used in either operating mode, a controller would usually be used as a master device.

5.3.2 Peer-to-peer mode data transmission

In the peer-to-peer operating mode, input and output data may be shared directly among devices. Although a master may be used in this mode, it would not necessarily have exclusive control of output data, nor would it have exclusive access to input data. More typically in the peer-to-peer mode, a simple clock source would be used to provide controller-device interface arbitration functions, but this device would not perform supervisory control. See figure 5 for the signal transmission format.

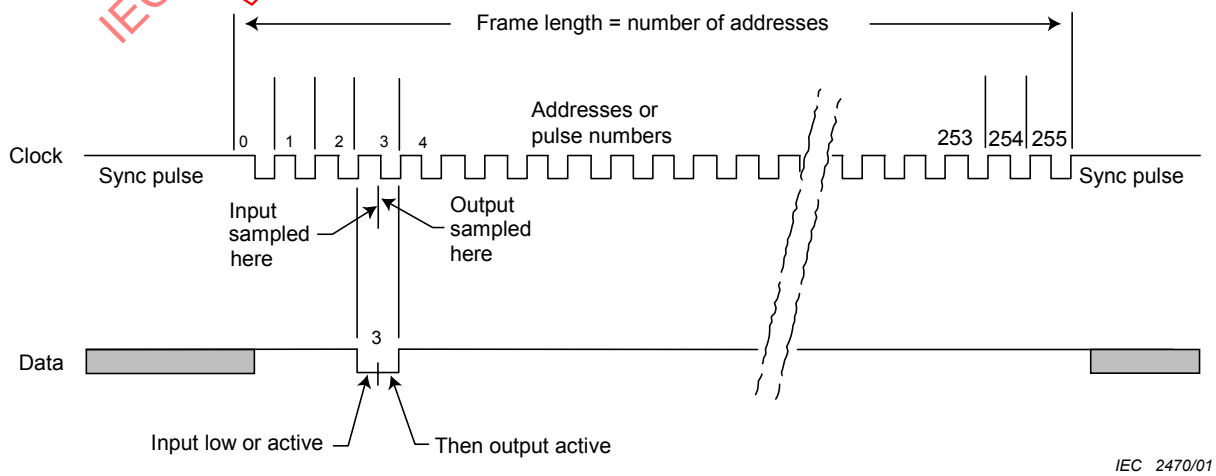

Figure 5 – Peer-to-peer transmission format

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Seriplex data is transmitted by means of the clock and data signals. Normal controller-device interface operation consists of a scanning process, wherein "frames" of data are transmitted repeatedly, so that all data signals are updated periodically at a set frequency. Each data transmission frame is defined by a series of pulses on the clock line, separated by sync periods during which the clock line remains inactive.

Each clock period corresponds to a signal address. In the peer-to-peer mode, each signal address corresponds to exactly one bit of information. Addresses are numbered from 0 to 255; clock pulses are numbered correspondingly. After each sync period, a new series of clock pulses is transmitted starting with pulse number 0, and continuing incrementally until the data frame is complete and the next sync period is begun. During each clock period, the corresponding data signal is reported to the controller-device interface through the data line. The data line normally rests at a high logic level, which corresponds to a data value of 0; a device may pull the data line low during a clock period to assert a data value of 1 for the corresponding signal address.

Every device which communicates through the Seriplex controller-device interface is assigned at least one signal address. Devices may be assigned multiple signal addresses; in fact a controller may be considered to be assigned to every available signal address. A device's assigned addresses may or may not be contiguous, but individual multi-bit data values (for instance, a 16-bit analogue signal) shall be assigned at least enough contiguous addresses to accommodate their value range.

In the peer-to-peer mode, each address used shall be assigned to at least one input device and one output device for communication to occur. Every bit of data sent through the controller-device interface shall be received by some device; otherwise, transmission of that bit serves no control purpose. In some cases a controller may be the only designated sender or receiver of a given data signal. To arrange direct control of an output device by an input device, those devices are assigned the same address (or addresses).

Each device on the controller-device interface counts the clock pulses within each data frame and monitors and/or controls the state of the data line during the clock periods corresponding to its assigned signal addresses. During clock periods which do not correspond to its assigned signal addresses, a Seriplex device does not attempt to pull the data line low, nor is its operation affected by the state of the data line.

Address 0 shall not be used by any Seriplex device. Therefore, the maximum data capacity within a single peer-to-peer mode data frame is 255 bits. Since each address is used as both an input and an output signal, this represents an I/O capacity of 255 discrete (that is, single-bit) inputs and 255 discrete outputs, for a total of 510 I/O devices.

5.3.3 Master/slave mode transmission

In the master/slave operating mode, data is exclusively controlled by a master device. All input data is reported exclusively to the master, and the master has exclusive control over the states of all output signals, with all I/O devices acting as slaves. In almost all cases, master/slave mode systems use a controller, which acts as both the clock source and as the master device. Figure 6 shows the master/slave transmission format.

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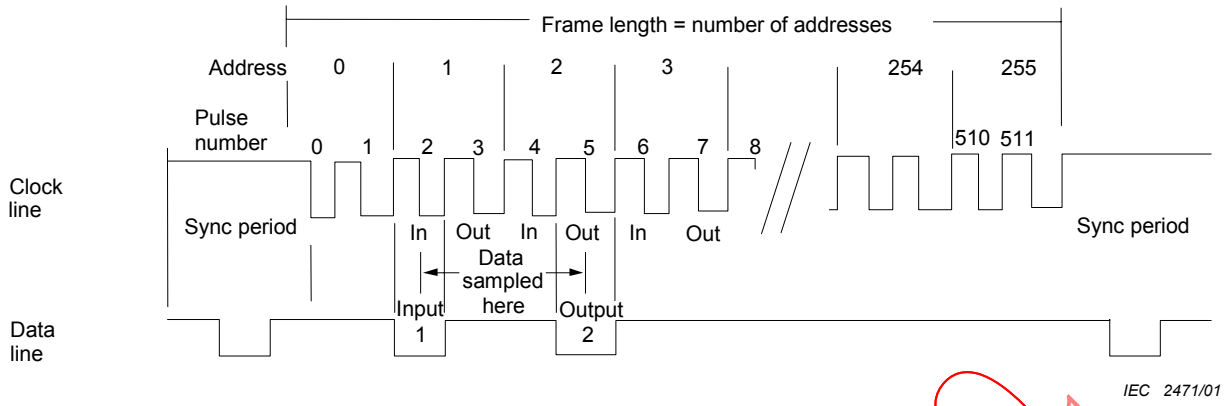

Figure 6 – Master/slave mode data transmission format

Master/slave mode data transmission is similar to that of the peer-to-peer mode in most respects. The most significant difference is that in the master/slave mode, there are two clock pulses per signal address instead of one as in the peer-to-peer mode. During the first clock pulse for each address, the corresponding input signal is reported, and the corresponding output signal is reported during the second clock pulse. In this mode, Seriplex devices divide the number of clock pulses by two to determine the currently active signal address.

Since Seriplex input and output signals are reported at different times, input signals do not exert direct control over output signals which share the same address, as they would in peer-to-peer mode; in fact, such input/output signal pairs may be completely unrelated in the control logic. This is true even if the input and output signals which share an address reside within the same Seriplex device. In master/slave mode, the state of output signals is exclusively under the control of the master. However, masters may include a "pass-through" feature to logically link input and output signals at the same address, so that peer-to-peer mode operation can be imitated for any or all signal addresses.

This logical separation of controller-device interface input signals and output signals at the same address allows the master to make all control decisions and to have exclusive control over the state of all output signals. That is, all input data is reported exclusively to the master; although slave devices report input data, they do not monitor the states of input signals. All controller-device interface output data is transmitted exclusively by the master; slave devices may monitor output data signals, but they do not produce them.

All other aspects of master/slave mode data transmission are identical to those of peer-to-peer mode. There are still 255 addresses available, although each address now corresponds to two separate logic signals; an input signal and an output signal.

Since the master/slave mode uses two clock pulses per address, it takes approximately twice as long to scan the same number of I/O addresses. Note, however, that the I/O capacity is the same as for peer-to-peer mode; 255 discrete inputs and 255 discrete outputs.

5.4 General data transmission features

5.4.1 Address multiplexing

The following subclauses describe operational characteristics of data transmission which are applicable to both peer-to-peer and master/slave operating modes.

The maximum data capacity of a single non-multiplexed data frame is 255 input bits and 255 output bits. While this is a considerable capacity for discrete I/O devices, the number of analogue signals within a single frame is limited to 15 (16-bit) inputs and 15 outputs, which is not sufficient for some applications.

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Address multiplexing is a means of expanding the data capacity of a Seriplex controller-device interface. It effectively extends the addressing range of the controller-device interface from an 8-bit number to a 12-bit number, resulting in an increase of the data capacity in a single controller-device interface from 510 signal bits to 7 680 signal bits.

In address multiplexing, multiple devices share the same signal addresses. Individual signals at the shared addresses are distinguished by assigning each to one of 16 unique multiplex channels. Each data frame transmits data for a single multiplex channel.

Multiplexed devices monitor the multiplex channel indication at the beginning of each data frame and determine whether it matches the assigned channel number. If a device's assigned channel is being scanned, that device reads and writes data normally. However, if the current channel does not correspond to that device's assigned channel, the device ignores output data and does not transmit its input data within that data frame.

The currently active multiplex channel is indicated by the clock source through output signals 1 through 4. These four signals form a binary number which indicates a multiplex channel between 0 and 15, with output 1 indicating the least-significant bit of the channel number. Multiplexed devices compare the value of these 4-bits to their assigned multiplex channels to determine whether their signals will be active within that data frame. See figure 4 for multiplex channel format.

Address multiplexing is performed on "words" composed of 16 contiguous addresses, located at 16-bit address boundaries (16-31, 32-47, …, 240-255). In order to multiplex any individual address, the entire 16-bit word in which it resides shall be multiplexed.

The word starting at address 0 is not multiplexed since the multiplex channel indication is contained within that word. This leaves 15 multiplexable address words. In master/slave mode, there are 15 multiplexable input data words and 15 multiplexable output data words. This supports a total of 480 multiplexed data words (15 words × 16 channels × 2 input/output), or 7 680 individual data bits.

If address multiplexing is used within a system, it is not necessary to multiplex all addresses. Multiplexing may be selected for individual words and not selected for others. There are no restrictions or requirements for which words are multiplexed within a system. In master/slave mode, input and output words may be multiplexed differently. For example, input word 16-31 may be multiplexed even if output word 16-31 is not.

Non-multiplexed devices simply ignore the multiplex channel indication and report and receive their data within every data frame. Multiplexed and non-multiplexed signals shall not share the same addresses, since this would result in data contention during multiplex channels assigned to multiplexed signals.

Since multiplexed signals are only updated during data frames which correspond to their assigned multiplex channels, multiplexed signal update time is related to the number of multiplex channels and the order in which they are scanned. The update time for multiplexed signals is typically calculated as [(frame time) × (number of multiplex channels)], although some applications may vary from this formula. Non-multiplexed signals are still updated once per data frame, even in systems which use address multiplexing at other signal addresses.

Although in a typical system multiplex channels are scanned in ascending numerical order and then repeated, there are no set requirements on the order of multiplex channel scanning. Multiplex channel scan order may be customized within an application to allow prioritizing of signal update times. For instance, a controller may support a "priority channel" which is scanned every second data frame, while other multiplex channels are scanned in ascending numerical order in between each priority channel frame.

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Any number of multiplex channels may be used within a system, up to the maximum of 16. Multiplexing may be implemented using sequential channels, e.g. 1, 2, and 3 or non-sequential channels, e.g. using channels 2, 5 and 8.

Seriplex systems which use address multiplexing cannot assign output signals 1 through 4 to any I/O device, since these bits are used for multiplex channel indication. The recommended practice is to avoid assigning any address within the first word (addresses 0 through 15) to any I/O device, except for dedicated functions (CDR input, outputs 5 – 8) described in 5.6.6.2 and 5.9.1.3.

Each multiplexed signal is assigned to a single multiplex channel. However, an I/O device that transmits and/or receives multiple signals may have different signals assigned to different multiplex channels. For example, a 4-point analogue input module may have each of its four signals assigned to addresses 48 through 63, with individual signals assigned to multiplex channels 0, 1, 2, and 3.

5.4.2 Sync period

The sync period is a period of inactivity on the clock line, which is detected by all devices and used to reset their internal address counters at the start of each data frame. It is measured from the positive (low-to-high) clock signal transition at the end of a data frame to the negative (high-to-low) clock transition which begins the next data frame (see figure 7).

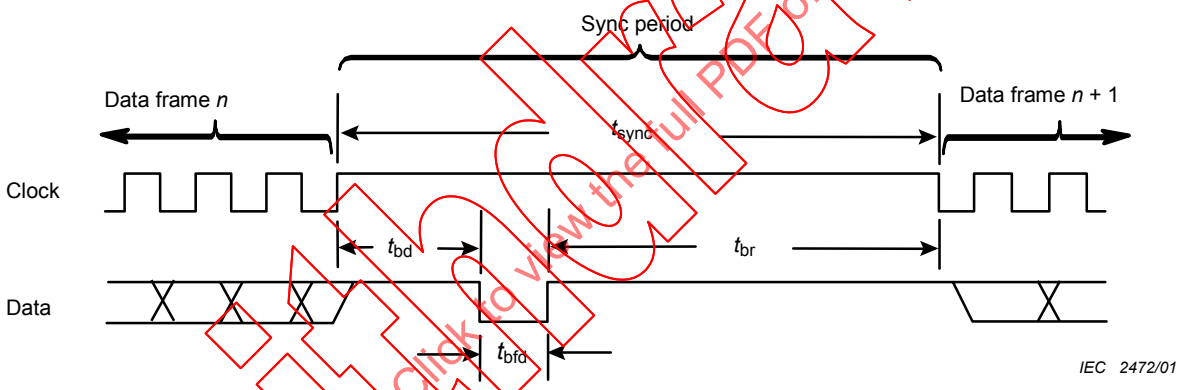

Figure 7 – Sync period diagram

Sync period parameters are shown in table 3.

Table 3 – Sync period parameters

Symbol	Parameter	Value		
		Minimum	Nominal	Maximum
t_{clock}	Clock period		1/clock rate	
t_{sync}	Sync period duration	82 µs [a]	8,5 * t_{clock} (≤100 kHz) 16,5 × t_{clock}(>100 kHz)	1 ms [b]
t_{bfd}	BFD pulse duration	2 × t_{clock} – 0,5 µs	2 × t_{clock}	–
t_{bd}	BFD pulse delay time	t_{clock} – 0,5 µs	t_{clock}	–
t_{br}	BFD pulse recovery time	2 × t_{clock} – 0,5 ms	–	–

[a] Minimum t_{sync} is 82 µs or 8,5 × t_{clock}, whichever is longer.

[b] Maximum t_{sync} is 1 ms or 16,5 × t_{clock}, whichever is shorter.

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The timing of the sync period is controlled by the clock source. Once all clock pulses for a given data frame have been completed, the clock source holds the clock line high for the duration of the sync period.

The minimum allowable sync period duration is 8,5 clock periods or 82 µs, whichever is longer. The maximum allowable duration is 16,5 clock periods or 1 ms, whichever is shorter. These minimum and maximum durations are selected to ensure that I/O devices can reliably detect the presence of a sync period over the clock rate range of 10 kHz to 200 kHz, without interpreting the inactivity as a loss of the controller-device interface clock signal.

The recommended practice for sync period duration is 8,5 clock periods for clock rates up to 100 kHz, and 16,5 clock periods for clock rates greater than 100 kHz.

Upon detection of a sync period, I/O devices shall reset their address counters to 0 in preparation for the next data frame, and monitor the data line for the presence of a Bus Fault Detection pulse to determine their appropriate output responses upon the end of the sync period.

5.4.3 Bus Fault Detection pulse

The Bus Fault Detection (BFD) pulse is a negative pulse on the data line during the sync period, which is used by both the clock source and I/O devices to determine the "health" of the controller-device interface. See t_{bfd} in figure 7.

As at other times, the controller device interface data line rests at a normally high logic state during the sync period. During each sync period, the clock source pulls the data line low and then releases it high again before the end of the sync period to create the BFD pulse.

The clock source shall monitor the data line during and after the BFD pulse to determine whether the data line can be driven to both high and low logic states. If the data line fails to reach either the low or the high logic state, the clock source shall recognize a controller-device interface fault and shall halt the operation of the clock signal.

Each I/O device on a Seriplex controller-device interface monitors for the presence of the BFD pulse during each sync period. If the BFD pulse is detected and the sync period ends normally, the I/O device can presume that the controller-device interface is operating properly and allow output data received during the previous data frame to be transmitted to its external output signals, subject to any other fault detection mechanisms which the device employs. If the device fails to detect a BFD pulse during a sync period, the device shall recognize a bus fault condition and its external output signals shall revert to their default or "shelf" state.

The BFD pulse shall fall entirely within a sync period. Its transition from a high to a low logic state shall occur after the clock line has reached the high logic state at the start of the sync period and after the minimum BFD pulse delay time has elapsed. Its transition from low to high shall precede the clock line's first transition from high to low at the start of the subsequent data frame by at least the minimum BFD pulse recovery time.

The BFD pulse duration and its position within the sync period may be freely defined within the ranges specified in table 3. It is recommended however that the BFD pulse should be exactly two clock periods in duration, and should occur during the second and third equivalent clock periods within the sync period.

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5.4.4 Frame length

Frame length is the number of addresses scanned within a data frame. That is, the frame length sets the number of individual input or output signal bits which are reported within a data frame.

The frame length may be any number up to a maximum of 256, corresponding to the maximum number of addresses available on the controller-device interface. Frame length shall be a multiple of 16 (16, 32, 48, ..., 240, 256) and the frame length shall be constant within a given system.

In the peer-to-peer mode, the frame length is equal to the number of clock pulses produced within a data frame. In the master/slave mode, the number of clock pulses is twice the frame length. Therefore the frame length directly affects signal update time, since it determines the duration of a data frame for a given clock rate.

The number of available addresses within a data frame is (frame length – 1), since address 0 is not usable. For instance, a frame length of 64 supports up to 63 input signal bits and 63 output bits.

5.4.5 Clock rate

The clock rate is the frequency at which clock pulses are transmitted during the data transmission portion of a data frame. This may be any value between 10 kHz and 200 kHz. Recommended nominal values (in kHz) are 10, 12, 16, 20, 25, 32, 50, 64, 75, 100, 125, 150, 167 and 192 kHz.

For a given frame length, the clock rate determines the duration of a data frame, and so determines signal update and response times. The clock rate also affects the number of I/O devices which may be connected to a single Seriplex cable, and the total cable length within a system, by establishing the maximum allowable charging time of the Seriplex data line (see 5.5).

NOTE The definition of clock rate excludes the sync period portion of a data frame. Therefore, direct measurement of the clock rate by a frequency counter connected to the Seriplex clock line might produce an inaccurate value, since the presence of sync periods reduces the observed frequency.

5.4.6 Data length

The length of a data signal transmitted through a controller-device interface may range from a single bit up to 255 bits. Recommended signal data lengths are 1, 2, 4, 8, 16, or any multiple of 16 bits up to 240.

A signal longer than 1 bit shall be assigned at least as many contiguous addresses as are required to accommodate the data value in binary form. If the assigned address space exceeds the data length, unused bits within the address space should be assigned a value of 0 by the signal-producing device.

5.4.7 Address sharing

Multiple Seriplex devices may be assigned to the same signal address or addresses. In fact, in the peer-to-peer mode at least two devices (one input device and one output device) shall be assigned to a signal address for the associated signal to perform any useful communication.

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In addition to input/output signal pairs, multiple input devices may also share an address. In this way, any of several input devices may produce the same input signal. The input signal is the logical OR combination of all input devices assigned to that address; this is frequently referred to as a "wire-OR" logic function. The recommended practice is to assign only discrete (single-bit) signals to a shared address; multi-bit signals (such as analogue values) should not share addresses except as allowed under the rules for address multiplexing.

Similarly, multiple output devices may also share an address. The output signal controls all associated output devices in the same way; this is referred to as a "wire-AND" logic function. Again, only single-bit signals should share addresses except in the case of multiplexing.

There is no set limit on the number of devices which may share addresses, although practical constraints will be imposed by the physical limits of a system.

The Seriplex address sharing capability enables the address multiplexing feature of the controller-device interface. In address multiplexing, multiple devices and signals share the same address space, but only one signal is active during a given data frame. See 5.4.1 for more information on address multiplexing.

5.4.8 Device address boundaries

There are no physical or protocol constraints which would prevent an I/O device from operating at any valid address from 1 through 255, providing that enough addresses are assigned for a multi-bit signal. However, the recommended practice is to assign starting addresses for signals of given data lengths as follows:

– assign 1-bit signals to any valid address;

– assign 2-bit signals to an even-numbered address (2, 4, 6, etc.);

– assign 3- or 4-bit signals on 4-bit address boundaries (4, 8, 12, etc.);

– assign 5- to 8-bit signals on 8-bit address boundaries (8, 16, 24, etc.);

– assign signals of more than 8 bits on 16-bit address boundaries (16, 32, 48, etc.).

In particular, multiplexable devices shall be assigned starting addresses which are multiples of 16.

NOTE These address assignments may result in some "wasted" addresses which are not used to carry actual data signals. However, assigning signal addresses according to these guidelines usually reduces the data processing requirements of control software.

5.5 Signal timing

The fundamental unit of time for Seriplex operation is the clock period t_{clock}, which is defined as the elapsed time between successive positive transitions of the clock signal during the data transmission portion of a data transmission frame. See figure 8 and table 4.

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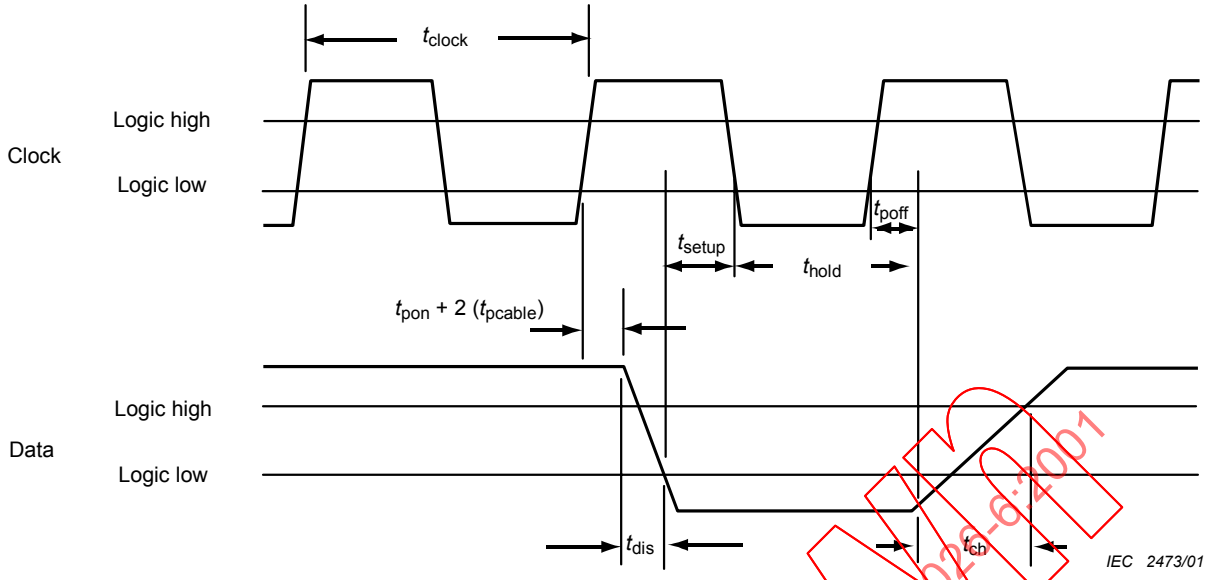

Figure 8 – Data signal timing diagram

Table 4 – Symbols and parameters

Symbol	Parameter	Value		
		Minimum	Nominal	Maximum
t_{clock}	Clock period		1/clock rate	-
t_{pon}	Data on propagation delay	0	–	2,25 µs
t_{poff}	Data off propagation delay	0	–	2,25 µs
t_{ch}	Data line charge time	0	–	$(0,5 \times t_{clock}) - t_{poff} - t_{setup} - 2(t_{pcable})$
t_{dis}	Data line discharge time	0	–	$(0,5 \times t_{clock}) - t_{pon} - t_{setup} - 2(t_{pcable})$
t_{setup}	Set-up time before data sampling	100 ns	–	–
t_{hold}	Hold time after data sampling	100 ns	–	–

The clock signal is nominally a 50 % duty cycle square wave, so that one-half clock period elapses between positive and negative transitions of the clock signal.

During the data transmission portion of a data frame, the clock source transmits a clock pulse for each clock period. During the sync period, clock pulses are not generated, but the clock period may be used as the unit of time measurement for events which occur within the sync period.

The positive (logic low-to-high) transition of the Seriplex clock signal triggers both assertion and removal of data signals from the data line. A device asserts its data on the data line immediately upon sensing the positive clock transition which begins a clock period corresponding to a signal that device produces. The device maintains data on the data line until it senses the next positive clock transition, and then releases the data line immediately.

When a device attempts to assert a signal value of 1 within a given clock period, it shall begin pulling the data line low within the propagation delay (t_{pon}) following the positive transition of the clock signal. The sum of the propagation delay (t_{pon}) plus 2 × transmission line delay and the data line discharge time (t_{dis}) shall be less than one-half of the clock period to ensure proper data sampling.

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When the clock period in which a given device is driving the data line low is completed, the device shall release the data line within the propagation delay (t_{poff}) following the next positive transition of the clock signal. The sum of the propagation delay (t_{poff}) plus 2 × transmission line delay and the data line charging time (t_{ch}) shall be less than one-half of the clock period to ensure that the following signal value may be sensed as 0 (logic high).

The clock rate determines the amount of time which is available for the data line to charge up to the high logic state following a clock period in which the data line is driven low. The maximum available charging time establishes a limit for the total data line capacitance within the system, since for a given data line source current level the charging time is proportional to the data line capacitance. Each segment of Seriplex cable and each connected node contributes to the total capacitance of a system's data line, and this total capacitance shall fall within the limit for the designated clock rate.

NOTE in practice, this charging of the data line is non-linear, due to cable resistance, inductance and transmission-line effects. Overshoot, undershoot and/or "ringing" of the data and clock lines is quite common. Therefore, the bulk capacitance is only an approximation of actual controller-device interface behaviour. However, this model is adequate when a Seriplex system is not operated at or near its performance limits.

Failure of the data line to properly charge to a logic high state before the next negative transition of the clock signal is known as the excess time-constant effect. This condition may result in invalid recognition of a value of 1 for a data signal whose intended value was 0. This effect shall be taken into consideration during the design of all Seriplex system applications.

Typically the data line discharge time (t_{dis}) will be much less than the data line charging time (t_{ch}), because properly selected data drive transistors will be able to sink much more current than the 30 mA produced by the data line current source.

Data is sampled at the negative transition of the clock signal within each clock period during the data-transmission portion of a data frame. All receiving devices for a particular data bit shall sample the data value within the hold time (t_{hold}) following the negative transition of the clock signal.

The clock loss detect time (t_{closs}) is the elapsed period, without a negative transition of the clock signal, which devices shall interpret as absence of the clock signal, rather than as a sync period.

The programming mode detect time (t_{prog}) is the minimum time during which the clock line remains high, and which shall elapse before a I/O device enters the programming mode.

5.6 Data definitions

5.6.1 General

The following subclauses describe conventions for the formulation and interpretation of data transmitted through the controller-device interface. In order to maintain maximum system flexibility, some of these conventions are recommended practices rather than explicit requirements. Within any given Seriplex system, data may be defined and used in any manner suitable to that system's purpose, provided that there is no conflict among devices in the use or meaning of any given data signal.

5.6.2 Special signal definitions

No restrictions are placed on the meaning of data transmitted through the controller-device interface. However, the following subclauses list requirements and recommendations for the meaning of controller-device interface data. These recommendations should be followed throughout any given Seriplex system.

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All signal meaning conventions shall be located within the first "word" of Seriplex data (addresses 1 through 15); no conventions or requirements are given for the specific meaning of signals with addresses higher than 16.

5.6.3 Address 0

Input signal 0 and output signal 0 shall not be used to transmit data among Seriplex devices. Physically, clock pulse number 0 is not usable by Seriplex devices because its negative transition, upon which data would be sampled, is not preceded by a positive transition; this preceding positive transition would be necessary to instruct any signal-transmitting device to assert a signal on the data line in advance of the negative clock signal transition.

5.6.4 Multiplex channel indication

Outputs number 1 through 4 are used by a clock source to indicate the signal multiplex channel to be updated within the current data frame. Output bits 5 through 8 are used by CDR; see 5.6.6.2.

Within a master/slave mode system, output signals 1 through 4 shall not be used for any other purpose to preclude interfering with the multiplex channel indication. Within a peer-to-peer mode system, neither inputs 1 through 4 nor outputs 1 through 4 shall be used, as these signals occupy the same clock periods.

The multiplex channel indication is a 4-bit binary number, with the least-significant bit corresponding to output signal number 1 and the most-significant to output 4.

5.6.5 Data echo signals

Data echo provides a method for a signal-transmitting device to verify that a single-bit data signal has been received correctly by another device. In this method, a device which receives a single-bit data signal retransmits that signal back to the controller-device interface, creating an "echoed" signal which confirms the logical state of the received data. The device transmitting the original signal compares the echoed signal value to the original value to determine whether the data was received correctly.

There are no requirements for the relationship between the addresses of the original signal and the echoed signal in master/slave mode. In master/slave mode, output signals and input signals are separated by the controller-device interface timing; therefore, it is conceivable that signals could be echoed to the same address as the original signal.

Because there is no distinction between output signals and input signals in peer-to-peer mode, a signal shall not be echoed to its same address, since this would create a "feedback" condition which would latch the signal to a value of 1. Otherwise, the same requirements apply as for master/slave mode.

A device may invert the polarity of a signal before echoing it back to the controller-device interface. This inversion should be a user-selectable feature.

5.6.6 Complementary Data Retransmission (CDR) signals

5.6.6.1 General

Complementary Data Retransmission, or CDR, is an optional method of verifying that a received multi-bit signal's value matches that transmitted by the signal's source device. This is accomplished by the source device sending an encoded version of the signal data along with the normal signal data and the receiving device comparing the two values. If the encoded value matches the original value, the data is accepted by the receiving device; otherwise, it shall be rejected as described in 5.9.

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5.6.6.2 CDR signal address assignments

When selected, CDR is performed on individual bytes of input or output data. The original data bytes shall be addressed on 8-bit boundaries, and shall fall within a 16-bit word which is addressed on a 32-bit boundary (i.e., address 32, 40, 64, 72, 96, 104,...). CDR shall not be used for the data word beginning at address 0. See table 5 for details.

Table 5 – CDR signal address assignments

Addr	0	8	16	24	32	40	48	56	64	72	80	88	96	104	112	120
	Data 0	Data 8	Data 16	Data 24	Data 32	Data 40	CDR 32	CDR 40	Data 64	Data 72	CDR 64	CDR 72	Data 96	Data 104	CDR 96	CDR 104
Addr	128	136	144	152	160	168	176	184	192	200	208	216	224	232	240	248
	Data 128	Data 136	CDR 128	CDR 136	Data 160	Data 168	CDR 160	CDR 168	Data 192	Data 200	CDR 192	CDR 200	Data 224	Data 232	CDR 224	CDR 232

Each data byte's corresponding CDR check value is transmitted 16 addresses after the original data value. For instance, the CDR check value for the data byte at addresses 32-39 is transmitted at addresses 48-53.

In multiplexed systems for which CDR is enabled for any data word, the clock source broadcasts the logical inverse (one's complement) of the multiplex channel indication bits (outputs 1 through 4) at outputs 5 through 8. Each bit's complement is transmitted four addresses after the original bit.

Input 9 may be used by CDR-enabled output devices to indicate detection of a CDR data error. Since this indication method is shared by all output devices, it is possible that multiple output devices could simultaneously detect and report CDR errors through this method. This part of IEC 62026 does not specify any method for determining which output device is reporting a CDR error.

Two adjacent data bytes may be treated as a single 16-bit data value for the purpose of CDR evaluation. In this case, an error detected in either byte would cause the entire word to be rejected by the receiving device.

Individual data bytes for which CDR is not enabled may be used for normal data transmission, as may their corresponding CDR bytes.

5.6.6.3 CDR data encoding format

In addition to verifying the value of a data signal, CDR data encoding verifies the identity of a data signal, i.e. it verifies the signal's complete address as well as the data itself. This shall be accomplished by encoding the data with values indicating the signal's address, multiplex channel and direction (input vs. output) according to the following formula:

$$c = d \oplus e$$

where

c is the CDR check byte;

d is the original data byte;

e is the encoding byte;

$\oplus$ represents a bitwise exclusive-OR logic function.

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The original data can be recovered from the encoded data by applying the converse formula:

$$d = c \oplus e$$

The encoding byte shall be formed by concatenating 4-bit codes representing a signal's assigned address and multiplex channel, with the multiplex channel code also modified according to whether the signal represents input or output data, according to the following formula:

$$e = a | (m' \oplus io)$$

where

e is the encoding byte;

a is the address code (4 bits);

m' is the multiplex channel code (4 bits);

io is the input vs. output code (4 bits);

| denotes a concatenation operation, with "a" occupying the four most-significant bits of the encoding byte and "m' ⊕ io" the least-significant bits.

The 4-bit address codes (a) are listed in table 6. These address codes ensure that encoding will invert at least one bit of the original data, and leave at least one bit non-inverted.

Table 6 – Address codes

Starting address	Address code
32	0001
40	0010
64	0011
72	0100
96	0101
104	0110
128	0111
136	1000
160	1001
168	1010
192	1011
200	1100
224	1101
232	1110

NOTE In this table the rightmost digit represents the least-significant bit of the code; data is transmitted through the Seriplex controller-device interface with least-significant bit first.

The 4-bit multiplex channel codes (m') are listed in table 7. The designation m' is used to indicate that the multiplex channel code represents the logical inversion (one's complement) of the multiplex channel indication broadcast by the clock source. The rightmost digit represents the least-significant bit of the code.

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Table 7 – Channel codes

MUX channel	MUX code m'
0	1111
1	1110
2	1101
3	1100
4	1011
5	1010
6	1001
7	1000
8	0111
9	0110
10	0101
11	0100
12	0011
13	0010
14	0001
15	0000

The 4-bit I/O direction codes are listed in table 8. These codes are selected to invert the most-significant bit of the multiplex channel code (m') if and only if the data represents master/slave mode output data. As before, the rightmost digit corresponds to the least-significant bit of the code.

Table 8 – I/O direction codes

Seriplex operating mode	Data transmission direction	Input/output code I/O
Peer-to-peer	Inputs	0000
Peer-to-peer	Outputs	0000
Master/slave	Inputs	0000
Master/slave	Outputs	1000

For example, if the original data byte were decimal 163 (binary 10100011), to be transmitted as master/slave mode output data at address 32 during multiplex channel 3, the corresponding check byte would be formed as shown in figure 9.

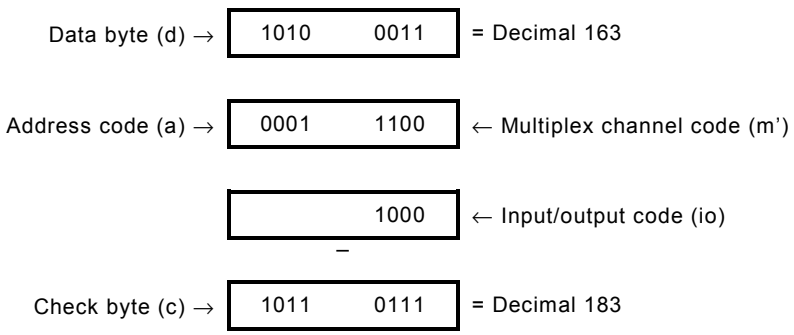

Figure 9 – Check byte formation

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5.7 Signal addressing conventions

5.7.1 General

The following are recommended practices for the assignment of signal addresses to devices.

– Signal addresses from 0 through 15 should not be used to transmit I/O data within a Seriplex system. These addresses should be reserved for designated system signals as described in 5.6.2, as well as for other designated signals which may be incorporated within future versions of the Seriplex standard specification. This convention still allows the full 7, 680-bit multiplexed data capacity.

– Multi-bit signals should be assigned on address boundaries as described in 5.4.8. In particular, multiplexed signals should be assigned starting addresses which are multiples of 16.

– The signal address usage of devices should be allocated in powers of 2 up to 16 bits; specifically, 1, 2, 4, 8, or 16 bits. Signals longer than 16 bits should be allocated addresses in 16-bit increments; 16, 32, 48, etc. Although this allows a maximum data length of 240 bits, the recommended practice is to limit data length to 64 bits or fewer.

If more addresses are allocated to a device or signal than are actually needed to transmit that signal, any unused data bits should be assigned the signal value of 0.

Address assignments for CDR signals are defined in 5.6.6.2.

5.7.2 Bit order

Multi-bit data values may represent a binary number. Such data values shall be transmitted least-significant bit first; i.e. the least-significant bit of the data value shall correspond to the lowest address number assigned to that signal, and the most-significant bit shall correspond to the highest assigned signal address.

A sign bit, if used, shall occupy the most-significant bit within the data value.

NOTE Multi-bit discrete signals (that is, multiple consecutive single-bit signals transmitted by a single device) may be transmitted in any order which is appropriate to a given device or application, although this order should remain fixed for all devices of a given type. As a general convention, input/output points should be numbered so that the lowest point number on the device corresponds to the lowest Seriplex address.

5.7.3 Data coherence

Multi-bit values shall be assigned contiguous signal address, and be entirely transmitted within a single data frame. The value of a controller-device interface signal shall not change during transmission of that signal, regardless of that signal's length.

Any device designed to transmit or receive a multi-bit data signal shall ensure that the signal is coherent, i.e. the entire signal is transmitted and received within a single data frame and is generated and used as a single unit. This requirement is intended to avoid data mismatches, wherein two portions of a signal could be received as two separate objects with a change in signal value occurring between transmission of the two objects.

Seriplex host interfaces should ensure data coherence for signal lengths up to at least 16 bits (including CDR check information, if any).

No method of ensuring data coherence of signals longer than 16 bits is required by this standard. Designers and users of devices and applications which make use of signals and/or messages longer than 16 bits should provide their own methods to ensure data coherence and should provide information as to the methods used.

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5.8 Operational characteristics

5.8.1 Controller-device interface initialization

Controller-device interface initialization and operation is controlled by a Seriplex system's clock source device. The conditions under which a clock source initiates controller-device interface operation will vary among different systems, but shall be predictable and repeatable for the application designer in all cases.

Before initiating Seriplex operation, a clock source shall first create a clock halt condition; i.e. it shall ensure that the clock signal has been idle for at least the duration of the clock loss detect time. This ensures that all I/O devices have assumed their default signal states and are ready for normal controller-device interface initialization to begin.

The clock source shall begin the controller-device interface initialization process by transmitting a bus fault detection (BFD) pulse and performing the associated controller-device interface fault tests. If the clock source detects a fault, it shall transmit a signal clock pulse, and then return to a clock halt state, i.e. it shall not transmit any clock pulses for at least the duration of the clock loss detect time. This single clock pulse ensures that I/O devices do not see enough consecutive BFD pulses on the data line to place them into programming mode (see 5.10). Since this clock pulse corresponds to address 0, no data shall be transmitted during this pulse.

NOTE While not recommended practice, it is acceptable for the clock source to transmit this single clock pulse before the BFD pulse instead of after, provided that the clock line has been idle for at least the duration of the clock loss detect time.

If no controller-device interface faults are detected by the clock source, it shall begin transmission of the clock signal and scanning of data frames. Upon the first negative clock signal transition, all properly connected and powered Seriplex devices shall begin their normal process of counting clock pulses and monitoring for the sync period, for loss of the clock signal, and for controller-device interface faults.

5.8.2 Device initialization

All Seriplex devices shall assume default input and output data signal states upon initial application of Seriplex power, upon detection of bus fault or undervoltage conditions, and upon any other controller-device interface initialization condition. All I/O devices' external output signals shall assume their default states (typically off or deactivated) under these conditions.

On the first negative clock signal transition following a clock loss condition, I/O devices shall begin their normal process of counting clock pulses and monitoring for the sync period, for loss of the clock signal and for controller-device interface faults.

Output slave devices may monitor output data, but shall not change their external output signals from their default "shelf" state, until they have detected at least five valid sync periods and BFD pulses without loss of the clock signal. This is intended to allow controller-device interface data and device logic conditions to stabilize before actual control activity takes place, as well as to prevent improper transmission and reception of data should a device become active during the course of a data frame instead of between frames. Similarly, I/O devices shall also withhold input signals (that is, to transmit only signal values of 0) upon controller-device interface initialization until they have detected at least four valid sync periods and BFD pulses.

NOTE 1 It is recommended for the master to withhold output signals (that is, to transmit only signal values of 0) for the first four data frames upon controller-device interface initialization, for the same reasons as given for withholding input data upon initialization.

NOTE 2 Seriplex version 1 I/O devices were not required by specification to withhold and/or ignore data for any period upon controller-device interface initialization.

NOTE 3 "Hot plugging", the practice of connecting an I/O device to a Seriplex cable while the controller-device interface is operating, is not recommended.

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5.8.3 Normal controller-device interface operation

Normal Seriplex operation begins when all devices have completed their initialization activities and begin reporting input data and responding to output data normally.

NOTE Normal controller-device interface operation typically begins with the fifth valid sync period following a clock halt condition.

During normal controller-device interface operation, the clock source continually generates data transmission frames by transmitting series of clock pulses separated by sync periods. Input devices report controller-device interface input data, output devices monitor and respond to output data, and the master monitors input data and reports output data, all according to their assigned signal addresses and internal logic.

If signal multiplexing is used within a given system, the clock source produces the multiplex channel indication through output signals 1 through 4, and multiplexed devices monitor this indication and respond accordingly.

All devices shall continually monitor for sync periods, clock loss, controller-device interface faults, under-voltage, and respond to each of these conditions according to the requirements of this standard. In addition, devices with CDR enabled shall transmit CDR data and monitor for CDR faults, and respond as required.

Normal controller-device interface operation ends with either the cessation of the clock signal or with detection of a bus fault condition. Devices shall respond to these conditions according to the requirements of this document.

5.8.4 Bus Fault Detection

Each I/O device on a Seriplex controller-device interface shall monitor for the presence of a bus fault detection (BFD) pulse during each sync period. The BFD pulse is illustrated in figure 10.

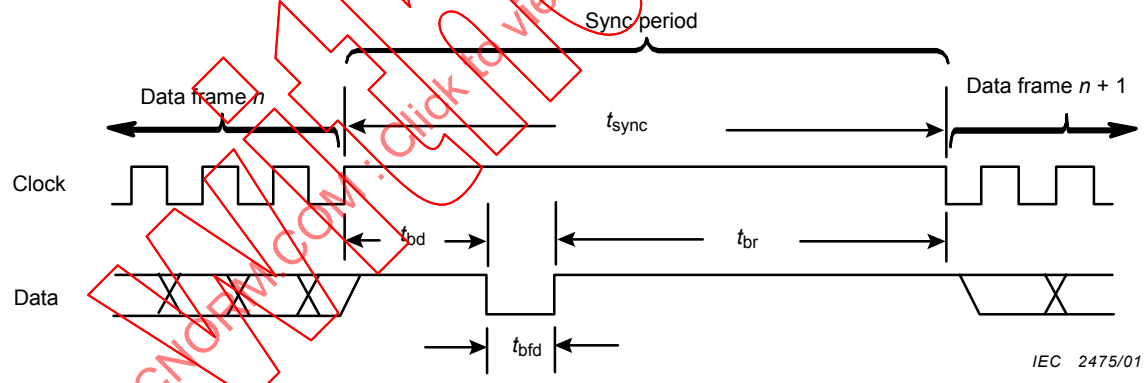

Figure 10 – Bus Fault Detection pulse

If the BFD pulse is detected and the sync period ends normally, the I/O device shall presume that the controller-device interface is operating properly and allow output data received during the previous data frame to be transmitted to its external output signals, subject to any other fault-detection mechanisms which the device employs.

If the device fails to detect a BFD pulse during a sync period, the device shall recognize a bus fault condition and its external output signals shall revert to their default or "shelf" state immediately.

See 5.4.3 and 5.5 for details about the BFD pulse.

NOTE The bus fault detection pulse was not required for version 1 Seriplex systems and was usually not provided by version 1 clock sources.

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5.8.5 Clock loss detection and response

During normal operation, each Seriplex device (including the clock source) shall continually monitor the clock line for signal activity. If a device does not detect any clock pulses for the duration of the clock loss detect time (t_{closs}; nominally 1,7 ms), that device shall recognize a clock loss condition.

Upon detecting a clock loss condition, I/O devices shall assume their default state, wherein external output signals are normally turned off. I/O devices shall remain in their default states until they have completed their own initialization activities upon controller-device interface initialization.

The clock loss condition is ended by any transition of the clock signal which begins the controller-device interface initialization process. Upon detection of this first clock signal transition, devices shall begin their initialization processes. If the clock signal becomes inactive again for the duration of the clock loss detect time before initialization is completed, devices shall remain in their default states without ever beginning normal operation, and the controller-device interface initialization process shall be restarted.

Upon detecting or asserting a clock loss condition, the clock source shall cease transmission of data through the data line, and shall not attempt to transmit the clock signal for at least the duration of the clock loss detect time. Following this period, the clock source may transmit one-half a clock pulse followed by a BFD pulse to check for the presence of controller-device interface faults. If a controller-device interface fault is detected, the clock source shall not attempt to transmit the clock signal or to transmit another BFD pulse for at least the duration of the clock loss detect time.

The clock source may remain in a clock halt condition indefinitely, according to controller-device interface conditions, the clock source's design and user configuration options. The clock source may attempt to restart the controller-device interface at a maximum rate of once per clock loss detect time period.

If at any time a clock source stops transmitting the clock signal for a period longer than the maximum sync period duration, the clock source shall wait for at least the duration of the clock loss detect time before transmitting a BFD pulse or attempting to resume transmission of the clock signal.

NOTE Clock loss is not necessarily a controller-device interface fault condition; a clock loss condition may be asserted intentionally by the clock source according to its design and that of the Seriplex application.

5.8.6 Data error detection methods

5.8.6.1 General

The following subclauses describe methods for the detection and reporting of discrepancies between a signal's value as transmitted by one device and that received by another device.

Digital debounce provides a method for a signal-receiving device to detect and filter errors in single-bit data transmissions.

Data echo provides a method for a signal-transmitting device to verify that a single-bit data signal has been received correctly by another device.

Complementary Data Retransmission (CDR) provides a method for a signal-receiving device to verify that a multi-bit data signal has been correctly received.

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5.8.6.2 Digital debounce

Digital debounce provides a method for a signal-receiving device to detect and filter errors in single-bit data transmissions. A device which employs digital debounce shall not respond to a momentary deviation in a received signal's value.

In this method, the receiving device compares a single-bit signal value received from the controller-device interface with the values received in a designated number of preceding data frames. If the data values are not identical, the device shall hold its internal logic signal at its most recent state. The device shall only change its internal logic state if the data received from the controller-device interface remains at the new logic state for the required number of data frames.

The number of data frames for which a signal value shall be identical for a device to change its logic state is called the "debounce length". All devices shall offer the ability to debounce received single-bit non-multiplexed signals for 2 or 3 data frames (debounce length = 2 or 3), as well as the ability to disable the digital debounce feature. Multi-bit and multiplexed data signals may be verified through use of the CDR feature instead of digital debounce.

Figure 11 depicts the state of a device's internal logic signal, given an example data stream, for debounce lengths of 2 and 3.

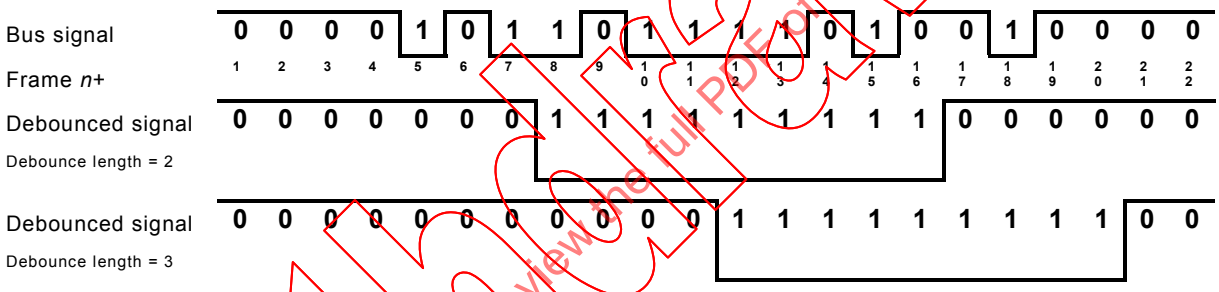

Figure 11 – Digital debounce

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NOTE The response time for a signal which employs digital debounce is increased by a factor of debounce length * frame period.

Upon controller-device interface initialization, each debounced signal shall remain in its default state at least until debounce conditions have been satisfied for that signal's change of state.

5.8.6.3 Data echo

Data echo provides a method for a signal-transmitting device to verify that a single-bit data signal has been received correctly by another device. This feature provides both message acknowledgement and data verification.

In this method, a device which receives a single-bit data signal retransmits that signal back to the controller-device interface. For example, a discrete output device such as a valve may echo its control signal back onto the controller-device interface as an input signal.

The device which transmits the original signal can compare the echoed signal value to the original value to determine whether the data has been received correctly. The echoed value may be complemented (inverted) to provide additional assurance that the data line is not being continually driven to a high- or low-logic state.

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There are no explicit requirements for the relationship between the addresses of the original signal and the echoed signal in master/slave mode. However, in peer-to-peer mode a signal shall not be echoed to its same address, as this would create a "feedback" condition which would latch the signal to a value of 1.

There are no requirements for a transmitting device's behaviour upon detection of a data echo error; this behaviour shall be determined by the designers of individual applications.

NOTE 1 The receiving device does not obtain data verification through this method, so the transmitting device is responsible for error detection, reporting and response.

Seriplex devices need not offer the data echo feature.

NOTE 2 A single-bit output device should offer data echo of its primary control signal as a user-selectable option.

5.8.6.4 Complementary Data Retransmission (CDR)

Complementary Data Retransmission, or CDR, is a method of verifying that a received multi-bit signal's value matches that transmitted by the signal's source device. This is accomplished by the source device sending an encoded version of the signal data along with the normal signal data, and the receiving device comparing the two values. If the encoded value matches the original value, the data is accepted by the receiving device; otherwise, it is rejected as described in 5.9.

When CDR is enabled for a given signal, the data is encoded and retransmitted as described in 5.6.6.

NOTE 1 CDR may be used for both input and output data, in both peer-to-peer and master/slave modes. It may be applied to either individual bytes of data or to 16-bit words (byte pairs), as described in 5.6.6. CDR may be applied independently to input and output signals sharing the same address, as well as to signals sharing the same address but assigned to different multiplex channels. It is recommended practice for devices to offer all of these options as user selections, as appropriate for a particular type of device.

All Seriplex devices which transmit multi-bit signals shall provide CDR transmission capability. All Seriplex devices which receive multi-bit signals shall provide CDR verification capability and shall respond to CDR errors as specified in 5.9. In addition to numeric signals, CDR capability shall be provided by multi-bit discrete output devices which do not support digital debounce for each individual signal bit.

I/O devices and clock sources shall detect and respond to CDR errors as defined in 5.9. Devices shall offer "ride-through" capability (see 5.9.2.10) and selection of default output states. Output CDR errors shall be reported to input 9, as described in 5.9. Methods for selection of these features are not specified in this part of IEC 62026.

NOTE 2 It is recommended for the enabling of a device's CDR feature to be user-selectable. Although there are no requirements for the method of enabling and disabling CDR, the most common method for Seriplex I/O devices is address assignment. For example, assigning a block of 32 addresses to a 16-bit input device would allow it to transmit its CDR check bytes, whereas assigning only 16 addresses would prevent CDR transmission.

5.9 Fault responses

5.9.1 I/O device faults and responses

5.9.1.1 Bus fault

Upon detecting a bus fault condition (immediately on detection of a missing BFD pulse), an I/O device's external output signals shall revert to their default or "shelf" state.

NOTE The default state corresponds to an "off" or deactivated state for most Seriplex I/O devices.

Once it has detected a bus fault condition, an I/O device shall be re-initialized before it shall resume normal operation. The I/O device's signals shall remain in their default states until all controller-device interface and I/O device initialization procedures have been completed upon controller-device interface re-initialization.

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5.9.1.2 Power loss and undervoltage

Each I/O device within a Seriplex system shall monitor for controller-device interface voltage below the specified minimum operating voltage. Upon detection of an under-voltage condition of the power line, an I/O device's external output signals shall revert to their default or "shelf" state.

NOTE The default state corresponds to an "off" or deactivated state for most I/O.

Once normal power has been restored to an I/O device following an under-voltage condition, the device shall be re-initialized before it shall resume normal operation. The I/O device's signals shall remain in their default states until all controller-device interface and I/O device initialization procedures have been completed.

5.9.1.3 Data validation error (CDR fault)

Seriplex output devices which receive multi-bit signals shall provide the capability to detect a data validation error, through use of the Complementary Data Retransmission (CDR) feature. Any mismatch between a signal byte's CDR check byte as received through the controller-device interface and the corresponding check byte calculated by the output device shall be recognized as a CDR error.

An output device's default response to detection of an output CDR error shall be to force its external output signals to their default or "shelf" state; this will correspond to a numeric value of 0 for most multi-bit signals.

By default, an output device shall respond immediately to detection of a CDR error.

NOTE 1 It is recommended that devices also provide user-selectable options to set output signal values to other predefined states (for example, zero, mid-range or full-range analogue values) upon detection of a CDR error.

NOTE 2 It is recommended that output devices also provide a user-selectable option to temporarily "ride through" a CDR error. That is, the output device may hold its last valid signal value until either it receives another valid transmission, or until some pre-determined number of consecutive invalid transmissions has been received. Upon detecting the maximum number of invalid data transmissions (typically 3), the device will recognize a Data Validation Fault, and will respond accordingly.

Seriplex output devices for which CDR detection is enabled shall provide the capability to turn on Seriplex input 9 to indicate the presence of a data validation fault.

NOTE 3 This indication mechanism does not provide a direct means to detect the individual signal or device which experienced the fault; any such detection shall be performed by the control application.

A data validation fault state for a given output signal shall be cleared upon detection of a single valid transmission of that signal. At that time, the signal value shall be accepted by the output device both for use by its external circuitry and for its last valid signal state, that signal's "ride-through" count shall be cleared to 0 if used and the output device shall stop asserting the data validation fault indication bit.

5.9.1.4 Data echo error

A data echo error is a mismatch between a data signal and its echoed value, as defined in 5.8.6.3. This part does not specify requirements for a device's response upon detection of a data echo error; this response may be defined by an application designer as appropriate.

NOTE In most cases, data echo is evaluated by a controller rather than an I/O device.

5.9.1.5 I/O device fault

A Seriplex I/O device may respond to fault conditions internal to that device in any manner deemed appropriate by the designer of that device and the designer of the application in which the device is installed.

NOTE It is recommended practice for I/O devices not to interfere with operation of the controller-device interface to the extent possible under device fault conditions. It is also recommended practice for I/O devices' signals to assume their default states upon detection of an internal device fault, to remain in this state until the internal fault has been cleared and to require complete device reinitialization before resuming normal operation.

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5.9.2 Clock source faults and responses

5.9.2.1 General

The following subclauses list fault conditions which a Seriplex clock source shall monitor and the required clock source responses to these fault conditions.

NOTE 1 It is recommended practice for a clock source to withstand any controller-device interface fault without incurring physical or permanent damage.

NOTE 2 The clock source might not directly detect the presence of controller-device interface faults at remote locations. For example, a clock source might not be able to detect the presence of a short-circuit between the data and power lines through 1 000 m of cable due to the resistance and voltage drop through the cable. Other methods should be employed to detect conditions such as excess time constant at locations remote from the clock source.

5.9.2.2 General clock source fault response

Except where specifically noted, the clock source shall cease transmission of the clock signal immediately upon detection of any of the Seriplex controller-device interface fault conditions listed below. This effectively halts transmission of data.

Upon initial detection of a fault during a sync period when the controller-device interface has been operating normally, the clock source shall not transmit a clock pulse at the end of that sync period, and shall not transmit any clock pulses for at least the duration of the clock loss detect time.

Once the clock loss detect time has elapsed without transmission of any clock pulses, the clock source may attempt to restart the controller-device interface, according to 5.8.2. Subsequent attempts to restart the controller-device interface following detection of a controller-device interface fault will require transmission of a single clock pulse between BFD pulses, to ensure that I/O devices do not enter their programming mode (see 5.8.1).

The clock source may remain in a clock halt condition indefinitely following detection of a controller-device interface fault condition, according to Seriplex conditions, the clock source's design and user configuration options. The clock source may attempt to restart the controller-device interface at a maximum rate of once per clock loss detect time period.

5.9.2.3 Data line faults

All Seriplex clock sources shall monitor the data line to determine whether it is possible to drive the data line to both high and low logic states. This test shall be performed during each sync period through the transmission and reception of the BFD pulse, in accordance with the requirements of 5.4.3 and 5.8.3.

If the clock source is not able to drive the data line to both high- and low-logic states, it shall recognize a data line fault condition. Data line faults may include both data stuck high and data stuck low conditions.

5.9.2.4 Clock line faults

All Seriplex clock sources shall continually monitor the clock line to determine whether the clock line is changing logic states in accordance with the clock source's commands. If the logic state of the clock line fails to match the commanded state (with allowance made for capacitive signal delays), the clock source shall recognize a clock fault condition. Clock fault conditions may include clock stuck high, clock stuck low, and clock loss.

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5.9.2.5 Clock-to-data short

All Seriplex clock sources shall continually monitor for the presence of electrical short-circuits between the Seriplex clock and data lines. A test for this condition shall be performed at least once per data frame.

NOTE The exact method for detecting this fault is not specified within this standard. However, one possible method is to measure data line current during the BFD pulse, to detect the excess current which would be fed from the clock line to the data line during a short-circuit condition.

5.9.2.6 Excess data line capacitance

All Seriplex clock sources shall continually monitor for excess time constant on the Seriplex data line.

NOTE This test is intended to detect the excess time constant effect, wherein the data line does not recharge fast enough to prevent false data readings. This effect usually results from operating the controller-device interface at a clock rate which is too fast for the amount of cable and/or quantity of I/O devices in the system.

The excess time constant test shall be performed during each sync period by testing the logic status of the data line one-half clock period after the positive transition of the BFD pulse. If the measured data line voltage is not greater than the logic high threshold specified in table 10 by this time, the clock source shall recognize an excess time constant fault.

The clock source may indicate the excess time constant fault to a user or to a controller by any means deemed appropriate by the clock source designer and application designers.

5.9.2.7 Power supply monitoring

All Seriplex clock sources shall continually monitor the Seriplex power voltage to determine whether it is above the specified minimum voltage. If this voltage is not present or is below the specified minimum, the clock source shall recognize an under-voltage condition.

5.9.2.8 Other controller-device interface faults

There are no explicit requirements for the detection of other types of bus faults by a clock source. However, the types of faults detected by a clock source and the clock source's responses to those faults shall be provided by the clock source manufacturer.

Other types of Seriplex faults which may be detected by a clock source include data line overcurrent and undercurrent.

It is recommended practice for the clock source to cease transmitting clock and data signals upon recognition of any controller-device interface fault condition. However, it may be acceptable for clock source designers to provide a user-selectable override feature which would allow the clock source to continue normal operation in the presence of any optionally-detected controller-device interface fault, provided that the application designer has determined that such a fault cannot cause unintentional equipment operation.

5.9.2.9 Internal faults

There are no requirements for types of internal clock source faults which shall be detected by a clock source. However, the types of faults detected by a clock source and the clock source's responses to those faults shall be provided by the clock source manufacturer.

NOTE Types of internal faults which may be detected by a clock source include internal RAM failure, internal watchdog fault and host watchdog fault.

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It is recommended practice for the clock source to cease transmitting clock and data signals upon recognition of any internal fault condition. However, it may be acceptable for clock source designers to provide a user-selectable override feature which would allow the clock source to continue controller-device interface operation in the presence of some types of internal clock source faults, provided that the application designer has determined that such a fault will not cause unintentional equipment operation.

5.9.2.10 Data validation error (CDR fault)

Host interface devices shall provide the capability for a controller to detect an input data validation error, through use of the Complementary Data Retransmission (CDR) feature defined in 5.8.6.4. Any mismatch between an input signal byte's CDR check byte as received through the controller-device interface and the corresponding check byte calculated by the master or host interface shall be recognized as a CDR error.

CDR error detection should be performed within the interface, rather than within the master.

Host interfaces shall also provide the capability for a controller to recognize an output data validation error based on the state of controller-device interface input. This indication mechanism does not provide a direct means to detect the individual signal or device which experienced the fault; any such detection shall be performed by the control application.

By default, an interface and/or controller shall halt the controller-device interface upon detection of either an input or output CDR error.

It is recommended practice for host interfaces to provide a user-selectable option to allow continued operation in the presence of CDR errors and for this option to be applied independently to input and output CDR errors.

By default, an interface and/or controller shall respond immediately to detection of a CDR error.

It is recommended practice for an interface and/or controller to also provide a user-selectable option to temporarily "ride through" a CDR error. That is, the host may hold its last valid input signal value until either it receives another valid transmission of that input signal or until some pre-determined number of consecutive invalid transmissions has been received. Upon detecting the maximum number of invalid data transmissions (typically 3), the host shall recognize a data validation fault and shall respond accordingly.

A host interface may indicate a data validation fault condition to a user or to a controller by any means deemed appropriate by the interface designer and application designers.

A data validation fault state for a given input signal shall be cleared upon detection of a single valid transmission of that signal. At that time, the signal value shall be accepted by the host both for use by its logic processing and for its last valid input signal state, that signal's "ride-through" count shall be cleared to 0, if used, and the host interface shall stop asserting its data validation fault programming indication.

5.9.2.11 Data echo error

A data echo error would typically be defined as a mismatch between a data signal and its echoed value, as defined in 5.8.6.3. Typically this error would be detected and responded to by application logic within a controller. It is conceivable that data echo errors could be detected by a clock source such as a host interface device, but this part of IEC 62026 does not specify any means by which original and echoed signal addresses and polarities are matched.

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This standard does not specify any requirements for a host's response upon detecting a data echo error; this response may be defined by an application designer as appropriate.

5.10 Device programming

The following are basic requirements and recommendations for Seriplex device programming. Device manufacturers may specify additional programming requirements.

- The operation of the Seriplex clock source, I/O devices, the Seriplex power supply, and or the controller-device interface itself shall not unintentionally place I/O devices into their programming mode, nor write configuration data into I/O devices.
- Programming of multiple Seriplex I/O devices simultaneously through the same Seriplex cable is not recommended, nor is programming a single I/O device while other devices are connected to the same Seriplex cable.
- There are no requirements, restrictions or conventions for programming of I/O devices by methods other than through their Seriplex connection ports.
- The programming sequence shall begin at least 100 ms after stabilization of the Seriplex power voltage. By this time the device shall complete any power-on reset checks and any other necessary processing.
- To place the Seriplex device into its programming mode, the Seriplex device power shall be within the range of 15 V to 16 V d.c., the clock signal shall remain idle for at least 40,5 ms and the Seriplex device shall detect 15 positive transitions of the data signal while the clock signal is held at the high logic state following the 40,5 ms waiting period.
- The state of the data line upon the 16th negative transition of the clock signal determines whether a Seriplex device data read or a write operation will be performed.
- Seriplex device configuration data is shifted into or out of the Seriplex device's memory through the clock and data lines.
- When the EEPROM write data has been successfully received by the Seriplex device, the Seriplex device shall assert a busy signal by holding the data line low until the EEPROM writing operation has been completed.

6 Product information

Production information shall be in accordance with IEC 62026-1.

7 Normal service, mounting and transport conditions

7.1 General

All Seriplex devices shall meet the minimum requirements for electromagnetic compatibility and environmental conditions specified in IEC 62026-1 in addition to those requirements specified below.

NOTE If the conditions for operation differ from those given in this standard or by the manufacturer, the user should state the deviation from the standard conditions and acquire an agreement with the manufacturer on the suitability for use under such conditions. Information given in the manufacturer's catalogue may take the place of such an agreement.

7.2 Ambient air temperature

Seriplex components shall operate between the ambient temperatures of –20 °C to +60 °C if not otherwise specified, with the exception that the cable shall operate correctly at temperatures up to 75 °C.

The operating characteristics shall be maintained over the specified range of ambient temperatures.

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7.3 Humidity

All Seriplex components shall be suitable for operation when the relative humidity (RH) of the air is 95 % or less, non-condensing. Special measures may be necessary in cases of occasional condensation due to variations in temperature.

7.4 Conditions during transport and storage

The storage temperature range shall be –40 °C to +85 °C unless otherwise specified by the manufacturer.

7.5 Mounting

Mounting dimensions and conditions shall be in accordance with the manufacturer's specifications.

7.6 Shock

In accordance with IEC 60068-2-27 (30 *g* shocks in each direction along three mutually perpendicular axes, 11 ms duration, half sine pulse shape).

7.7 Vibration

In accordance with IEC 60068-2-6 (5 min sweep from 10 Hz to 55 Hz in each of three mutually perpendicular axis (three sweeps), 1 mm peak-to-peak amplitude, 30 min dwell at resonant frequencies or at 55 Hz if there is no resonance).

8 Constructional and performance requirements

8.1 Seriplex power supply

The Seriplex power supply provides power for the Seriplex controller-device interface itself, i.e. for the controller-device interface circuitry within each Seriplex device. The Seriplex power supply provides a 24 V d.c. source for the controller-device interface. Multiple Seriplex power supplies may be used within a single system.

NOTE In general, the Seriplex power supply does not provide power to monitoring and control devices, so that an I/O fault would not cause a Seriplex power supply failure and, in turn, halt the operation of the controller-device interface.

The controller-device interface operates from a 24 V d.c. nominal source, with the positive voltage connected to the power conductor and the negative lead connected to the common conductor. Power supply requirements are summarized in table 9.

Table 9 – Seriplex power supply requirements

Characteristic	Value
Maximum voltage	30,0 V d.c. (including ripple)
Minimum voltage	19,2 V d.c. (including ripple)
Maximum ripple	2,0 V peak-to-peak, 47 Hz to 378 Hz
Minimum hold-up time	Application-dependent
Maximum rise/fall time	1 data frame period

Seriplex power supply voltage shall not be within the range of 15 V to 19,2 V d.c. for longer than 100 ms, because that is the EEPROM programming voltage range of the Seriplex device.

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Seriplex power supply current output requirements are dependent upon the current requirement of Seriplex devices installed within a given system. The Seriplex power supply shall be capable of providing sufficient current to drive the Seriplex power loads of all connected devices while holding Seriplex power voltage and ripple within the specified levels.

Seriplex power supply input or line regulation requirements are not fixed. However, the Seriplex power supply shall be capable of holding Seriplex power voltage and ripple within the specified levels at the rated load specified by the manufacturer.

Seriplex power specifications shall be met at all device connection points within a system. This implies that the Seriplex power supply voltage shall be set to a sufficient level to compensate for any voltage drops which may exist through the cable.

8.2 Power distribution

The Seriplex power supply shall be capable of supplying specified voltage levels through the Seriplex cable to all connected devices. In cases where the voltage drop through the cable would reduce the supply voltage or shift the common potential at remote I/O devices outside the specified levels, it may be necessary to install multiple Seriplex power supplies within a single Seriplex system.

In systems where multiple Seriplex power supplies are used to ensure correct voltage to all devices, the recommended practice is to connect all supplies' common conductors together, but to separate the power conductors from separate supplies. Connecting the common conductors provides a common reference for the clock and data signals. Isolating the different supplies' power conductors serves two purposes:

– it eliminates the possibility of "contention" among supplies which are not adjusted to identical voltage levels;

– it may allow portions of a Seriplex system to continue operation despite the failure of a single power supply since the failed supply will not be exerting a load on the other power supplies.

NOTE 1 Multiple power supplies may also be used to provide redundancy, to allow the controller-device interface to continue operating despite the failure of a power supply. In this case the recommended practice is to connect all redundant Seriplex power supplies' positive conductors to the power line through isolating diodes thus preventing a failed supply from presenting a load to other connected power supplies.

NOTE 2 Connecting multiple power supplies' positive conductors directly to the same Seriplex power line is not recommended.

8.3 Isolation

Seriplex I/O devices and clock sources shall isolate their external input and output signals from the Seriplex power and signals except as specified by this part of IEC 62026.

Isolated devices shall be capable of withstanding 500 V a.c. applied between the Seriplex conductors and any I/O connection points for a minimum of 1 s.

Seriplex power may only be used by circuitry other than controller-device interface circuitry under the following conditions:

– such circuitry is isolated from any other power source or supply circuit;

– the load presented by the device to the Seriplex power supply during normal operation does not vary by more than 100 mA, including changes induced by changing signal states.

Any internal device power supply which draws current from the Seriplex power supply shall be overload-protected so that a short or overload condition on the device supply's output does not result in excessive current consumption from the Seriplex power supply.

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The following devices shall isolate controller-device interface connections from their external I/O signals:

– large inductive loads such as contactors, solenoids, etc.;

– switches and sensors which make use of another power source such as 120 V a.c. or another 24 V d.c. supply;

– incandescent lamps.

8.4 Data line characteristics

The data line is driven by a 30 mA current source within the clock source, as shown in figure 12, so that it normally resets at a "high" logic level of approximately 12 V d.c. as referenced to the common line. Data line characteristics are summarized in table 10.

Table 10 – Data line characteristics

Characteristic	Value		
	Minimum	Nominal	Maximum
High signal voltage at clock source	11,4 V d.c.	12 V d.c.	14 V d.c.
High signal voltage at I/O device	8,4 V d.c.	12 V d.c.	17 V d.c.
Source current	27 mA	30 mA	33 mA
High logic threshold	6,75 V d.c.	7,5 V d.c.	8,25 V d.c.
Low logic threshold	2,7 V d.c.	3,0 V d.c.	3,3 V d.c.
I/O device leakage current (at logic low)	10,8 µA	12 µA	15,7 µA
Input current consumption (at logic high)	–	–	12 µA
Data driver on-state voltage (@ $I_{data} \leq 33$ mA)	0 V d.c.	–	0,7 V d.c.

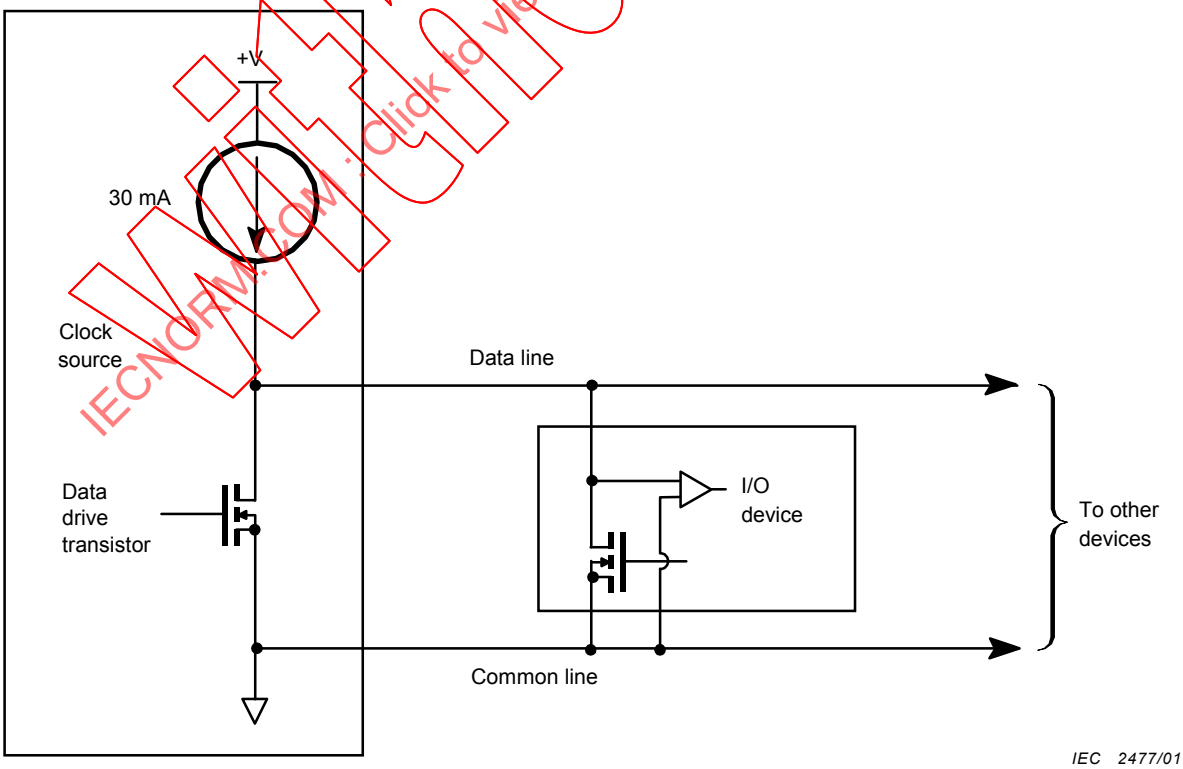

Figure 12 – Data line diagram

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The data line is low-true; a logic high level corresponds to a data value of 0, and logic low corresponds to a data value of 1. The data line rests at the logic high or 0 state and is pulled to logic low when a device asserts a data value of 1 for a particular signal.

Data line logic thresholds incorporate hysteresis to protect against spurious changes in logic state induced by electrical noise or signal reflections. When a device has sensed a high logic level on the data line, the data line voltage shall drop below the low logic threshold (V_{low}) in order for that device to sense a logic low condition. Similarly, when the data line has been sensed as low, it shall exceed the high logic threshold (V_{high}) before being sensed high. See figure 13.

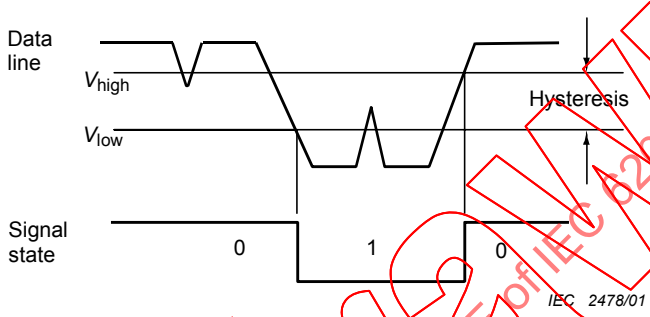

Figure 13 – Hysteresis

Controller-device interface data is sampled at the negative (logic high-to-low) transition of the clock signal within each clock period. The state of the data line at other times within the data frame is ignored by all devices including the clock source.

The data line current source usually sees a primarily capacitive load on the data line, consisting of the controller-device interface cable as well as I/O devices. When driven by the current source, the capacitive data line charges at a nearly linear rate. The time required to charge the data line to the logic high threshold determines the maximum clock rate, number of connected devices and cable length for a given system (see 5.5).

Each I/O device shall connect a 1 MΩ pull-up resistor between the data and power lines to ensure that, in the event of an open data line, the device's data line connection is pulled to a high logic state. This means that each I/O device contributes approximately 12 µA to the data line current seen by any device which pulls the data line to a low logic state.

8.5 Clock line characteristics

The clock line is driven by a "totem-pole" driver circuit within the clock source, as shown in figure 14, so that it oscillates between common (0 V) and 12 V d.c. Clock line characteristics are summarized in table 11.

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Table 11 – Clock line characteristics

Characteristic	Value		
	Minimum	Nominal	Maximum
"High" signal voltage at clock source	11,4 V d.c.	12 V d.c.	14 V d.c.
"High" signal voltage at I/O device	8,4 V d.c.	12 V d.c.	17 V d.c.
"Low" signal voltage at clock source	0 V d.c.	–	0,7 V d.c.
Source current (high)	–	150 mA	–
Sink current (low)	–	150 mA	–
High logic threshold	6,75 V d.c.	7,5 V d.c.	8,25 V d.c.
Low logic threshold	2,7 V d.c.	3,0 V d.c.	3,3 V d.c.
I/O device leakage current (at logic low)	10,8 µA	12 µA	15,7 µA
Input current consumption (at logic high)	–	–	12 µA
Duty cycle	49 %	50 %	51 %

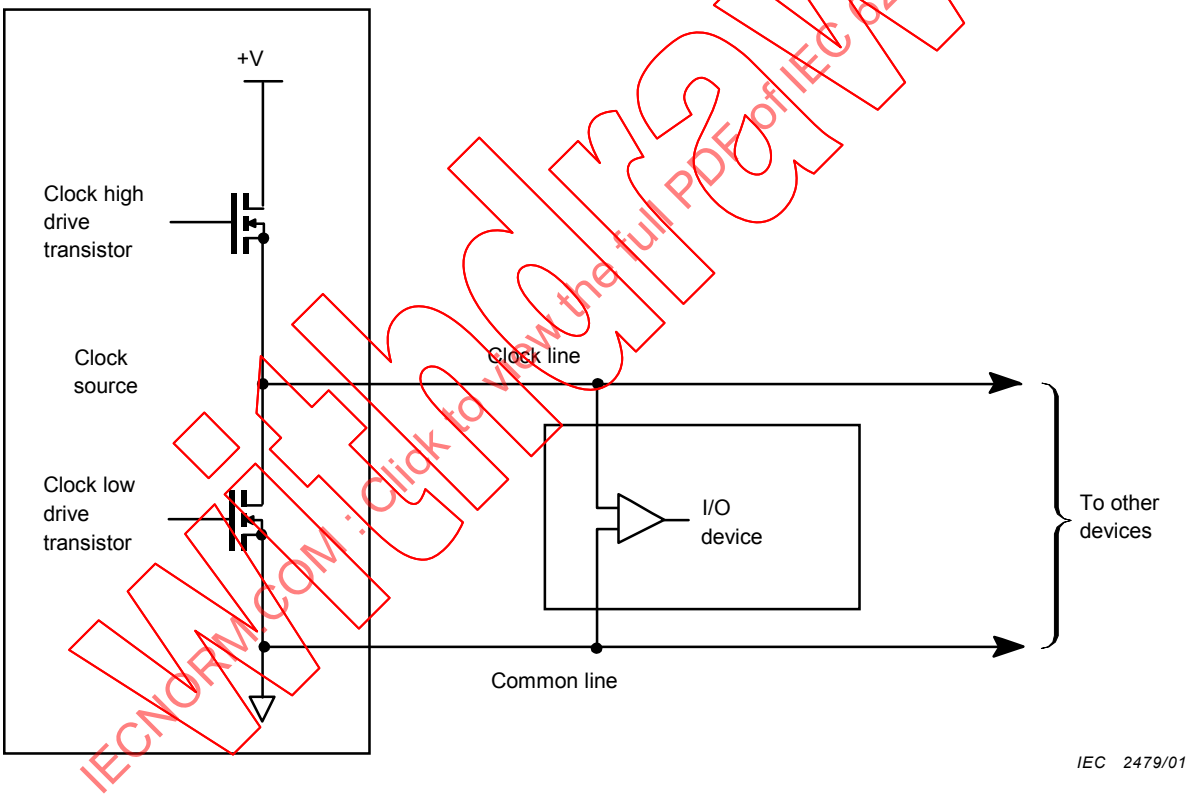

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Figure 14 – Clock line diagram

The clock line oscillates with a 50 % duty cycle, at the designated clock rate for a given system.

Clock line logic thresholds incorporate hysteresis to protect against spurious changes in logic state induced by electrical noise or signal reflections. When a device has sensed a high logic level on the clock line, the clock line voltage shall drop below the low logic threshold in order for that device to sense a logic low condition. Similarly, when the clock line is sensed as low, it shall exceed the logic high threshold to be sensed high (see figure 13).

The clock line normally rests at a high logic state during the sync period and at other times when the clock signal is halted by the clock source.

Each I/O device shall connect a 1 MΩ pull-up resistor between the clock and power lines to ensure that, in the event of an open clock line, the device's clock line connection shall be pulled to a high logic state. This means that each I/O device contributes approximately 12 µA to the clock line current seen by the clock source when it pulls the clock line to a low logic state.

8.6 Seriplex cable topology

There are no requirements for the topology of the Seriplex cable within a system, nor are there fixed limits for the total length of cable or number of nodes within a system. Cable length and node limits are determined by a system's clock rate and the total data line capacitance within a system.

Cable topology may be of any type. Recommended topologies are daisy chain or trunk and drop (see figure 15), since their performance is most predictable and easily characterized. Each drop length in a trunk and drop or loop system should be limited to less than 10 m.

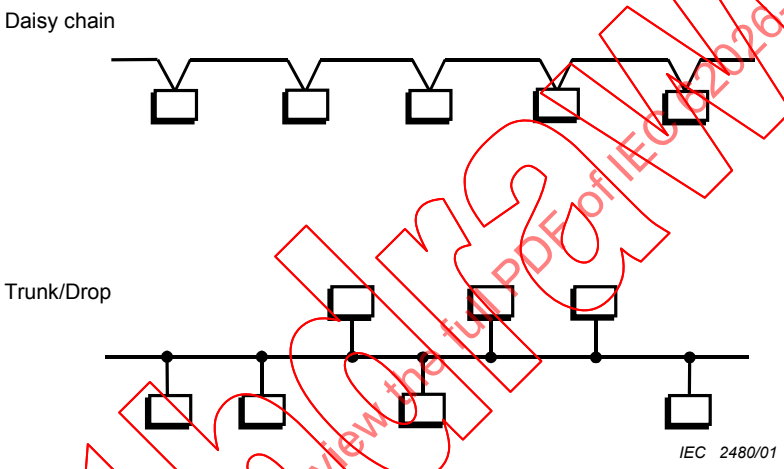

Figure 15 – Preferred Seriplex topologies

Other topologies may be used; however, it is the user's responsibility to determine that a system will work under all operating conditions. Examples of other topologies are shown in figure 16.

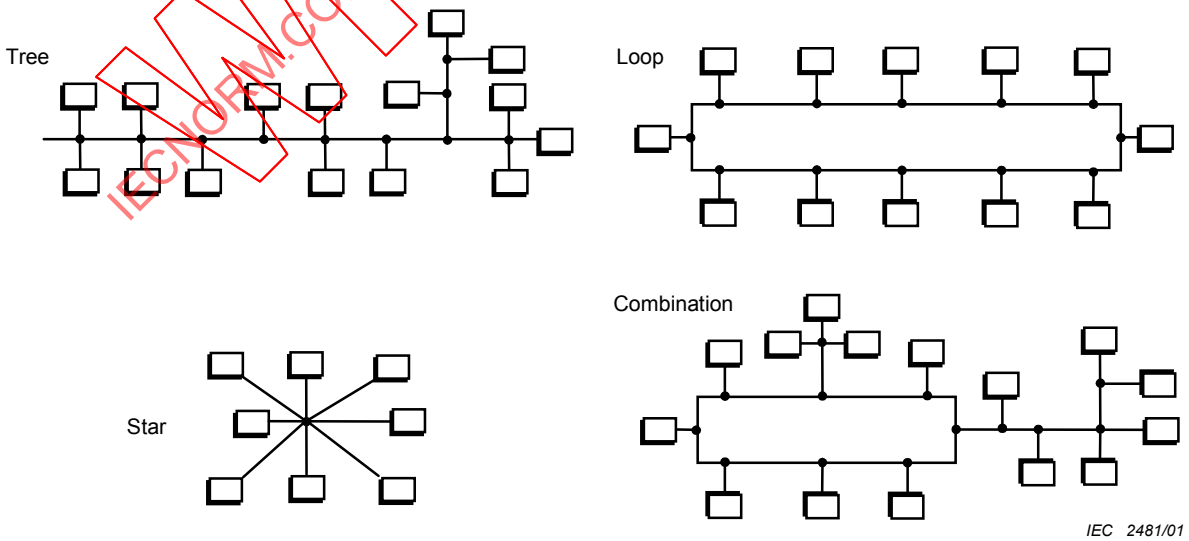

Figure 16 – Other controller-device interface topologies

The maximum length of cable and the maximum number of nodes which may be connected to a single Seriplex cable are interdependent and are determined by the following factors:

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– clock rate;
– data source current;
– data line capacitance per unit of cable;
– data line capacitance per connected node;
– clock and data line resistance per unit of cable;
– power and common line resistance per unit of cable.

8.7 Cable specifications

The following subclauses list characteristics of methods and devices used to physically connect Seriplex devices and to convey signals within a Seriplex system.

Cables shall consist of either four or six power/signal conductors, each insulated with high-density foam-polyethylene (HDPE). Additionally, each cable shall contain an aluminium/polyester foil shield and either a 0,344 mm^2 drain wire or braid shield. All cables shall be jacketed overall with either orange polyvinyl chloride (PVC) or, for direct-burial cables, black polyethylene.

The four primary Seriplex conductors (power, common, data, clock) and the drain wire shall be contained within the shield. The cable lay-up shall be a 101,6 mm left-hand lay with the following order: power, data, common, clock (see figure 17).

NOTE This lay-up order reduces coupling between the data and clock conductors.

In the case of six-conductor cables, the two additional conductors (I/O+ and I/O–) shall be located outside the shield but within the outer jacket (see figure 18).

All constituent wires shall be stranded, with the characteristics as specified in table 12. Each strand shall be tin-coated, soft annealed copper.

Table 12 – Wire size and characteristics

Wire size	Construction
0,344 mm^2 (AWG 22)	7 strands × 0,25 mm
0,785 mm^2 (AWG 18)	16 strands × 0,25 mm
1,276 mm^2 (AWG 16)	26 strands × 0,25 mm
1,828 mm^2 (AWG 14)	19 strands × 0,35 mm
3,191 mm^2 (AWG 12)	65 strands × 0,25 mm

General electrical characteristics common to all Seriplex cables are as specified in table 13.

Table 13 – General Seriplex cable characteristics

Characteristic	Value
Working voltage	300 V
Dielectric strength (primary conductors)	5 000 V d.c.
Dielectric strength (I/O+ and I/O– conductors)	1 500 V d.c.

Ground capacitance is specified for each of the two-signal conductors (data, clock), and is measured for each individual conductor with respect to all other conductors (i.e., with all other conductors shorted together). Table 14 lists these parameters.

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Table 14 – Seriplex cable specifications

OD (nominal) mm	Shield and drain	First pair size (power, common) mm^2	Second pair size (data, clock) mm^2	Third pair size I/O+, I/O-	Grounded capacitance (second pair)	Propagation velocity m/ns	Cable features
9,14	Foil with 0,344 mm^2	1,276	0,344	N/A	52,5 pF/m	0,234	
9,52	Foil and braid	1,276	0,344	N/A	52,5 pF/m	0,234	
9,14	Foil with 0,344 mm^2	1,276	0,344	N/A	52,5 pF/m	0,234	Direct burial jacket
0,9 × 8,92	Foil with 0,344 mm^2	1,276	0,344	3,191 mm^2	52,5 pF/m	0,234	
11,5 × 8.92	Foil with 0,344 mm^2	1,276	0,344	1,828 mm^2	52,5 pF/m	0,234	
11,2 × 8.92	Foil with 0,344 mm^2	1,276	0,344	1,276 mm^2	52,5 pF/m	0,234	
7,62	Foil with 0,344 mm^2	0,785	0,344	N/A	65,6 pF/m	0,234	
7,87	Foil with 0,344 mm^2	1,276	0,344	N/A	52,5 pF/m	0,234	PTFE coated
10,67 × 7,87	Foil with 0,344 mm^2	1,276	0,344	3,191 mm^2	52,5 pF/m	0,234	PTFE coated

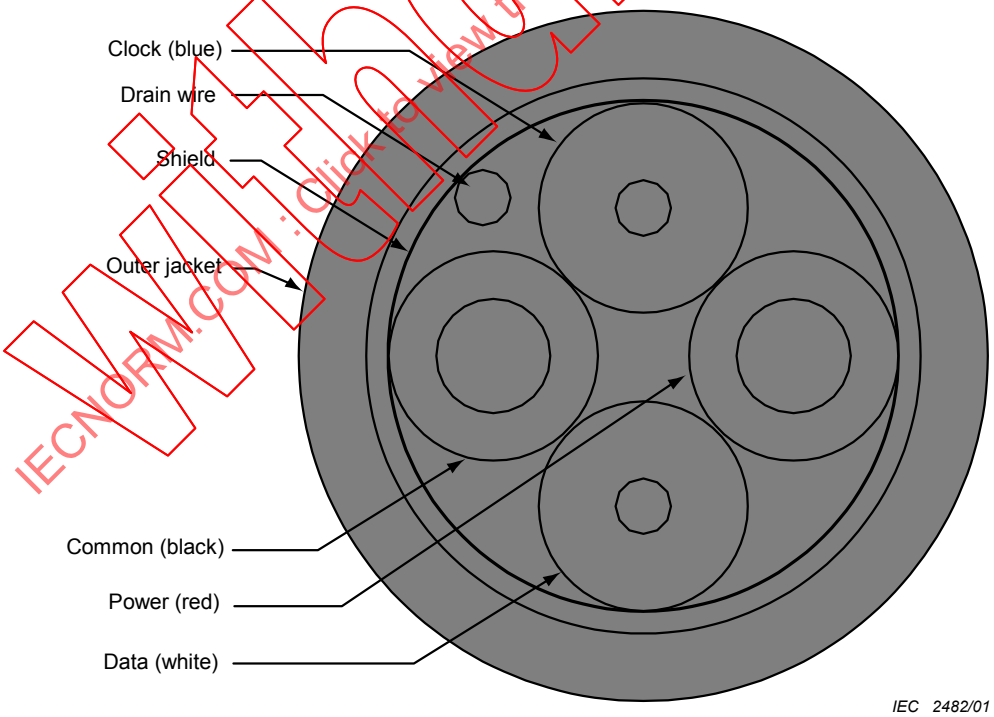

Figure 17 – Four-conductor Seriplex cable

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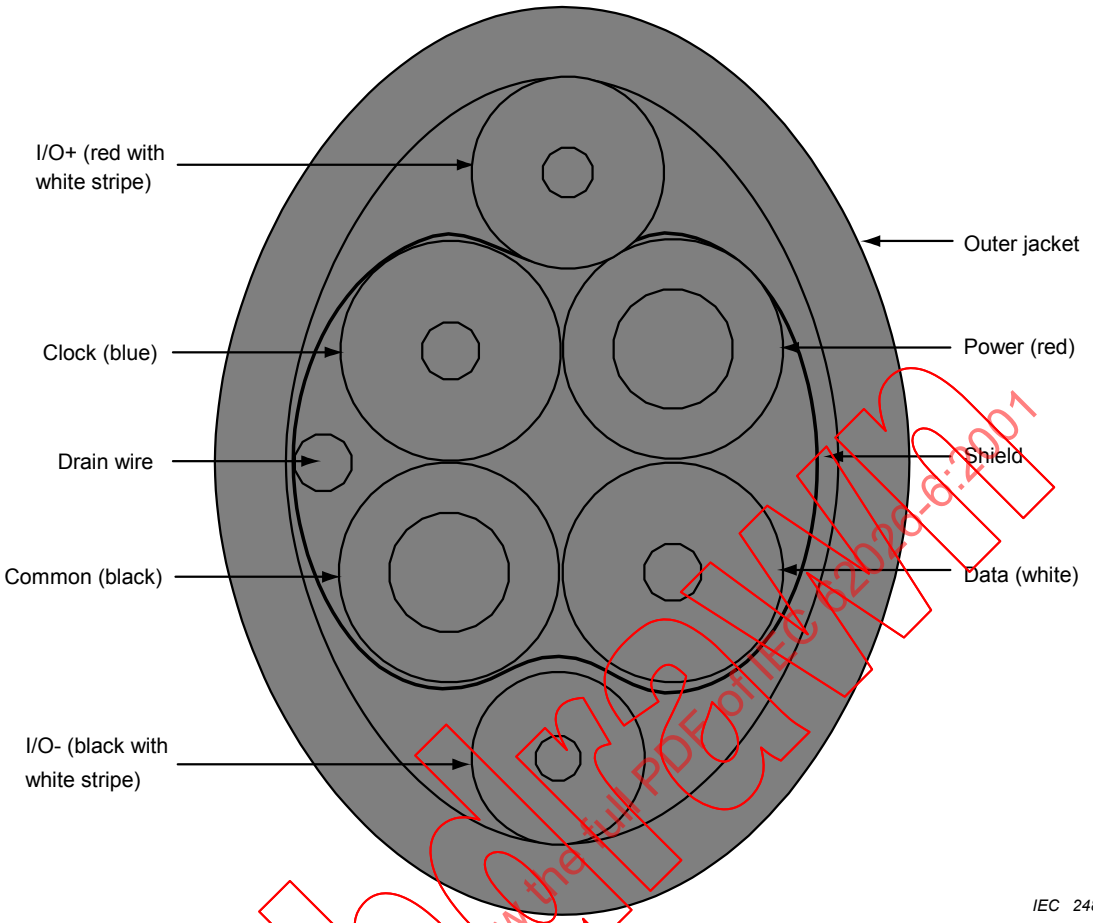

Figure 18 – Six-conductor Seriplex cable

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8.8 Electromagnetic compatibility

8.8.1 General

The operating characteristics of the Seriplex system shall be maintained at the relevant levels of electromagnetic compatibility (EMC).

All emission and immunity tests are type tests and shall be performed under representative conditions, both operational and environmental, using the recommended wiring practices and including all equipment necessary for communication and data transfer.

This requirement can be met by the use of one master, one slave and one Seriplex power supply.

A 100 m length of cable shall be used for the Seriplex line unless otherwise stated in the test instructions.

8.8.2 Immunity

8.8.2.1 Performance criteria

The test results are specified using the following performance criteria.

Criterion A: normal performance within the specification limits and statistical maximum of one disturbed transaction per 30 transactions during the test stress periods.

Criterion B: during the tests, a temporary loss of the data communication may occur; thereafter, the device shall continue to operate as intended. No change of actual operating state or stored data shall occur.

The Seriplex device to be tested shall have all the essential design details of the type which it represents and shall be in a clean and new condition.

Maintenance or replacement of parts during or after a testing cycle is not permitted.

8.8.2.2 Electrostatic discharge (ESD) immunity

The test shall be performed in accordance with IEC 61000-4-2.

10 positive and 10 negative pulses shall be applied to each selected point.

The test voltage shall be applied by the contact discharge method to Seriplex devices with metallic enclosures at a minimum test voltage of 4 kV.

The test voltage shall be applied by the air gap discharge method to Seriplex devices with non-metallic enclosures at a minimum test voltage of 8 kV.

Performance criterion A shall apply.

8.8.2.3 Radiated radio-frequency electromagnetic field immunity

The test shall be performed in accordance with IEC 61000-4-3.

The minimum test field strength shall be 10 V/m.

The frequency band shall be 80 MHz to 1 000 MHz, amplitude modulated.

Performance criterion A shall apply.

8.8.2.4 Conducted radio-frequency disturbance immunity

The test shall be performed in accordance with IEC 61000-4-6.

The minimum test level shall be 10 V.

The frequency band shall be 150 kHz to 80 MHz.

Performance criterion A shall apply.

NOTE The operating environment of these devices using Seriplex power supplies is considered to be well protected against conducted radio frequency disturbances.

8.8.2.5 Fast transient immunity

The test shall be performed in accordance with IEC 61000-4-4, as follows:

a) at a minimum test voltage of 1 kV;

b) at a minimum test voltage of 2 kV.

The test voltage shall be applied by the capacitive coupling clamp.

For test a), performance criterion A shall apply.

For test b), performance criterion B shall apply.

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8.8.2.6 Surge immunity

Seriplex field devices shall not be tested for surge immunity.

The Seriplex power supply shall be installed in such a way that it is not subject to line surges on the output side.

NOTE The operating environment of these devices is considered to be well protected against surge voltages caused by lightning strikes.

8.8.2.7 Immunity to voltage dips

Seriplex field devices shall not be tested for immunity to voltage dips.

8.8.3 Emission

8.8.3.1 Conditions during measurement

The measurement shall be made in the operating mode, including grounding conditions, which produces, in the relevant frequency band, the highest emission consistent with normal applications.

Each measurement shall be performed in defined and reproducible conditions.

Additional information needed for the practical application of the tests is given in this part.

8.8.3.2 Emission limits

The emission of the Seriplex device shall meet the requirements given in CISPR 11 for class A, group 1.

9 Tests

9.1 Supply polarity

Reverse the polarity of the supply connections to the EUT.

Verify that the EUT does not suffer any permanent damage.

9.2 Power supply

9.2.1 Voltage

Measure the output of the Seriplex power supply to verify that it is within the range 19,2 V to 30 V, including ripple.

The peak shall be less than 30,0 V, the minimum shall be greater than 19,2 V and the ripple shall be less than 2,0 V as specified in 8.1.

9.2.2 Current

There is no minimum current requirement for a Seriplex power supply therefore no test is required.

NOTE For any system there should be sufficient current capability to supply current for all attached devices. Multiple power supplies may be used (see 8.1).

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9.2.3 Rise and fall times

Verify by examination of the waveform that the rise and fall times of the power supply are less than one frame time.

The minimum frame time is as follows:

15,5 clock cycles at 200 kHz + 82 µs minimum sync time = 162,5 µs (mode 1).

The maximum frame time is as follows:

(256 × 2 + 8) clock cycles at 10 kHz = 52 ms (mode 2).

9.3 Clock source

9.3.1 Power consumption

Current consumption for the clock source is not specified by this part. However, current consumption shall be identified for the product in order that the power supply can be correctly specified and to make voltage drop calculations. Therefore the current consumption of the clock source shall be measured and shall be within the range specified by the manufacturer (see figure 19).

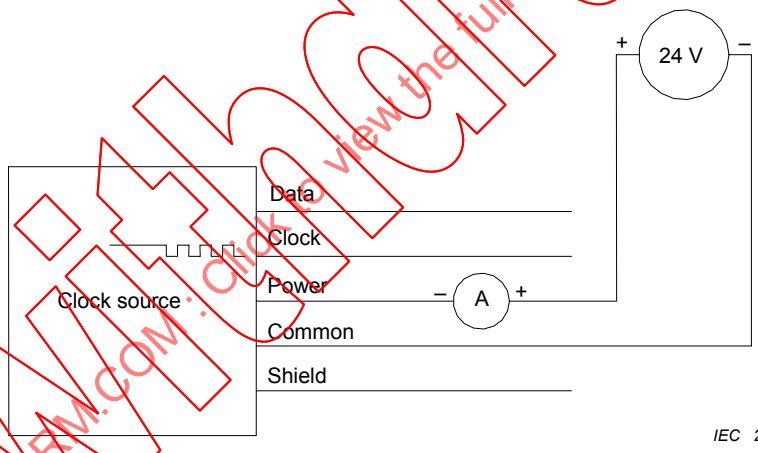

Figure 19 – Circuit for verification of clock source power consumption

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9.3.2 Clock signal

9.3.2.1 General

Measure the clock signal generated by the clock source.

Connect as shown in figure 20.

See figure 21 for the waveform.

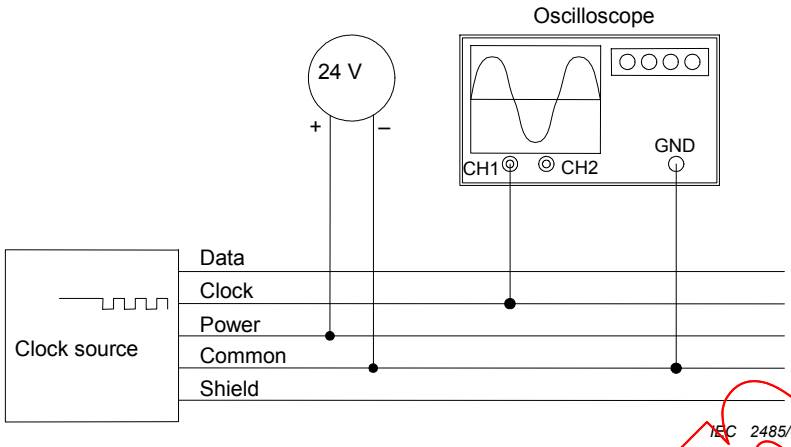

Figure 20 – Connections for clock signal tests

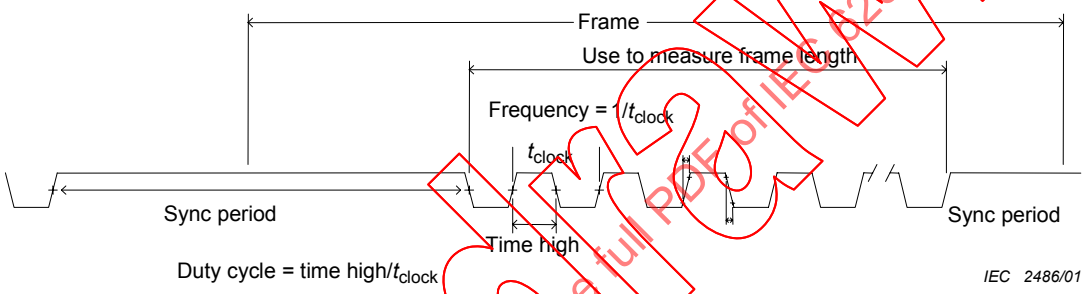

Figure 21 – Clock signal waveform

9.3.2.2 Minimum frequency setting

Set the clock source to the minimum frequency setting.

Measure the frequency of the clock signal excluding the sync period.

Verify that the frequency is greater than or equal to 10 kHz as specified in 5.4.5.

Measure the duty cycle of the clock signal excluding the sync pulse.

Verify that the duty cycle is 50 % ± 1 % as specified in 8.5.

Measure the sync period.

Verify that the sync period is greater than 82 µs and less than 1 ms as specified in 5.4.2.

9.3.2.3 Maximum frequency setting

Set the clock source to the maximum frequency setting.

Measure the frequency of the clock signal excluding the sync period.

Verify that the frequency is less than or equal to 200 kHz as specified in 5.4.5.

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Measure the duty cycle of the clock signal excluding the sync pulse.

Verify that the duty cycle is 50 % ± 1 % as specified in 8.5.

Measure the sync period.

Verify that the sync period is greater than 82 µs and less than 1 ms as specified in 5.4.2.

9.3.2.4 Maximum frame length (peer-to-peer)

Set the clock source to mode 1, peer-to-peer.

Set the clock source to the maximum frame length setting.

Measure the number of positive clock edges between frames.

NOTE The easiest way to do this may be to measure the time from the end of one sync period to the beginning of the next sync period, add the time high and then divide this sum by the period.

The number of clock pulses is the frame length for mode 1, peer-to-peer.

Verify that the maximum frame length is exactly divisible by 16 and is less than or equal to 256.

9.3.2.5 Minimum frame length (peer-to-peer)

Set the clock source to mode 1, peer-to-peer.

Set the clock source to the minimum frame length setting.

Measure the number of positive clock edges between frames.

NOTE The easiest way to do this may be to measure the time from the end of one sync period to the beginning of the next sync period, add the time high and then divide this sum by the period.

The number of clock pulses is the frame length for mode 1, peer-to-peer.

Verify that the minimum frame length is exactly divisible by 16 and is greater than or equal to 16.

9.3.2.6 Minimum frame length (master/slave)

Set the clock source to mode 2, master/slave.

NOTE 1 Mode 2 may not be offered by clock sources intended for peer-to-peer operation only. In such cases this test should be omitted.

Set the clock source to the maximum frame length setting.

Measure the number of positive clock edges within a frame.

NOTE 2 The easiest way to do this may be to measure the time from the end of one sync period to the beginning of the next sync period, add the time high and then divide this sum by the period.

To determine the frame length, divide this result by two since there are two clock pulses for each address in mode 2.

Verify that the maximum frame length is exactly divisible by 16 and is less than or equal to 256.

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9.3.2.7 Maximum frame length (master/slave)

Set the clock source to mode 2, master/slave.

NOTE 1 Mode 2 may not be offered by clock sources intended for peer-to-peer operation only. In such cases this test should be omitted.

Set the clock source to the maximum frame length setting.

Measure the number of positive clock edges within a frame.

NOTE 2 The easiest way to do this may be to measure the time from the end of one sync period to the beginning of the next sync period, add the time high and then divide this sum by the period.

To determine the frame length, divide this result by two since there are two clock pulses for each address in mode 2.

Verify that the maximum frame length is exactly divisible by 16 and is greater than or equal to 16.

9.3.2.8 Clock signal high level and rise time

9.3.2.8.1 Test procedure

Add a 600 pF capacitor between the clock line and the common line (refer to figure 22).

a) Measure the rise time of the charge cycle (refer to figure 23).

b) Measure the voltage at the high level, V_h, of the clock signal.

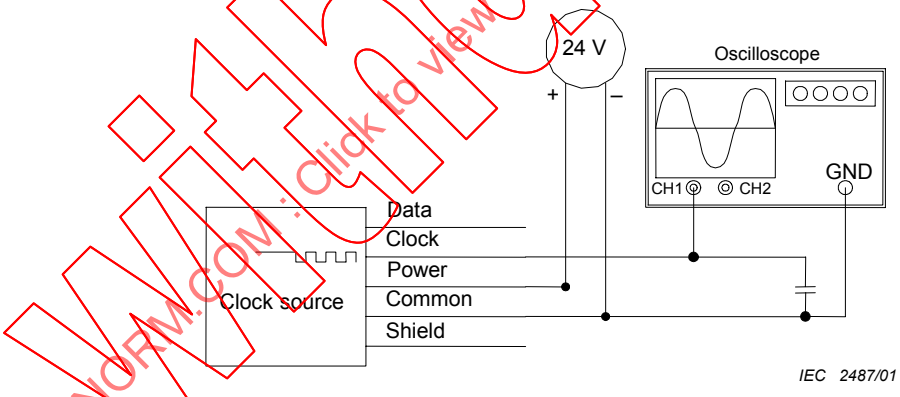

Figure 22 – Test circuit for clock signal

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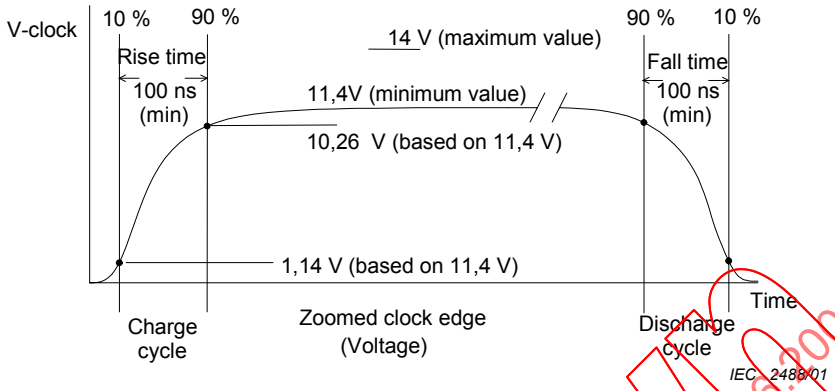

Figure 23 – Waveform of clock pulse

9.3.2.8.2 Verification

The transient charge and discharge currents sourced to and drawn from the capacitor should be similar to figure 24 and shall have a peak value of 150 mA or greater.

NOTE It is not necessary to actually measure this current directly; the given test procedures will indirectly verify the minimum current specification.

a) Verify that the rise time is 100 ns ± 5 ns.

b) Verify that V_h is between 11,4 V and 14 V as specified in 8.5.

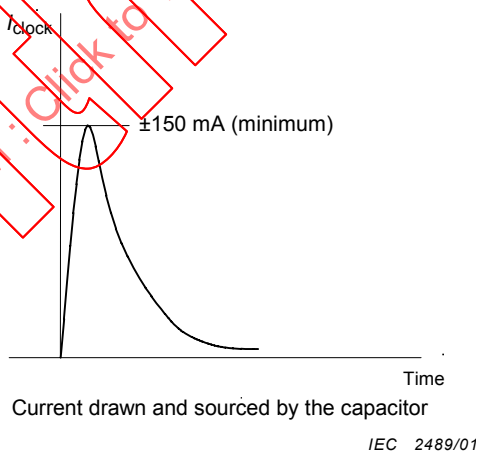

Figure 24 – Transient current

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9.3.2.9 Clock signal low voltage and fall time

9.3.2.9.1 Test procedure

Add a 600 pF capacitor between the clock line and the common line (refer to figure 22).

a) Measure the fall time of the discharge cycle (refer to figure 23).

b) Measure the voltage at the low level, Vl, of the clock signal.

9.3.2.9.2 Verification

a) Verify that the fall time is 100 ns ± 5 ns.

b) Verify that V_I is between 0 V and 0,7 V as specified in 8.5.

9.3.3 Data signal

9.3.3.1 General

Examine the data signal generated by the clock source.

Connect as shown in figure 25.

See figure 26 for the waveform.

NOTE For all data line tests, there should be no activity on the data line other than that required by the specific test. (For example, the controller should not be commanding any outputs to turn on.)

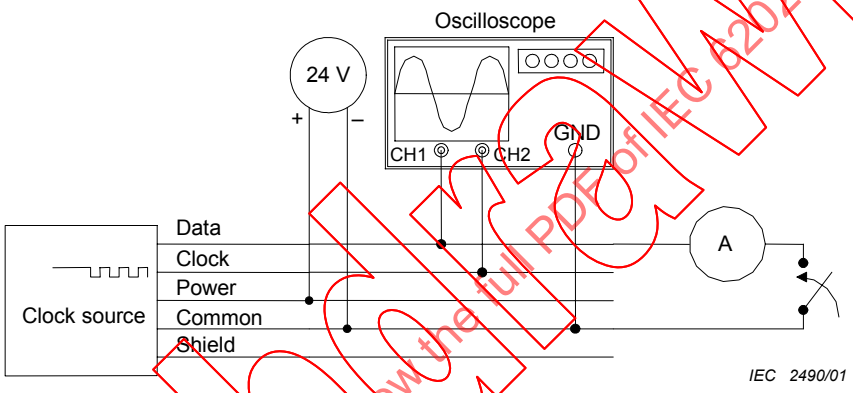

Figure 25 – Test circuit for CDI data signal

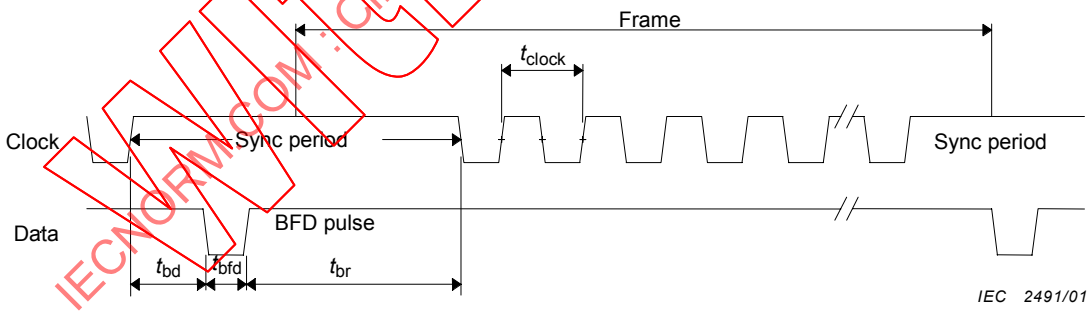

Figure 26 – Waveform for CDI data signal

9.3.3.2 Bus Fault Detect (BFD) pulse

9.3.3.2.1 Test procedure

a) Observe the Bus Fault Detection (BFD) pulse.

b) Measure the time between the beginning of the sync pulse and the falling edge of the BFD pulse on the data line, see t_{bd}, figure 26.

c) Measure the pulse width of the BFD pulse, see t_{bfd}, figure 26.

d) Measure the time between the end of the BFD pulse and the end of the sync pulse, see t_{br}, figure 26.

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9.3.3.2.2 Verification

a) Verify that the data line is high except for a negative pulse during the sync period on the clock line.

b) Verify that this time t_{bd} is greater than t_{clock} – 0,5 µs.

c) Verify that this time t_{bfd} is greater than 2 × t_{clock} – 0,5 µs.

d) Verify that this time t_{br} is greater than 2 × t_{clock} – 0,5 µs.

9.3.3.3 V_h of the square wave data signal

9.3.3.3.1 Test procedure

Measure the voltage at the high level, V_h, of the square wave data signal.

9.3.3.3.2 Verification

Verify that V_h is between 11,4 V and 14 V as specified in 8.4.

9.3.3.4 V_l of the square wave data signal

9.3.3.4.1 Test procedure

Measure the voltage at the low level, V_l, of the square wave data signal.

9.3.3.4.2 Verification

Verify that V_l is between 0 V and 0,7 V as specified in 8.4.

9.3.3.5 Source current of the data line

9.3.3.5.1 Test procedure

Set the frame length to the maximum and measure the source current of the data line to the common line.

9.3.3.5.2 Verification

Verify that the current is between 27 mA and 33 mA as specified in 8.4.

9.3.3.6 Data on the data line

9.3.3.6.1 Test procedure

The test shall be performed in mode 2 at a clock frequency of 10 kHz, with the frame length set to the maximum.

a) Check address 1 and the maximum address.

b) Command the host interface to drive the data line low during address 1.

c) Measure the time between the clock line going high and the data line going low at address 1.

d) Measure the time between the clock line going high and the data line going high at the end of address 1.

e) Command the host interface to drive the data line low during the maximum address. This is usually address 255. If the host interface under test does not support 255 addresses then substitute the maximum address for address 255.

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f) Measure the time from when the clock line goes high until the data line goes low at address 255.

g) Measure the time from when the clock line goes high until the data line goes high at the end of address 255.

h) Using an I/O module, drive the data line low during the input clock cycle of address 1.

i) Using an I/O module, drive the data line low during the input clock cycle of the maximum address. This is usually address 255. If the host interface under test does not support 255 addresses then substitute the maximum address for address 255.

9.3.3.6.2 Verification

a) Check that no other addresses are driven low (see figure 27).

b) Verify that the data line is driven low during the output cycle of the address under test and that the data line is not driven low at any other time except during the BFD pulse.

c) This time should be less than the data-on propagation delay time of 2,25 µs as specified in table 4.

d) This time should be less than the data off propagation delay time of 2,25 µs as specified in table 4.

e) Only the input corresponding to the address under test shall be activated.

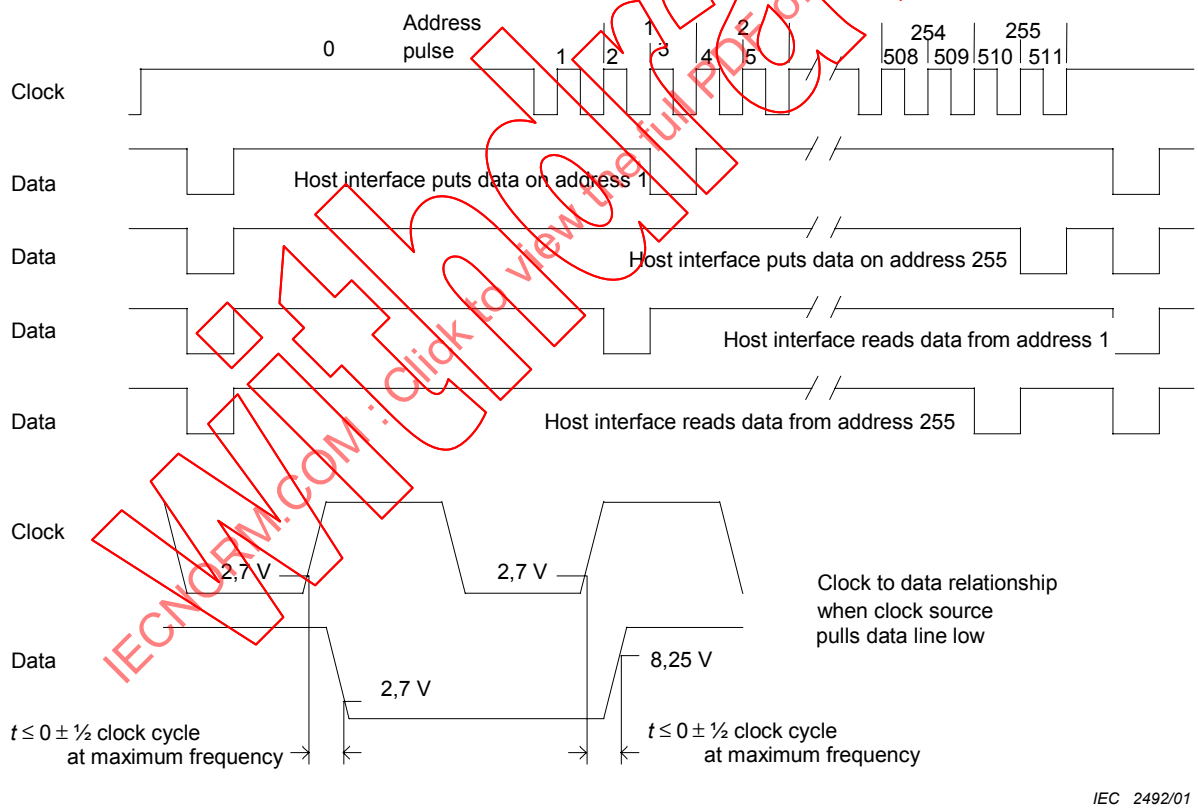

Figure 27 – Data line waveforms

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9.3.3.7 Input threshold on data line

9.3.3.7.1 General

Connect as shown in figure 28. See figure 29 for the waveform.

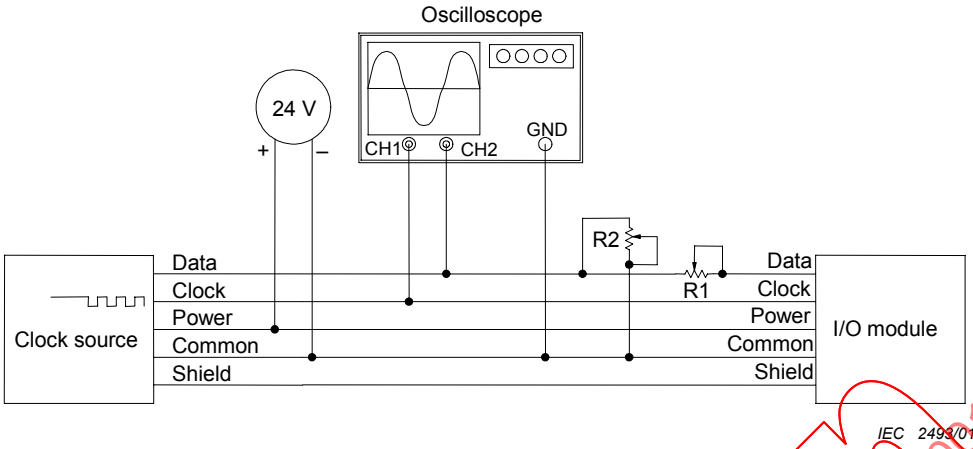

Figure 28 – Connections for verification of data line requirements

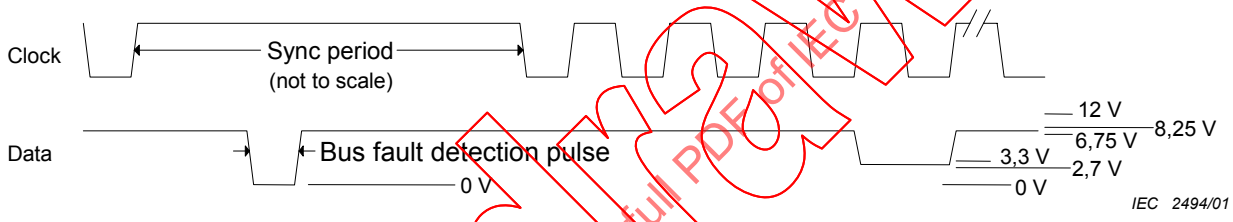

Figure 29 – Waveforms for verification of data line requirements

9.3.3.7.2 Logic low threshold

9.3.3.7.2.1 Test procedure

Connect variable resistor R1 in series with the data line between the clock source and the I/O module, the I/O module is used to place input data on the CDI, and the particular type of module is not critical as long as it has input capability.

R2 is not used and the connection is left open.

R1 should have a minimum adjustable range of ≥500 Ω. Start with R1 = ≥500 Ω. By using the I/O module as instructed in the I/O module instructions, drive one input address low.

a) While monitoring the input on the controller, increase R1 until the lower level on the data line is = 2,7 V for this input address.

b) While monitoring the input on the controller, increase R1 until the lower level on the data line is = 3,3 V for this input address.

9.3.3.7.2.2 Verification

a) Verify that the controller still responds to a logic-low signal at the input module's address.

b) Verify that the controller no longer responds to a logic low signal at the input module's address. The controller should respond to a logic high signal at the input module's address.

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