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REDLINE VERSION

INTERNATIONAL STANDARD

colour
inside

Integrated circuits – Measurement of electromagnetic emissions~~, 150 kHz to 1 Ghz~~ – Part 4: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method

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IEC 61967-4 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices. It is an International Standard.

This second edition cancels and replaces the first edition published in 2002 and Amendment 1:2006. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) frequency range of 150 kHz to 1 GHz has been deleted from the title;

b) recommended frequency range for 1 Ω method has been reduced to 30 MHz;

c) Annex G with recommendations and guidelines for frequency range extension beyond 1 GHz has been added.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47A/1101/CDV	47A/1107/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts of the IEC 61967 series, under the general title *Integrated circuits – Measurement of electromagnetic emissions* can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

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INTEGRATED CIRCUITS – MEASUREMENT OF ELECTROMAGNETIC EMISSIONS~~,~~ ~~150 kHz TO 1 GHz~~ –

Part 4: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method

1 Scope

This part of IEC 61967 specifies a method to measure the conducted electromagnetic emission (EME) of integrated circuits by direct radio frequency (RF) current measurement with a 1 Ω resistive probe and RF voltage measurement using a 150 Ω coupling network. These methods ~~guarantee~~ ensure a high degree of ~~repeatability~~ reproducibility and correlation of EME ~~measurements~~ measurement results.

~~IEC 61967-1 specifies general conditions and definitions of the test methods.~~

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61000-4-6, *Electromagnetic compatibility (EMC) – Part 4-6: Testing and measurement techniques – Immunity to conducted disturbances, induced by radio-frequency fields*

IEC 61967-1, *Integrated circuits – Measurement of electromagnetic emissions~~, 150 kHz to 1 GHz~~ – Part 1: General conditions and definitions*

~~CISPR 16-1-1, *Specification for radio disturbance and immunity measuring apparatus and methods – Part 1-1: Radio disturbance and immunity measuring apparatus – Measuring apparatus*~~

~~CISPR 16-1-2, *Specification for radio disturbance and immunity measuring apparatus and methods – Part 1-2: Radio disturbance and immunity measuring apparatus – Ancillary equipment – Conducted disturbances*~~

~~CISPR 16-1-3, *Specification for radio disturbance and immunity measuring apparatus and methods – Part 1-3: Radio disturbance and immunity measuring apparatus – Ancillary equipment – Disturbance power*~~

~~CISPR 16-1-4, *Specification for radio disturbance and immunity measuring apparatus and methods – Part 1-4: Radio disturbance and immunity measuring apparatus – Ancillary equipment – Radiated disturbances*~~

~~CISPR 16-1-5, *Specification for radio disturbance and immunity measuring apparatus and methods – Part 1-5: Radio disturbance and immunity measuring apparatus – Antenna calibration test sites for 30 MHz to 1 000 MHz*~~

3 Terms and definitions

For the purposes of this document, the terms and definitions of IEC 61967-1 apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

4 General

4.1 Measurement basics

The maximum tolerated emission level from an integrated circuit (IC) depends on the permitted maximum emission level of the electronic system, which includes the IC, and also on the immunity level of other parts of the electronic system itself (so called inherent EMC). The value of this emission level is dependent on system and application specific (ambient) parameters. To characterise ICs, i.e. to provide typical EME values for a data sheet, a simple measurement procedure and non-resonant measurement setup are required to guarantee a high degree of ~~repeatability~~ reproducibility. Subclause 4.1 describes the basis of this test procedure.

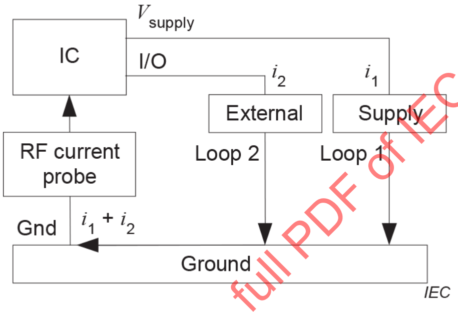

Figure 1 – Example of two emitting loops returning to the IC via common ground

The emission of an IC is generated by sufficiently fast changes of voltages and currents inside the IC. These changes drive RF currents inside and outside the IC. The RF currents cause conducted EME, which is mainly distributed via the IC pins conductor loops in the printed circuit board (PCB) and the cabling. These loops are regarded as the emitting loop antennas. In comparison to the dimension of these loops, the loops in the internal IC structure are considered to be small.

The RF currents that accompany ICs action are different in amplitude, phase and spectral content. Any RF current has its own loop that returns to the IC. All loops return mostly via the ground or supply connection back to the IC. In Figure 1, this is shown for two loops returning via ground. Loop 1 represents the supply wiring harness for the IC while loop 2 represents the routing of an output signal. The common return path via ground is a suitable location to measure the conducted EME as the measurement of the common RF sum current of the ground pin. This test is named the “RF current measurement”.

If the IC under test has only one ground pin and all other pins are suspected to contribute essentially to the EME, then the RF sum current is measured between the ground pin of the IC under test and the ground (see $i_1 + i_2$ in Figure 1).

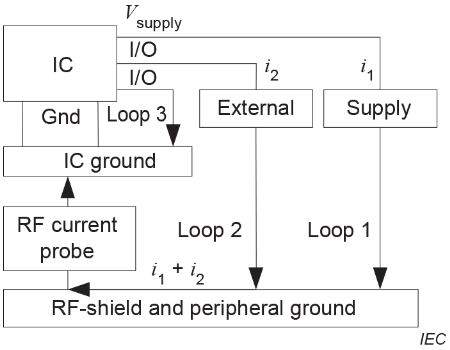

Figure 2 – Example of IC with two ground pins, a small I/O loop and two emitting loops

If the IC under test has more than one ground pin or some of the pins are not suspected to contribute much to the whole EME, then the IC under test gets its own ground plane as shown in Figure 2. This ground plane is named “IC ground”. It is kept separately from the other ground, that is named “RF-shield and peripheral ground”. The RF current is measured between the IC ground and the peripheral ground.

ICs are often used in different configurations based on the application. For instance, a microcontroller could be used as a single chip controller, with the I/O ports directly connected to the external cabling system. In order to understand the influence of a single I/O pin on the emission level of the IC, an additional measurement procedure, using the same equipment, is provided. This measurement is named “single pin RF voltage measurement at IC pins” (see also 4.3). In addition to the RF sum current measurement, the RF current measurement of a single supply pin ~~may~~ can be of interest in the analysis of an IC. This can also be attained with application of the RF current measurement probe. For example, the RF current probe can be applied to any of the multiple ground or supply pins in order to quantify the contribution of the measured pin to the whole emission.

4.2 RF current measurement

In the test procedure, this measurement shall be made by measuring the voltage across the 1 Ω resistance of a RF current probe using a ~~test~~ measurement receiver. The measurement shall be made at the location shown in Figure 1 and Figure 2. The construction of the RF current probe is specified in 6.2. The RF voltage level measured by the receiver is the voltage resulting from all of RF currents returning to the IC through the probe impedance. The voltage measurement can be converted to current by dividing the voltage by the probe impedance, if the probe impedance is determined for the applicable frequency range e.g. in a verification report.

NOTE 1 The probe impedance can be frequency dependant, caused by stray inductances of the probe, and thus the usable frequency range can be limited.

NOTE 2 The probe impedance causes, depending on the IC current consumption, a voltage drop that can affect the proper operation of the IC and limit the application of this method.

4.3 RF voltage measurement at IC pins

This measurement is used to identify the contribution of a single pin or a group of pins to the EME of the IC under test. This measurement is only applied to those pins of the IC under test that are intended to be connected directly to long (longer than 10 cm) PCB traces or wiring harnesses (e.g. I/O, supply). These pins are loaded by a typical ~~antenna~~ common mode impedance of 150 Ω, as specified in IEC 61000-4-6. In order to connect the ~~test~~ measurement receiver, that has an input-impedance of 50 Ω, the load has to be built as an impedance matching network. This matching network is defined in 6.4.

Other I/O-pins of an IC may be loaded as specified in the general part of IEC 61967-1.

4.4 Assessment of the measurement technique

The above techniques have the following properties:

- high measurement reproducibility, because few parameters influence the result;
- capability to compare different IC configurations (e.g. packages);
- single pin EME measurements of the various I/O pins are dependent on their importance for the emission in a specific application;
- assessment of the EME contribution of the IC using current sum measurement;
- ~~linear transfer function with constant frequency response as the measurement is made using resistive impedance;~~
- simple ~~calibration~~ verification of the measurement impedance using insertion loss measurement;
- measurement is also possible at very low frequencies.

With these characteristics, it is possible to measure the EME of ICs with a high degree of reproducibility and therefore this technique offers a good method for comparison.

Annex D gives an example of how the measurement techniques ~~may~~ can be used for the assessment of ICs.

5 Test conditions

All test conditions ~~needed~~ required in this document are specified in IEC 61967-1.

6 Test equipment

6.1 ~~Test receiver specification~~ RF measuring instrument

The measurement equipment ~~has to~~ shall fulfil the requirements described in IEC 61967-1.

6.2 RF current probe specification

Figure 3 shows the basic construction of the 1 Ω RF current probe.

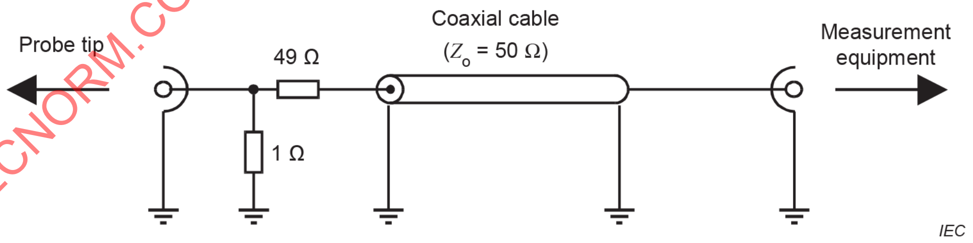

Figure 3 – Construction of the 1 Ω RF current probe ~~[1]~~

Table 1 presents a detailed specification of the RF current probe.

To prevent the measurement equipment from being damaged by DC voltage, the use of a DC block is recommended. This shall have an attenuation of <0,5 dB at the lowest frequency to be measured.

~~[1] To prevent the measurement equipment from being damaged by DC voltage, the use of a DC block is recommended. This shall have an attenuation of <0,5 dB at the lowest frequency to be measured.~~

Table 1 – Specification of the RF current probe

Frequency range	~~DC – 1 GHz~~ DC to 30 MHz The applicable frequency range of the used probe shall be evaluated e.g. in a S-parameter measurement and documented in the test report. Current probes available on the market have proved to be usable e.g. only up to 30 MHz. Therefore bandwidth and impedance over frequency of the used probe shall be verified and documented in a diagram. The same applies to on-board probes with SMD components. In future, for enhanced RF probes, the usable frequency range may change.
Measurement resistor	RF resistor (low inductance)[a] 1 Ω (±1 %). The measurement resistor can also consist of resistors in parallel, which increases the maximum permissible current through the probe (e.g. 2 Ω//2 Ω) and reduce the stray inductance.
Matching resistor	49 Ω (±1 %)
Maximum current	< 0,5 A
Output impedance Z_O	40 Ω to 60 Ω
Insertion loss in ~~calibration~~ verification circuit	34 dB ± 2 dB
Decoupling in ~~calibration~~ verification circuit	See Figure A.1 and Figure A.5.
Cable connection	Flexible, double shielded coaxial cable with 50 Ω ± 2 Ω line impedance. The RF connector shall be mounted with low reflection. The insertion loss includes the cable and the probe. Changes to the cable length will result in additional attenuation to be considered with the measurement results.
Construction	Coaxial probe or comparable construction, which can be connected to a 4 mm coaxial socket. The measurement resistor shall be as close as possible to the probe tip. It shall be built in such a way that no mechanical damage is possible. The connection of the probe cable shall be coaxial; the probe tips should be replaceable, but nevertheless firmly connected to the cable.

[a] The series impedance caused by the parasitic inductance should be lower than the resistor in the used measurement range.

6.3 Test of the RF current probe capability

The current probe shall be ~~tested for qualification and calibration~~ functionally verified in a test circuit shown and described in detail in Annex A.

6.4 Matching network specification

Based on IEC 61000-4-6, a cabling network can be represented in most cases by an antenna with an impedance of about 150 Ω. In order to get accurate measurement results over the full frequency range, a termination network of ~~150~~ 145 Ω ± 20 Ω shall be used. Usual measurement equipment provides an input impedance of 50 Ω so that the matching network shall match the signal line impedance to the equipment impedance. The circuitry is shown in Figure 4, and the characteristics of the impedance matching network used are shown in Table 2. Additional information of matching networks for differential pin measurements are provided in Annex F and recommendations.

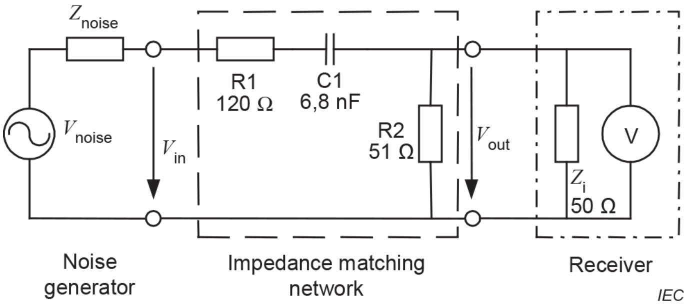

Figure 4 – Impedance matching network corresponding with IEC 61000-4-6

Table 2 – Characteristics of the impedance matching network

Frequency range ~~B_f~~	150 kHz – 1 GHz
Input impedance with 50 Ω termination Z_i	145 Ω ± 20 Ω
Insertion loss within a 50 Ω system	0,258 6 (−11,75 dB ± 2 dB)
Voltage ratio V_{out} / V_{in}	0,173 8 (−15,20 dB ± 2 dB)

7 Test setup

7.1 General test configuration

~~The test set-up shall be in accordance with figure 5.~~ A general test configuration is shown in Figure 5. This general test configuration can be built up in the form of a special test configuration (an example is described in Clause E.2) or in any other configuration, e.g. also in a real application.

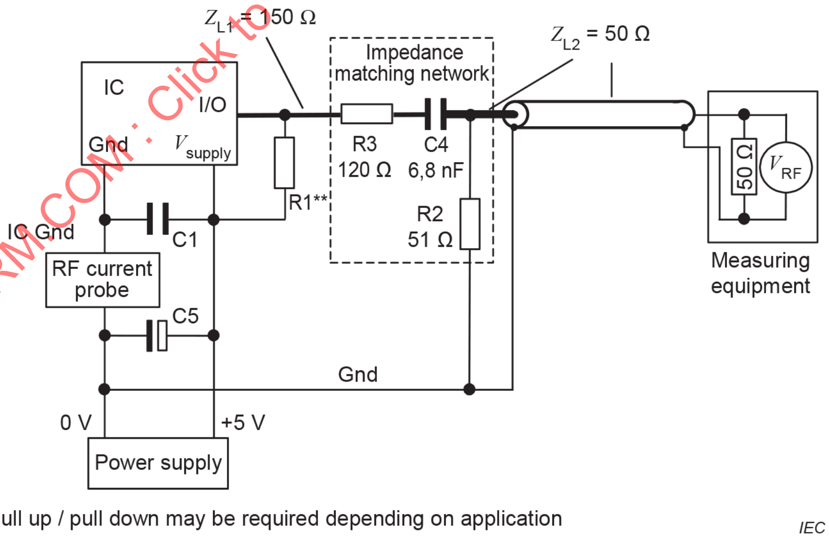

Figure 5 – General test configuration

7.2 Printed circuit test board layout

In order to obtain a high degree of ~~repeatability of measurements~~ reproducibility of measurement results and be able to make a valid comparison between different printed circuit test boards, the following guidance is given.

The test board should be built using PCB material of epoxy type (thickness 0,6 mm to 3 mm, dielectric constant about 4,7). The top side and the bottom side are covered with a minimal 35 µm copper layer.

The bottom layer should be used as ground plane.

If peripheral ground and IC ground are used for the 1 Ω method, these two grounds are isolated by an isolation gap. This isolation gap should be between 0,5 mm and 0,6 mm. If needed, the IC ground shall be located underneath the DUT. The maximum size of this area should not exceed the size of the package minimum footprint by more than 3 mm on each side.

To obtain the necessary accuracy for higher frequencies, parasitic coupling capacitance between IC ground and peripheral ground shall be controlled. This parasitic coupling capacitance between IC ground and peripheral ground shall be lower than 30 pF.

The IC ground is solely connected to the peripheral ground via the 1 Ω probe. ~~A socket for the~~ In case of external RF current probe, a socket should be used. The shield of the RF current probe tip should be connected to the RF peripheral ground by the socket, while the IC ground or the IC ground pin is connected to the current probe tip. The connection between the IC ground and the probe tip shall be as short as possible. In any case, the trace length shall not exceed 15 mm. The trace should be connected to the IC ground at the shortest distance to the centre point of the DUT.

If the above-mentioned ~~directives~~ guidelines are not applicable, the transfer characteristic of modified design shall be determined and documented in the test report.

The DUT and all components needed to operate the DUT should be mounted onto the top side of the test board. As much wiring as possible should be routed in the top layer. The ~~device under test~~ DUT should be placed in the centre of the PCB, while the needed matching networks should be placed around this centre. The wiring between the IC pins and the matching network should be designed to have a line impedance of 150 Ω. In case the 150 Ω line impedance is difficult to implement, the line ~~must~~ shall be of the maximum reasonable impedance but short enough, in order to comply with the requirements of Table 2.

The wiring of the outputs of the matching networks should be designed to have a line impedance of 50 Ω. An example of a PCB layout can be found in Annex E.

The supply shall be connected with a single wire directly to the capacitor C5. C5 could be a surface mount device, of electrolytic type and having a value of at least 10 µF. The capacitor C5 shall be positioned near the probe socket.

The test board may have any rectangular or circular shape.

Additional information and guidelines for extended frequency applications are described in Annex G.

8 Test procedure

The requirements for the test procedure are described in IEC 61967-1.

9 Test report

The requirements for the test report are described in IEC 61967-1.

Emission measurement results may be presented using classification or reference levels. An example of a classification scheme for emission levels is presented in Annex B. In addition, Annex C shows how this classification scheme may be applied to set up reference levels for ICs used in the automotive industry.

Annex A
(~~normative~~ informative)

Probe ~~calibration~~ verification procedure

The test circuit shown in Figure A.1 is recommended for the probe ~~calibration~~ verification. It consists of a PCB laid out using microstrip techniques (see Figure A.3). The PCB has an input port to which the RF generator is connected. The RF current probe to be ~~calibrated~~ verified is connected to the output port. The RF current probe output is connected to a test receiver (see Figure A.4). This ~~calibration~~ verification procedure measures the isolation provided by the test circuit in a 50 Ω system (see also CISPR 16-1-2 [1][2]) and the insertion loss of the RF current probe.

Two separate measurements are ~~required~~ recommended. The first measurement is performed with the test circuit configured as shown in Figure A.1, circuit diagram A. Note that clamp A is not inserted. While sweeping the RF generator over the required frequency range, measure the voltage appearing at the output of the RF current probe.

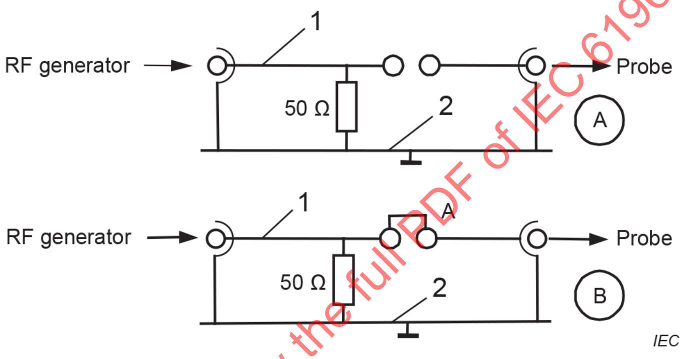

Figure A.1 – Test circuit

The second measurement is performed identically to the first one but with clamp A installed to shunt the RF generator to the probe input as shown in Figure A.1, circuit diagram B. This measurement results in the RF current probe insertion loss which indicates its sensitivity. Figure A.2 shows a result of such a measurement.

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[2] Numbers in square brackets refer to the Bibliography.

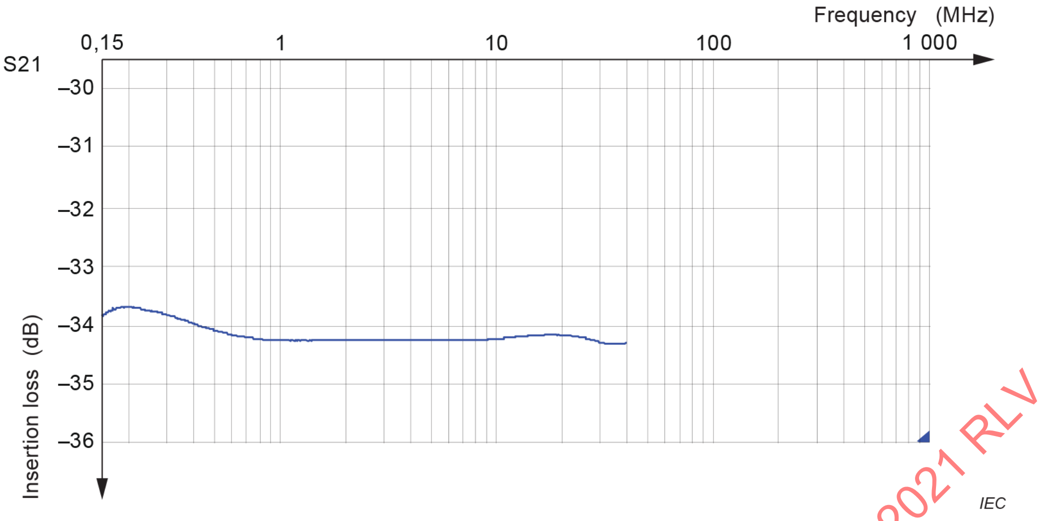
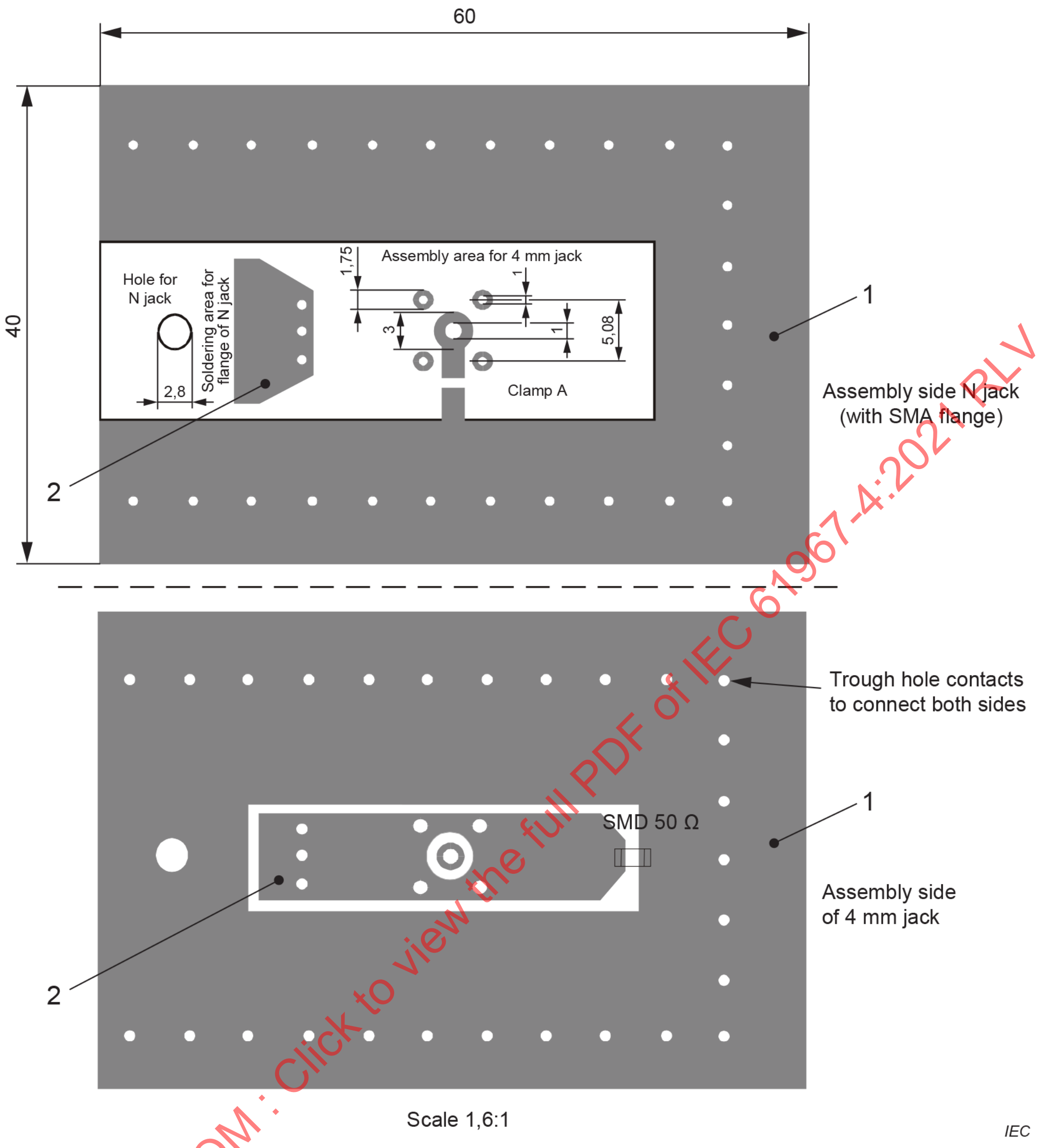


Figure A.2 – Insertion loss of the 1 Ω probe

The calculated difference of both measurements is called the "decoupling". The decoupling ~~shall~~ should be above the limit shown in Figure A.5. The decoupling is equal to the measurement dynamics in relation to the signal source. The decoupling does include the quality characteristics, the sensitivity and the shielding of the probe.

Dimensions in millimetres



Key

1	coupling area
2	reference ground

Figure A.3 – Layout of the ~~calibration~~ verification test circuit

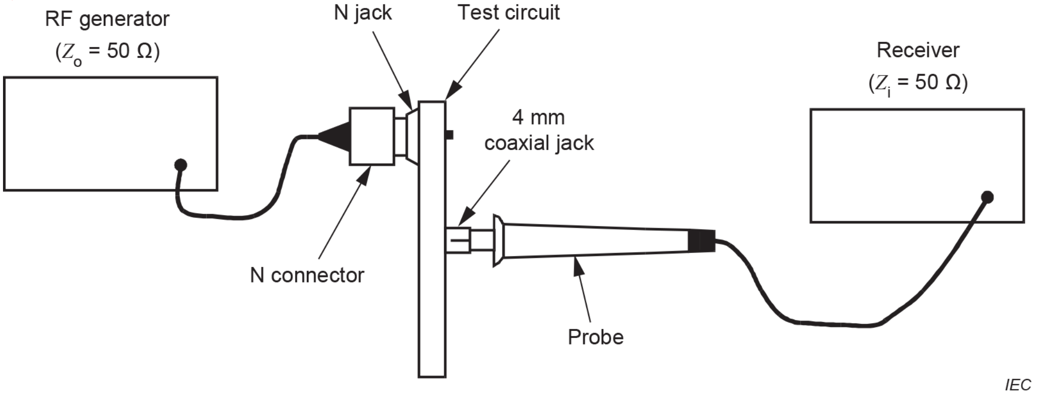


Figure A.4 – Connection of the ~~calibration~~ verification test circuit

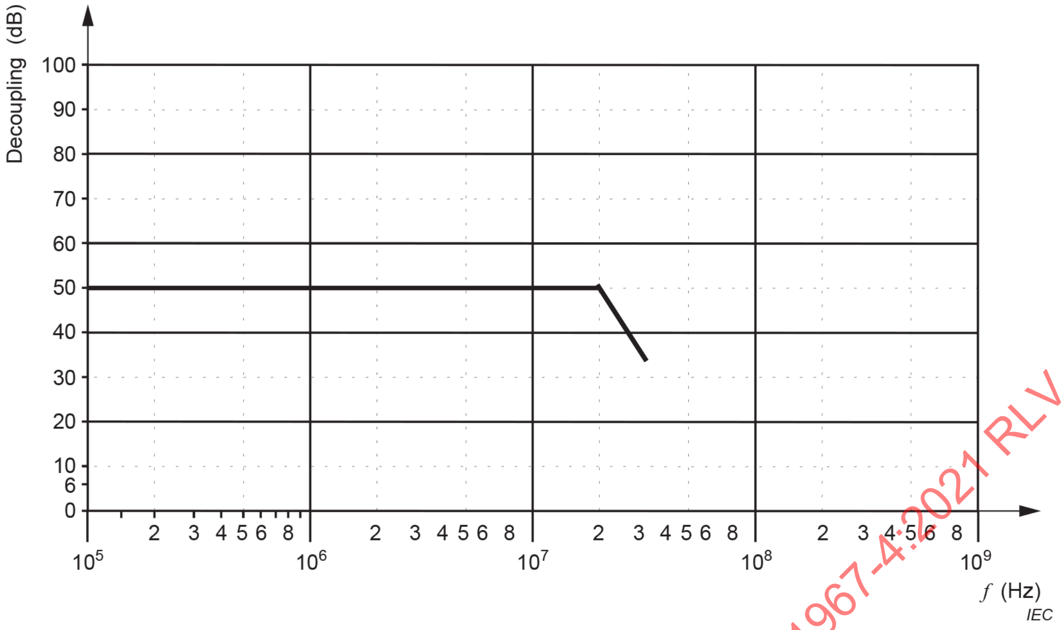


Figure A.5 – Minimum decoupling limit versus frequency

In order to evaluate the performance and the applicable frequency range of the used 1 Ω probe, it is recommended to characterize the probe input impedance characteristic. This can be done with a scattering parameter measurement using a vector network analyser. For the measurements, the vector network analyser should be calibrated including all connectors, cable and traces to exclude all setup parasites from the result. An example of a 1 Ω probe input impedance characteristic is shown in Figure A.6.

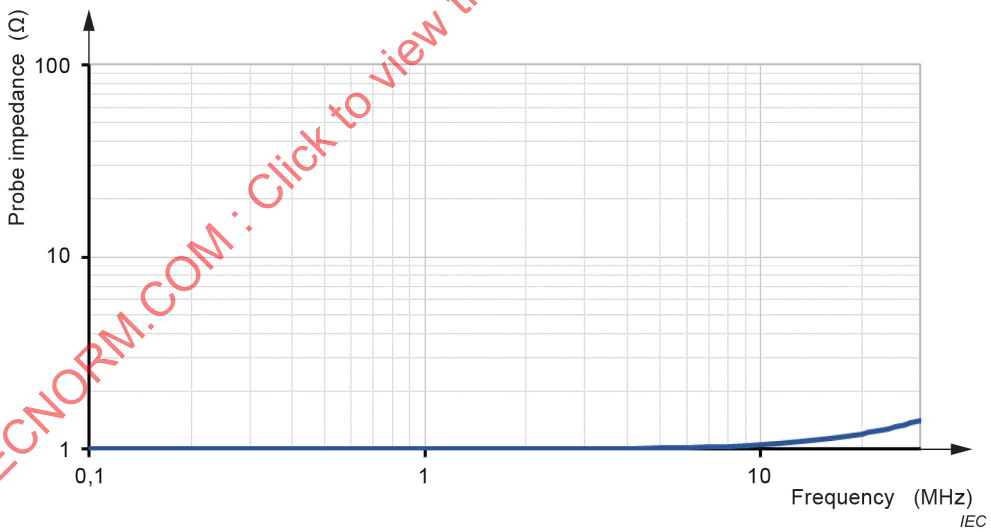


Figure A.6 – Example of 1 Ω probe input impedance characteristic

Annex B
(informative)

Classification of conducted emission levels

B.1 Introductory remark

The purpose of this Annex B is to provide a method of classifying the conducted emissions levels of integrated circuits by application of the test conditions described in this specification.

B.2 General

This annex is not intended to specify or imply conducted emissions limits for ICs. However, by careful application and agreement between manufacturer and user, it is possible to develop a device specification that specifies the maximum conducted EME allowable for a specific integrated circuit in a specific application when tested in accordance with the procedures in this document.

It should also be noted that Annex B is not meant to be a product specification and cannot function as one. Nevertheless, using the concept described in this document and by careful application and agreement between manufacturer and user, it would be possible to develop a document giving the EME behaviour for a specific integrated circuit.

B.3 Definition of emission levels

The diagram in Figure B.1 defines the conducted emissions classification levels used to define the overall envelope of the measured emissions. This diagram can be used to classify both the RF current measured with the RF current probe and the RF voltage at IC pins, measured using the impedance matching network.

The scheme follows the theory of a periodical trapezoidal pulse response and offers three different slopes of emission amplitudes with a 6 dB distance:

- 0 dB/decade (theory: constant amplitude line till the first corner frequency $1/(\pi\tau)$)
- −20 dB/decade (theory: decrease of amplitude till second corner frequency $1/(\pi\tau_r)$)
- −40 dB/decade (theory: decrease of amplitude at frequencies $>1/(\pi\tau_r)$).

The corner frequencies are dependent on the rise/fall times (τ_r) and the duration (τ) of the pulse.

The emission level diagram shown in Figure B.1 enables the selection of different slopes for different frequencies to better describe the measured conducted EME. The EME can be described with one, two or three slopes as required to best fit the measured data.

Various combinations are possible reflecting the actual requirements of the application much more precisely (e.g. adapted to the switching frequency of the ports of a microcontroller).

B.4 Presentation of results

B.4.1 General

The description of the maximum emission level can consist of up to three digits. Each digit represents one of three available slope identifiers as described in Clause B.3 and shown in Figure B.1. Capital letters are used to indicate a 0 dB/decade slope. Numbers are used to indicate a −20 dB/decade slope. Small letters are used to indicate a −40 dB/decade slope.

Assuming that one of the three slopes is not needed, then the corresponding letter or number will be left off. The defined maximum emission level in Figure B.1 offers a standardised way to communicate maximum emission levels unambiguously.

In general, the first digit is a capital letter that represents the maximum amplitude of the measured data. The second digit can either be a number or small letter that defines the position of the −20 dB/decade slope or −40 dB/decade slope, respectively. The third digit can be a capital letter, small letter or number.

In the case of measured emissions that approximate those resulting from a trapezoidal waveform, the capital letter is first and represents the position of the horizontal line with 0 dB/decade slope. Second is the number which defines the slope of −20 dB/decade. The third and small letter defines the position of the −40 dB/decade slope.

The points of intersection of the slopes represent the first and second corner frequencies as described in Clause B.3.

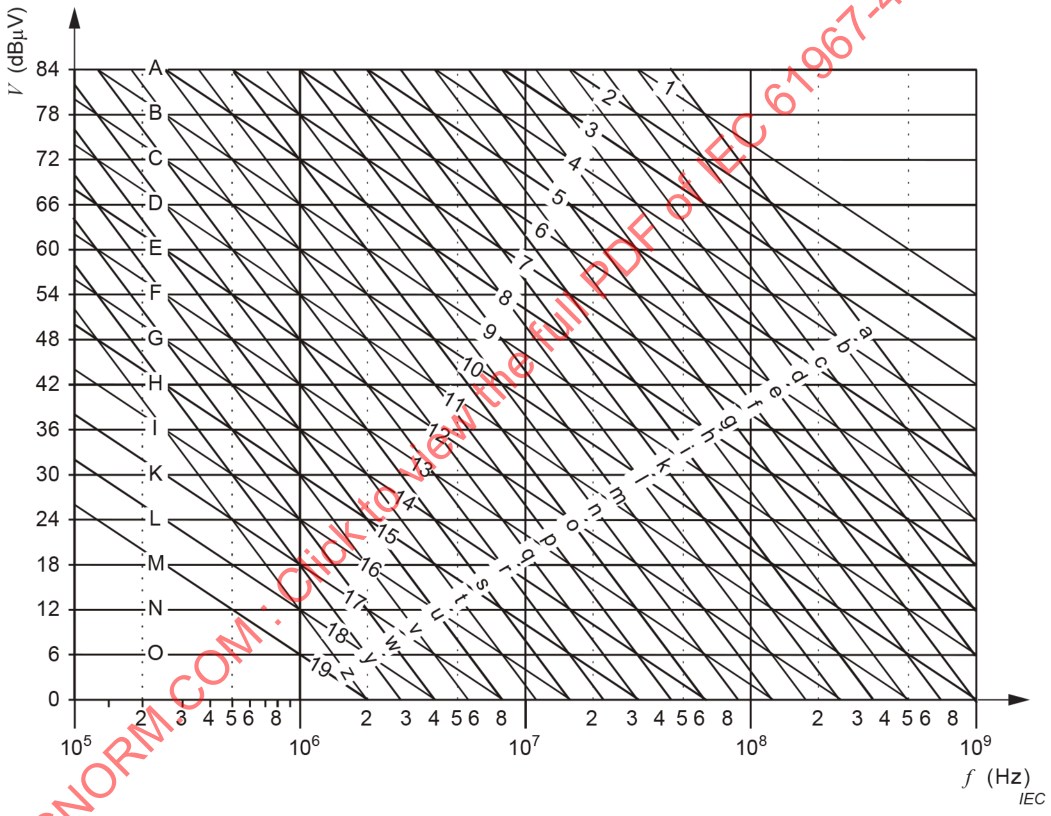


Figure B.1 – Emission level scheme

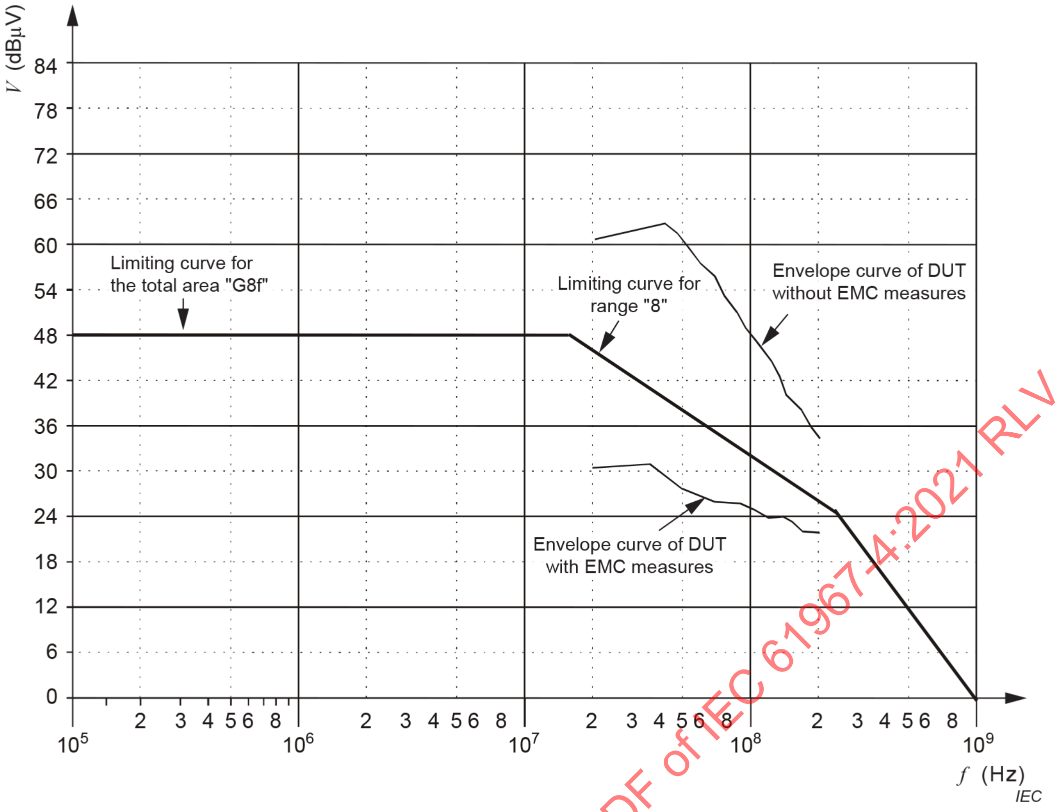


Figure B.2 – Example of the maximum emission level G8f

B.4.2 Examples

Figure B.2 represents an example whereby slope lines “G”, “8” and “f” are selected to describe the measured IC conducted EME.

Other notations are also possible:

“8f”: no 0 dB/decade slope; this is useful if the lowest frequency to be measured is higher than the first corner frequency;

“f”: only the −40 dB/decade slope is used; this is useful if the lowest frequency to be measured is higher than the second corner frequency;

“8”: only the −20 dB/decade slope is used; this is useful if the lowest frequency to be measured is higher than the first corner frequency, and the highest frequency to be measured is lower than the second corner frequency.

This second example shows how the IC supplier ~~might~~ can characterise the emission performance of an integrated circuit for sales or engineering purposes. Table B.1 shows the limit curves (voltage) for all IC pins and the limit curve for the sum current (given in dBµV).

Table B.1 – Emission levels

PIN number	Limit curve
1	H11m
2	H11m
3	H11m
4	H11m
5	H11m
6	13q
7	13g
8	
Sum current	L15s

Annex C
(informative)

Example of reference levels for automotive applications

C.1 Introductory remark

Annex C contains examples of reference levels intended to be used on the emission test procedures according to this standard for the measurements of radio disturbances in the frequency range of 150 kHz to 1 000 MHz.

The reference levels are a selection from the scheme in Annex B. It applies to semiconductors used for automotive components. The requirements for semiconductors on other applications may be different.

The reference levels in this Annex C are recommended and subject to modification as agreed between the vehicle manufacturer, the component and the semiconductor supplier.

Based on the experience of the automotive industry, the following is stated:

Semiconductor emission measurements cannot completely characterise the disturbance capability of electronic vehicle components in which they are applied. The reason for this is seen in various effects in the vehicle and vehicle components (e.g. grounding, resonance, attenuation and coupling), which ~~may~~ can also contribute to the emission behaviour or change the emission behaviour. Therefore, semiconductor emission measurements cannot fully replace vehicle and component measurements according to CISPR 25 [2].

C.2 General

Since the mounting location, vehicle body construction, harness, grounding and printed circuit board (PCB) design can affect the coupling of radio disturbances generated by the operation of semiconductor devices to the on-board radio, this annex defines reference levels.

The levels to be used on a specific semiconductor device (as a function of frequency band) are to be agreed by the vehicle manufacturer, the component and the semiconductor supplier.

In specific cases, a deviation from these reference level classes can be agreed between the users of this document in accordance with Annex D.

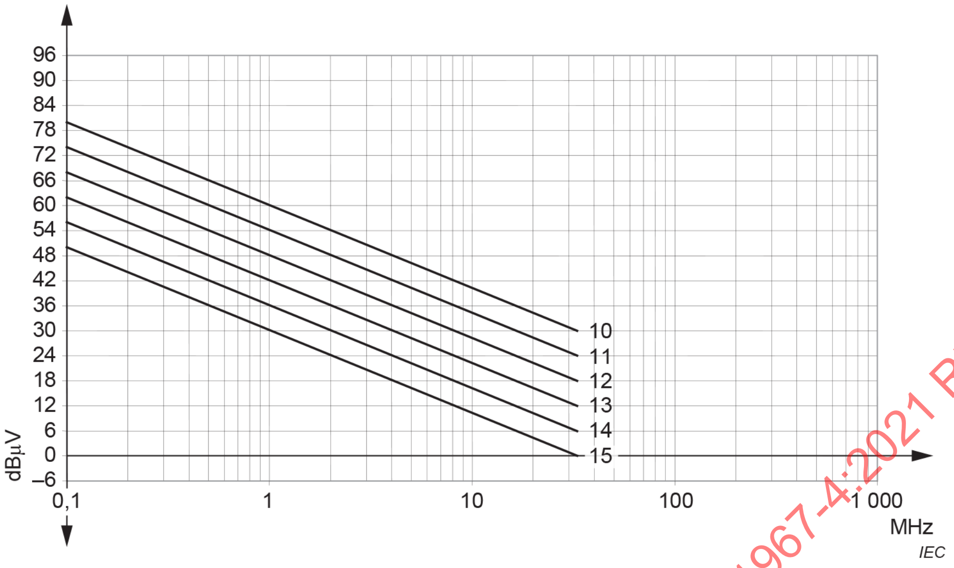
C.3 Reference levels

C.3.1 General

For acceptable radio reception in a vehicle, the conducted noise should not exceed one of the agreed values shown in Figure C.1 and Figure C.2.

NOTE Results of measurements using the 1 Ω method do not correspond to those using the 150 Ω method in all cases (e.g. in cases of different source or terminal impedance).

C.3.2 Measurements of conducted emissions, 1 Ω method



NOTE Reference levels shown up to 30 MHz due to current usable probe range

Figure C.1 – 1 Ω method – Examples of reference levels for conducted disturbances from semiconductors (peak detector)

Conformance with the reference levels in Figure C.1 does not ensure a sufficient noise suppression emitted by a semiconductor in all cases, e.g. if the disturbance currents distribution does not include all significant lines. However, measurements only on the ground lines can often give an average impression concerning the semiconductor's capability to emit disturbances.

C.3.3 Measurements of conducted emissions, 150 Ω method

This method is able to characterise the emission levels on single pins. Therefore, it is usual that further measurements have to be performed to completely describe the semiconductor's capability to emit disturbances.

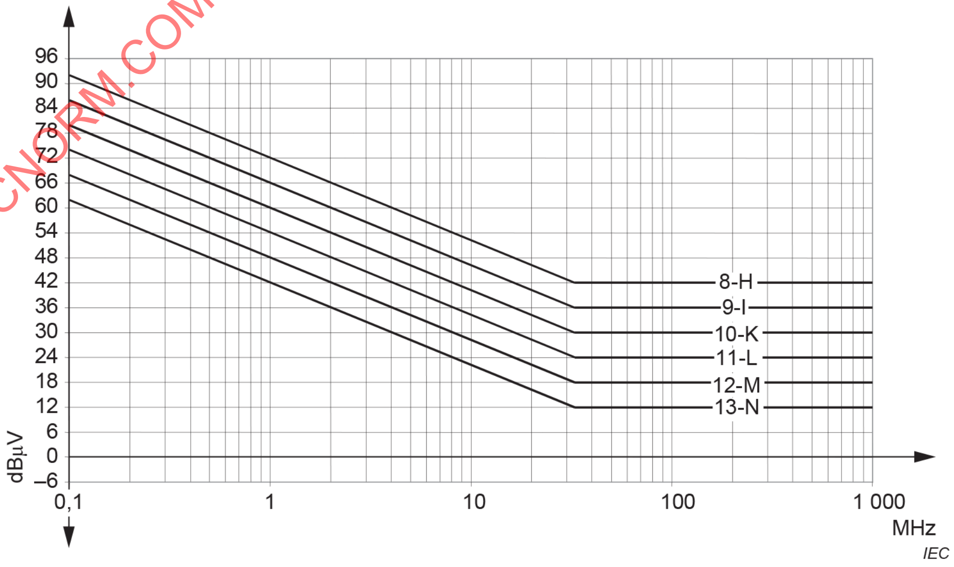


Figure C.2 – 150 Ω method – Examples of reference levels for conducted disturbances from semiconductors (peak detector)

Annex D
(informative)

EMC requirements and how to use EMC IC measurement techniques

D.1 ~~Introduction~~ Introductory remark

The development of EMC optimised systems, modules and ICs requires the definition of emission classification levels and suitable test procedures to measure the generated emissions. EMC standards with emission limits exist for electronic systems, subsystems, and modules, but do not yet exist for the ICs used within those systems, subsystems and modules. Standardised IC EMC measurement procedures are attempting to close the gap, but significant problems exist which ~~must first~~ need to be overcome first.

D.2 Using EMC measurement procedures

Based on what is known today, a full qualification of an IC can only be obtained if, together with the RF current measurement, the individual pins are also measured applying the single pin method. In specific applications with reduced requirements, only a selection of pins may be tested with the single pin method. If this has been made, this has to be documented with an explanation for the user.

Table D.1 lists some possibilities whereby the measurement procedure can be reduced.

Table D.1 – Examples in which the measurement procedure can be reduced

Component related parameters	Configuration of the IC
– Several pins not used and therefore not connected to the PCB (no potential current loop) – Existing blocks on the IC not used	– Several pins (I/O ports) with the same EMC behaviour

Because of different technical ambient parameters (see also Table D.2), there is no direct correlation possible between system and module EMC measurements as well as between module and IC EMC measurements. The final approval of a module, and therefore also for the IC, is only possible after a successful EMC measurement of the system.

Normally, additional suppression of interference is needed such as filters and metal screening. The implementation of those various EMC measures within the IC and/or outside the IC on the PCB is very much dependent on the cost aspects and feasibility (space availability, etc.).

D.3 Assessment of the IC influence to the EMC behaviour of the modules

Depending on the development status of a system, different aspects can be seen in relation to the EMC:

a) selection of existing ICs, which are already used in other systems of the same application field, and in production with a known EMC behaviour;

b) redesign of ICs, which are already used in other applications and in production;

c) customised ICs for systems for the same field of application.

In the case of a), the experience of the system manufacturer/subcontractors is necessary in order to understand and decide which EMC ambient parameters will influence the IC. The selection of the maximum emission levels will be based on these parameters (see Table D.2).

Table D.2 – System- and module-related ambient parameters

Component-related ambient parameters	System-specific ambient parameters
– Ground concept	– System type
– Filter concept	– Fitting area of the module
– Screening	– Fitting area of the antenna
– Layout	– Ground concept
– Working conditions, software	– Wiring harness concept

In the case of b), Table D.3 lists a set of development activities, which influence the EMC behaviour of the system.

In the case of c), the EMC IC requirement has to be determined based on the application. The product specification needs to define the maximum emission levels and the extent of the measurements to be taken in order to achieve a successful development.

Table D.3 – Changes at the IC which influence the EMC

Changes on silicon	Changes off silicon
– Hardware redesign	– Change of leadframe
– Change of chip layout	– Change of package
– Shrink to smaller geometry	– Change of V_{supply}
– Software changes (user's responsibility)	

In all cases, a preliminary decision should be taken to accept the test results of the ICs based on the proposed measurement method.

Annex E
(informative)

Example of a test setup consisting of an EMC main test board and an EME IC test board

E.1 Introductory remark

Annex E describes a test setup, which has been designed for propagation delay measurements of fast logic devices; it is well suited for EMC measurements too. The setup consists of an EMC main test board, which can be used for all measurements with no change in layout. Up to 84 connections can be made to the so-called EME IC test board. This test board carries the IC under test together with the components needed to let the IC operate and the components of the 150 Ω to 50 Ω matching network. Consequently, the IC test board has to be designed from new for each IC or at least for a group of ICs. In this annex, both test boards are described.

E.2 EMC main test board

Clause E.2 describes the EMC main test board, which is built to comply with a 50 Ω impedance measurement equipment. The EMC main test board (see Figure F.1) is used to connect the EME IC test board to the measurement equipment. It is built on a seven-layer printed circuit board with the dimensions 293 mm × 293 mm. The three inner layers are used as power supply layers V1, V2 and V3 for the EME IC test board. The following layers on both sides are ground layers, which are also used as the RF-shield ground to the signal layers on the top and the bottom of the PCB.

The EME IC test board is mounted on top of the EMC main test board and centred with four screws (M3x6; the length of the screws is dependent on the thickness of the EME IC test board). The screws provide the ground connection between EMC main test board and EME IC test board. All other electrical connections are made through the 84 pogo-pin ring. The pogo pins are soldered into the main board and are mechanically fixed with a ~~PTFE ring~~ nonconductive ring, e.g. made of Teflon (polytetrafluorethylen – PTFE). Four of the 84 connections are already connected with the power supply lines V1, V2, V3 and GND, and are used to provide the power supply to the EME IC test board.

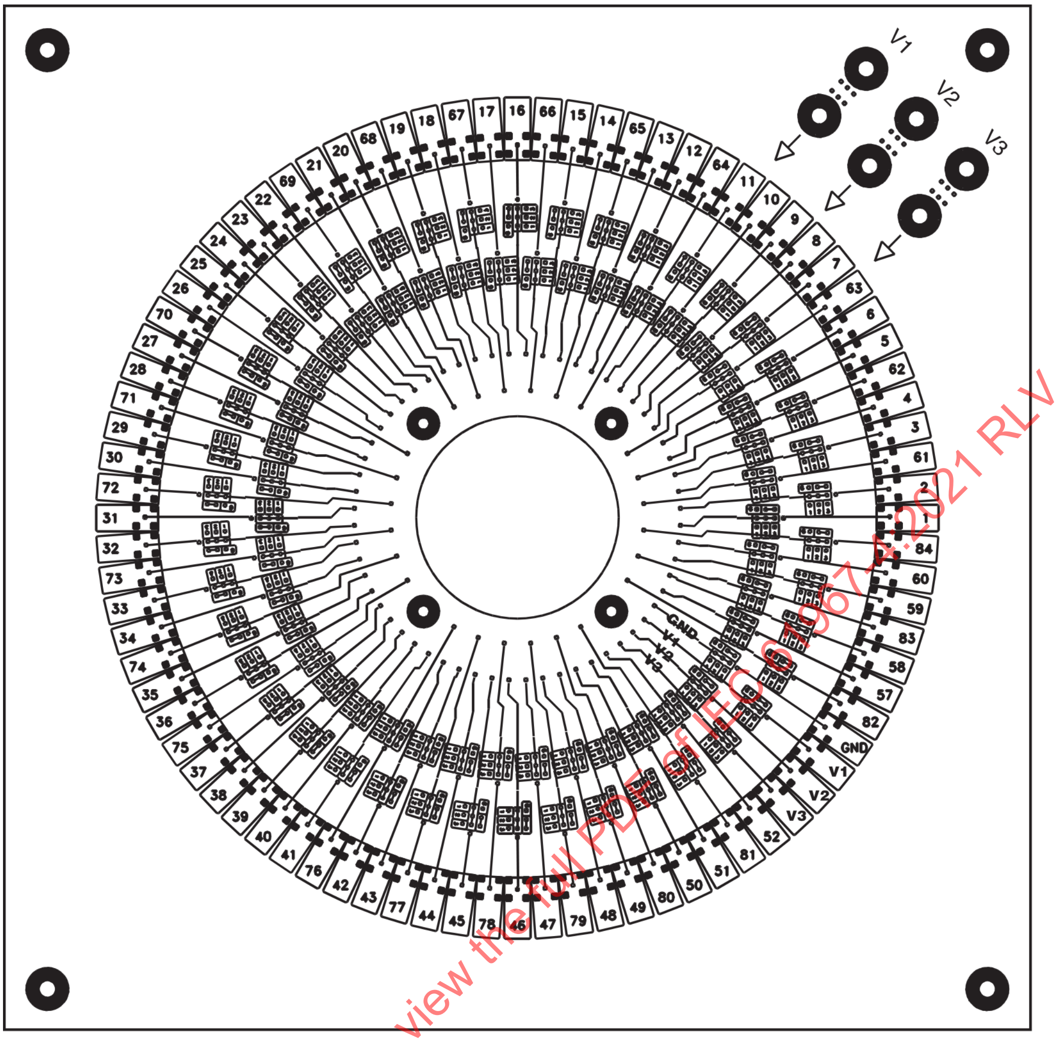


Figure E.1 – EMC main test board

All 84 signal lines are routed on the top layer and are implemented as a stripline with a 50 Ω line impedance. The striplines connect the pogo pins with the miniature coax connectors on the outer side, where the measurement equipment is connected. Each signal line is connected to a jumper field, which allows the connection to the coax connector or one of the four supply lines V1, V2, V3 and GND (see Figure E.2).

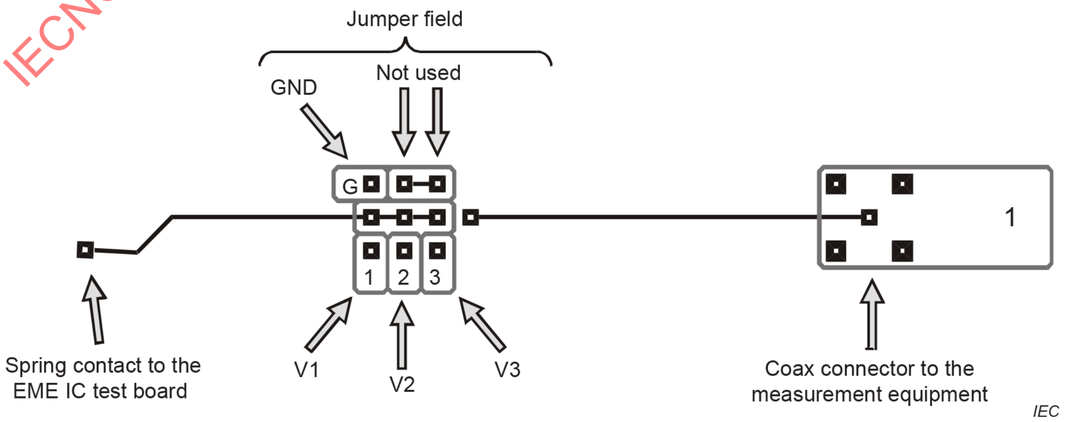


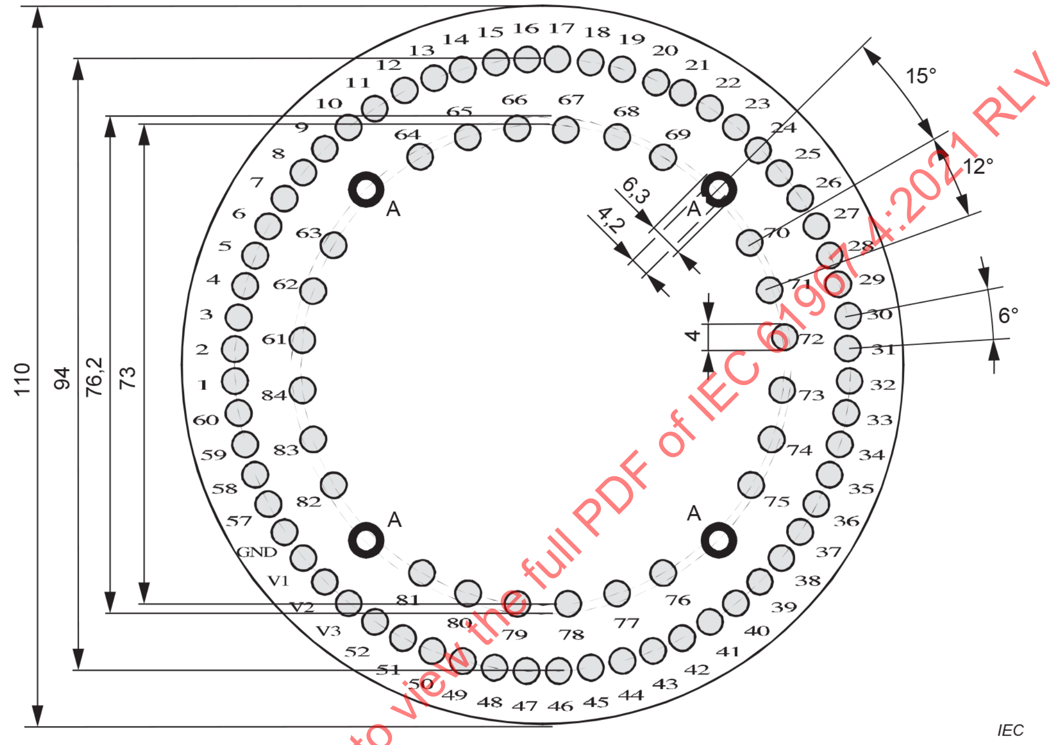
Figure E.2 – Jumper field

E.3 EME IC test board

E.3.1 General explanation of the test board

Figure E.3 shows a mechanical drawing of the bottom side of the IC test board. For each IC test board, the positions of the spring contact area and the through-hole connections remain as shown in the drawing. Other parts on the IC test board may be laid out as needed for the IC under test (see an example in Figure E.5 and Figure E.6).

Dimensions in millimetres



NOTE The through-hole connections **A** are used as Gnd connections to the EMC main test board.

Figure E.3 – EME IC test board (contact areas for the spring connector pins of the main test board)

E.3.2 How to build the test system

The EME IC test board should be constructed in such a way that the operating conditions of the DUT correspond to those of a typical application.

The EME IC test board ~~shall~~ should have three ground connections: IC ground, peripheral ground and RF-shield ground (see Figure E.4, Figure E.5, Figure E.6).

All components, which are normally placed close to the IC in the final application, should be close to the IC on the EME IC test board, too. They should be connected to the IC ground in order to measure only those noise currents which are relevant for emission. The EME current can be measured with the RF current probe.

All other connections, which are possibly made directly to external cabling or long PCB traces, should be connected to an impedance-matching network. This matching network is connected to the peripheral ground on the component side of the PCB. This allows single point measurements using 50 Ω impedance measurement equipment according to the specification in 6.4 (see also Figure E.4, for example R3, C4, R2). In order to obtain constant RF characteristics in a large frequency range, the peripheral ground and the RF-shield ground should be connected close to the matching network (see also Figure E.4, connection d3).

EME relevant currents returning to the IC through the peripheral ground and RF-shield ground can be measured by connecting them to the IC ground using only the 1 Ω RF current probe.

PCB specification:

– Size:	Circular PCB, maximum diameter 110 mm (for mechanical size, see Figure E.3)
– Material:	
epoxy type:	NEMA FRL
thickness:	3 mm
copper:	35 µm
layers:	2
dielectric constant:	4,7

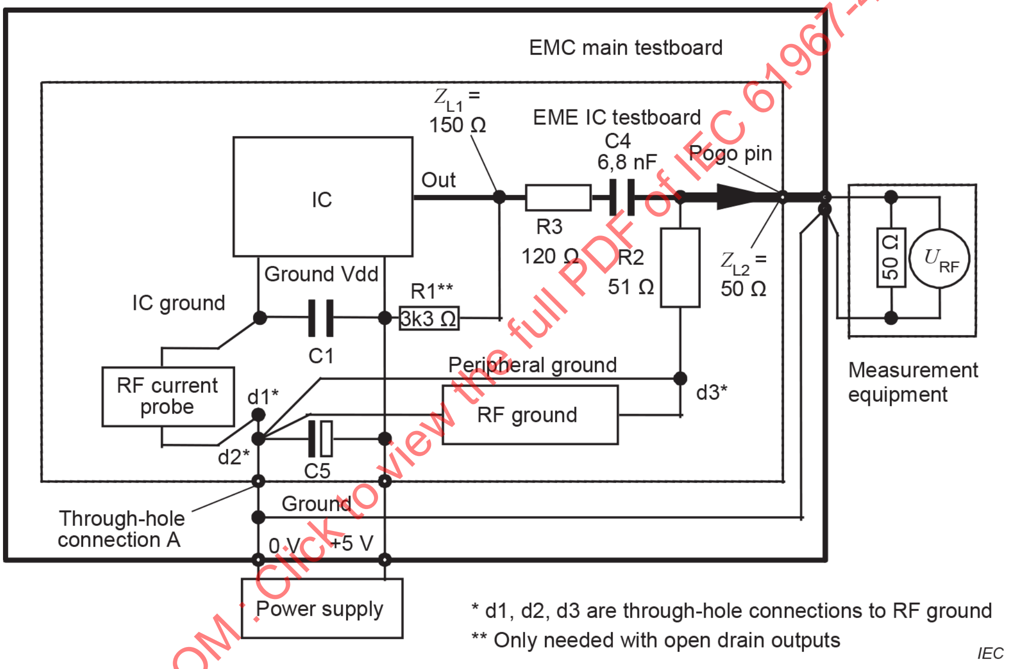


Figure E.4 – Example of an EME IC test system

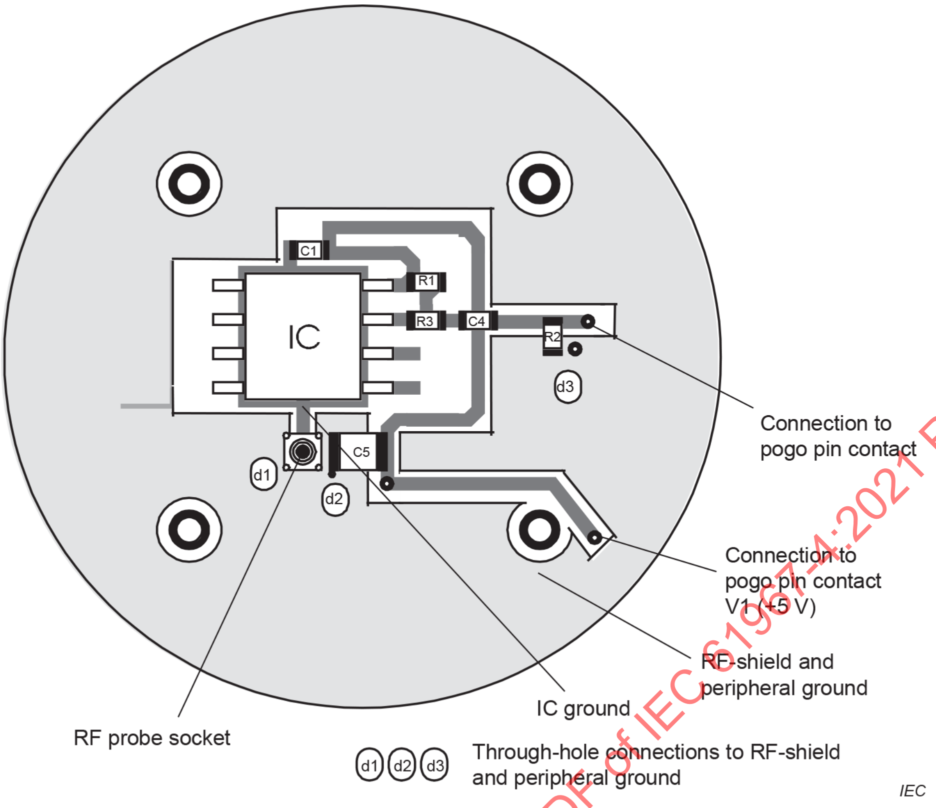


Figure E.5 – Component side of the EME IC test board

E.3.3 PCB layout and component positioning

In order to achieve a high degree of ~~repeatability~~ reproducibility of measurement results between different test boards, the EMC IC test board has to meet certain requirements.

The IC PCB traces should have an impedance of 150 Ω to connect the impedance matching network with low reflection. To achieve this, the PCB traces should be made in microstrip line technique, whereby the signal trace is carried on the component side and the RF-shield ground on the bottom side. For a dielectric constant of approximately 4,7, the ratio of track width to the thickness of the PCB should be 0,1 which results in a PCB thickness of 3 mm to a track width of 0,3 mm.

The IC under test should be centred and mounted onto the component side (see also Figure E.5).

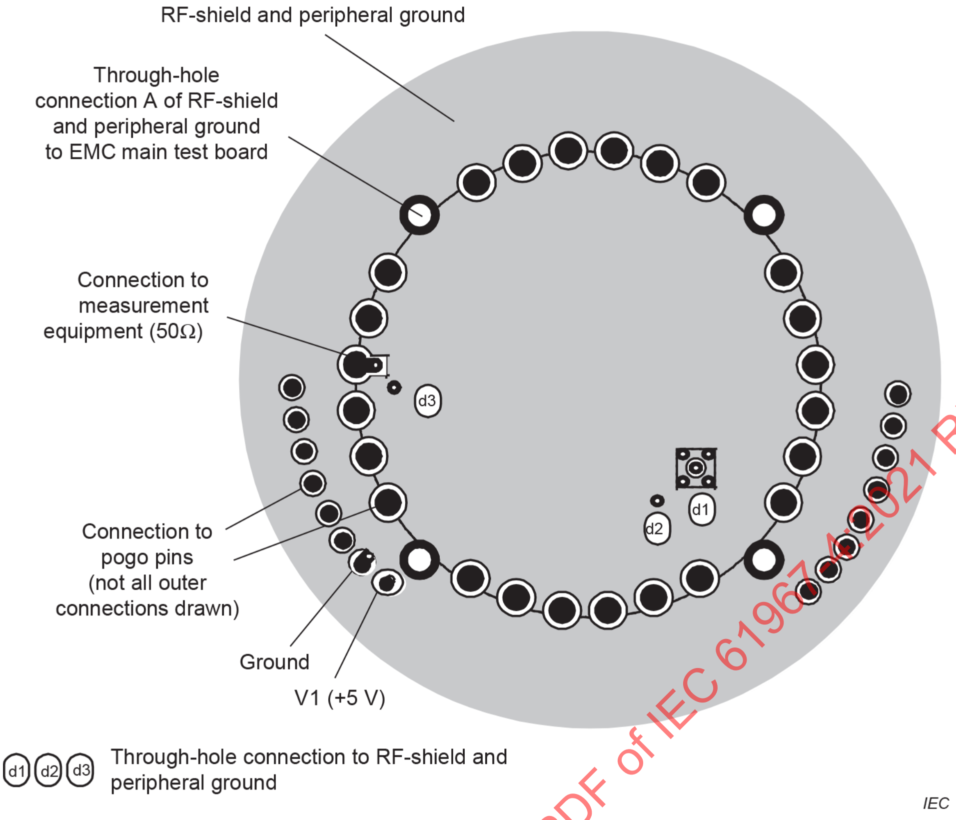


Figure E.6 – Bottom side of the EME IC test board

The impedance matching network should be placed on the outer side close to the pogo pin, so that the connection from the EME IC test board to the EMC main test board achieves a transfer impedance of 50 Ω. SMD components should be used (see Figure E.4).

The IC ground, the peripheral ground and Vdd should be routed on the component side. Ideally, the bottom side should be a continuous area of RF-shield ground and no signal traces should be routed if possible (see Figure E.6).

Apart from the central connection of peripheral ground and RF-shield ground at the matching networks (Figure E.5, Figure E.6, connection d2), they ~~shall~~ should be connected at one additional point (preferably at the supply filter capacitor C5).

Annex F
(informative)

150 Ω direct coupling networks for common mode emission measurements of differential mode data transfer ICs and similar circuits

F.1 Basic direct coupling network

In Figure F.1 the basic circuit of a coupling network is shown. The resistors R4, R5 and R6 represent termination resistors which ~~may~~ can be needed to operate the DUT properly. They also may be incorporated in the coupling network in whole or in part if appropriate. Examples are shown later (see Clauses F.2, F.3 and F.4).

~~NOTE~~ Other types of coupling networks, e.g. ~~z-transformers~~ impedance matching networks and suitable couplers as defined in the ~~CISPR 16-1 series, may~~ CISPR 16-1-2 [1] can be used too.

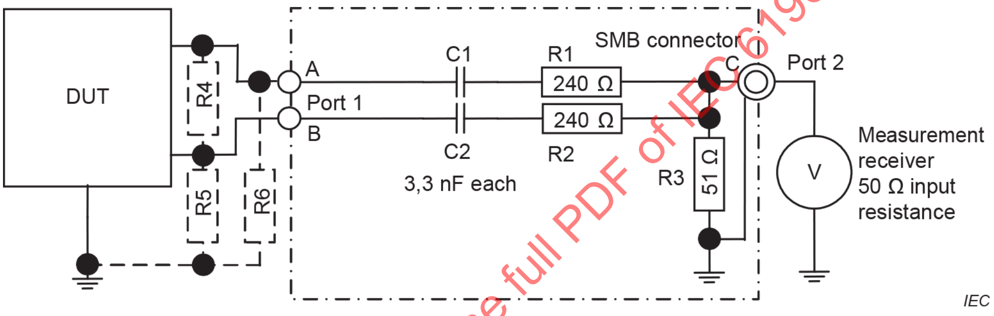


Figure F.1 – Basic direct coupling for common mode EMC measurements

The connections A and B have to be connected to the DUT during the emission or immunity measurement. For the emission measurement, a test receiver is connected to connection C.

By default, the resistor values R1, R2 will be chosen to represent a common-mode 150 Ω load together with R3 in parallel connection with the test receiver input impedance. The common-mode impedance tolerances from IEC 61000-4-6 ~~shall~~ apply.

R1 and R2 ~~shall~~ should closely match. By default, the matching tolerance ~~shall~~ should be better than 10^{-3}. The values of C1 and C2 are about half of the value of the capacitor value used for a single pin measurement setup. C1 and C2 ~~shall~~ should also closely match. Because the impedances of C1 and C2 ~~shall~~ should be small compared respectively to R1 and R2, the matching tolerance may be not so tight as with the resistors. By default, for C1 and C2 a matching tolerance of better than 10^{-2} is sufficient.

The absolute values of R1 and R2 may be changed if needed for proper function of the IC or other needs. In that case, the new values ~~have to~~ shall be presented in the test report and test specification together with the S21 measurement and S21 calculation.

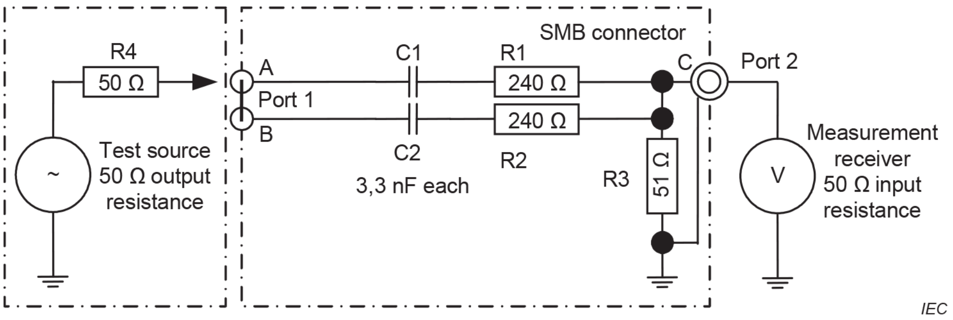


Figure F.2 – Measurement setup for the S21 measurement of the common-mode coupling

For the measurement of the S21 of the coupling network with respect to emission, the IC is replaced by a test source and connection A and B are connected together to form port 1 (see Figure F.2). Due to the simple coupling network, the magnitude of S21 can be estimated by the following equation:

$$|S21| = 20 \times \log\left(\frac{2 \times (R3 // 50)}{R1 // R2 + R3 // 50 + R4}\right) (\text{dB})$$

C1 and C2 are used for DC-blocking. They cause a deviation from the calculated value of S21 towards low frequencies. The corner (−3 dB) frequency can be estimated with the following equation:

$$f_{c\_s21} = \frac{1}{(4 \times \pi \times C1 \times (0{,}5 \times R1) + R3 // 50) + R4}$$

Taking the values in Figure F.3 as an example, the calculation results in:

$|S21| = -11{,}8$ dB

$f_{c\_s21} = 123{,}5$ kHz

F.2 Example of a common-mode coupling network alternative for ~~high speed CAN or~~ LVDS or RS485 or similar systems

In Figure F.3, the RF-coupling network is changed to get an appropriate termination for the ~~high speed CAN~~ bus (60 Ω). This termination can also be used for the measurement of other communication ICs that operate with such low differential termination impedance.

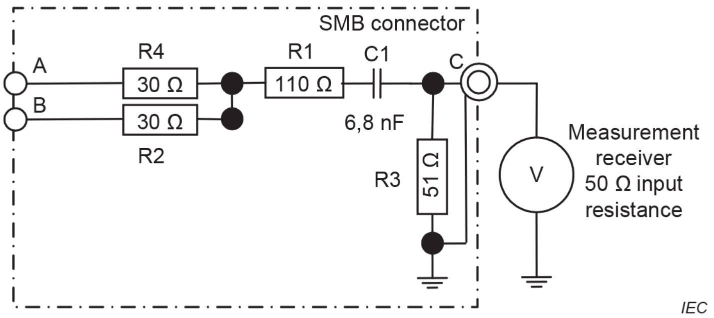


Figure F.3 – Using split load termination as coupling for measuring equipment

NOTE R1, R2 and R4 as a star-network can be substituted by a delta-network instead, which would allow the line-loading resistance to be applied outside this network.

The calculation of the relevant parameter results in:

|S21| = −12 dB

f_{c_S21} = 117 kHz.

F.3 Example of a common-mode coupling network alternative for differential IC outputs to resistive loads (e.g. airbag ignition driver)

Here, the basic principle of the split termination coupling is adapted to a differential load of only 2 Ω.

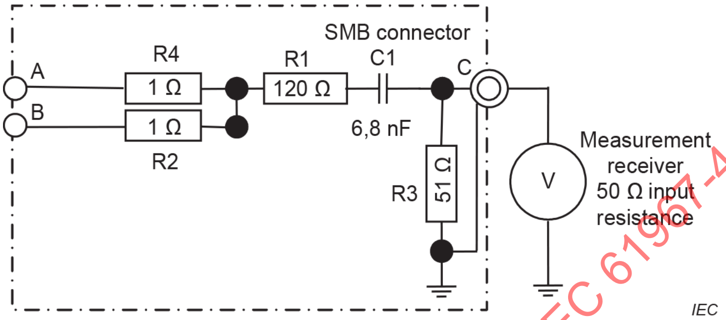


Figure F.4 – Using split load termination as coupling for measuring equipment

The results of the calculation are as follows:

|S21| = –12,2 dB

f_{c_S21} = 114 kHz

F.4 Example of a common-mode coupling network for ~~fault tolerant~~ CAN systems

This exclusive example coupling network is already in use. ~~Fault tolerant~~ CAN systems do not have a differential termination which can be used for injection. Thus, the basic configuration (see Figure F.1) is used with changed component values (see Figure F.5). The S21 is now changed from −11,8 dB to −8,6 dB. This has to be shown in the test report by S21 measurement and by calculation.

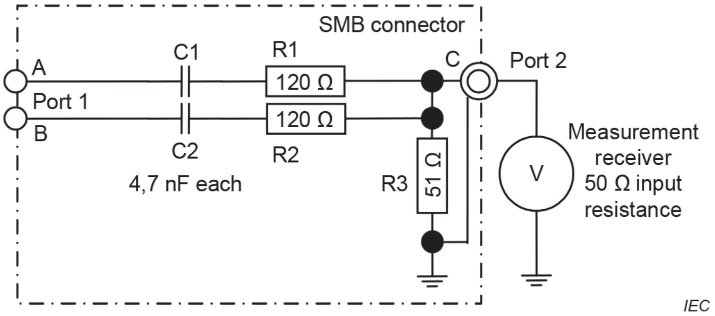


Figure F.5 – Example of an acceptable adaptation for special network requirements (e.g. for ~~fault tolerant~~ CAN systems)

NOTE This network does not represent the 150 Ω common-mode loading as indicated.

The results of the calculation are as follows:

|S21| = −8,6 dB

$f_{c\_S21} = 125\ \text{kHz}$

Annex G
(informative)

Measurement of conducted emissions in extended frequency range

G.1 General

The measurement methods described in the main part of this document have been developed to enable reliable and comparable measurements of conducted emissions at pin level of ICs in the frequency range from 150 kHz up to 1 GHz. This was based on the assumption that relevant emissions of IC applications are caused by RF currents or voltages generated by internal circuit blocks of the IC which are distributed via IC pins, PCB traces and the connected wiring harness.

New digital broadcast and mobile services with operating frequencies up to 6 GHz create a demand for RF emission results of ICs also in an extended frequency range. The frequency range above 1 GHz is currently covered by radiated emission measurement methods of ICs, defined in other parts of this series of standards. In addition to that, there is an interest to extend the frequency range for conducted test methods to enable also selective emission analyses at IC pin level in extended frequency range.

The relevance and applicability of conducted test becomes more and more limited with increasing frequency. A frequency extension of the conducted emission measurement method with several restrictions could be achieved e.g. up to 3 GHz. The correlation between conducted and radiated emission results to emission phenomena in real application still needs to be determined. Therefore, the appropriate measurement method (conducted or radiated) should be carefully selected depending on the investigation target, known or expected disturbance phenomena and the application of the IC.

For conducted emission measurements in the extended frequency range above 1 GHz, special care needs to be taken to avoid that parasitics and coupling of passive components and layout or unwanted radiation of test setups affect or dominate the measurement result. Therefore, just to increase the measurement frequency range is not sufficient. This can lead to wrong results and interpretations, especially when different test boards and setups are used and a result comparison and reproducibility is of interest.

This Annex G describes requirements and limitations of conducted emission measurements methods in the extended frequency range above 1 GHz; it is intended to support the development of proper measurement setups for reliable and comparable conducted emission results, and provides some guidance.

G.2 Guidelines

G.2.1 Measurement network

The requirements for measurement networks in the extended frequency range are in principle the same as for the current frequency range up to 1 GHz described in 6.2 and 6.4. The measurement network and related coupling and decoupling components should not affect the function or performance of the IC under test (DUT) configured to operate in typical application conditions.

In order to ensure reliable and comparable results, the measurement networks assembled on the test board should provide a continuous transfer frequency characteristic (S21) within the ±3 dB tolerance band free of resonances in the used frequency range.

In Figure G.1, an example of a test circuit with a 150 Ω network is shown. The typical 1 Ω RF current probes have a limited RF performance in the higher frequency range and therefore they are not considered as a proper solution for the extended frequency.

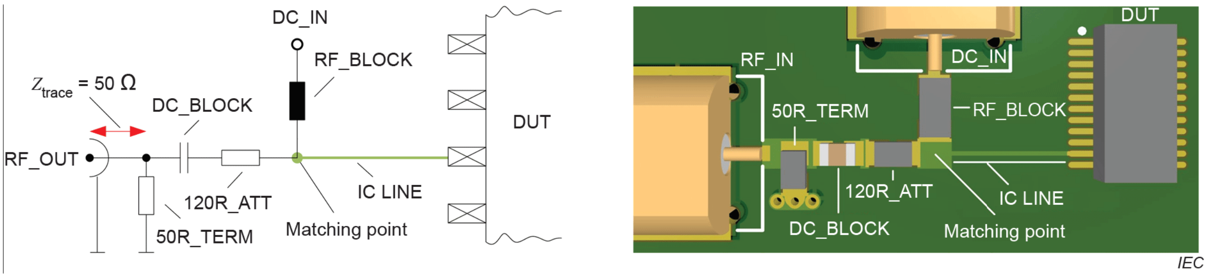
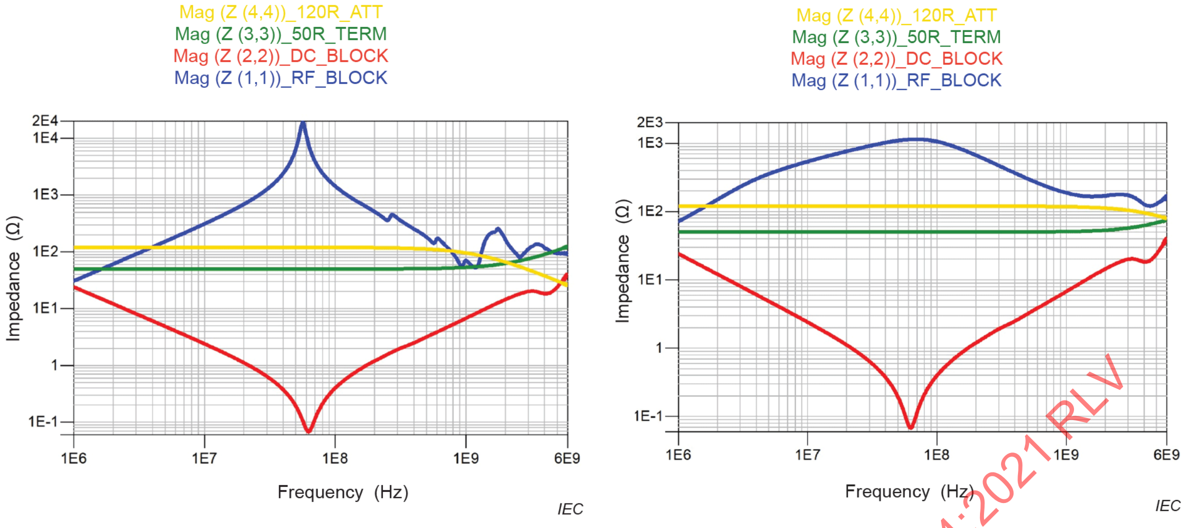


Figure G.1 – Example of a 150 Ω measurement network

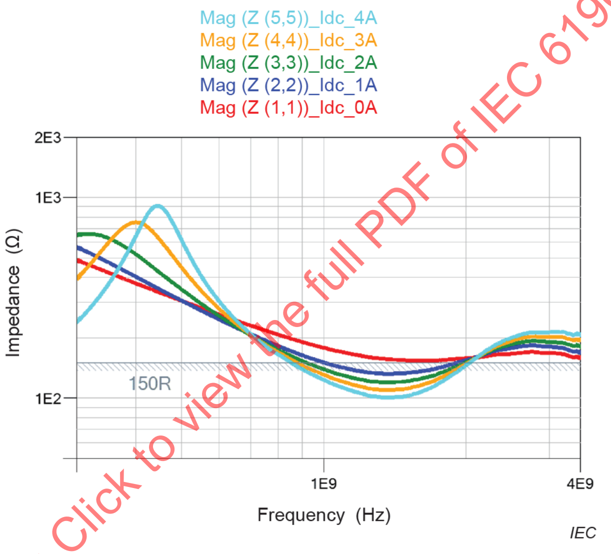
G.2.2 Network components

The network components used to build up the measurement and coupling/decoupling network should be selected to support both, IC operation and RF performance properly.

For the measurement network, it is recommended to use components for surface mounted assembly with defined value up to the targeted frequency range or special RF components. It is recommended to verify the RF performance of the components by measurements under application conditions on a test board that does not affect the results. The RF decoupling component (e.g. DC feed inductors, RF decoupling chokes) should be verified under loading condition, e.g. the rated DC current. In Figure G.2, examples of the frequency characteristic for matching/termination resistor, DC decoupling capacitor and RF decoupling choke are shown.



a) typical components used up to 1 GHz **b) RF components to be used above 1 GHz**



c) Load current effect on RF decoupling chokes

Figure G.2 – Example of RF characteristic of network components

Above a certain frequency, the RF performance of network components is affected by parasitics. This limits the application frequency range of the measurement network to keep the 150 Ω performance in the ± 3 dB tolerance band.

To avoid unwanted effects on the measurement results, special care should be taken on the RF decoupling components. The impedance of the RF decoupling component should be as high as possible but at least 150 Ω in the used frequency range. This requirement is challenging if a DC supply or load current of several amperes (e.g. 20 A for a power IC) needs to be handled. RF decoupling chokes with a broadband characteristic above 1 GHz have a limited current handling capability (e.g. 100 mA up to 4 A). This limits the application of the method to ICs with lower supply and load current, or needs a respective current adjustment for testing.

The connectors used to connect the RF cable from the measurement system with the coupling network on the test board should provide a respective RF performance over the frequency range to avoid reflections and resonances in the RF path.

NOTE The RF performance varies significantly between straight and edge connectors as well as between soldered and screwed connectors.

Mandatory or recommended filter components of the IC are not considered here, they are considered as part of the IC.

G.2.3 Network layout

The layout of the measurement network as well as all traces connected to the IC pin under test are important for the RF performance. The network components should be placed as compact as possible and the trace length between coupling network and the IC pin under test should be as short as possible to meet the ± 3 dB criteria. For example, for 3 GHz the critical trace length (l_{crit}) should be less than 10 mm to keep $l_{\mathrm{crit}} < \lambda/10$, respectively for 6 GHz the trace length should be less than 5 mm.

NOTE Nominal velocity of propagation depends on PCB material parameters (ε_r).

The impedances depending on the operation mode of the IC and/or optional and mandatory components are not considered.

In order to get a proper impedance characteristic for the RF traces of the network, the material parameter (e.g. ε_r, tan(δ)) of the test board should be known and controlled to keep tolerances within the target range. Care should be taken by selecting test board material. Standard PCB material has much wider tolerances than RF material in this respect. In any case, a simulation of the network layout with the right test board material parameters is recommended to design and verify the RF performance of the measurement network over the whole frequency range.

The test board should provide a solid GND plane underneath the measurement network. The effect of top layer GND on the RF performance of the coupling network should be considered for test board design. Vias and layer changes in the RF path should be avoided.

G.2.4 Network verification

The RF performance of the measurement network should be verified by a S21 parameter measurement between the RF connector of the test network and the pad of the IC pin under test, or if used the pad of the mandatory component in front of the IC pin under test. The IC and the mandatory or recommended filter components are removed for this measurement. Supply planes, mandatory for proper connection of the IC, may remain connected but can affect the result. This needs to be documented and considered by result evaluation. All other components connected to the measurement network as RF decoupling components of biasing, signal stimulation or monitoring networks remain populated and connected as intended during the measurement. Auxiliary equipment does not need to be connected and can be replaced by a termination or short to GND.

The measurement should be performed with a network analyzer calibrated up to the cable ends to be connected to the connector of the measurement network. Reflections at the transition point from the cable to the connector should be avoided.

Examples of respective S21 characteristics of the measurement networks implemented on a test board are shown in Figure G.3. The characteristics are derived from different board design simulations with real component models and tuned component models. The diagram shows the challenge in the higher frequency range dependent on trace length from network to the IC.

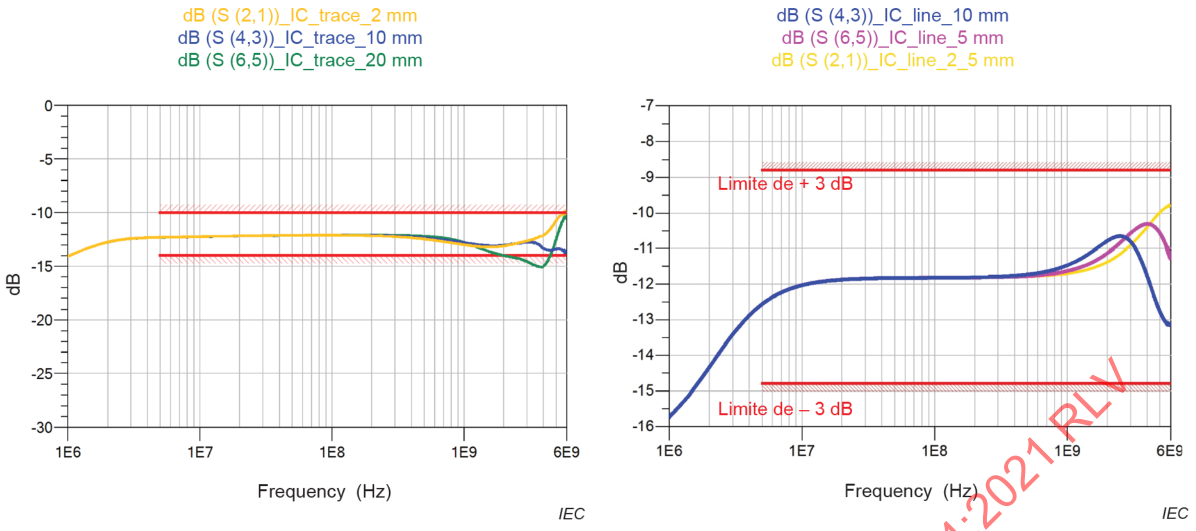


Figure G.3 – Examples of S21 characteristic by simulation

If a network is designed and simulation and measurement show the same S21 characteristic with less than 0,5 dB deviation, it can be considered as reliable enough and used multiple times on a test board as fixed building block without a demand for multiple measurement verification.

G.2.5 Test board

The test board usually combines an application circuit of the IC under test and the measurement networks on the same PCB. In order to achieve the RF characteristic of the measurement networks as described above, they shall be placed and connected very close to the IC pins of interest. Moreover, for proper setting and operation of the IC, a typical application circuit with mandatory components, loading and auxiliary circuits for stimulation and monitoring shall be placed as well. Depending on the complexity and pin count of the IC, this can become very challenging and provide some constraints for the test PCB design.

As described above, the measurement network design should be compact and connected via short traces to the IC pin. It is recommended to use fixed building blocks with a known RF performance. If the network design needs to be modified or newly designed, it is recommended to use simulation tools for test board design and first verification. This also allows the identification of unwanted cross coupling between RF traces and other signal lines on the test board.

An example of a simple test board section with RF measurement network, IC with mandatory components and other signal lines are shown in Figure G.4. The red highlighted signal line in Figure G.4 is exposed for cross coupling.

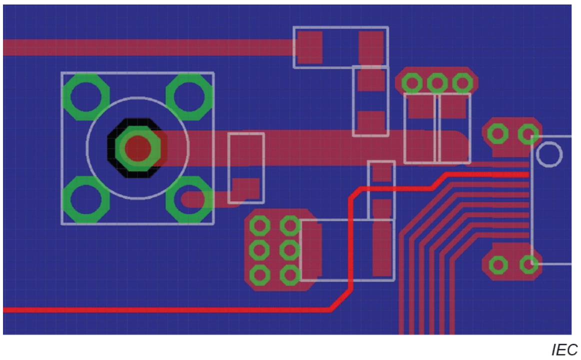
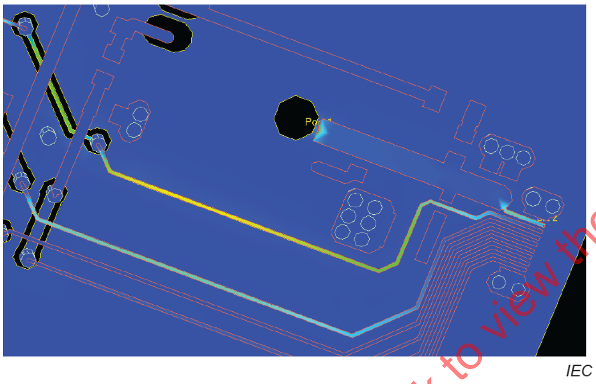


Figure G.4 – Examples of test board section

A simulation result of the cross coupling between the RF measurement network and signal lines is shown in Figure G.5 and the related effect on the S21 transfer characteristic is shown in Figure G.6. Special care should be taken to avoid parallel traces over longer distance in order to minimize unwanted resonances and cross coupling in compact designs.



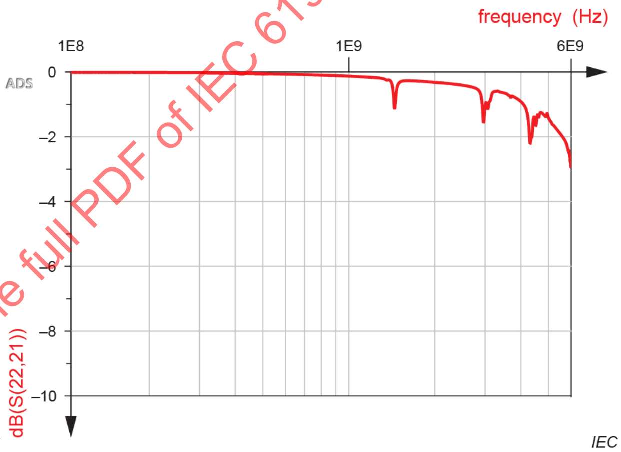
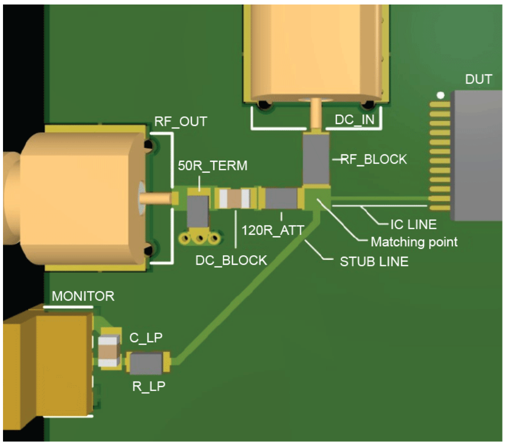


Figure G.5 – Examples of unwanted cross coupling between measurement network and traces on test PCB

Figure G.6 – Examples of unwanted signal line cross coupling on S21 transfer characteristic of RF measurement network

Another important aspect that needs to be considered for test board design is the connection of other signal lines (e.g. pull up, monitoring) to the IC pin under test where the measurement network is connected. In Figure G.7, an example of a test board with additional signal stub line (42 mm length) connected to IC pin is shown. The effect of the stub line length on the S21 transfer characteristic is shown in Figure G.8. The impedance of the line termination and the position of this termination is important and needs to be considered for board design.



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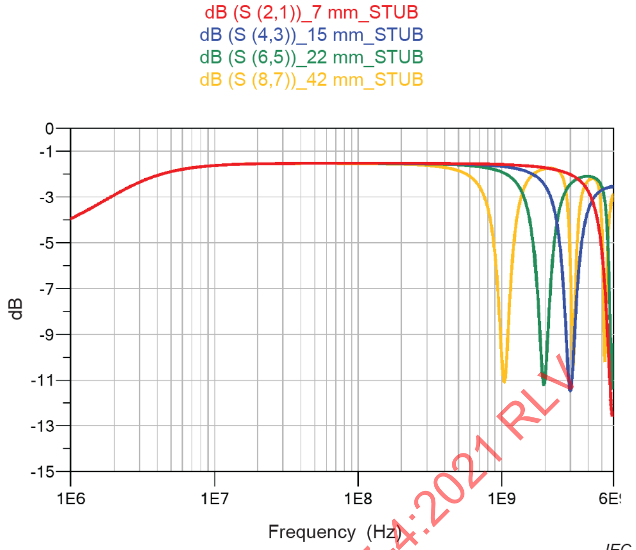

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Figure G.7 – Examples of test board with additional signal line connected to IC pin

Figure G.8 – Examples of stub lines length effects on S21 transfer characteristic of RF measurement network

G.3 Application area

The emission measurements conducted in the frequency range above 1 GHz become more and more challenging with increasing frequency due to several effects.

The size of the measurement network and the connection to the IC pin requires a compact design, proper matching and/or short trace length $l_{crit} < \lambda/10$ to fulfil ± 3 dB requirement free of resonances. Furthermore, the consideration and minimization of unwanted cross coupling between traces on the board introduce additional constraints and requires special measures or multi-layer boards to avoid unwanted effects on the single pin result. Therefore, the application of the method is limited to a low number of selected pins of an IC. The method can be useful for dedicated analyses of single, special selected pins, but not for a full characterization of complex ICs with higher pin count.

The components used for RF measurement networks and RF decoupling circuits for biasing, loading, stimulating and monitoring IC functions have to ensure a proper RF characteristic in the frequency range of interest while providing unaffected operation conditions for the functionality of the IC under test. Proper RF characteristic in the higher frequency range and higher voltage and current rating of the components seems to be a contradiction. Thus, the conducted test method application is limited to few amperes (e.g. 100 mA to 4 A) of supply or load current due to component limitation. A typical application e.g. of power ICs with 80 % loading condition cannot be realized because reduced supply or load currents can lead to performance limitations or untypical operation modes of the IC.

Considering IC applications and conducted test method origin, the validity of the assumption, that RF currents and voltages distributed from the IC source via pins and connected traces and wires are the dominant cause for the emission phenomena of an application, needs to be verified for the frequency range above 1 GHz. With increasing frequency, the effects of direct radiation from the IC and its external circuitry can increase significantly and also the system implementation can play a significant role. Therefore, it is recommended to analyze the phenomena behind emission issues in application to choose the right measurement method to generate useful data of the IC.

It is not applicable and thus not recommended to apply conducted emission measurements in the extended frequency range to all pins of an IC and also not to all ICs. A selection guide or table, such as Table G.1, can support the user to make a smart choice for IC types, IC functions, operation frequency, current consumption, pin classes, package types, dimensions, etc. in future. In general, ICs with operating frequencies and harmonics (e.g. < 10th harmonics) exceeding 1 GHz could be more relevant for emission in the extended frequency range than others. Then pin selection should be done based on IC design to link high frequency IC functions to respective global and/or local pins.

Table G.1 – Draft selection table for conducted emission measurements at pins above 1 GHz

IC type	IC functions	Operating frequency (MHz)			Pin current rate (A)			Pin type / class	Package type / dimension	Test applicable recommended	
		< 10	10 to 100	> 100	< 1	1 to 4	> 4			yes	no

If a conducted emission measurement in the extended frequency range is performed and results are distributed, it is strongly recommended to provide the S21 verification diagram of the measurement network(s) along with the full layout of the test board to make an interpretation of the data possible. The simple approach just to design a test board and run measurements into the extended frequency range above 1 GHz is strongly discouraged when independent reliable data are needed.

Bibliography

[1] CISPR 16-1-2, *Specification for radio disturbance and immunity measuring apparatus and methods – Part 1-2: Radio disturbance and immunity measuring apparatus – Coupling devices for conducted disturbance measurements*

[2] CISPR 25, *Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers*

IEC 61967-4

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INTERNATIONAL STANDARD

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Integrated circuits – Measurement of electromagnetic emissions – Part 4: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method

Circuits intégrés – Mesure des émissions électromagnétiques – Partie 4: Mesure des émissions conduites – Méthode par couplage direct 1 Ω/150 Ω

IEC 61967-4:2021-03(en-fr)

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

INTEGRATED CIRCUITS – MEASUREMENT OF ELECTROMAGNETIC EMISSIONS –

Part 4: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method

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IEC 61967-4 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices. It is an International Standard.

This second edition cancels and replaces the first edition published in 2002 and Amendment 1:2006. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) frequency range of 150 kHz to 1 GHz has been deleted from the title;
b) recommended frequency range for 1 Ω method has been reduced to 30 MHz;
c) Annex G with recommendations and guidelines for frequency range extension beyond 1 GHz has been added.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47A/1101/CDV	47A/1107/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts of the IEC 61967 series, under the general title *Integrated circuits – Measurement of electromagnetic emissions* can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTEGRATED CIRCUITS –
MEASUREMENT OF ELECTROMAGNETIC EMISSIONS –

Part 4: Measurement of conducted emissions –
1 Ω/150 Ω direct coupling method

1 Scope

This part of IEC 61967 specifies a method to measure the conducted electromagnetic emission (EME) of integrated circuits by direct radio frequency (RF) current measurement with a 1 Ω resistive probe and RF voltage measurement using a 150 Ω coupling network. These methods ensure a high degree of reproducibility and correlation of EME measurement results.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61000-4-6, *Electromagnetic compatibility (EMC) – Part 4-6: Testing and measurement techniques – Immunity to conducted disturbances, induced by radio-frequency fields*

IEC 61967-1, *Integrated circuits – Measurement of electromagnetic emissions – Part 1: General conditions and definitions*

3 Terms and definitions

For the purposes of this document, the terms and definitions of IEC 61967-1 apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

4 General

4.1 Measurement basics

The maximum tolerated emission level from an integrated circuit (IC) depends on the permitted maximum emission level of the electronic system, which includes the IC, and also on the immunity level of other parts of the electronic system itself (so called inherent EMC). The value of this emission level is dependent on system and application specific (ambient) parameters. To characterise ICs, i.e. to provide typical EME values for a data sheet, a simple measurement procedure and non-resonant measurement setup are required to guarantee a high degree of reproducibility. Subclause 4.1 describes the basis of this test procedure.

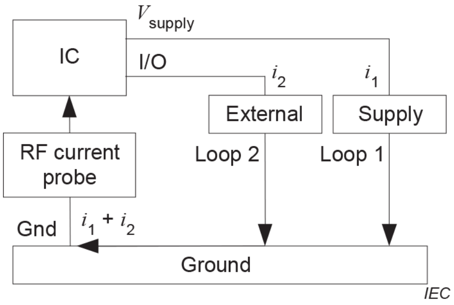


Figure 1 – Example of two emitting loops returning to the IC via common ground

The emission of an IC is generated by sufficiently fast changes of voltages and currents inside the IC. These changes drive RF currents inside and outside the IC. The RF currents cause conducted EME, which is mainly distributed via the IC pins conductor loops in the printed circuit board (PCB) and the cabling. These loops are regarded as the emitting loop antennas. In comparison to the dimension of these loops, the loops in the internal IC structure are considered to be small.

The RF currents that accompany ICs action are different in amplitude, phase and spectral content. Any RF current has its own loop that returns to the IC. All loops return mostly via the ground or supply connection back to the IC. In Figure 1, this is shown for two loops returning via ground. Loop 1 represents the supply wiring harness for the IC while loop 2 represents the routing of an output signal. The common return path via ground is a suitable location to measure the conducted EME as the measurement of the common RF sum current of the ground pin. This test is named the “RF current measurement”.

If the IC under test has only one ground pin and all other pins are suspected to contribute essentially to the EME, then the RF sum current is measured between the ground pin of the IC under test and the ground (see $i_1 + i_2$ in Figure 1).

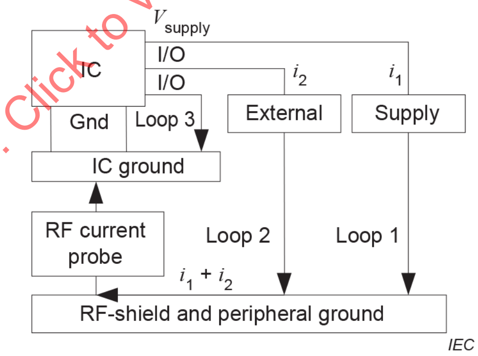


Figure 2 – Example of IC with two ground pins, a small I/O loop and two emitting loops

If the IC under test has more than one ground pin or some of the pins are not suspected to contribute much to the whole EME, then the IC under test gets its own ground plane as shown in Figure 2. This ground plane is named “IC ground”. It is kept separately from the other ground, that is named “RF-shield and peripheral ground”. The RF current is measured between the IC ground and the peripheral ground.

ICs are often used in different configurations based on the application. For instance, a microcontroller could be used as a single chip controller, with the I/O ports directly connected to the external cabling system. In order to understand the influence of a single I/O pin on the emission level of the IC, an additional measurement procedure, using the same equipment, is provided. This measurement is named “single pin RF voltage measurement at IC pins” (see also 4.3). In addition to the RF sum current measurement, the RF current measurement of a single supply pin can be of interest in the analysis of an IC. This can also be attained with application of the RF current measurement probe. For example, the RF current probe can be applied to any of the multiple ground or supply pins in order to quantify the contribution of the measured pin to the whole emission.

4.2 RF current measurement

In the test procedure, this measurement shall be made by measuring the voltage across the 1 Ω resistance of a RF current probe using a measurement receiver. The measurement shall be made at the location shown in Figure 1 and Figure 2. The construction of the RF current probe is specified in 6.2. The RF voltage level measured by the receiver is the voltage resulting from all of RF currents returning to the IC through the probe impedance. The voltage measurement can be converted to current by dividing the voltage by the probe impedance, if the probe impedance is determined for the applicable frequency range e.g. in a verification report.

NOTE 1 The probe impedance can be frequency dependant, caused by stray inductances of the probe, and thus the usable frequency range can be limited.

NOTE 2 The probe impedance causes, depending on the IC current consumption, a voltage drop that can affect the proper operation of the IC and limit the application of this method.

4.3 RF voltage measurement at IC pins

This measurement is used to identify the contribution of a single pin or a group of pins to the EME of the IC under test. This measurement is only applied to those pins of the IC under test that are intended to be connected directly to long (longer than 10 cm) PCB traces or wiring harnesses (e.g. I/O, supply). These pins are loaded by a typical common mode impedance of 150 Ω, as specified in IEC 61000-4-6. In order to connect the measurement receiver, that has an input-impedance of 50 Ω, the load has to be built as an impedance matching network. This matching network is defined in 6.4.

Other I/O-pins of an IC may be loaded as specified in the general part of IEC 61967-1.

4.4 Assessment of the measurement technique

The above techniques have the following properties:

- high measurement reproducibility, because few parameters influence the result;
- capability to compare different IC configurations (e.g. packages);
- single pin EME measurements of the various I/O pins are dependent on their importance for the emission in a specific application;
- assessment of the EME contribution of the IC using current sum measurement;
- simple verification of the measurement impedance using insertion loss measurement;
- measurement is also possible at very low frequencies.

With these characteristics, it is possible to measure the EME of ICs with a high degree of reproducibility and therefore this technique offers a good method for comparison.

Annex D gives an example of how the measurement techniques can be used for the assessment of ICs.

5 Test conditions

All test conditions required in this document are specified in IEC 61967-1.

6 Test equipment

6.1 RF measuring instrument

The measurement equipment shall fulfil the requirements described in IEC 61967-1.

6.2 RF current probe specification

Figure 3 shows the basic construction of the 1 Ω RF current probe.

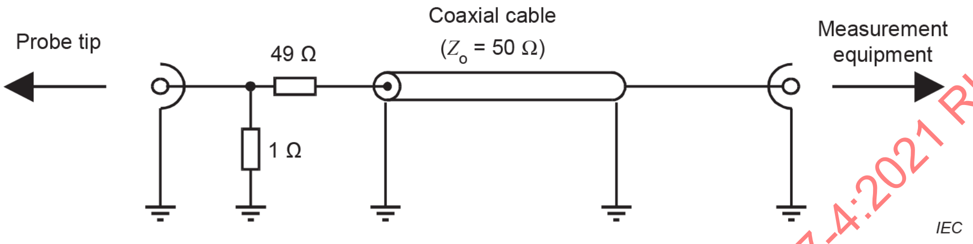


Figure 3 – Construction of the 1 Ω RF current probe

Table 1 presents a detailed specification of the RF current probe.

To prevent the measurement equipment from being damaged by DC voltage, the use of a DC block is recommended. This shall have an attenuation of <0,5 dB at the lowest frequency to be measured.

Table 1 – Specification of the RF current probe

Frequency range	DC to 30 MHz The applicable frequency range of the used probe shall be evaluated e.g. in a S-parameter measurement and documented in the test report. Current probes available on the market have proved to be usable e.g. only up to 30 MHz. Therefore bandwidth and impedance over frequency of the used probe shall be verified and documented in a diagram. The same applies to on-board probes with SMD components. In future, for enhanced RF probes, the usable frequency range may change.
Measurement resistor	RF resistor (low inductance)[a] 1 Ω (±1 %). The measurement resistor can also consist of resistors in parallel, which increases the maximum permissible current through the probe (e.g. 2 Ω//2 Ω) and reduce the stray inductance.
Matching resistor	49 Ω (±1 %)
Maximum current	< 0,5 A
Output impedance Z_o	40 Ω to 60 Ω
Insertion loss in verification circuit	34 dB ± 2 dB
Decoupling in verification circuit	See Figure A.1 and Figure A.5.
Cable connection	Flexible, double shielded coaxial cable with 50 Ω ± 2 Ω line impedance. The RF connector shall be mounted with low reflection. The insertion loss includes the cable and the probe. Changes to the cable length will result in additional attenuation to be considered with the measurement results.
Construction	Coaxial probe or comparable construction, which can be connected to a 4 mm coaxial socket. The measurement resistor shall be as close as possible to the probe tip. It shall be built in such a way that no mechanical damage is possible. The connection of the probe cable shall be coaxial; the probe tips should be replaceable, but nevertheless firmly connected to the cable.

[a] The series impedance caused by the parasitic inductance should be lower than the resistor in the used measurement range.

6.3 Test of the RF current probe capability

The current probe shall be functionally verified in a test circuit shown and described in detail in Annex A.

6.4 Matching network specification

Based on IEC 61000-4-6, a cabling network can be represented in most cases by an antenna with an impedance of about 150 Ω. In order to get accurate measurement results over the full frequency range, a termination network of 145 Ω ± 20 Ω shall be used. Usual measurement equipment provides an input impedance of 50 Ω so that the matching network shall match the signal line impedance to the equipment impedance. The circuitry is shown in Figure 4, and the characteristics of the impedance matching network used are shown in Table 2. Additional information of matching networks for differential pin measurements are provided in Annex F and recommendations.

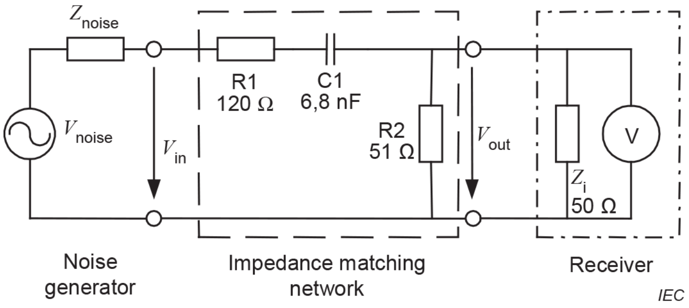


Figure 4 – Impedance matching network corresponding with IEC 61000-4-6

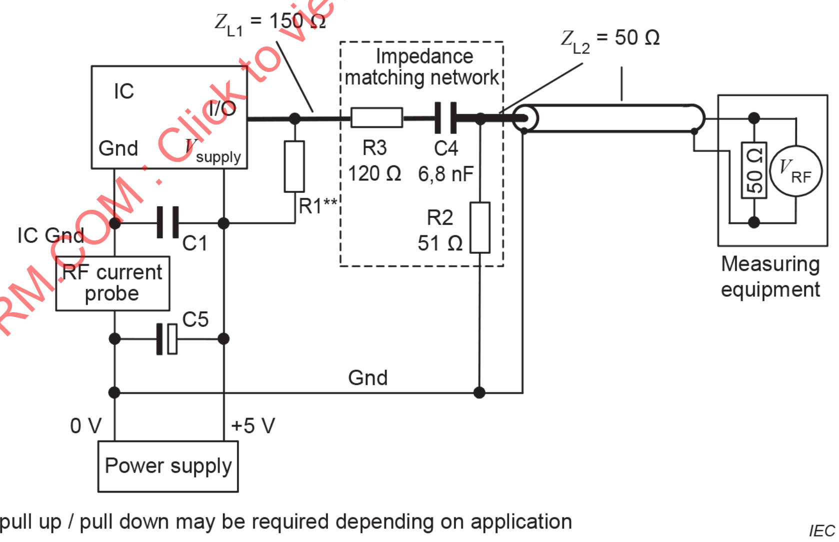
Table 2 – Characteristics of the impedance matching network

Frequency range	150 kHz – 1 GHz
Input impedance with 50 Ω termination Z_i	145 Ω ± 20 Ω
Insertion loss within a 50 Ω system	0,258 6 (−11,75 dB ± 2 dB)
Voltage ratio V_{out} / V_{in}	0,173 8 (−15,20 dB ± 2 dB)

7 Test setup

7.1 General test configuration

A general test configuration is shown in Figure 5. This general test configuration can be built up in the form of a special test configuration (an example is described in Clause E.2) or in any other configuration, e.g. also in a real application.



** pull up / pull down may be required depending on application

Figure 5 – General test configuration

7.2 Printed circuit test board layout

In order to obtain a high degree of reproducibility of measurement results and be able to make a valid comparison between different printed circuit test boards, the following guidance is given.

The test board should be built using PCB material of epoxy type (thickness 0,6 mm to 3 mm, dielectric constant about 4,7). The top side and the bottom side are covered with a minimal 35 µm copper layer.

The bottom layer should be used as ground plane.

If peripheral ground and IC ground are used for the 1 Ω method, these two grounds are isolated by an isolation gap. This isolation gap should be between 0,5 mm and 0,6 mm. If needed, the IC ground shall be located underneath the DUT. The maximum size of this area should not exceed the size of the package minimum footprint by more than 3 mm on each side.

To obtain the necessary accuracy for higher frequencies, parasitic coupling capacitance between IC ground and peripheral ground shall be controlled. This parasitic coupling capacitance between IC ground and peripheral ground shall be lower than 30 pF.

The IC ground is solely connected to the peripheral ground via the 1 Ω probe. In case of external RF current probe, a socket should be used. The shield of the RF current probe tip should be connected to the RF peripheral ground by the socket, while the IC ground or the IC ground pin is connected to the current probe tip. The connection between the IC ground and the probe tip shall be as short as possible. In any case, the trace length shall not exceed 15 mm. The trace should be connected to the IC ground at the shortest distance to the centre point of the DUT.

If the above-mentioned guidelines are not applicable, the transfer characteristic of modified design shall be determined and documented in the test report.

The DUT and all components needed to operate the DUT should be mounted onto the top side of the test board. As much wiring as possible should be routed in the top layer. The DUT should be placed in the centre of the PCB, while the needed matching networks should be placed around this centre. The wiring between the IC pins and the matching network should be designed to have a line impedance of 150 Ω. In case the 150 Ω line impedance is difficult to implement, the line shall be of the maximum reasonable impedance but short enough, in order to comply with the requirements of Table 2.

The wiring of the outputs of the matching networks should be designed to have a line impedance of 50 Ω. An example of a PCB layout can be found in Annex E.

The supply shall be connected with a single wire directly to the capacitor C5. C5 could be a surface mount device, of electrolytic type and having a value of at least 10 µF. The capacitor C5 shall be positioned near the probe socket.

The test board may have any rectangular or circular shape.

Additional information and guidelines for extended frequency applications are described in Annex G.

8 Test procedure

The requirements for the test procedure are described in IEC 61967-1.

9 Test report

The requirements for the test report are described in IEC 61967-1.

Emission measurement results may be presented using classification or reference levels. An example of a classification scheme for emission levels is presented in Annex B. In addition, Annex C shows how this classification scheme may be applied to set up reference levels for ICs used in the automotive industry.

Annex A
(informative)

Probe verification procedure

The test circuit shown in Figure A.1 is recommended for the probe verification. It consists of a PCB laid out using microstrip techniques (see Figure A.3). The PCB has an input port to which the RF generator is connected. The RF current probe to be verified is connected to the output port. The RF current probe output is connected to a test receiver (see Figure A.4). This verification procedure measures the isolation provided by the test circuit in a 50 Ω system (see also CISPR 16-1-2 [1][1]) and the insertion loss of the RF current probe.

Two separate measurements are recommended. The first measurement is performed with the test circuit configured as shown in Figure A.1, circuit diagram A. Note that clamp A is not inserted. While sweeping the RF generator over the required frequency range, measure the voltage appearing at the output of the RF current probe.

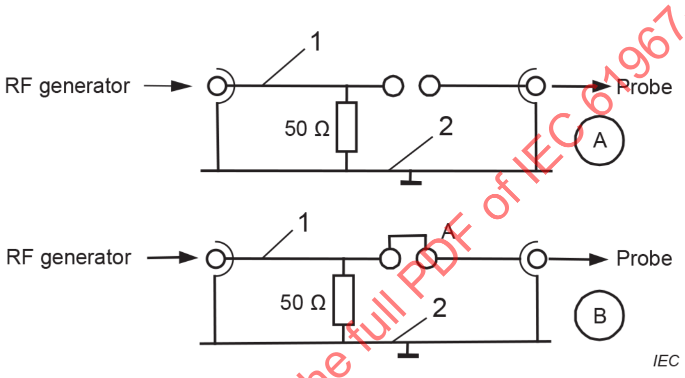


Figure A.1 – Test circuit

The second measurement is performed identically to the first one but with clamp A installed to shunt the RF generator to the probe input as shown in Figure A.1, circuit diagram B. This measurement results in the RF current probe insertion loss which indicates its sensitivity. Figure A.2 shows a result of such a measurement.

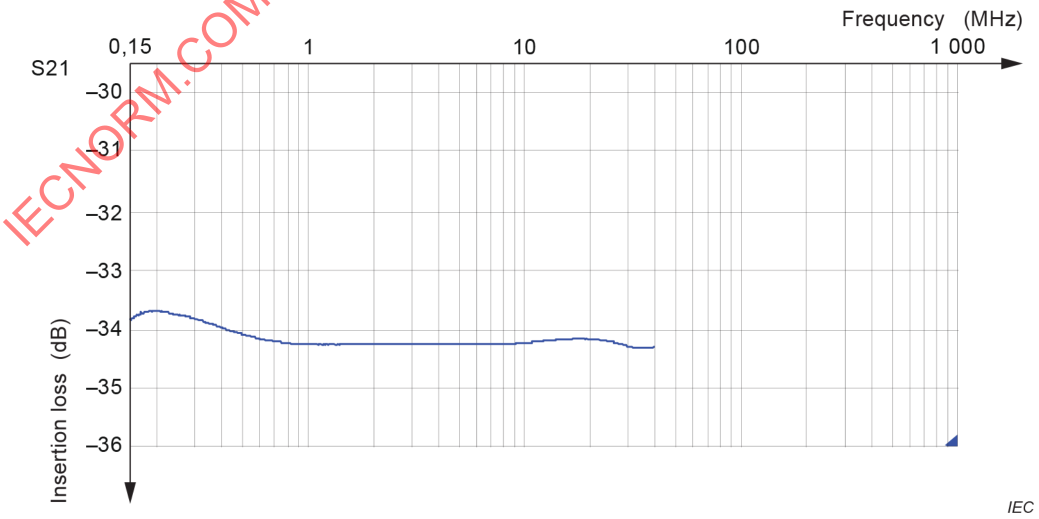


Figure A.2 – Insertion loss of the 1 Ω probe

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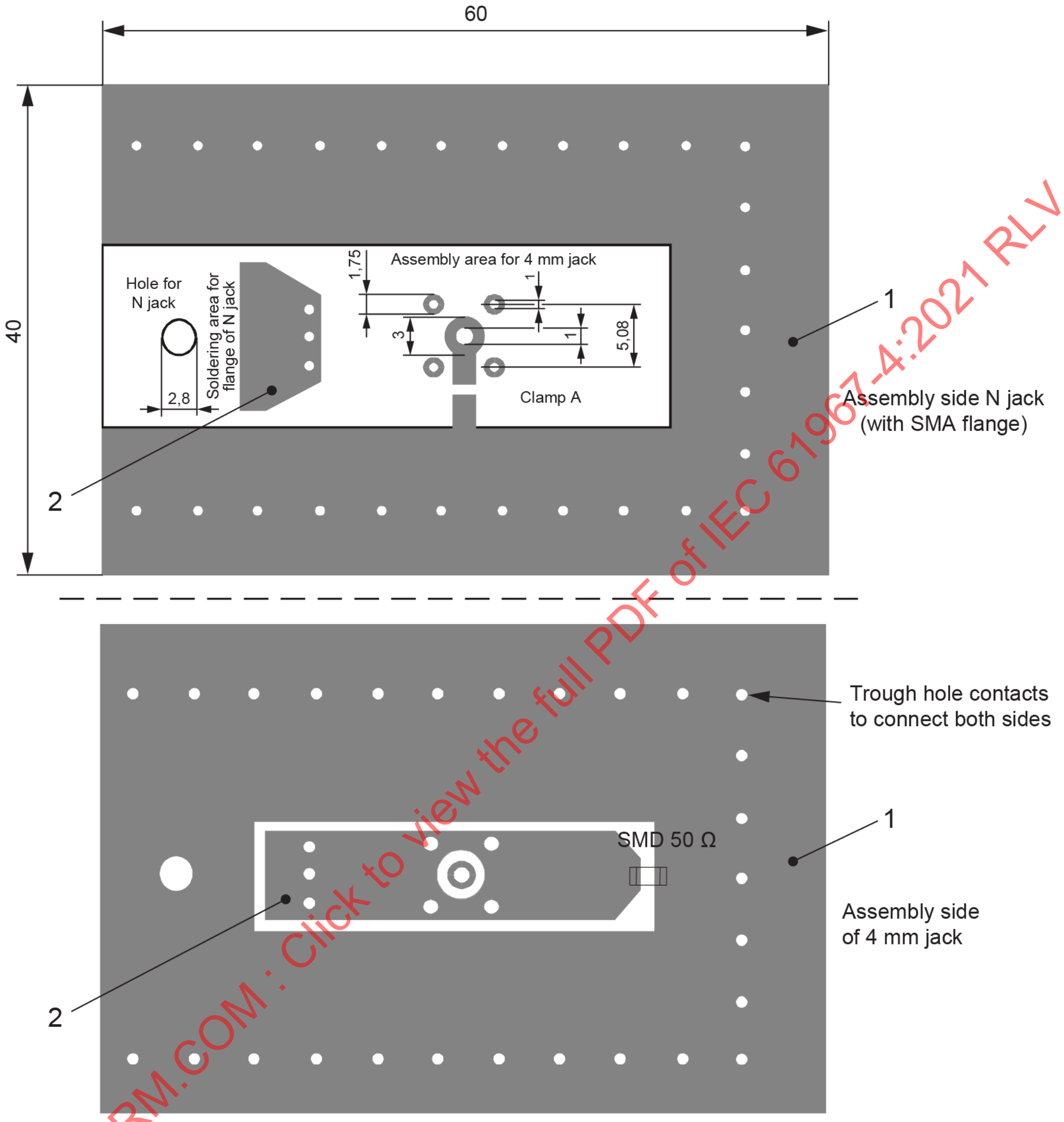
[1] Numbers in square brackets refer to the Bibliography.

The calculated difference of both measurements is called the "decoupling". The decoupling should be above the limit shown in Figure A.5. The decoupling is equal to the measurement dynamics in relation to the signal source. The decoupling does include the quality characteristics, the sensitivity and the shielding of the probe.

Dimensions in millimetres



Scale 1,6:1

IEC

Key

1 coupling area

2 reference ground

Figure A.3 – Layout of the verification test circuit

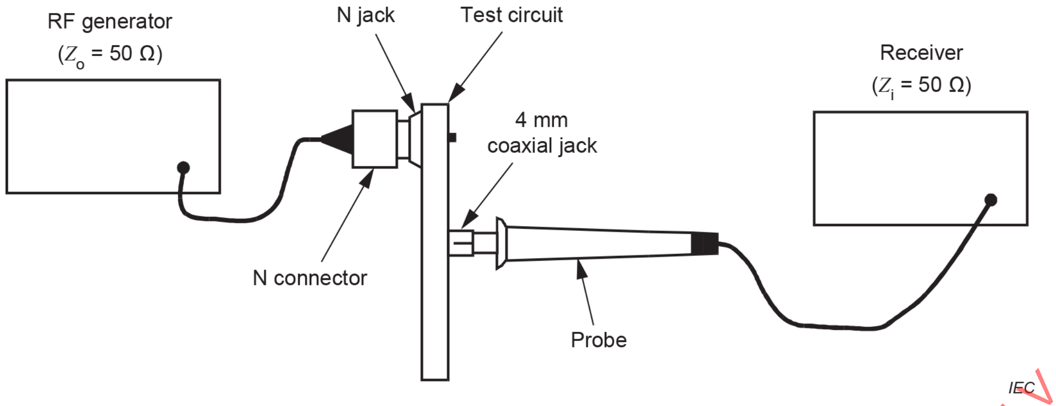


Figure A.4 – Connection of the verification test circuit

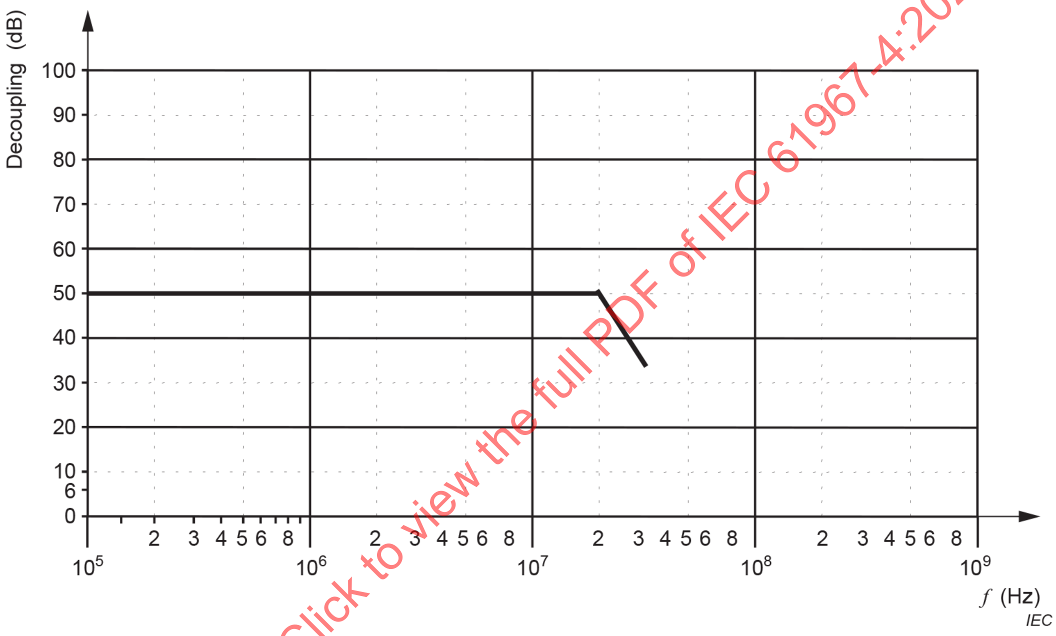


Figure A.5 – Minimum decoupling limit versus frequency

In order to evaluate the performance and the applicable frequency range of the used 1 Ω probe, it is recommended to characterize the probe input impedance characteristic. This can be done with a scattering parameter measurement using a vector network analyser. For the measurements, the vector network analyser should be calibrated including all connectors, cable and traces to exclude all setup parasites from the result. An example of a 1 Ω probe input impedance characteristic is shown in Figure A.6.

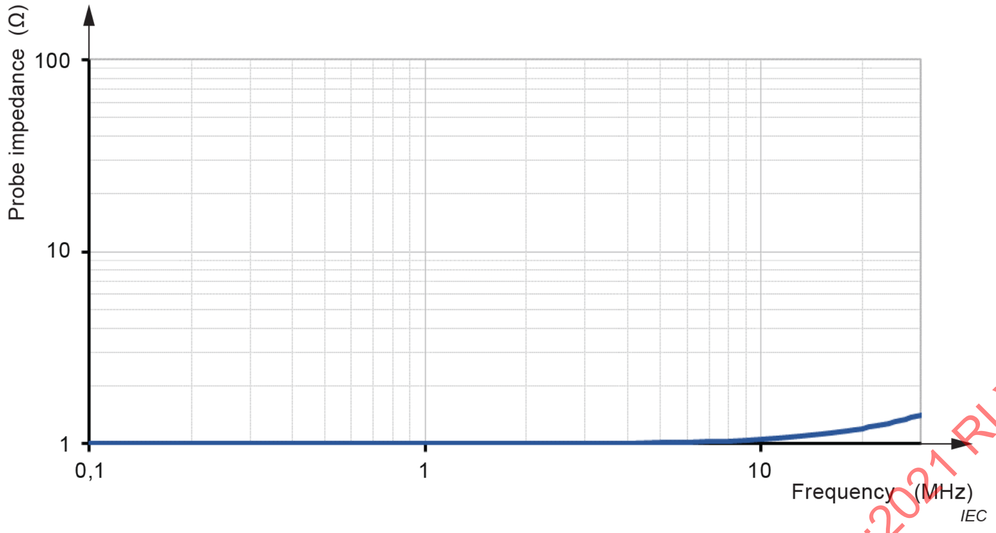


Figure A.6 – Example of 1 Ω probe input impedance characteristic

Annex B
(informative)

Classification of conducted emission levels

B.1 Introductory remark

The purpose of this Annex B is to provide a method of classifying the conducted emissions levels of integrated circuits by application of the test conditions described in this specification.

B.2 General

This annex is not intended to specify or imply conducted emissions limits for ICs. However, by careful application and agreement between manufacturer and user, it is possible to develop a device specification that specifies the maximum conducted EME allowable for a specific integrated circuit in a specific application when tested in accordance with the procedures in this document.

It should also be noted that Annex B is not meant to be a product specification and cannot function as one. Nevertheless, using the concept described in this document and by careful application and agreement between manufacturer and user, it would be possible to develop a document giving the EME behaviour for a specific integrated circuit.

B.3 Definition of emission levels

The diagram in Figure B.1 defines the conducted emissions classification levels used to define the overall envelope of the measured emissions. This diagram can be used to classify both the RF current measured with the RF current probe and the RF voltage at IC pins, measured using the impedance matching network.

The scheme follows the theory of a periodical trapezoidal pulse response and offers three different slopes of emission amplitudes with a 6 dB distance:

- 0 dB/decade (theory: constant amplitude line till the first corner frequency $1/(\pi\tau)$)
- −20 dB/decade (theory: decrease of amplitude till second corner frequency $1/(\pi\tau_r)$)
- −40 dB/decade (theory: decrease of amplitude at frequencies $>1/(\pi\tau_r)$).

The corner frequencies are dependent on the rise/fall times (τ_r) and the duration (τ) of the pulse.

The emission level diagram shown in Figure B.1 enables the selection of different slopes for different frequencies to better describe the measured conducted EME. The EME can be described with one, two or three slopes as required to best fit the measured data.

Various combinations are possible reflecting the actual requirements of the application much more precisely (e.g. adapted to the switching frequency of the ports of a microcontroller).

B.4 Presentation of results

B.4.1 General

The description of the maximum emission level can consist of up to three digits. Each digit represents one of three available slope identifiers as described in Clause B.3 and shown in Figure B.1. Capital letters are used to indicate a 0 dB/decade slope. Numbers are used to indicate a −20 dB/decade slope. Small letters are used to indicate a −40 dB/decade slope.

Assuming that one of the three slopes is not needed, then the corresponding letter or number will be left off. The defined maximum emission level in Figure B.1 offers a standardised way to communicate maximum emission levels unambiguously.

In general, the first digit is a capital letter that represents the maximum amplitude of the measured data. The second digit can either be a number or small letter that defines the position of the −20 dB/decade slope or −40 dB/decade slope, respectively. The third digit can be a capital letter, small letter or number.

In the case of measured emissions that approximate those resulting from a trapezoidal waveform, the capital letter is first and represents the position of the horizontal line with 0 dB/decade slope. Second is the number which defines the slope of −20 dB/decade. The third and small letter defines the position of the −40 dB/decade slope.

The points of intersection of the slopes represent the first and second corner frequencies as described in Clause B.3.

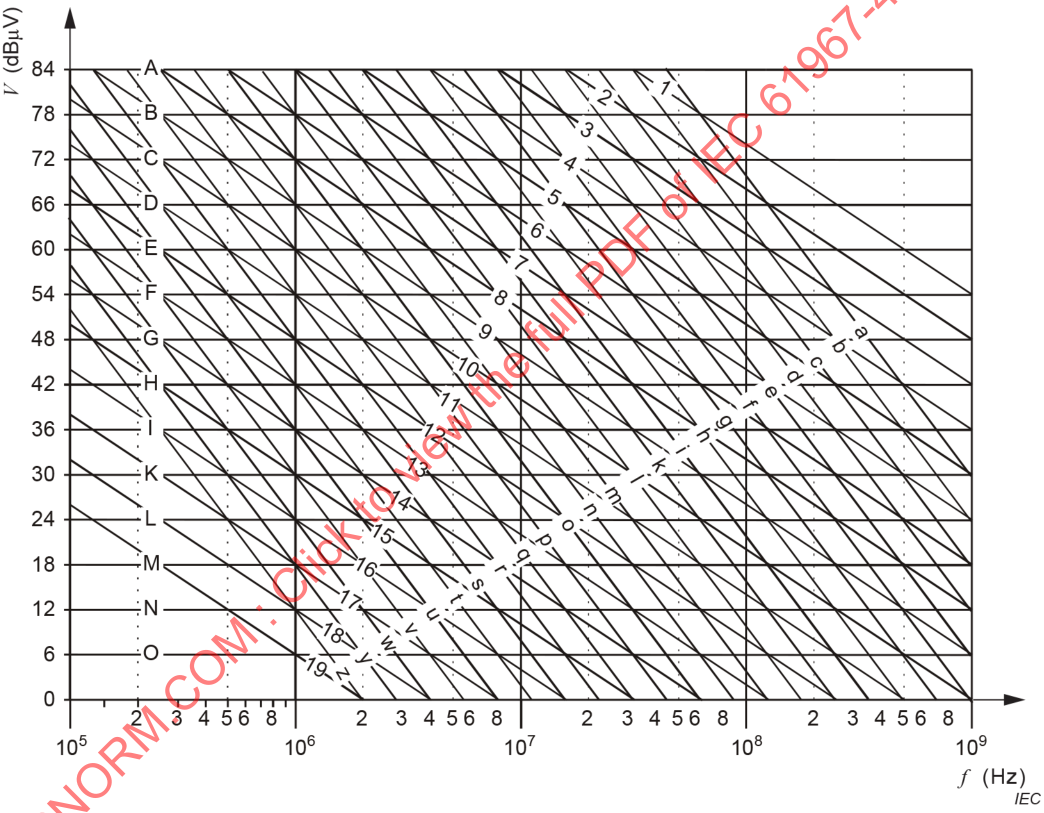


Figure B.1 – Emission level scheme

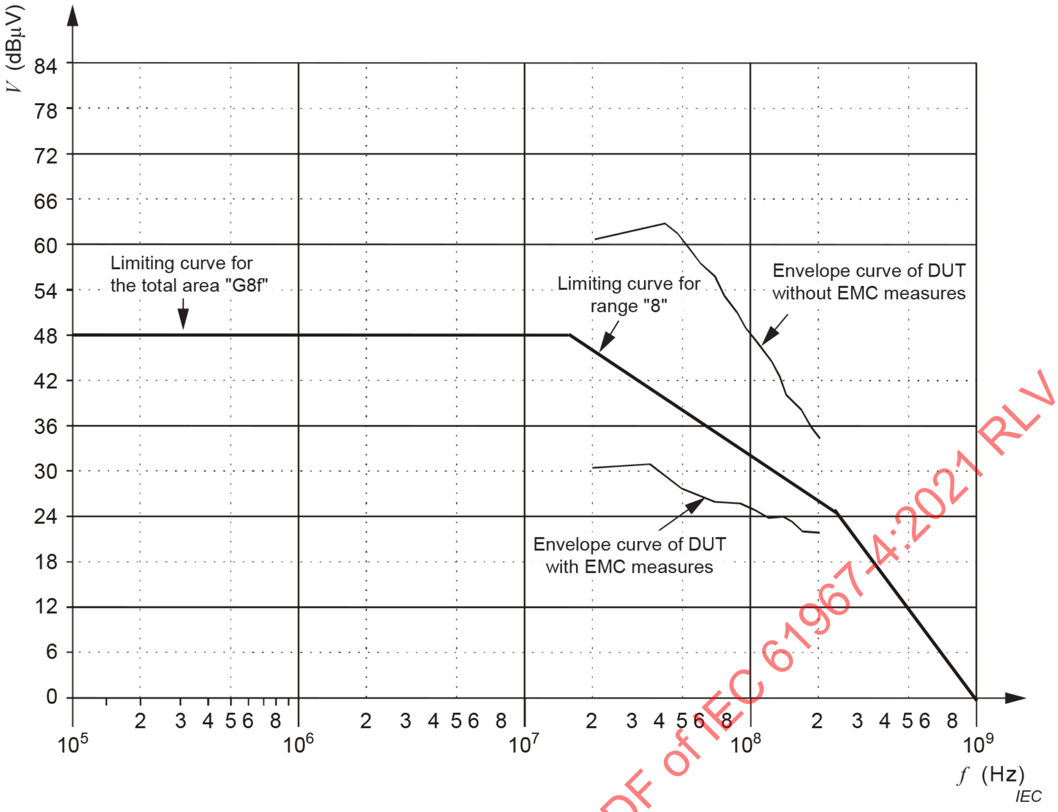


Figure B.2 – Example of the maximum emission level G8f

B.4.2 Examples

Figure B.2 represents an example whereby slope lines “G”, “8” and “f” are selected to describe the measured IC conducted EME.

Other notations are also possible:

“8f”: no 0 dB/decade slope; this is useful if the lowest frequency to be measured is higher than the first corner frequency;

“f”: only the −40 dB/decade slope is used; this is useful if the lowest frequency to be measured is higher than the second corner frequency;

“8”: only the −20 dB/decade slope is used; this is useful if the lowest frequency to be measured is higher than the first corner frequency, and the highest frequency to be measured is lower than the second corner frequency.

This second example shows how the IC supplier can characterise the emission performance of an integrated circuit for sales or engineering purposes. Table B.1 shows the limit curves (voltage) for all IC pins and the limit curve for the sum current (given in dBµV).

Table B.1 – Emission levels

PIN number	Limit curve
1	H11m
2	H11m
3	H11m
4	H11m
5	H11m
6	13q
7	13g
8	
Sum current	L15s

Annex C
(informative)

Example of reference levels for automotive applications

C.1 Introductory remark

Annex C contains examples of reference levels intended to be used on the emission test procedures according to this standard for the measurements of radio disturbances in the frequency range of 150 kHz to 1 000 MHz.

The reference levels are a selection from the scheme in Annex B. It applies to semiconductors used for automotive components. The requirements for semiconductors on other applications may be different.

The reference levels in this Annex C are recommended and subject to modification as agreed between the vehicle manufacturer, the component and the semiconductor supplier.

Based on the experience of the automotive industry, the following is stated:

Semiconductor emission measurements cannot completely characterise the disturbance capability of electronic vehicle components in which they are applied. The reason for this is seen in various effects in the vehicle and vehicle components (e.g. grounding, resonance, attenuation and coupling), which can also contribute to the emission behaviour or change the emission behaviour. Therefore, semiconductor emission measurements cannot fully replace vehicle and component measurements according to CISPR 25 [2].

C.2 General

Since the mounting location, vehicle body construction, harness, grounding and printed circuit board (PCB) design can affect the coupling of radio disturbances generated by the operation of semiconductor devices to the on-board radio, this annex defines reference levels.

The levels to be used on a specific semiconductor device (as a function of frequency band) are to be agreed by the vehicle manufacturer, the component and the semiconductor supplier.

In specific cases, a deviation from these reference level classes can be agreed between the users of this document in accordance with Annex D.

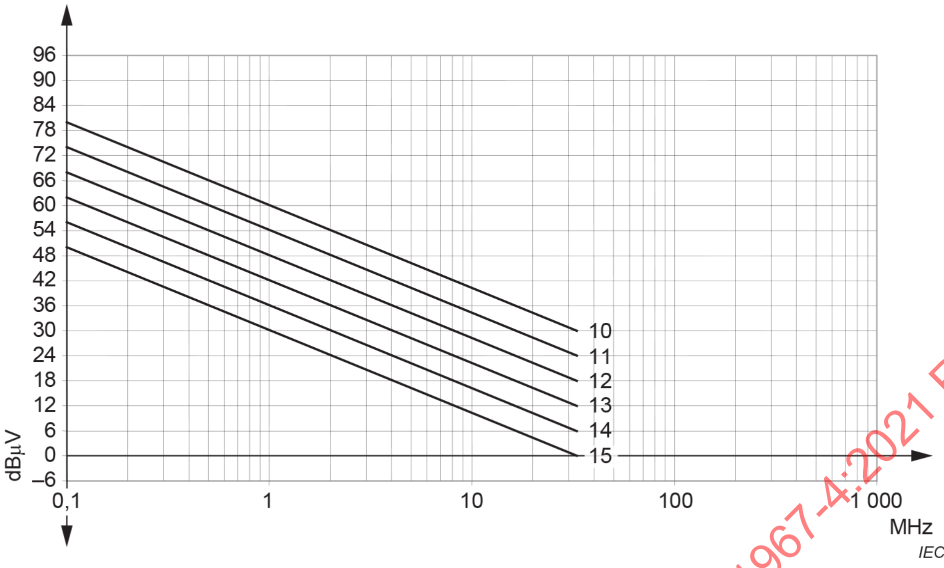
C.3 Reference levels

C.3.1 General

For acceptable radio reception in a vehicle, the conducted noise should not exceed one of the agreed values shown in Figure C.1 and Figure C.2.

NOTE Results of measurements using the 1 Ω method do not correspond to those using the 150 Ω method in all cases (e.g. in cases of different source or terminal impedance).

C.3.2 Measurements of conducted emissions, 1 Ω method



NOTE Reference levels shown up to 30 MHz due to current usable probe range

Figure C.1 – 1 Ω method – Examples of reference levels for conducted disturbances from semiconductors (peak detector)

Conformance with the reference levels in Figure C.1 does not ensure a sufficient noise suppression emitted by a semiconductor in all cases, e.g. if the disturbance currents distribution does not include all significant lines. However, measurements only on the ground lines can often give an average impression concerning the semiconductor's capability to emit disturbances.

C.3.3 Measurements of conducted emissions, 150 Ω method

This method is able to characterise the emission levels on single pins. Therefore, it is usual that further measurements have to be performed to completely describe the semiconductor's capability to emit disturbances.

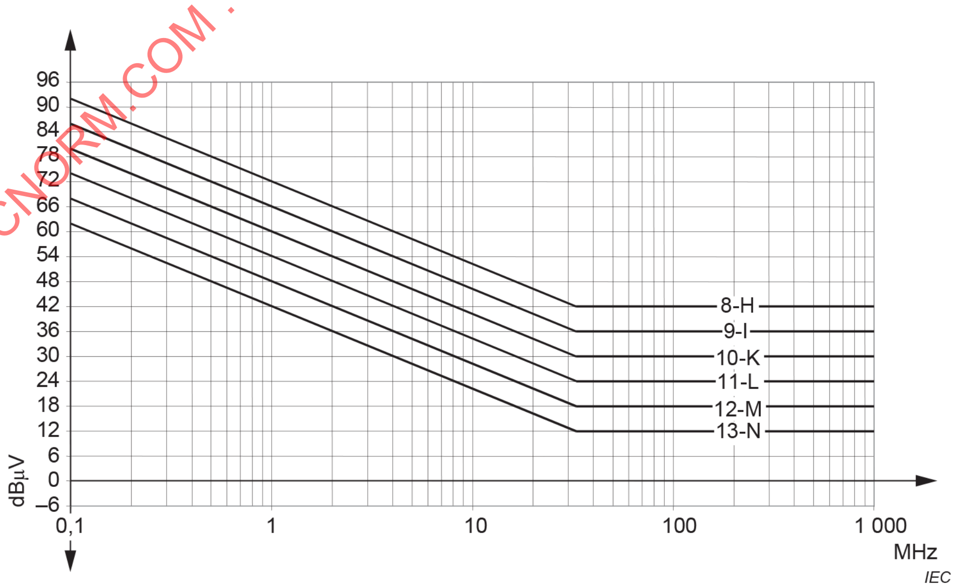


Figure C.2 – 150 Ω method – Examples of reference levels for conducted disturbances from semiconductors (peak detector)

Annex D
(informative)

EMC requirements and how to use EMC IC measurement techniques

D.1 Introductory remark

The development of EMC optimised systems, modules and ICs requires the definition of emission classification levels and suitable test procedures to measure the generated emissions. EMC standards with emission limits exist for electronic systems, subsystems, and modules, but do not yet exist for the ICs used within those systems, subsystems and modules. Standardised IC EMC measurement procedures are attempting to close the gap, but significant problems exist which need to be overcome first.

D.2 Using EMC measurement procedures

Based on what is known today, a full qualification of an IC can only be obtained if, together with the RF current measurement, the individual pins are also measured applying the single pin method. In specific applications with reduced requirements, only a selection of pins may be tested with the single pin method. If this has been made, this has to be documented with an explanation for the user.

Table D.1 lists some possibilities whereby the measurement procedure can be reduced.

Table D.1 – Examples in which the measurement procedure can be reduced

Component related parameters	Configuration of the IC
– Several pins not used and therefore not connected to the PCB (no potential current loop) – Existing blocks on the IC not used	– Several pins (I/O ports) with the same EMC behaviour

Because of different technical ambient parameters (see also Table D.2), there is no direct correlation possible between system and module EMC measurements as well as between module and IC EMC measurements. The final approval of a module, and therefore also for the IC, is only possible after a successful EMC measurement of the system.

Normally, additional suppression of interference is needed such as filters and metal screening. The implementation of those various EMC measures within the IC and/or outside the IC on the PCB is very much dependent on the cost aspects and feasibility (space availability, etc.).

D.3 Assessment of the IC influence to the EMC behaviour of the modules

Depending on the development status of a system, different aspects can be seen in relation to the EMC:

a) selection of existing ICs, which are already used in other systems of the same application field, and in production with a known EMC behaviour;

b) redesign of ICs, which are already used in other applications and in production;

c) customised ICs for systems for the same field of application.

In the case of a), the experience of the system manufacturer/subcontractors is necessary in order to understand and decide which EMC ambient parameters will influence the IC. The selection of the maximum emission levels will be based on these parameters (see Table D.2).

Table D.2 – System- and module-related ambient parameters

Component-related ambient parameters	System-specific ambient parameters
– Ground concept	– System type
– Filter concept	– Fitting area of the module
– Screening	– Fitting area of the antenna
– Layout	– Ground concept
– Working conditions, software	– Wiring harness concept

In the case of b), Table D.3 lists a set of development activities, which influence the EMC behaviour of the system.

In the case of c), the EMC IC requirement has to be determined based on the application. The product specification needs to define the maximum emission levels and the extent of the measurements to be taken in order to achieve a successful development.

Table D.3 – Changes at the IC which influence the EMC

Changes on silicon	Changes off silicon
– Hardware redesign	– Change of leadframe
– Change of chip layout	– Change of package
– Shrink to smaller geometry	– Change of V_{supply}
– Software changes (user's responsibility)	

In all cases, a preliminary decision should be taken to accept the test results of the ICs based on the proposed measurement method.

Annex E
(informative)

Example of a test setup consisting of an EMC main test board and an EME IC test board

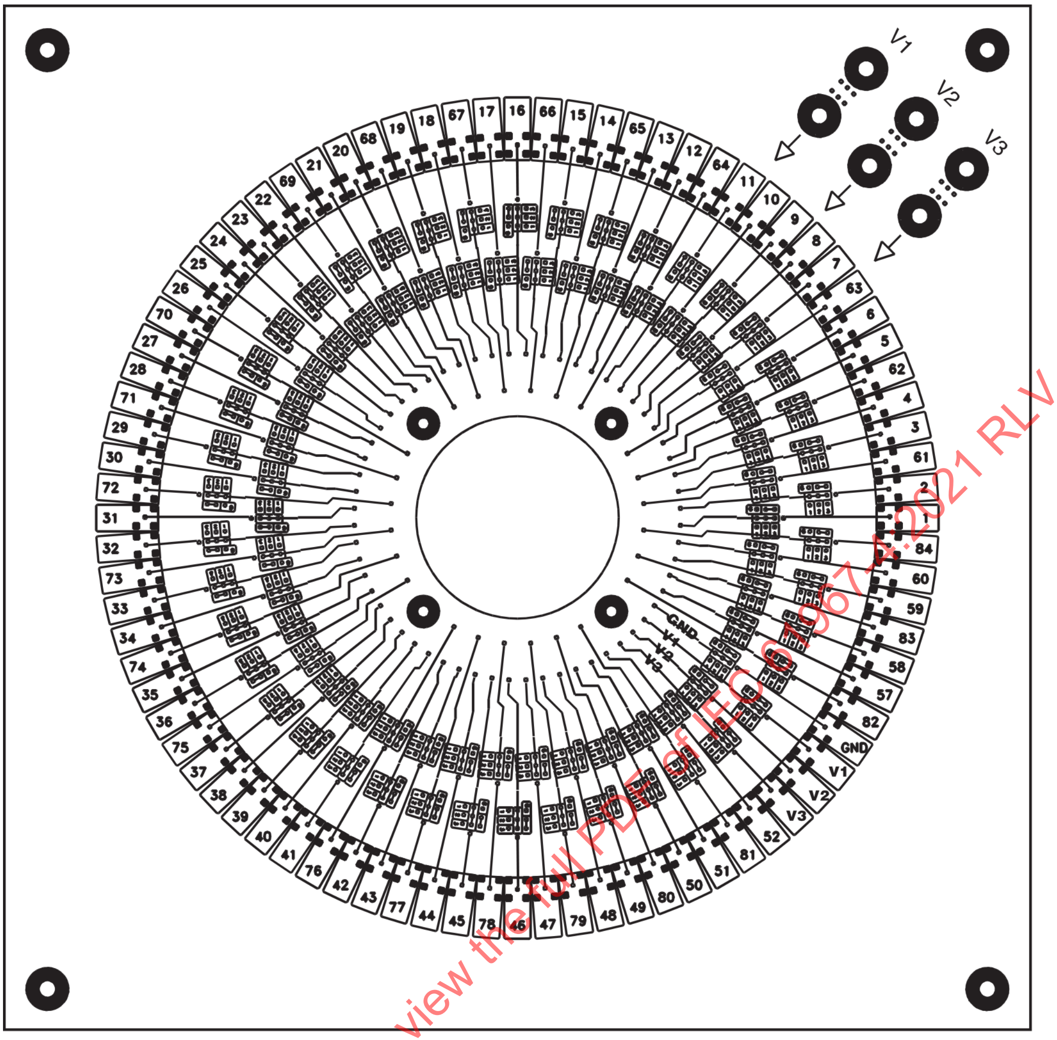
E.1 Introductory remark

Annex E describes a test setup, which has been designed for propagation delay measurements of fast logic devices; it is well suited for EMC measurements too. The setup consists of an EMC main test board, which can be used for all measurements with no change in layout. Up to 84 connections can be made to the so-called EME IC test board. This test board carries the IC under test together with the components needed to let the IC operate and the components of the 150 Ω to 50 Ω matching network. Consequently, the IC test board has to be designed from new for each IC or at least for a group of ICs. In this annex, both test boards are described.

E.2 EMC main test board

Clause E.2 describes the EMC main test board, which is built to comply with a 50 Ω impedance measurement equipment. The EMC main test board (see Figure F.1) is used to connect the EME IC test board to the measurement equipment. It is built on a seven-layer printed circuit board with the dimensions 293 mm × 293 mm. The three inner layers are used as power supply layers V1, V2 and V3 for the EME IC test board. The following layers on both sides are ground layers, which are also used as the RF-shield ground to the signal layers on the top and the bottom of the PCB.

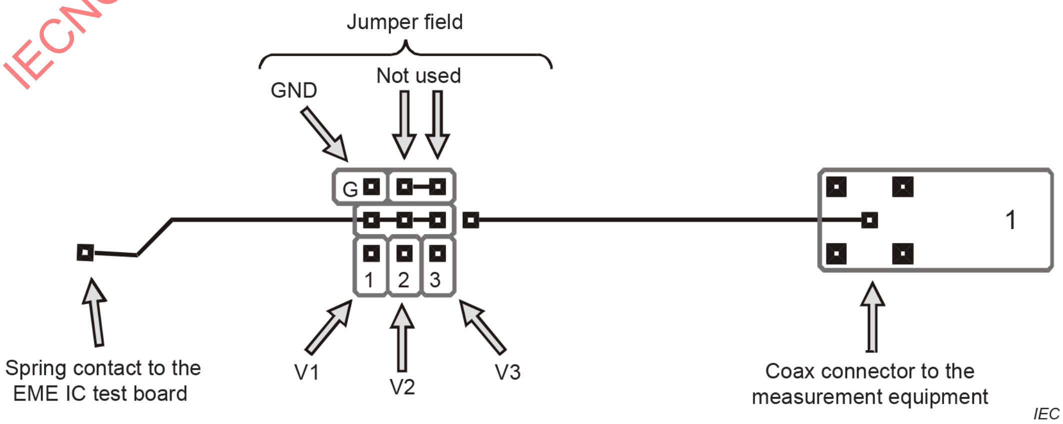
The EME IC test board is mounted on top of the EMC main test board and centred with four screws (M3x6; the length of the screws is dependent on the thickness of the EME IC test board). The screws provide the ground connection between EMC main test board and EME IC test board. All other electrical connections are made through the 84 pogo-pin ring. The pogo pins are soldered into the main board and are mechanically fixed with a nonconductive ring, e.g. made of Teflon (polytetrafluorethylen – PTFE). Four of the 84 connections are already connected with the power supply lines V1, V2, V3 and GND, and are used to provide the power supply to the EME IC test board.



IEC

Figure E.1 – EMC main test board

All 84 signal lines are routed on the top layer and are implemented as a stripline with a 50 Ω line impedance. The striplines connect the pogo pins with the miniature coax connectors on the outer side, where the measurement equipment is connected. Each signal line is connected to a jumper field, which allows the connection to the coax connector or one of the four supply lines V1, V2, V3 and GND (see Figure E.2).



IEC

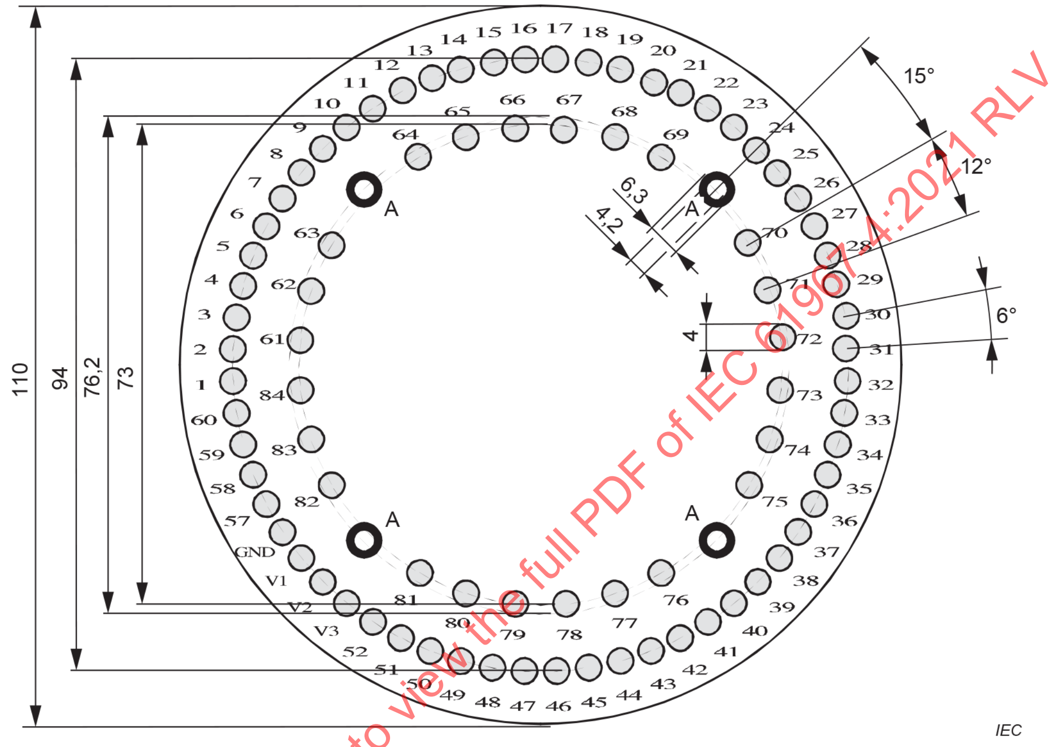
Figure E.2 – Jumper field

E.3 EME IC test board

E.3.1 General explanation of the test board

Figure E.3 shows a mechanical drawing of the bottom side of the IC test board. For each IC test board, the positions of the spring contact area and the through-hole connections remain as shown in the drawing. Other parts on the IC test board may be laid out as needed for the IC under test (see an example in Figure E.5 and Figure E.6).

Dimensions in millimetres



NOTE The through-hole connections **A** are used as Gnd connections to the EMC main test board.

Figure E.3 – EME IC test board (contact areas for the spring connector pins of the main test board)

E.3.2 How to build the test system

The EME IC test board should be constructed in such a way that the operating conditions of the DUT correspond to those of a typical application.

The EME IC test board should have three ground connections: IC ground, peripheral ground and RF-shield ground (see Figure E.4, Figure E.5, Figure E.6).

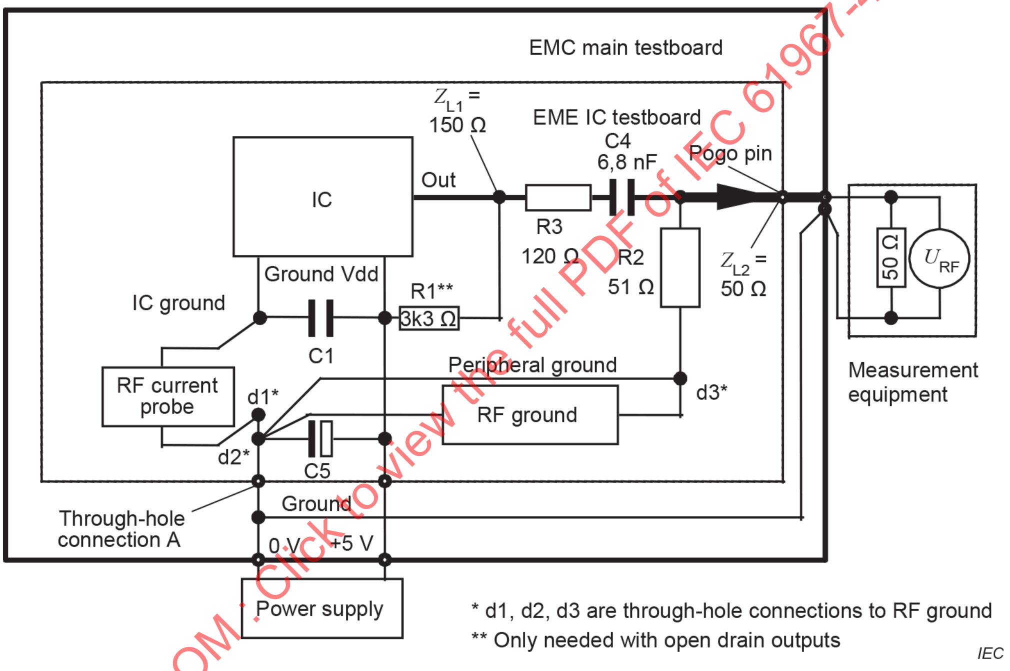
All components, which are normally placed close to the IC in the final application, should be close to the IC on the EME IC test board, too. They should be connected to the IC ground in order to measure only those noise currents which are relevant for emission. The EME current can be measured with the RF current probe.

All other connections, which are possibly made directly to external cabling or long PCB traces, should be connected to an impedance-matching network. This matching network is connected to the peripheral ground on the component side of the PCB. This allows single point measurements using 50 Ω impedance measurement equipment according to the specification in 6.4 (see also Figure E.4, for example R3, C4, R2). In order to obtain constant RF characteristics in a large frequency range, the peripheral ground and the RF-shield ground should be connected close to the matching network (see also Figure E.4, connection d3).

EME relevant currents returning to the IC through the peripheral ground and RF-shield ground can be measured by connecting them to the IC ground using only the 1 Ω RF current probe.

PCB specification:

– Size:	Circular PCB, maximum diameter 110 mm (for mechanical size, see Figure E.3)
– Material:	
epoxy type:	NEMA FRL
thickness:	3 mm
copper:	35 µm
layers:	2
dielectric constant:	4,7



* d1, d2, d3 are through-hole connections to RF ground

** Only needed with open drain outputs

Figure E.4 – Example of an EME IC test system

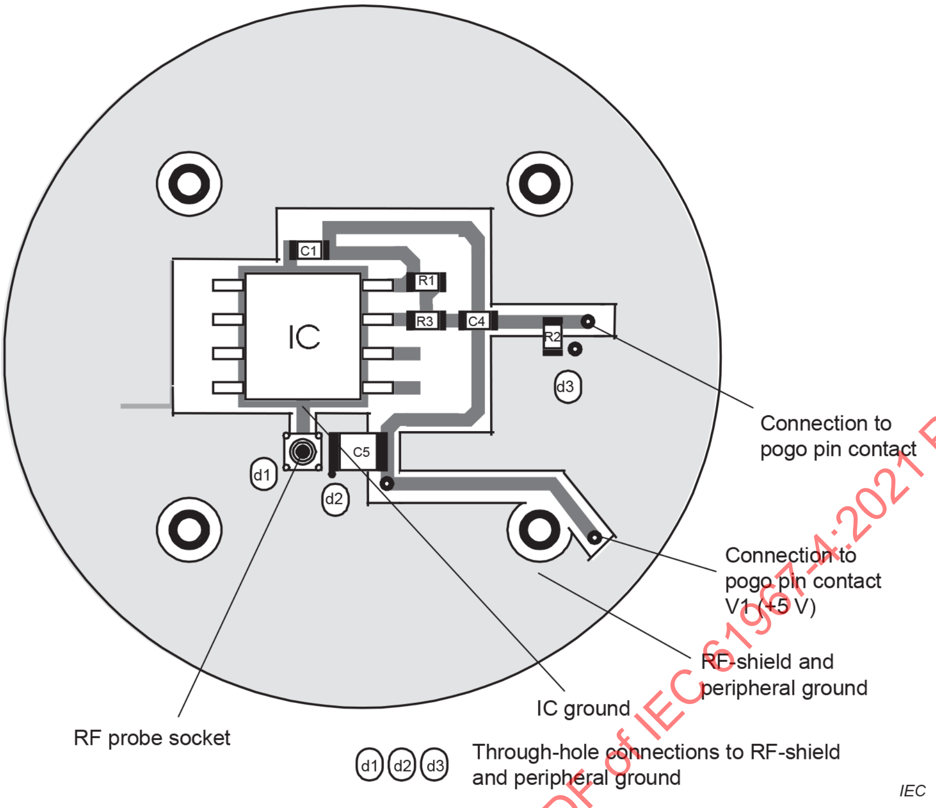


Figure E.5 – Component side of the EME IC test board

E.3.3 PCB layout and component positioning

In order to achieve a high degree of reproducibility of measurement results between different test boards, the EMC IC test board has to meet certain requirements.

The IC PCB traces should have an impedance of 150 Ω to connect the impedance matching network with low reflection. To achieve this, the PCB traces should be made in microstrip line technique, whereby the signal trace is carried on the component side and the RF-shield ground on the bottom side. For a dielectric constant of approximately 4,7, the ratio of track width to the thickness of the PCB should be 0,1 which results in a PCB thickness of 3 mm to a track width of 0,3 mm.

The IC under test should be centred and mounted onto the component side (see also Figure E.5).

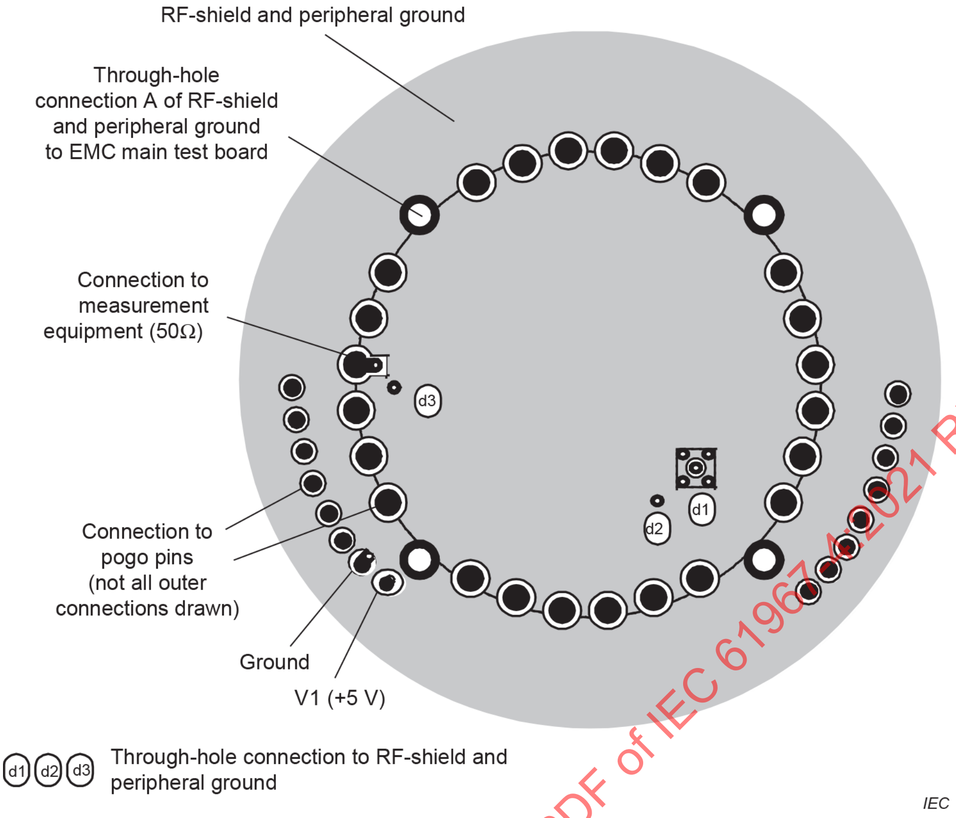


Figure E.6 – Bottom side of the EME IC test board

The impedance matching network should be placed on the outer side close to the pogo pin, so that the connection from the EME IC test board to the EMC main test board achieves a transfer impedance of 50 Ω. SMD components should be used (see Figure E.4).

The IC ground, the peripheral ground and Vdd should be routed on the component side. Ideally, the bottom side should be a continuous area of RF-shield ground and no signal traces should be routed if possible (see Figure E.6).

Apart from the central connection of peripheral ground and RF-shield ground at the matching networks (Figure E.5, Figure E.6, connection d2), they should be connected at one additional point (preferably at the supply filter capacitor C5).

Annex F
(informative)

150 Ω direct coupling networks for common mode emission measurements of differential mode data transfer ICs and similar circuits

F.1 Basic direct coupling network

In Figure F.1 the basic circuit of a coupling network is shown. The resistors R4, R5 and R6 represent termination resistors which can be needed to operate the DUT properly. They also may be incorporated in the coupling network in whole or in part if appropriate. Examples are shown later (see Clauses F.2, F.3 and F.4).

Other types of coupling networks, e.g. impedance matching networks and suitable couplers as defined in the CISPR 16-1-2 [1] can be used too.

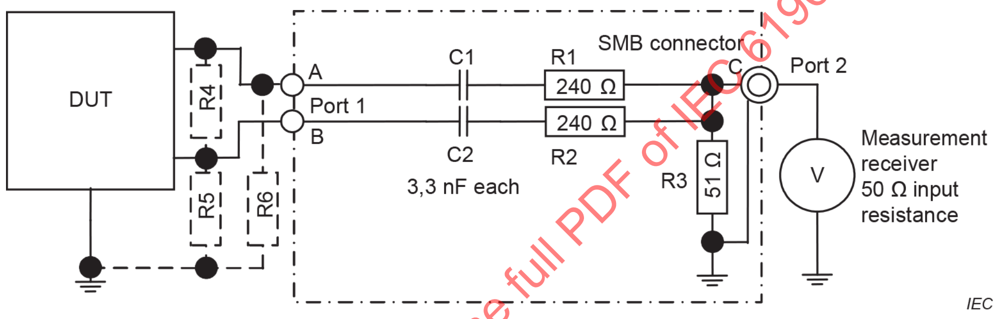


Figure F.1 – Basic direct coupling for common mode EMC measurements

The connections A and B have to be connected to the DUT during the emission or immunity measurement. For the emission measurement, a test receiver is connected to connection C.

By default, the resistor values R1, R2 will be chosen to represent a common-mode 150 Ω load together with R3 in parallel connection with the test receiver input impedance. The common-mode impedance tolerances from IEC 61000-4-6 apply.

R1 and R2 should closely match. By default, the matching tolerance should be better than 10^{-3}. The values of C1 and C2 are about half of the value of the capacitor value used for a single pin measurement setup. C1 and C2 should also closely match. Because the impedances of C1 and C2 should be small compared respectively to R1 and R2, the matching tolerance may be not so tight as with the resistors. By default, for C1 and C2 a matching tolerance of better than 10^{-2} is sufficient.

The absolute values of R1 and R2 may be changed if needed for proper function of the IC or other needs. In that case, the new values shall be presented in the test report and test specification together with the S21 measurement and S21 calculation.

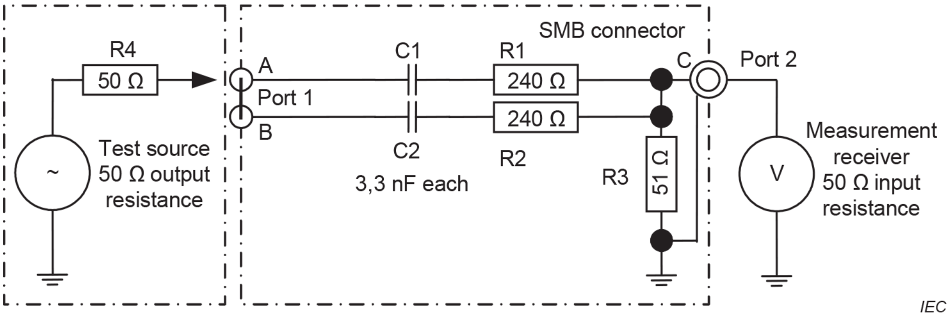


Figure F.2 – Measurement setup for the S21 measurement of the common-mode coupling

For the measurement of the S21 of the coupling network with respect to emission, the IC is replaced by a test source and connection A and B are connected together to form port 1 (see Figure F.2). Due to the simple coupling network, the magnitude of S21 can be estimated by the following equation:

$$|S21| = 20 \times \log\left(\frac{2 \times (R3 // 50)}{R1 // R2 + R3 // 50 + R4}\right) (dB)$$

C1 and C2 are used for DC-blocking. They cause a deviation from the calculated value of S21 towards low frequencies. The corner (−3 dB) frequency can be estimated with the following equation:

$$f_{c\_s21} = \frac{1}{(4 \times \pi \times C1 \times (0{,}5 \times R1) + R3 // 50) + R4}$$

Taking the values in Figure F.3 as an example, the calculation results in:

|S21| = −11,8 dB

f_{c_s21} = 123,5 kHz

F.2 Example of a common-mode coupling network alternative for LVDS or RS485 or similar systems

In Figure F.3, the RF-coupling network is changed to get an appropriate termination for the bus (60 Ω). This termination can also be used for the measurement of other communication ICs that operate with such low differential termination impedance.

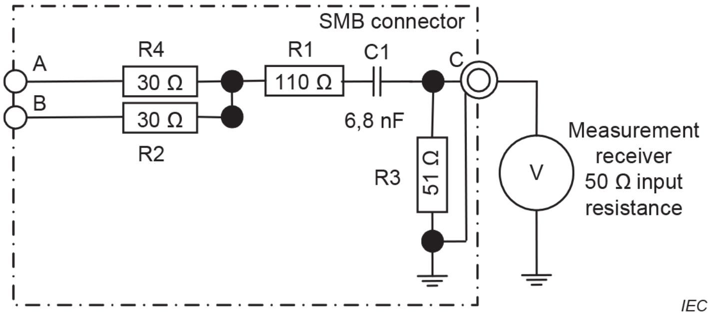


Figure F.3 – Using split load termination as coupling for measuring equipment

NOTE R1, R2 and R4 as a star-network can be substituted by a delta-network instead, which would allow the line-loading resistance to be applied outside this network.

The calculation of the relevant parameter results in:

$|S21| = -12$ dB

$f_{c\_S21} = 117$ kHz.

F.3 Example of a common-mode coupling network alternative for differential IC outputs to resistive loads (e.g. airbag ignition driver)

Here, the basic principle of the split termination coupling is adapted to a differential load of only 2 Ω.

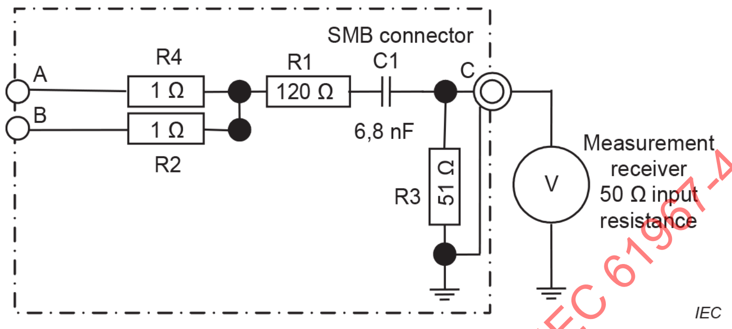


Figure F.4 – Using split load termination as coupling for measuring equipment

The results of the calculation are as follows:

$|S21| = -12{,}2$ dB

$f_{c\_S21} = 114$ kHz

F.4 Example of a common-mode coupling network for CAN systems

This exclusive example coupling network is already in use. CAN systems do not have a differential termination which can be used for injection. Thus, the basic configuration (see Figure F.1) is used with changed component values (see Figure F.5). The S21 is now changed from −11,8 dB to −8,6 dB. This has to be shown in the test report by S21 measurement and by calculation.

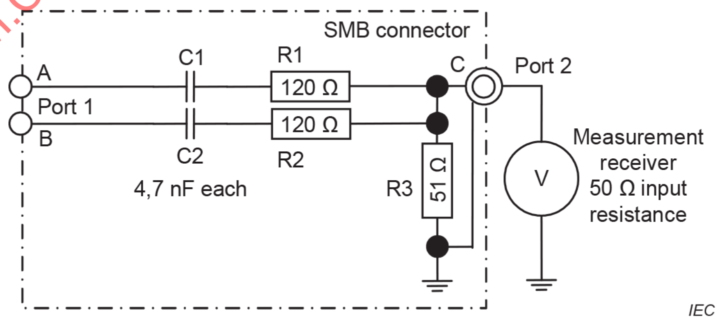


Figure F.5 – Example of an acceptable adaptation for special network requirements (e.g. for CAN systems)

NOTE This network does not represent the 150 Ω common-mode loading as indicated.

The results of the calculation are as follows:

$|S21| = -8{,}6$ dB

$f_{c\_S21} = 125$ kHz

Annex G
(informative)

Measurement of conducted emissions in extended frequency range

G.1 General

The measurement methods described in the main part of this document have been developed to enable reliable and comparable measurements of conducted emissions at pin level of ICs in the frequency range from 150 kHz up to 1 GHz. This was based on the assumption that relevant emissions of IC applications are caused by RF currents or voltages generated by internal circuit blocks of the IC which are distributed via IC pins, PCB traces and the connected wiring harness.

New digital broadcast and mobile services with operating frequencies up to 6 GHz create a demand for RF emission results of ICs also in an extended frequency range. The frequency range above 1 GHz is currently covered by radiated emission measurement methods of ICs, defined in other parts of this series of standards. In addition to that, there is an interest to extend the frequency range for conducted test methods to enable also selective emission analyses at IC pin level in extended frequency range.

The relevance and applicability of conducted test becomes more and more limited with increasing frequency. A frequency extension of the conducted emission measurement method with several restrictions could be achieved e.g. up to 3 GHz. The correlation between conducted and radiated emission results to emission phenomena in real application still needs to be determined. Therefore, the appropriate measurement method (conducted or radiated) should be carefully selected depending on the investigation target, known or expected disturbance phenomena and the application of the IC.

For conducted emission measurements in the extended frequency range above 1 GHz, special care needs to be taken to avoid that parasitics and coupling of passive components and layout or unwanted radiation of test setups affect or dominate the measurement result. Therefore, just to increase the measurement frequency range is not sufficient. This can lead to wrong results and interpretations, especially when different test boards and setups are used and a result comparison and reproducibility is of interest.

This Annex G describes requirements and limitations of conducted emission measurements methods in the extended frequency range above 1 GHz; it is intended to support the development of proper measurement setups for reliable and comparable conducted emission results, and provides some guidance.

G.2 Guidelines

G.2.1 Measurement network

The requirements for measurement networks in the extended frequency range are in principle the same as for the current frequency range up to 1 GHz described in 6.2 and 6.4. The measurement network and related coupling and decoupling components should not affect the function or performance of the IC under test (DUT) configured to operate in typical application conditions.

In order to ensure reliable and comparable results, the measurement networks assembled on the test board should provide a continuous transfer frequency characteristic (S21) within the ±3 dB tolerance band free of resonances in the used frequency range.

In Figure G.1, an example of a test circuit with a 150 Ω network is shown. The typical 1 Ω RF current probes have a limited RF performance in the higher frequency range and therefore they are not considered as a proper solution for the extended frequency.

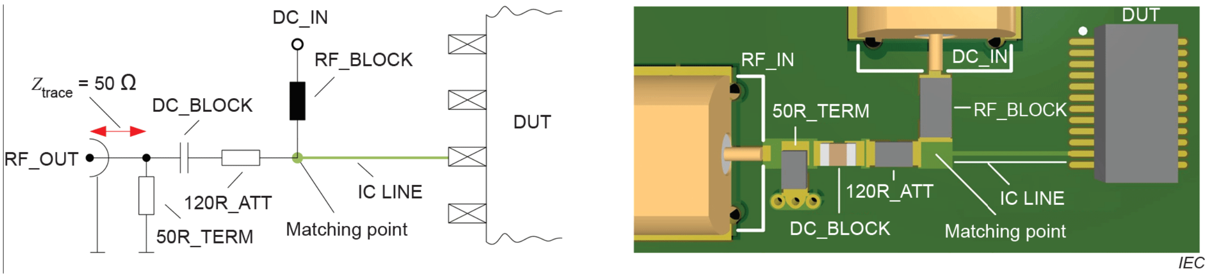
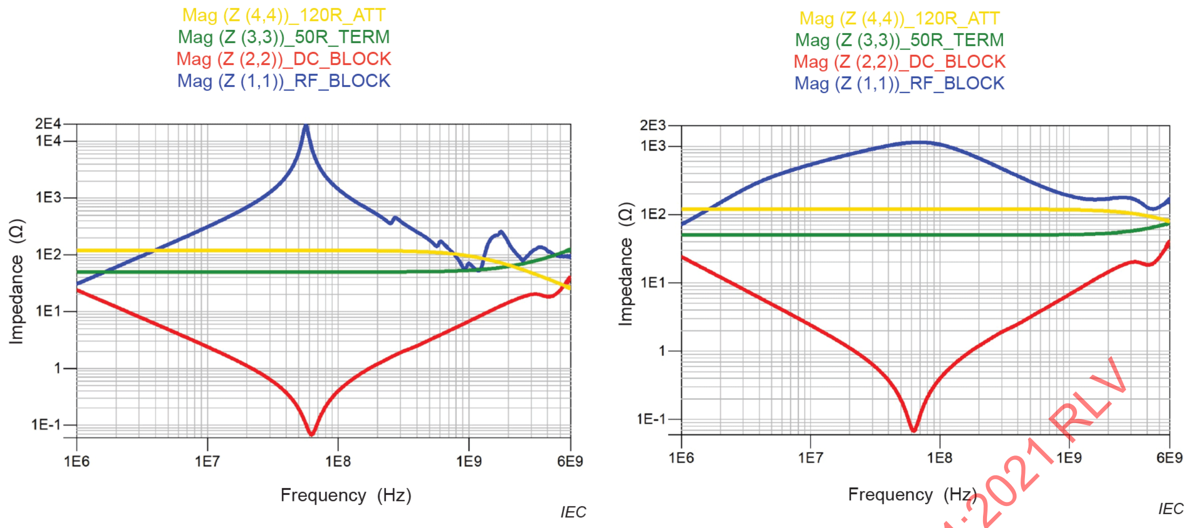


Figure G.1 – Example of a 150 Ω measurement network

G.2.2 Network components

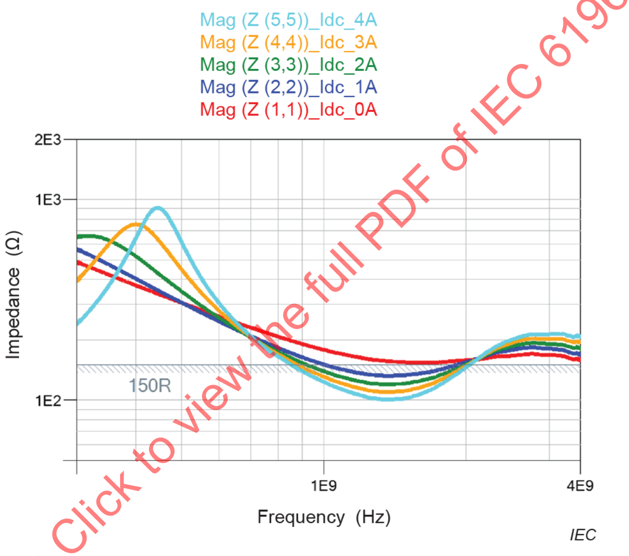
The network components used to build up the measurement and coupling/decoupling network should be selected to support both, IC operation and RF performance properly.

For the measurement network, it is recommended to use components for surface mounted assembly with defined value up to the targeted frequency range or special RF components. It is recommended to verify the RF performance of the components by measurements under application conditions on a test board that does not affect the results. The RF decoupling component (e.g. DC feed inductors, RF decoupling chokes) should be verified under loading condition, e.g. the rated DC current. In Figure G.2, examples of the frequency characteristic for matching/termination resistor, DC decoupling capacitor and RF decoupling choke are shown.



a) **typical components used up to 1 GHz**

b) **RF components to be used above 1 GHz**



c) **Load current effect on RF decoupling chokes**

Figure G.2 – Example of RF characteristic of network components

Above a certain frequency, the RF performance of network components is affected by parasitics. This limits the application frequency range of the measurement network to keep the 150 Ω performance in the ± 3 dB tolerance band.

To avoid unwanted effects on the measurement results, special care should be taken on the RF decoupling components. The impedance of the RF decoupling component should be as high as possible but at least 150 Ω in the used frequency range. This requirement is challenging if a DC supply or load current of several amperes (e.g. 20 A for a power IC) needs to be handled. RF decoupling chokes with a broadband characteristic above 1 GHz have a limited current handling capability (e.g. 100 mA up to 4 A). This limits the application of the method to ICs with lower supply and load current, or needs a respective current adjustment for testing.

The connectors used to connect the RF cable from the measurement system with the coupling network on the test board should provide a respective RF performance over the frequency range to avoid reflections and resonances in the RF path.

NOTE The RF performance varies significantly between straight and edge connectors as well as between soldered and screwed connectors.

Mandatory or recommended filter components of the IC are not considered here, they are considered as part of the IC.

G.2.3 Network layout

The layout of the measurement network as well as all traces connected to the IC pin under test are important for the RF performance. The network components should be placed as compact as possible and the trace length between coupling network and the IC pin under test should be as short as possible to meet the ± 3 dB criteria. For example, for 3 GHz the critical trace length (l_{crit}) should be less than 10 mm to keep $l_{crit} < \lambda/10$, respectively for 6 GHz the trace length should be less than 5 mm.

NOTE Nominal velocity of propagation depends on PCB material parameters (ε_r).

The impedances depending on the operation mode of the IC and/or optional and mandatory components are not considered.

In order to get a proper impedance characteristic for the RF traces of the network, the material parameter (e.g. ε_r, tan(δ)) of the test board should be known and controlled to keep tolerances within the target range. Care should be taken by selecting test board material. Standard PCB material has much wider tolerances than RF material in this respect. In any case, a simulation of the network layout with the right test board material parameters is recommended to design and verify the RF performance of the measurement network over the whole frequency range.

The test board should provide a solid GND plane underneath the measurement network. The effect of top layer GND on the RF performance of the coupling network should be considered for test board design. Vias and layer changes in the RF path should be avoided.

G.2.4 Network verification

The RF performance of the measurement network should be verified by a S21 parameter measurement between the RF connector of the test network and the pad of the IC pin under test, or if used the pad of the mandatory component in front of the IC pin under test. The IC and the mandatory or recommended filter components are removed for this measurement. Supply planes, mandatory for proper connection of the IC, may remain connected but can affect the result. This needs to be documented and considered by result evaluation. All other components connected to the measurement network as RF decoupling components of biasing, signal stimulation or monitoring networks remain populated and connected as intended during the measurement. Auxiliary equipment does not need to be connected and can be replaced by a termination or short to GND.

The measurement should be performed with a network analyzer calibrated up to the cable ends to be connected to the connector of the measurement network. Reflections at the transition point from the cable to the connector should be avoided.

Examples of respective S21 characteristics of the measurement networks implemented on a test board are shown in Figure G.3. The characteristics are derived from different board design simulations with real component models and tuned component models. The diagram shows the challenge in the higher frequency range dependent on trace length from network to the IC.

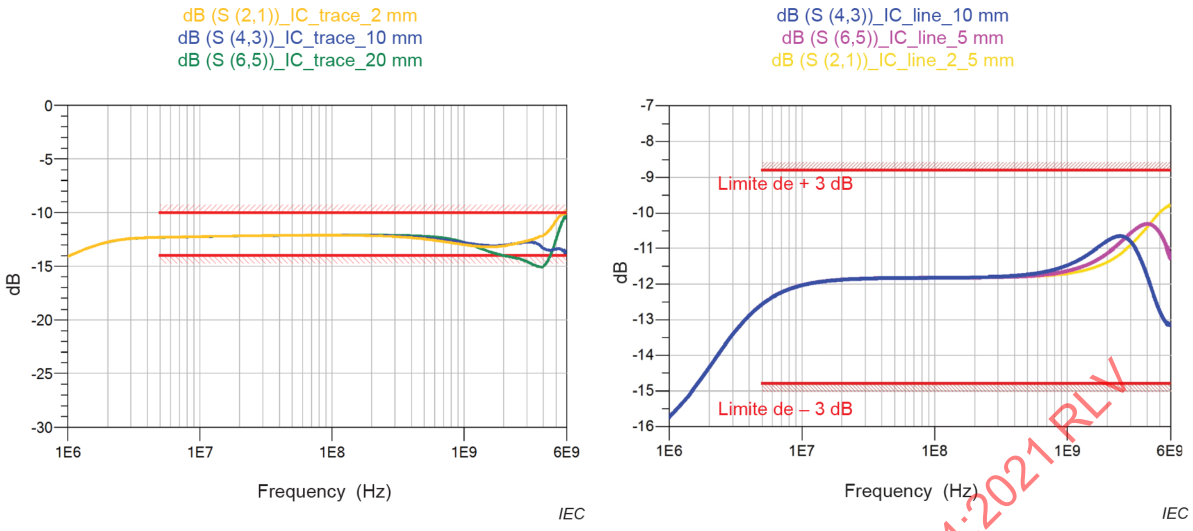


Figure G.3 – Examples of S21 characteristic by simulation

If a network is designed and simulation and measurement show the same S21 characteristic with less than 0,5 dB deviation, it can be considered as reliable enough and used multiple times on a test board as fixed building block without a demand for multiple measurement verification.

G.2.5 Test board

The test board usually combines an application circuit of the IC under test and the measurement networks on the same PCB. In order to achieve the RF characteristic of the measurement networks as described above, they shall be placed and connected very close to the IC pins of interest. Moreover, for proper setting and operation of the IC, a typical application circuit with mandatory components, loading and auxiliary circuits for stimulation and monitoring shall be placed as well. Depending on the complexity and pin count of the IC, this can become very challenging and provide some constraints for the test PCB design.

As described above, the measurement network design should be compact and connected via short traces to the IC pin. It is recommended to use fixed building blocks with a known RF performance. If the network design needs to be modified or newly designed, it is recommended to use simulation tools for test board design and first verification. This also allows the identification of unwanted cross coupling between RF traces and other signal lines on the test board.

An example of a simple test board section with RF measurement network, IC with mandatory components and other signal lines are shown in Figure G.4. The red highlighted signal line in Figure G.4 is exposed for cross coupling.

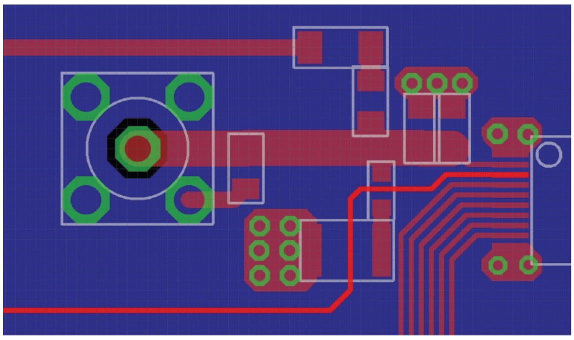


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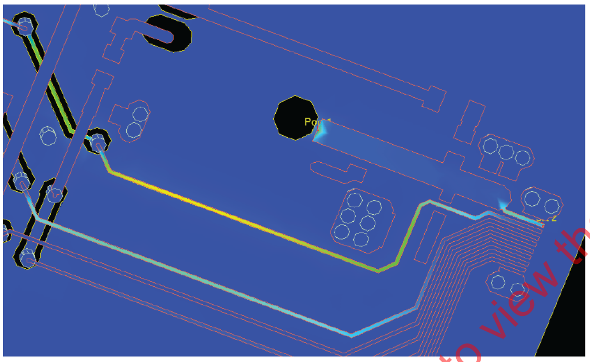
Figure G.4 – Examples of test board section

A simulation result of the cross coupling between the RF measurement network and signal lines is shown in Figure G.5 and the related effect on the S21 transfer characteristic is shown in Figure G.6. Special care should be taken to avoid parallel traces over longer distance in order to minimize unwanted resonances and cross coupling in compact designs.



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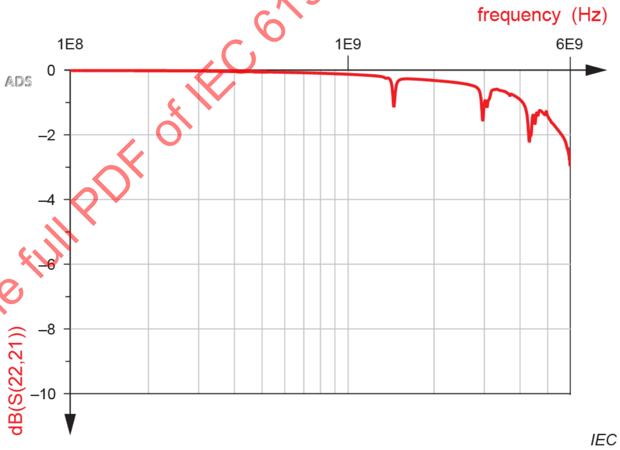

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Figure G.5 – Examples of unwanted cross coupling between measurement network and traces on test PCB

Figure G.6 – Examples of unwanted signal line cross coupling on S21 transfer characteristic of RF measurement network

Another important aspect that needs to be considered for test board design is the connection of other signal lines (e.g. pull up, monitoring) to the IC pin under test where the measurement network is connected. In Figure G.7, an example of a test board with additional signal stub line (42 mm length) connected to IC pin is shown. The effect of the stub line length on the S21 transfer characteristic is shown in Figure G.8. The impedance of the line termination and the position of this termination is important and needs to be considered for board design.

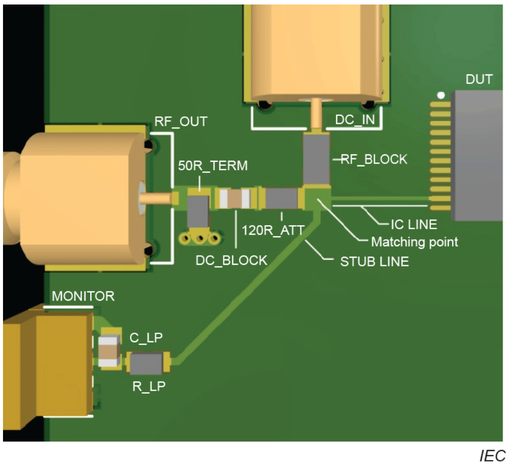

Figure G.7 – Examples of test board with additional signal line connected to IC pin

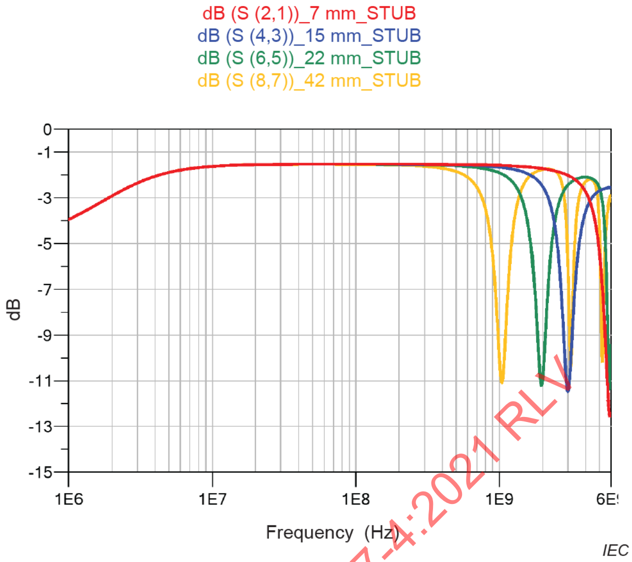

Figure G.8 – Examples of stub lines length effects on S21 transfer characteristic of RF measurement network

G.3 Application area

The emission measurements conducted in the frequency range above 1 GHz become more and more challenging with increasing frequency due to several effects.

The size of the measurement network and the connection to the IC pin requires a compact design, proper matching and/or short trace length $l_{\text{crit}} < \lambda/10$ to fulfil ± 3 dB requirement free of resonances. Furthermore, the consideration and minimization of unwanted cross coupling between traces on the board introduce additional constraints and requires special measures or multi-layer boards to avoid unwanted effects on the single pin result. Therefore, the application of the method is limited to a low number of selected pins of an IC. The method can be useful for dedicated analyses of single, special selected pins, but not for a full characterization of complex ICs with higher pin count.

The components used for RF measurement networks and RF decoupling circuits for biasing, loading, stimulating and monitoring IC functions have to ensure a proper RF characteristic in the frequency range of interest while providing unaffected operation conditions for the functionality of the IC under test. Proper RF characteristic in the higher frequency range and higher voltage and current rating of the components seems to be a contradiction. Thus, the conducted test method application is limited to few amperes (e.g. 100 mA to 4 A) of supply or load current due to component limitation. A typical application e.g. of power ICs with 80 % loading condition cannot be realized because reduced supply or load currents can lead to performance limitations or untypical operation modes of the IC.

Considering IC applications and conducted test method origin, the validity of the assumption, that RF currents and voltages distributed from the IC source via pins and connected traces and wires are the dominant cause for the emission phenomena of an application, needs to be verified for the frequency range above 1 GHz. With increasing frequency, the effects of direct radiation from the IC and its external circuitry can increase significantly and also the system implementation can play a significant role. Therefore, it is recommended to analyze the phenomena behind emission issues in application to choose the right measurement method to generate useful data of the IC.

It is not applicable and thus not recommended to apply conducted emission measurements in the extended frequency range to all pins of an IC and also not to all ICs. A selection guide or table, such as Table G.1, can support the user to make a smart choice for IC types, IC functions, operation frequency, current consumption, pin classes, package types, dimensions, etc. in future. In general, ICs with operating frequencies and harmonics (e.g. < 10th harmonics) exceeding 1 GHz could be more relevant for emission in the extended frequency range than others. Then pin selection should be done based on IC design to link high frequency IC functions to respective global and/or local pins.

Table G.1 – Draft selection table for conducted emission measurements at pins above 1 GHz

IC type	IC functions	Operating frequency (MHz)			Pin current rate (A)			Pin type / class	Package type / dimension	Test applicable recommended	
		< 10	10 to 100	> 100	< 1	1 to 4	> 4			yes	no

If a conducted emission measurement in the extended frequency range is performed and results are distributed, it is strongly recommended to provide the S21 verification diagram of the measurement network(s) along with the full layout of the test board to make an interpretation of the data possible. The simple approach just to design a test board and run measurements into the extended frequency range above 1 GHz is strongly discouraged when independent reliable data are needed.

Bibliography

[1] CISPR 16-1-2, *Specification for radio disturbance and immunity measuring apparatus and methods – Part 1-2: Radio disturbance and immunity measuring apparatus – Coupling devices for conducted disturbance measurements*

[2] CISPR 25, *Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers*

SOMMAIRE

COMMISSION ÉLECTROTECHNIQUE INTERNATIONALE

CIRCUITS INTÉGRÉS – MESURE DES ÉMISSIONS ÉLECTROMAGNÉTIQUES –

Partie 4: Mesure des émissions conduites – Méthode par couplage direct 1 Ω/150 Ω

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La Norme internationale IEC 61967-4 a été établie par le sous-comité 47A: Circuits intégrés, du comité d'études 47 de l'IEC: Dispositifs à semiconducteurs.

Cette deuxième édition annule et remplace la première édition parue en 2002 et l'Amendement 1:2006. Cette édition constitue une révision technique.

Cette édition inclut les modifications techniques majeures suivantes par rapport à l'édition précédente:

a) la gamme de fréquences de 150 kHz à 1 GHz a été supprimée du titre;
b) la gamme de fréquences recommandée pour la méthode à 1 Ω a été réduite à 30 MHz;

c) l’Annexe G avec les recommandations et les lignes directrices pour l’extension de gamme de fréquences au-dessus de 1 GHz a été ajoutée.

Le texte de cette Norme internationale est issu des documents suivants:

Projet	Rapport de vote
47A/1101/CDV	47A/1107/RVC

Le rapport de vote indiqué dans le tableau ci-dessus donne toute information sur le vote ayant abouti à son approbation.

La langue utilisée pour le développement de la présente Norme internationale est l’anglais.

Ce document a été rédigé selon les Directives ISO/IEC, Partie 2, il a été développé selon les Directives ISO/IEC, Partie 1 et les Directives ISO/IEC, Supplément IEC, disponibles sous www.iec.ch/members_experts/refdocs. Les principaux types de documents développés par l'IEC sont décrits plus en détail sous www.iec.ch/standardsdev/publications.

Une liste de toutes les parties de la série IEC 61967, sous le titre général *Circuits intégrés – Mesure des émissions électromagnétiques* peut être consultée sur le site web de l'IEC.

Les futures normes de cette série porteront dorénavant le nouveau titre général cité ci-dessus. Le titre des normes existant déjà dans cette série sera mis à jour lors de la prochaine édition.

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CIRCUITS INTÉGRÉS –
MESURE DES ÉMISSIONS ÉLECTROMAGNÉTIQUES –

Partie 4: Mesure des émissions conduites –
Méthode par couplage direct 1 Ω/150 Ω

1 Domaine d'application

La présente partie de l'IEC 61967 spécifie une méthode de mesure de l'émission électromagnétique (EME) conduite des circuits intégrés par mesure directe des courants RF avec une sonde résistive de 1 Ω et mesure des tensions RF en utilisant un réseau de couplage de 150 Ω. Ces méthodes assurent un degré élevé de reproductibilité, ainsi que la corrélation des résultats des mesures EME.

2 Références normatives

Les documents suivants sont cités dans le texte de sorte qu'ils constituent, pour tout ou partie de leur contenu, des exigences du présent document. Pour les références datées, seule l'édition citée s'applique. Pour les références non datées, la dernière édition du document de référence s'applique (y compris les éventuels amendements).

IEC 61000-4-6, *Compatibilité électromagnétique (CEM) – Partie 4-6: Techniques d'essai et de mesure – Immunité aux perturbations conduites, induites par les champs radioélectriques*

IEC 61967-1, *Circuits intégrés – Mesure des émissions électromagnétiques – Partie 1: Conditions générales et définitions*

3 Termes et définitions

Pour les besoins du présent document, les termes et définitions de l'IEC 61967-1 s'appliquent.

L'ISO et l'IEC tiennent à jour des bases de données terminologiques destinées à être utilisées en normalisation, consultables aux adresses suivantes:

- IEC Electropedia: disponible à l'adresse http://www.electropedia.org/;
- ISO Online browsing platform: disponible à l'adresse http://www.iso.org/obp.

4 Généralités

4.1 Principes de base de mesure

Le niveau d'émission maximal toléré d'un CI (circuit intégré) dépend du niveau d'émission maximal admis du système électronique qui contient le circuit intégré, ainsi que du niveau d'immunité des autres éléments du système électronique proprement dit (appelé CEM intrinsèque). La valeur de ce niveau d'émission dépend des paramètres (ambiants) spécifiques au système et à l'application. Pour caractériser les CI, c'est-à-dire fournir des valeurs EME types pour une fiche technique, une méthode de mesure simple et des montages de mesure non résonants sont exigés pour garantir un degré élevé de reproductibilité. La base de cette procédure d'essai est explicitée dans le Paragraphe 4.1.

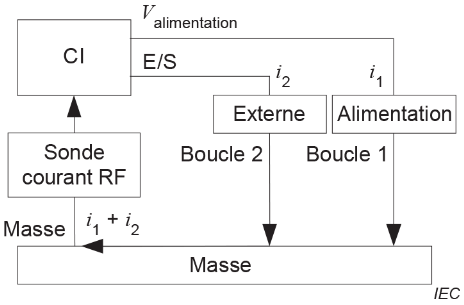


Figure 1 – Exemple de deux boucles d'émission retournant au CI par l'intermédiaire de la masse de référence

L'émission d'un CI est générée par des variations de tensions et de courants suffisamment rapides à l'intérieur du CI. Ces variations entraînent les courants RF à l'intérieur et à l'extérieur du CI. Les courants RF provoquent une EME conduite qui est principalement distribuée par les boucles de conducteurs de broches du CI dans la carte à circuit imprimé et le câblage. Ces boucles sont considérées comme des antennes d'émission. Par comparaison avec la dimension de ces boucles, les boucles de la structure interne du CI sont considérées comme petites.

Les courants RF qui accompagnent l'action des CI ont une amplitude, une phase et une répartition spectrale différentes. Tout courant RF a sa propre boucle de retour vers le CI. Toutes les boucles retournent principalement vers le CI par l'intermédiaire de la liaison à la masse ou de la liaison d'alimentation. La Figure 1 représente ce processus pour deux boucles avec retour par la liaison à la masse. La boucle 1 représente le faisceau de câblage d'alimentation pour le CI, tandis que la boucle 2 représente l'acheminement d'un signal de sortie. Le trajet de retour commun par la masse constitue un emplacement approprié pour mesurer l'EME conduite en tant que mesure du courant somme RF revenant à la broche de masse. Cet essai est appelé "essai de mesure du courant RF".

Lorsque le CI en essai ne dispose que d'une seule broche de masse et que toutes les autres broches sont supposées contribuer sensiblement à l'EME, le courant somme RF est mesuré entre la broche de masse du CI en essai et la masse elle-même (voir $i_1 + i_2$ à la Figure 1).

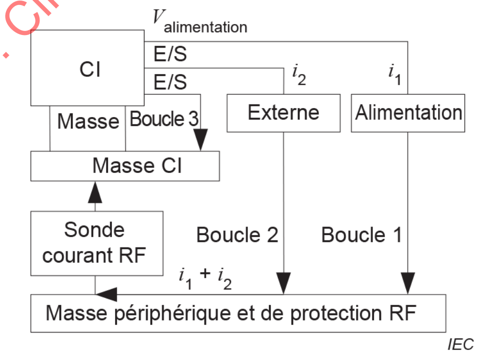


Figure 2 – Exemple de CI avec deux broches à la masse, une petite boucle E/S et deux boucles d'émission

Si le CI en essai dispose de plusieurs broches à la masse ou si certaines broches ne sont pas supposées contribuer outre mesure à l'EME dans son ensemble, le CI en essai a alors son propre plan de masse comme représenté à la Figure 2. Ce plan de masse est appelé "masse CI". Il est isolé de l'autre masse, appelée "masse périphérique et de protection RF". Le courant RF est mesuré entre la masse CI et la masse périphérique.

Les CI sont souvent utilisés dans des configurations différentes selon l'application. Par exemple, un microcontrôleur peut être utilisé comme un contrôleur monopuce dont les accès E/S sont directement reliés au système de câblage externe. Afin de comprendre l'influence d'une seule broche E/S sur le niveau d'émission du CI, une méthode de mesure supplémentaire, utilisant le même matériel, est prévue. Cette mesure est appelée "mesure de la tension RF monobroche des broches du CI" (voir également 4.3). Outre le courant somme RF, il peut être intéressant de mesurer le courant RF d'une seule broche d'alimentation pour l'analyse d'un CI. Cela peut également être effectué par l'application de la sonde de mesure des courants RF. La sonde de courant RF peut par exemple être appliquée à l'une des broches de masse ou d'alimentation, afin de quantifier la contribution de la broche mesurée à l'émission dans son ensemble.

4.2 Mesure du courant RF

Dans la procédure d'essai, cette mesure doit être effectuée en mesurant la tension à travers une résistance de 1 Ω sous forme d'une sonde de courant RF utilisant un récepteur de mesure. La mesure doit être effectuée à l'emplacement indiqué à la Figure 1 et à la Figure 2. La construction de la sonde de courant RF est spécifiée en 6.2. Le niveau de tension RF mesuré par le récepteur est la tension résultant de tous les courants RF retournant au CI à travers l'impédance de la sonde. La mesure de tension peut être convertie en courant en divisant la tension par l'impédance de la sonde, si l'impédance de la sonde est déterminée pour la gamme de fréquences applicable, par exemple dans un rapport de vérification.

NOTE 1 L'impédance de la sonde peut varier en fonction de la fréquence, causée par des inductances parasites de la sonde, la gamme de fréquences utilisables peut donc être limitée.

NOTE 2 L'impédance de la sonde provoque, en fonction du courant du CI, une chute de tension qui peut affecter le bon fonctionnement du CI et limiter l'application de cette méthode.

4.3 Mesure de la tension RF aux broches du CI

Cette mesure est utilisée pour identifier la contribution d'une seule broche ou d'un groupe de broches à l'EME du CI en essai. Cette mesure est uniquement appliquée aux broches du CI en essai qui sont destinées à être reliées directement à des pistes de cartes à circuit imprimé ou à des faisceaux de câblage de grande longueur (plus de 10 cm) (par exemple E/S, alimentation). Ces broches sont chargées par une impédance typique de mode commun de 150 Ω comme spécifié dans l'IEC 61000-4-6. Pour relier le récepteur de mesure, qui a une impédance d'entrée de 50 Ω, la charge est à établir comme un réseau d'adaptation d'impédance. Ce réseau d'adaptation est défini en 6.4.

D'autres broches E/S d'un CI peuvent être chargées comme spécifié dans la partie générale de l'IEC 61967-1.

4.4 Evaluation de la technique de mesure

Les techniques mentionnées ci-dessus ont les propriétés suivantes:

- reproductibilité élevée des mesures, du fait que peu de paramètres ont une influence sur le résultat;
- capacité de comparer différentes configurations CI (par exemple boîtiers);
- les mesures EME monobroches des différentes broches E/S dépendent de leur importance pour l'émission dans une application spécifique;
- évaluation de la contribution EME du CI en utilisant la mesure de la somme des courants;
- vérification simple de l'impédance de mesure en utilisant la mesure de la perte d'insertion;
- la mesure est également possible à de très basses fréquences.

Avec ces caractéristiques, il est possible de mesurer l'EME des CI avec un degré élevé de reproductibilité et cette technique offre par conséquent une bonne méthode de comparaison.

L'Annexe D donne un exemple de la manière dont les techniques de mesure peuvent être utilisées pour l'évaluation des CI.

5 Conditions d'essai

Toutes les conditions d'essai exigées dans le présent document sont spécifiées dans l'IEC 61967-1.

6 Appareillage d'essai

6.1 Appareil de mesure RF

L'appareillage de mesure doit satisfaire aux exigences décrites dans l'IEC 61967-1.

6.2 Spécification de la sonde de courant RF

La Figure 3 représente la construction de base de la sonde de courant RF de 1 Ω.

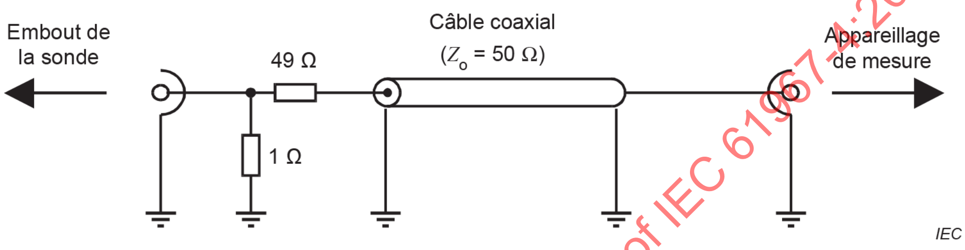


Figure 3 – Construction de la sonde de courant RF de 1 Ω

Le Tableau 1 donne une spécification détaillée pour la sonde de courant RF.

L'utilisation d'un bloc de suppression de la composante continue est recommandée pour éviter tout endommagement de l'appareillage de mesure par la tension continue. Ce bloc doit avoir un affaiblissement < 0,5 dB à la plus basse fréquence à mesurer.

Tableau 1 – Spécification de la sonde de courant RF

Gamme de fréquences	Courant continu à 30 MHz La gamme de fréquences applicable de la sonde utilisée doit être évaluée, par exemple lors d'une mesure des paramètres S, et consignée dans le rapport d'essai. Les sondes de courant actuellement commercialisées se sont avérées utilisables, par exemple jusqu'à 30 MHz seulement. Par conséquent, la largeur de bande et l'impédance en fonction de la fréquence de la sonde utilisée doivent être vérifiées et consignées dans un diagramme. Le même principe s'applique aux sondes sur carte avec des composants pour montage en surface (CMS). A l'avenir, la gamme de fréquences utilisables pourrait changer pour les sondes RF améliorées.
Résistance de mesure	Résistance RF (faible inductance) [a] 1 Ω (±1 %). La résistance de mesure peut également être composée de résistances en parallèle, ce qui accroît le courant maximal admissible traversant la sonde (par exemple 2 Ω//2 Ω) et réduit l'inductance parasite.
Résistance d'adaptation	49 Ω (±1 %)
Courant maximal	< 0,5 A
Impédance de sortie, Z_o	40 Ω à 60 Ω
Perte d'insertion dans le circuit de vérification	(34 ± 2) dB
Découplage dans le circuit de vérification	Voir la Figure A.1 et la Figure A.5.
Liaison câble	Câble coaxial souple à double protection avec une impédance de ligne de (50 ± 2) Ω. Le connecteur RF doit être monté avec une faible réflexion. La perte d'insertion comprend le câble et la sonde. Les variations de la longueur du câble impliquent la prise en compte d'un affaiblissement supplémentaire dans les résultats des mesures.
Construction	Sonde coaxiale ou construction comparable pouvant être reliée à une embase connecteur coaxial 4 mm. La résistance de mesure doit être le plus près possible de l'embout de la sonde. Elle doit être réalisée de manière à éviter tout dommage de nature mécanique. La liaison du câble de sonde doit être coaxiale; il convient que les embouts de la sonde puissent être remplacés, ils doivent toutefois être solidement reliés au câble.

[a] Il convient que l'impédance série due à l'inductance parasite soit inférieure à la résistance dans la gamme de mesures utilisée.

6.3 Essai de la capacité de la sonde de courant RF

La sonde de courant doit être soumise à un essai de fonctionnalité avec le circuit d'essai représenté et décrit en détail à l'Annexe A.

6.4 Spécification du réseau d'adaptation

Selon l'IEC 61000-4-6, un réseau de câblage peut être représenté dans la plupart des cas par une antenne d'une impédance d'environ 150 Ω. Un réseau terminal de (145 ± 20) Ω doit être utilisé pour obtenir des résultats de mesures précis sur toute la gamme de fréquences. L'appareillage de mesure habituel fournit une impédance d'entrée de 50 Ω de sorte que le réseau d'adaptation doit adapter l'impédance de la ligne de signal à l'impédance de l'appareillage. Le schéma des circuits est représenté à la Figure 4 et les caractéristiques du réseau d'adaptation d'impédance utilisé sont indiquées dans le Tableau 2. L'Annexe F et les recommandations fournissent des informations supplémentaires sur les réseaux d'adaptation pour les mesures différentielles des broches.

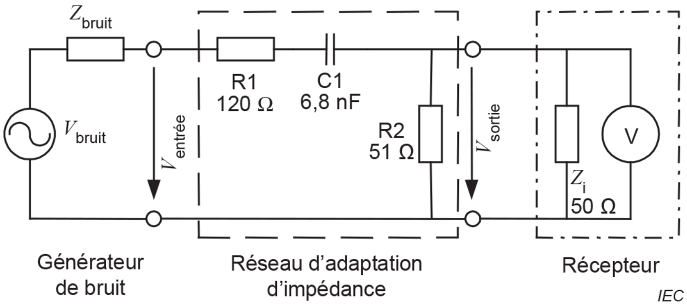


Figure 4 – Réseau d'adaptation d'impédance correspondant à l'IEC 61000-4-6

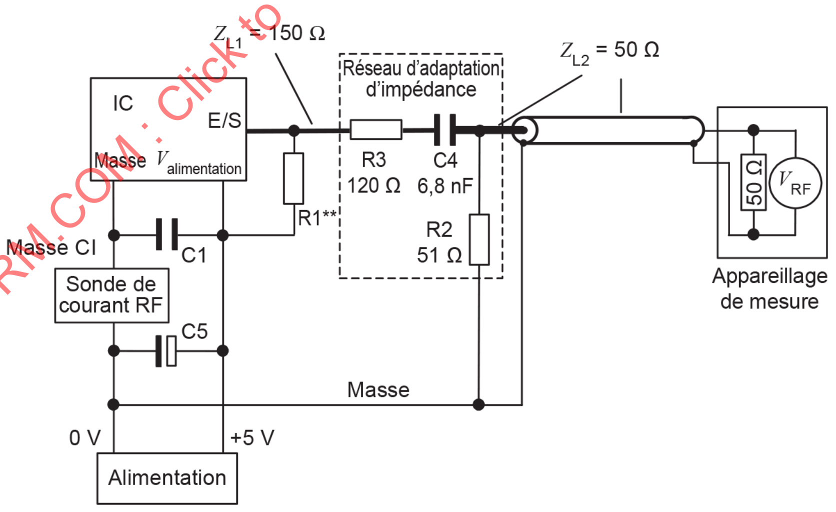
Tableau 2 – Caractéristiques du réseau d'adaptation d'impédance

Gamme de fréquences	150 kHz à 1 GHz
Impédance d'entrée, Z_i, avec impédance terminale de 50 Ω	(145 ± 20) Ω
Perte d'insertion dans un système à 50 Ω	0,258 6 (−11,75 dB ± 2 dB)
Rapport de tension $V_{\text{sortie}}/V_{\text{entrée}}$	0,173 8 (−15,20 dB ± 2 dB)

7 Montage d'essai

7.1 Configuration générale d'essai

La Figure 5 représente une configuration générale d'essai. Cette configuration générale d'essai peut être réalisée sous la forme d'une configuration spéciale d'essai (dont un exemple est donné en E.2) ou de toute autre configuration, par exemple également dans une application réelle.



** Une résistance de polarisation à l'alimentation/à la masse peut être nécessaire en fonction de l'application

Figure 5 – Configuration générale d'essai

7.2 Routage d'une carte d'essai à circuit imprimé

Les recommandations suivantes sont données pour obtenir une reproductibilité élevée des résultats des mesures et pour pouvoir faire une comparaison valable entre différentes cartes d'essai à circuit imprimé.

Il convient que la carte d'essai à circuit imprimé soit en matériau de type époxyde (d'une épaisseur de 0,6 mm à 3 mm, avec une constante diélectrique d'environ 4,7). Les faces supérieure et inférieure sont recouvertes d'une couche de cuivre d'au moins 35 µm.

Il convient que la couche inférieure soit utilisée comme plan de masse.

Si la masse périphérique et la masse CI sont utilisées pour la méthode à 1 Ω, ces deux masses sont isolées par un intervalle d'isolation. Il convient que cet intervalle d'isolation ait une valeur comprise entre 0,5 mm et 0,6 mm. Si nécessaire, la masse CI doit être située en dessous du DUT. Il convient que la taille maximale de cette surface ne dépasse pas l'empreinte minimale de boîtier de plus de 3 mm sur chaque face.

Pour obtenir la précision nécessaire pour des fréquences élevées, la capacité de couplage parasite entre masse CI et masse périphérique doit être contrôlée. Cette capacité de couplage parasite entre masse CI et masse périphérique doit être inférieure à 30 pF.

La masse CI est seulement connectée à la masse périphérique par une sonde de 1 Ω. Il convient d'utiliser une prise dans le cas d'une sonde de courant RF externe. Il convient que le blindage de l'embout de la sonde de courant RF soit connecté à la masse périphérique RF par la prise, tandis que la masse CI ou la broche de masse CI est connectée à l'embout de la sonde de courant. La connexion entre la masse CI et l'embout de la sonde doit être aussi courte que possible. Dans tous les cas, la longueur de piste ne doit pas dépasser 15 mm. Il convient que la piste soit connectée à la masse CI à la distance la plus courte par rapport au centre du DUT.

Si les lignes directrices indiquées ci-dessus ne s'appliquent pas, la caractéristique de transfert de la conception modifiée doit être déterminée et consignée dans le rapport d'essai.

Il convient que le DUT et tous les composants nécessaires pour le faire fonctionner soient montés sur la face supérieure de la carte d'essai. Il convient que la plus grande partie possible du câblage soit acheminée dans la couche supérieure. Il convient que le DUT soit placé au centre de la carte à circuit imprimé et que les réseaux d'adaptation nécessaires soient placés autour de cette partie centrale. Il convient que le câblage entre les broches du CI et le réseau d'adaptation soit conçu de manière à avoir une impédance de ligne de 150 Ω. Si l'impédance de ligne de 150 Ω est difficile à mettre en œuvre, la ligne doit avoir l'impédance maximale raisonnable, mais suffisamment courte pour être conforme aux exigences du Tableau 2.

Il convient que le câblage des sorties des réseaux d'adaptation soit conçu pour avoir une impédance de ligne de 50 Ω. L'Annexe E fournit un exemple de routage de carte à circuit imprimé.

L'alimentation doit être connectée avec un seul fil directement au condensateur C5. Ce condensateur C5 peut être un composant pour montage en surface, de type électrolytique, et avoir une valeur d'au moins 10 µF. Le condensateur C5 doit être positionné à proximité de la prise de la sonde.

La carte d'essai peut être de forme rectangulaire ou circulaire.

L'Annexe G fournit des informations supplémentaires et des lignes directrices pour les applications à gamme de fréquences étendue.

8 Procédure d'essai

Les exigences de cette procédure d'essai sont décrites dans l'IEC 61967-1.

9 Rapport d’essai

Les exigences pour le rapport d’essai sont décrites dans l’IEC 61967-1.

Les résultats des mesures des émissions peuvent être présentés en utilisant des niveaux de classification ou de référence. Un exemple de plan de classification pour niveaux d’émission est présenté à l’Annexe B. De plus, l’Annexe C montre comment ce plan de classification peut être appliqué aux niveaux de référence de montage pour les CI utilisés dans l’industrie automobile.

Annexe A
(informative)

Procédure de vérification de la sonde

Le circuit d'essai représenté à la Figure A.1 est recommandé pour la vérification de la sonde. Il se compose d'une carte à circuit imprimé utilisant les techniques de lignes microruban (voir Figure A.3). La carte à circuit imprimé a un accès d'entrée auquel le générateur RF est connecté. La sonde de courant RF à vérifier est connectée à l'accès de sortie. La sortie de la sonde de courant RF est connectée au récepteur d'essai (voir Figure A.4). Cette procédure de vérification mesure l'isolation fournie par le circuit d'essai dans un système à 50 Ω (voir également le document CISPR 16-1-2 [1][1]) et la perte d'insertion de la sonde de courant RF.

Deux mesures séparées sont recommandées. La première mesure est réalisée avec le circuit d'essai configuré comme représenté à la Figure A.1, schéma A. Noter que le shunt A n'est pas inséré. Pendant le balayage par le générateur RF de la gamme de fréquences exigée, mesurer la tension apparaissant à la sortie de la sonde de courant RF.

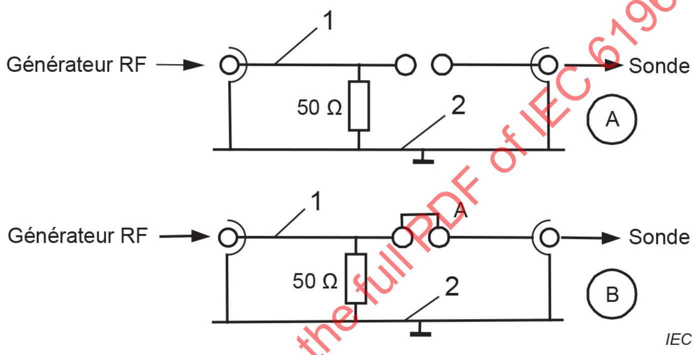


Figure A.1 – Circuit d'essai

La deuxième mesure est réalisée de manière identique à la première, mais avec le shunt A installé pour shunter le générateur RF à l'entrée de la sonde comme représenté à la Figure A.1, schéma B. Cette mesure donne la perte d'insertion de la sonde de courant RF qui indique sa sensibilité. La Figure A.2 montre un résultat d'une telle mesure.

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[1] Les chiffres entre crochets se réfèrent à la Bibliographie.

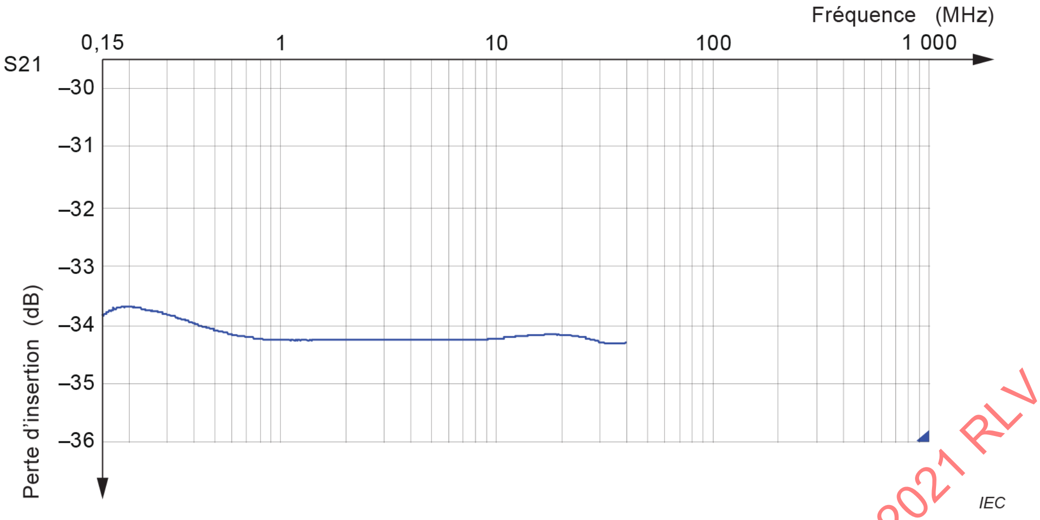
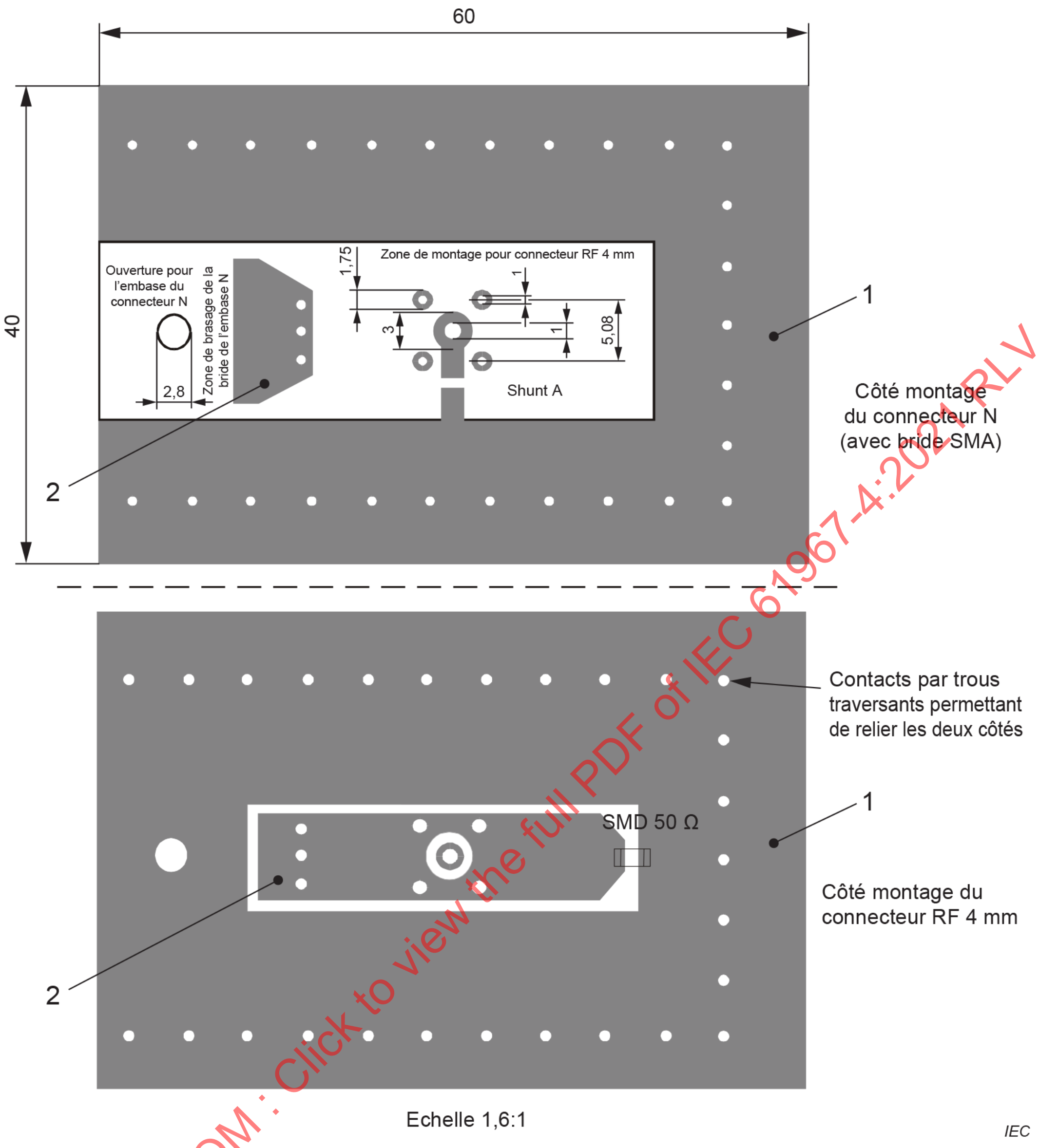


Figure A.2 – Perte d'insertion de la sonde de 1 Ω

La différence calculée des deux mesures est appelée "découplage". Il convient que le découplage soit supérieur à la limite indiquée à la Figure A.5. Le découplage est égal à la dynamique de mesure par rapport à la source du signal. Le découplage inclut les caractéristiques de qualité, la sensibilité et le blindage de la sonde.

Dimensions en millimètres



Légende

1 zone de couplage

2 masse de référence

Figure A.3 – Routage du circuit d'essai de vérification

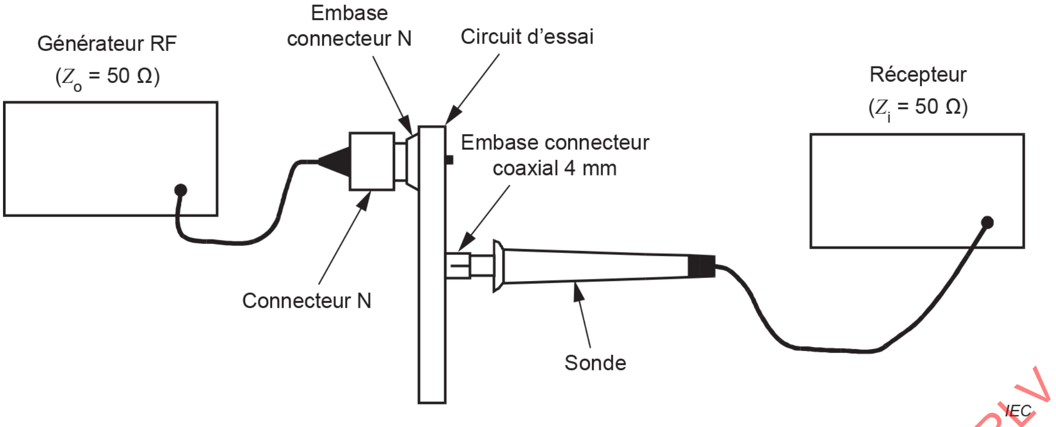


Figure A.4 – Connexion du circuit d'essai de vérification

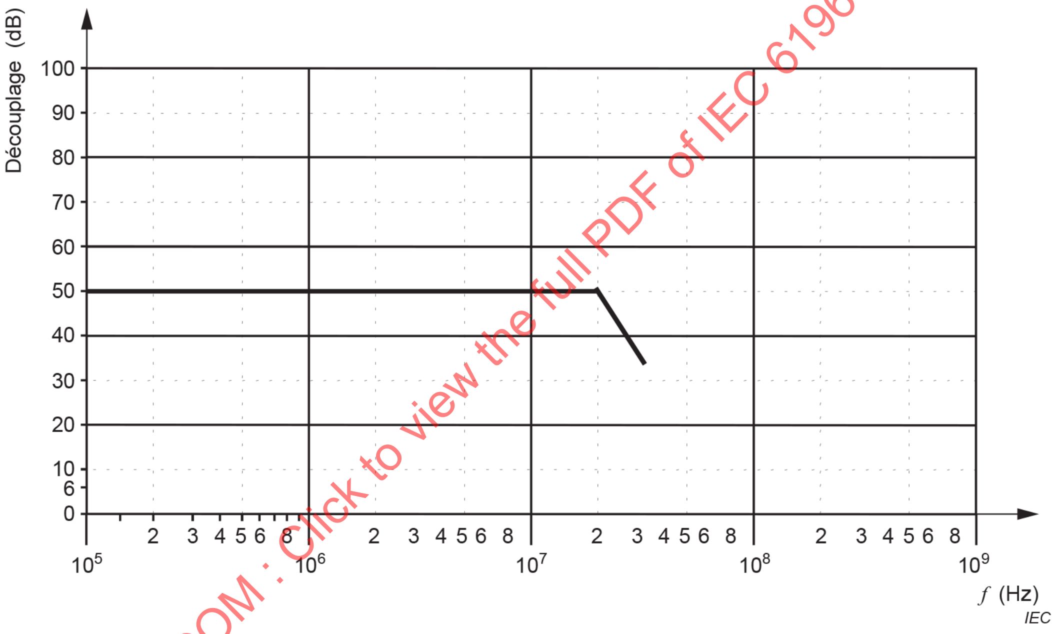


Figure A.5 – Limite minimale de découplage par rapport à la fréquence

Afin d'évaluer les performances et la gamme de fréquences applicables de la sonde de 1 Ω utilisée, il est recommandé de qualifier la caractéristique d'impédance d'entrée de la sonde. Pour ce faire, il est possible de mesurer les paramètres de diffusion à l'aide d'un analyseur de réseau vectoriel. Pour les mesures, il convient d'étalonner l'analyseur de réseau vectoriel, y compris tous les connecteurs, câbles et pistes, afin d'exclure du résultat tous les parasites du montage. Un exemple de caractéristique d'impédance d'entrée de la sonde de 1 Ω est représenté à la Figure A.6.

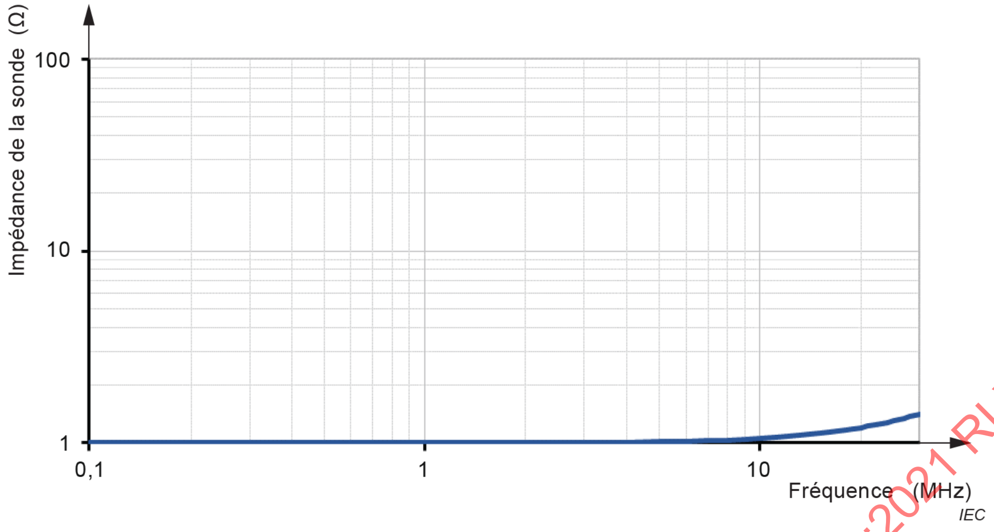


Figure A.6 – Exemple de caractéristique d'impédance d'entrée de la sonde de 1 Ω

Annexe B
(informative)

Classification des niveaux d’émission conduite

B.1 Remarque d’introduction

La présente Annexe B est destinée à fournir une méthode de classification des niveaux des émissions conduites des circuits intégrés par l’application des conditions d’essai décrites dans la présente spécification.

B.2 Généralités

La présente annexe n’est pas destinée à spécifier ou à impliquer des limites d’émissions conduites pour les CI. Cependant, par application soigneuse et accord entre le fabricant et l’utilisateur, il est possible d’établir une spécification de dispositif qui stipule l’EME conduite maximale admissible pour un circuit intégré particulier dans une application spécifique lorsque l’essai est réalisé conformément aux procédures du présent document.

Il convient aussi de noter que l’Annexe B n’est pas une spécification de produit et ne peut fonctionner comme telle. Néanmoins, en utilisant le concept décrit dans le présent document, et par une application prudente couplée à un accord entre le fabricant et l’utilisateur, il est possible de développer un document précisant le comportement EME pour un circuit intégré spécifique.

B.3 Définition des niveaux d’émission

Le schéma de la Figure B.1 définit les niveaux de classification des émissions conduites utilisés pour définir une enveloppe globale des émissions mesurées. Ce schéma peut être utilisé pour classer à la fois le courant RF mesuré avec la sonde de courant RF et la tension RF aux broches du CI, mesurée en utilisant le réseau d’adaptation d’impédance.

Le schéma suit la théorie d’une réponse à impulsions trapézoïdales et propose trois pentes différentes d’amplitudes d’émission avec une distance de 6 dB:

- 0 dB/décade [théorie: ligne d’amplitude constante jusqu’à la première fréquence de coude $1/(\pi\tau)$];
- −20 dB/décade [théorie: réduction d’amplitude jusqu’à la seconde fréquence de coude $1/(\pi\tau_r)$];
- −40 dB/décade [théorie: réduction d’amplitude aux fréquences > $1/(\pi\tau_r)$].

Les fréquences de coude dépendent des temps de montée/descente (τ_r), ainsi que de la durée (τ) d’impulsion.

Le schéma de niveau d’émission représenté à la Figure B.1 permet le choix de différentes pentes pour différentes fréquences pour mieux décrire l’EME conduite mesurée. L’EME peut être décrite avec une, deux ou trois pentes selon ce qui est exigé pour mieux correspondre aux données mesurées.

Différentes combinaisons sont possibles qui reflètent les exigences actuelles de l’application de manière bien plus précise (par exemple adaptées à la fréquence de commutation des accès du microcontrôleur).