NORME INTERNATIONALE

INTERNATIONAL STANDARD

CEI
IEC
60821

1991

AMENDEMENT 1
AMENDMENT 1

1999-01

Amendment 1

VMEbus – Microprocessor system bus for 1 byte to 4 byte data

Amendement 1

Bus VMEbus –
Bus système à microprocesseurs
pour données de 1 octet à 4 octets

International Electrotechnical Commission 3, rue de Varembé Geneva, Switzerland
Telefax: +41 22 919 0300 e-mail: inmail@iec.ch IEC web site http: //www.iec.ch

Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия

CODE PRIX
PRICE CODE J

Pour prix, voir catalogue en vigueur
For price, see current catalogue

FOREWORD

This amendment has been prepared by subcommittee 26: Microprocessor systems, of the Joint Technical Committee ISO/IEC JTC 1: Information technology.

The text of this amendment is based on the following documents:

Text	Report on voting
ISO/IEC JTC1/SC 26 N 237	ISO/IEC JTC1/SC 26 N 218

Full information the voting for the approval of this amendment can be found in the report on voting indicated in the above table.

_____

CHAPTER 2: IEC 60821 BUS DATA TRANSFER BUS

Page 67

2.2.4.5 WRITE*

Replace the first sentence of this subclause by the following:

WRITE* is a level significant signal line that is strobed by the falling edge of the first data strobe (DSA*) and is valid as long as any data strobe (DSA* or DSB*) is low.

Page 89

2.3.6 Basic data transfer capabilities

Replace Rule 2.65 by the following:

D08(O) SLAVES MUST NOT respond by driving DTACK* low during cycles that request access to byte locations BYTE(0), BYTE(2), BYTE(1-2), BYTE(2-3), BYTE(0-2), BYTE(1-3), or BYTE(0-3).

Insert, at the end of Suggestion 2.8, the following text:

4) When a D08(O) SLAVE is requested to do a BYTE(0) or BYTE(2) transfer.

Page 93

Table 2-10 – Mnemonics that specify basic data transfer capabilities

Replace in the third column the words "can accept" *and* "can monitor" *by* "must accept" *and* "must monitor".

2.3.7 Block transfer capabilities

Add, on page 95, at the end of Rule 2.12, the words "in the address space."

Replace, on page 97, at the end of the first sentence of Observation 2.87, "D08-D15" *by* "D00-D15".

Page 99

Table 2-11 – Mnemonic that specifies block transfer capabilities

Replace, in the third column, the words "Can accept" *and* "Can monitor" *by* "Must accept" *and* "Must monitor".

Page 101

Table 2-12 – Mnemonic that specifies read-modify-write capabilities

Replace, in the third column, the words "Can accept" *and* "Can monitor" *by* "Must accept" *and* "Must monitor".

Page 103

2.3.9 Unaligned transfer capabilities

Page 105

Table 2-13 – Transferring 32 bits of data using multiple byte transfer cycles

Replace, in row B, line 3, and line 6, "Group 1, BYTE(0)" *by* "GROUP 2, BYTE(0)".

Replace, in row D, line 6, "D00-D23" *by* "D00-D07".

Page 107

Table 2-14 – Transferring 16 bits of data using multiple byte transfer cycles

Replace, in row F, line 1, "D08-D15" *by* "D00-D07".

Replace, in row F, line 2, "D16-D23" *by* "D08-D15".

RULE 2.6

Replace, at the beginning of the sentence, "D08(0)" by "D08(O)"

Replace the text before table 2-15 and after RULE 2.6 by:

Table 2-15 lists how the unaligned transfer (UAT) mnemonic is used to describe MASTERS and SLAVES.

Table 2-15 – Mnemonic that specifies unaligned transfer capability

Replace table 2-15 by the following revised table:

The following mnemonic	When applied to a	Means that it
UAT	D32 MASTER D32 SLAVE	Can generate the following cycles: MUST accept the following cycles: Quad byte read cycles: BYTE(0-3) READ Quad byte write cycle: BYTE (0-3) WRITE Triple byte read cycles: BYTE(0-3) READ BYTE(1-3) READ Triple byte write cycles: BYTE(0-2) WRITE BYTE(1-3) WRITE Double byte read cycles: BYTE(1-2) READ Double byte write cycles: BYTE(1-2) WRITE

Page 109

Table 2-16 – Mnemonic that specifies ADDRESS-ONLY capability

Replace, in the first column, "AD0" *by* "ADO".

Page 133

Table 2-17 – Timing diagrams that define MASTER, SLAVE and LOCATION MONITOR operation

Replace, in the first row of the first column, "AD0" *by* "ADO".

Page 135

Table 2-18 – Definitions of mnemonics used in tables 2-19, 2-20 and 2-21

Replace, in the seventh row, "DRIVEN BY SLAVE" *by* "DRIVEN BY SLAVE?".

Page 139

Table 2-20 – Use of DS1*, DS0*, AO1 and LWORD* during the various cycles

Replace, in the first row, "AD0" *by* "ADO".

Page 141

Table 2-21 – Use of the data lines to transfer data

Replace, in the first row, "AD0" by "ADO".

CHAPTER 3: IEC 60821 BUS DATA TRANSFER BUS ARBITRATION

Page 213

3.3.1 ARBITER

Replace, on page 215, in the first sentence of the eighth paragraph, "BRO*" *by* "BR0*" *and* "BGOIN*" *by* "BG0IN*".

Page 221

3.3.2 REQUESTER

Replace, on page 225, RULE 3.14 by the following:

After having been granted the bus, the FAIR ARBITER MUST monitor its bus request line and it MUST NOT issue a new bus request until its bus request line has once been high.

CHAPTER 4: IEC 60821 BUS PRIORITY INTERRUPT BUS

Page 259

4.2.1 Interrupt request lines

Replace the title of this subclause by the following new title:

Interrupt request lines – IRQ1* – IRQ7*

4.2.2 Interrupt acknowledge line

Replace the title of this subclause by the following new title:

Interrupt acknowledge line – IACK*

Page 261

4.3 Priority Interrupt Bus modules – Basic description

Replace, in the first sentence of the first paragraph, "IACK*" *by* "IACK".

Replace, in the first sentence of the second paragraph, "IACK*" *by* "IACK".

Page 275

Table 4-2 – INTERRUPTERS: RULES and PERMISSIONS for driving and monitoring the dotted lines

Replace, in the second and in the last row, "MAY or MAY NOT" *by* "MAY".

Page 281

4.3.7 Interrupt release capabilities

Replace, on page 283, in the second line of Rule 4.5, and the second line of Rule 4.6, "before DSA* has fallen" *by* "before it detects a falling edge on DSA*".

Page 285

Figure 4-8

Replace figure 4-8 by the following new figure:

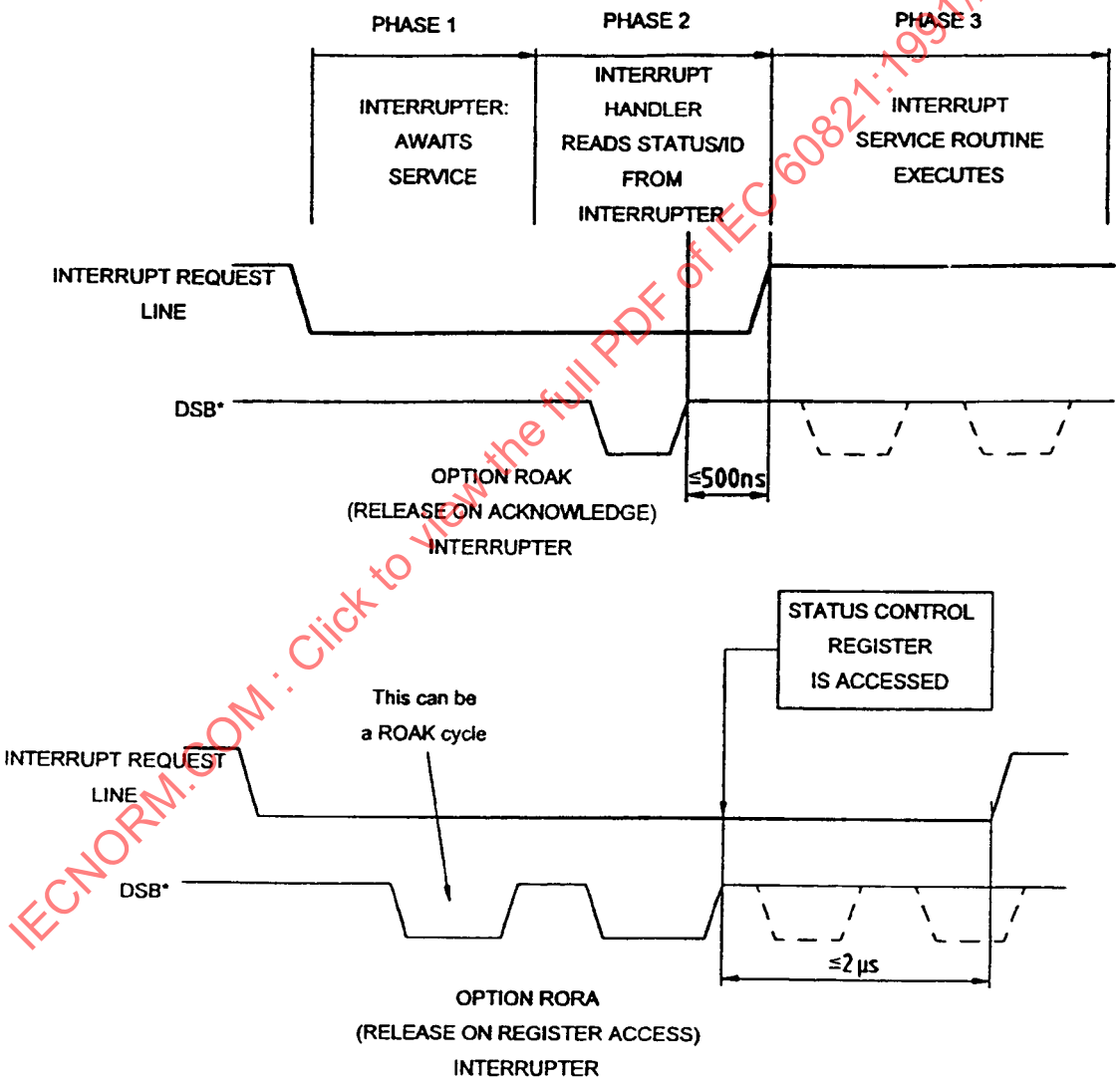

Figure 4-8 – Release of the interrupt request lines by ROAK and RORA INTERRUPTERS

CHAPTER 7: IEC 60821 BUS MECHANICAL SPECIFICATIONS

Page 415

7.2 IEC 60821 BUS boards

Replace RECOMMENDATION 7.1 by the following new RECOMMENDATION 7.1:

Make IEC 60821 BUS boards 1,6 mm ± 0,2 mm (0,063 in ± 0,008 in) thick.

Page 439

Figure 7-2

Replace RULE 7.32 by the following new RULE 7.32:

Boards MUST be 1,6 mm ± 0,2 mm (0,063 in ± 0,008 in) thick in the guide area.

Page 441

Figure 7-3

Replace RULE 7.33 by the following new RULE 7.33:

Boards MUST be 1,6 mm ± 0,2 mm (0,063 in ± 0,008 in) thick in the guide area.

Page 465

Figure 7-15

Replace, in PERMISSION 7.24, "J_1 or a J_2" *by* "J_1/J_2".

Page 481

Appendix A – Glossary of IEC 60821 bus terms

Add, under the title of this appendix, the term "normative".

Replace, in the sixth paragraph, the title "AD0" *by* "ADO".

Page 493

Appendix B – IEC 60821 bus connector/pin description

Add, under the title of this appendix, the term "normative".

Page 499

Appendix C – Use of the SERCLK and SERDAT* lines

Add, under the title of this appendix, the term "informative".

Page 503

Appendix D – Metastability and resynchronisation

Add, under the title of this appendix, the term "informative".

Replace, on page 527, figure D-5 by the following new figure:

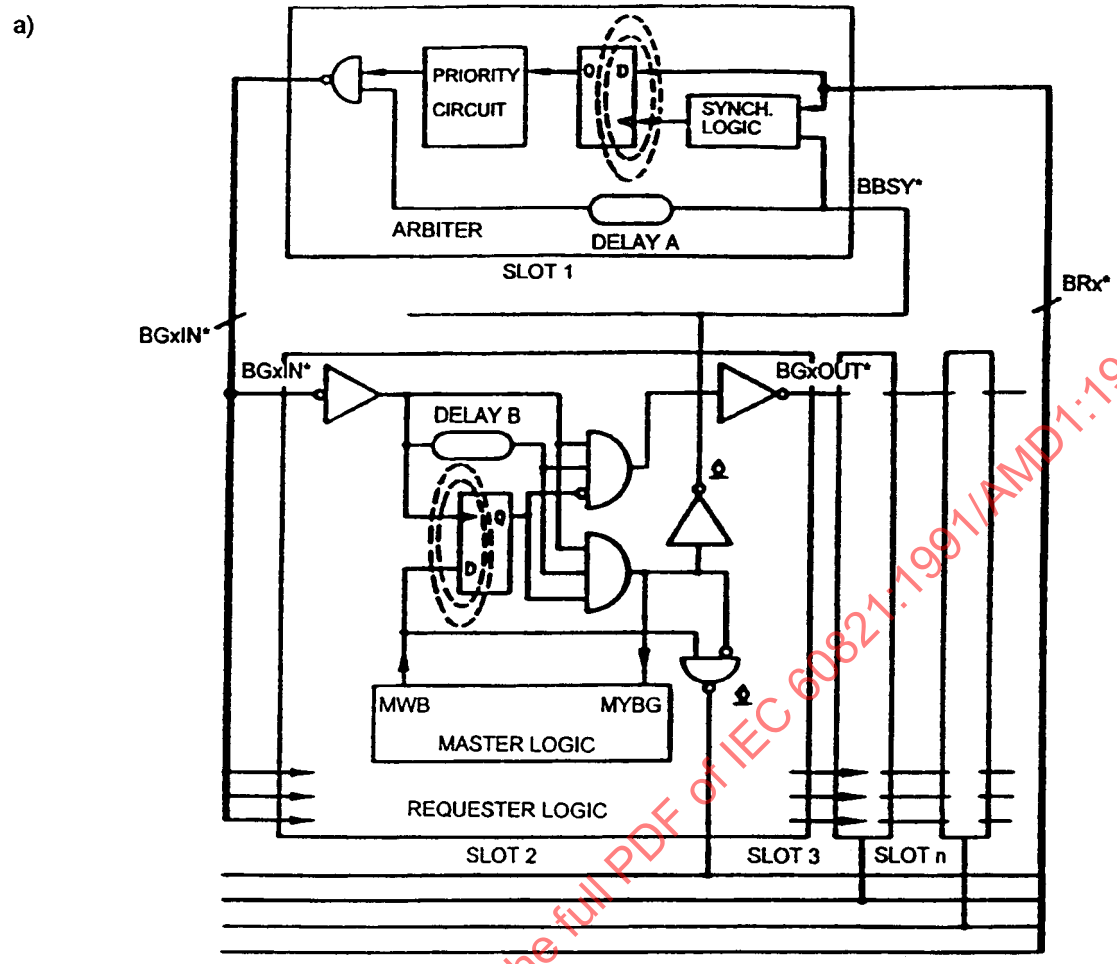

Figure D-5 – VMEbus arbitration structure; dashed circles indicate where critical input conditions can arise
a) simplified block diagram;
b) control signals, with evidence of the handshake loop (MASTER - REQUESTER - ARBITER - REQUESTER - MASTER)