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INTERNATIONAL STANDARD

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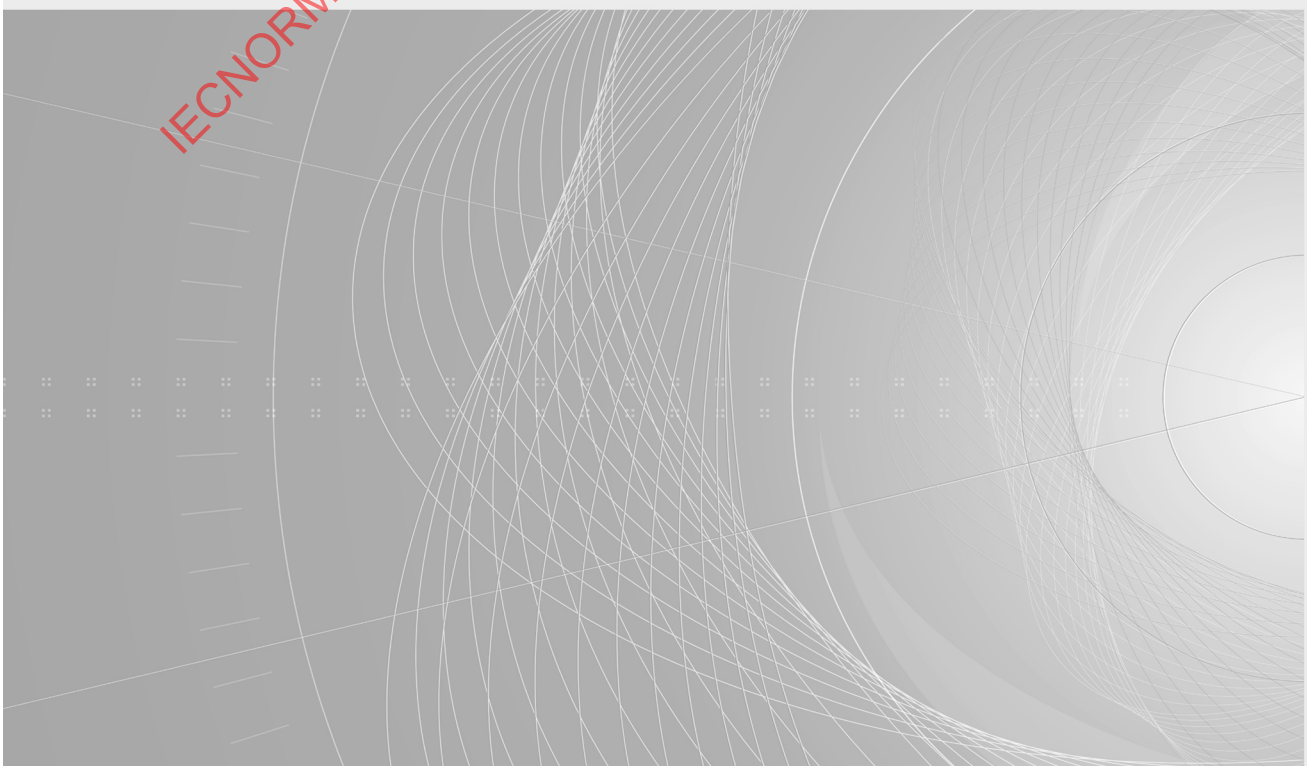
Semiconductor devices – Mechanical and climatic test methods – Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level



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CONTENTS

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

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International Standard IEC 60749-28 has been prepared by IEC technical committee 47: Semiconductor devices in collaboration with IEC technical committee 101: Electrostatics.

This standard is based on ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002 which resulted from the merging of JESD22-C101 and ANSI/ESD S5.3.1). It contains the essential elements from both standards. The co-operation of ANSI/ESDA/JEDEC is gratefully acknowledged.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
47/2362/FDIS	47/2379/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices –Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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INTRODUCTION

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a device and discharging through the device. The most common example is IEC 60749-26, the human body model (HBM). However, with the increasing use of automated device handling systems, another potentially destructive discharge mechanism, the charged device model (CDM), becomes increasingly important. In the CDM, a device itself becomes charged (e.g. by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object. A critical feature of the CDM is the metal-metal discharge, which results in a very rapid transfer of charge through an air breakdown arc. The CDM test method also simulates metal-metal discharges arising from other similar scenarios, such as the discharging of charged metal objects to devices at different potential.

Accurately quantifying and reproducing this fast metal-metal discharge event is very difficult, if not impossible, due to the limitations of the measuring equipment and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the device will vary considerably depending on a large number of factors, including package type and parasitics. The typical failure mechanism observed in MOS devices for the CDM model is dielectric damage, although other damage has been noted.

The CDM charge voltage sensitivity of a given device is package dependent. For example, the same integrated circuit (IC) in a small area package can be less susceptible to CDM damage at a given voltage compared to that same IC in a package of the same type with a larger area. It has been shown that CDM damage susceptibility correlates better to peak current levels than charge voltage.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

1 Scope

This part of IEC 60749 establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined field-induced charged device model (CDM) electrostatic discharge (ESD). All packaged semiconductor devices, thin film circuits, surface acoustic wave (SAW) devices, opto-electronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this document. To perform the tests, the devices are assembled into a package similar to that expected in the final application. This CDM document does not apply to socketed discharge model testers. This document describes the field-induced (FI) method. An alternative, the direct contact (DC) method, is described in Annex I.

The purpose of this document is to establish a test method that will replicate CDM failures and provide reliable, repeatable CDM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of CDM ESD sensitivity levels.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
CDM ESD
charged device model electrostatic discharge
electrostatic discharge (ESD) using the charged device model (CDM) to simulate the actual discharge event that occurs when a charged device is quickly discharged to another object at a lower electrostatic potential through a single pin or terminal

3.2
CDM ESD tester
charged device model electrostatic discharge tester
equipment that simulates the device level CDM ESD event using the non-socketed test method

Note 1 to entry: "Equipment" is referred to as "tester" in this document.

3.3
dielectric layer
thin insulator placed atop the field plate used to separate the device from the field plate

3.4
field plate
conductive plate used to elevate the potential of the device under test (DUT) by capacitive coupling

Note 1 to entry: See Figure 1.

3.5
ground plane
conductive plate used to complete the circuitry for grounding/discharging the DUT

Note 1 to entry: See Figure 1.

3.6
software voltage
user/operator-entered voltage that, when combined with the scale factor or offset, sets the actual field plate voltage on the system in order to achieve the waveform parameters

Note 1 to entry: Waveform parameters are defined in Table 1 or Table 2.

3.7
test condition
TC
tester plate voltage that meets the waveform parameter conditions

Note 1 to entry: The waveform parameter conditions are found in a particular column of Table 1 and Table 2.

4 Required equipment

4.1 CDM ESD tester

4.1.1 General

Figure 1 represents the hardware schematic for a CDM tester setup to conduct field-induced CDM ESD testing assuming the use of a resistive current probe. The DUT may be an actual device or it may be one of the two verification modules (metal discs) described in Annex A. The pogo pin shall be connected to the ground plane with a 1 Ω current path with a minimum bandwidth (BW) of 9 gigahertz (GHz). The 1 Ω pogo pin to ground connection of the resistive current sensor may be a parallel combination of a 1 Ω resistor between the pogo pin and the ground plane, and the 50 Ω impedance of the oscilloscope and its coaxial cable. In Figure 1, K1 is the switch between charging the field plate and grounding the field plate. The CDM ESD testers used within the context of this document shall meet the waveform characteristics specified in Figure 2, and Table 1 and Table 2, without additional passive or active devices, such as ferrites, in the probe's assembly.

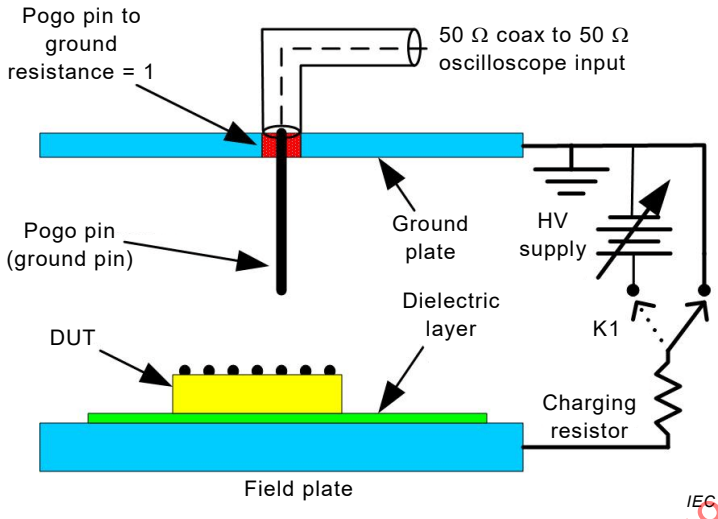


Figure 1 – Simplified CDM tester hardware schematic

When constructing the test equipment, the parasitics in the charge and discharge paths should be minimized since the resistance inductance-capacitance (RLC) parasitics in the equipment greatly influence the test results.

For existing equipment, it is recommended to contact qualified service personnel to determine compliance to this document upon removal of ferrite components.

4.1.2 Current-sensing element

A current-sensing element shall be incorporated into the ground plane. The resistance of this element shall have a value of (1,0 ± 10 %) Ω. A resistor, as specified in 4.1.1, shall be used as the current-sensing element. The value of resistance (including the 50 Ω cable/oscilloscope termination) shall be measured using an ohmmeter as described in 4.5. The resistance value shall be used to calculate the first peak current.

The current-sensing element shall have a minimum frequency response of 9 GHz (specified by a maximum roll-off of 3 dB at 9 GHz).

4.1.3 Ground plane

The probe assembly shall contain a square ground plane with the probe pin centred within it as shown in Figure 1. The dimensions of the ground plane shall be 63,5 mm × 63,5 mm ± 6,35 mm (2,5 inches × 2,5 inches ± 0,25 inches).

4.1.4 Field plate/field plate dielectric layer

The field plate shall have a surface flatness to vary no more than ± 0,127 mm (0,005 inches). The field plate dielectric layer should be made with an FR4 or similar epoxy-glass material. For FR4, the thickness and thickness tolerance of this dielectric layer should be 0,381 mm ± 0,0254 mm (0,015 inches ± 0,001 inches) in order to result in a capacitance measurement (as specified in normative Annex B) in the range specified in Table A.1.

If a different material is used, the material thickness is chosen to result in a capacitance measurement in the range specified in Table A.1.

4.1.5 Charging resistor

The charging resistor shown in Figure 1 shall nominally be 100 MΩ or greater.

Resistor values higher than 100 MΩ may be used, but this may not allow very large devices (refer to 5.9 and Annex H) to charge fully before being discharged by the probe assembly. This effect can be overcome by adding a delay between discharges in the CDM tester programming software. If using a resistor greater than 100 MΩ, it is recommended that the tester or the device itself be characterized to determine if a delay is needed for discharging large devices. A procedure for this large device delay characterization is given in Annex H.

4.2 Waveform measurement equipment

4.2.1 General

The CDM waveform measurement equipment shall consist of the following components.

4.2.2 Cable assemblies

Cable assemblies with combined internal tester cable and external cable total loss of no more than 2 dB at frequencies up to 9 GHz and a nominal 50 Ω impedance.

4.2.3 Equipment for high-bandwidth waveform measurement

4.2.3.1 High-bandwidth oscilloscope

An oscilloscope or transient digitizer with a minimum real-time (single shot) 3 dB BW of at least 6 GHz and ≥ 20 gigasample/s sampling rate with a nominal 50 Ω input impedance.

4.2.3.2 Attenuator

A 20 dB attenuator with a precision of ±0,5 dB, at least 12 GHz BW, and an impedance of 50 Ω ± 5,0 Ω.

4.2.4 Equipment for 1,0 GHz waveform measurement

4.2.4.1 1 GHz oscilloscope

An oscilloscope or transient digitizer with a real-time (single shot) 3 dB BW of 1 GHz with a nominal 50 Ω input impedance. The sampling rate shall be ≥ 5 gigasample/s.

NOTE The user has the option of using a higher BW oscilloscope and using a hardware or software filter to produce a bandwidth and sampling rate equivalent to that specified in 4.2.4.1.

4.2.4.2 Attenuator

A 20 dB attenuator with a precision of ± 0,5 dB, at least 4 GHz BW, and an impedance of 50 Ω ± 5 Ω.

4.3 Verification modules (metal discs)

The large verification module shall have a capacitance of (55 ± 5 %) pF and the small verification module shall have a capacitance of (6,8 ± 5 %) pF. Refer to normative Annex A for information on the verification module physical dimensions and normative Annex B for information on the capacitance measurement procedure.

4.4 Capacitance meter

Capacitance meter with a resolution of 0,2 pF, a measurement accuracy of 3 %, and a measurement frequency of 1,0 MHz as described in normative Annex B.

4.5 Ohmmeter

The ohmmeter used to measure the resistance of the resistive probe shall be capable of measuring to an accuracy of 0,01 Ω. Use of Kelvin 4-wire connections is recommended.

5 Periodic tester qualification, waveform records, and waveform verification requirements

5.1 Overview of required CDM tester evaluations

The CDM tester shall be qualified, re-qualified, and periodically verified as described in 5.5 and 5.6.

NOTE 1 Dielectric layers, ground planes (ground plates), the coaxial discharging resistor (probe), the distance between the ground plane and the field plate, the verification modules and the discharge contacts (e.g., pogo pins) are key elements of the tester construction. Any change to these elements requires a waveform verification.

NOTE 2 Changes in the shape of the discharge pulse, even though they can still be within specification, can indicate degradation of the discharge path.

5.2 Waveform capture hardware

Waveform capture requires the following instrumentation and tester set voltage procedure:

- an oscilloscope – as specified in 4.2;
- an attenuator and cable assembly as defined in 4.2;
- verification modules (as described in 4.3) – with the dimensions and attributes listed in normative Annex A and the method of measurement listed in normative Annex B.

5.3 Waveform capture setup

The waveform capture setup shall be carried out as follows.

a) Clean the verification modules. Avoid skin contact with the modules prior to, and during testing. A recommended procedure is described in normative Annex A.

b) Using an alcohol wipe, clean the discharge probe and the field charge plate on which the device is placed to remove any surface contamination that could result in charge loss. Ensure the pogo pin is free of particulates.

c) Attach the appropriate 20 dB attenuator as described in 4.2.3.2 to the oscilloscope. Attach one end of the external cable assembly, as described in 4.2.2, to the attenuator and the other end to the CDM tester. Verify all connections in the measurement chain are tight.

See informative Annex E for an example of oscilloscope settings and captured waveforms.

5.4 Waveform capture procedure

The waveform capture procedure shall be carried out as follows.

a) Place the verification module to be used on the field plate dielectric, ensuring intimate contact between the field plate dielectric and verification module.

b) Set the potential of the field plate to the needed voltage for the test condition being run.

c) Align the ground pin to approximately the centre of the verification module.

d) Either the single discharge or dual discharge method as described in Clause F.2 or Clause F.3 respectively can be used, but the discharge method chosen should be consistent with how products will be tested. When using the dual discharge method, waveforms for positive and negative pulses require a change in the oscilloscope trigger conditions to capture only positive or negative pulses.

e) Discharge the verification module at least ten times at the polarity being verified.

f) Observe at least ten successive waveforms during the set of discharges above and record the average waveform parameters for I_p, T_r, full width at half maximum (FWHM), and Ip2 for this group of waveforms as shown in Figure 2.

g) If the waveform characteristics do not meet the requirements as defined in either Table 1 or Table 2 for the target test condition (see 5.6 and 5.7 for the appropriate table and test conditions to use), re-clean the verification modules and ground pin, check that all connections are tight, make adjustments in the field plate voltage and repeat steps a) to g).

If this still does not work, check the system vacuum or look at replacement of the ground pin. Consult the tester manufacturer for more information.

Repeat the procedure for the opposite polarity.

5.5 CDM tester qualification/requalification procedure

5.5.1 CDM tester qualification/requalification procedure

The intent of the qualification/requalification procedure is to determine the field plate voltage needed for each test condition setting (125 – 1 000) in Table 3 to produce peak current in the ranges corresponding to Table 1 and Table 2, and therefore corresponding to the classification levels as specified in Table 3.

Two alternative procedures for how to qualify and routinely check the CDM test system are introduced in Annex G. These procedures are based on generally available CDM test systems and offer two methods for adjusting the field plate voltage to meet the waveform parameters of Table 1 or Table 2.

CDM test system manufacturers, or test system operators, may develop alternate qualification procedures from the two procedures in Annex G, as long as they result in waveforms that meet the requirements of Table 1 or Table 2 for the various test conditions.

It is recommended that settings determined from this qualification procedure be recorded for a particular test system, oscilloscope BW and polarity. This allows for detection of drift over time on the system, which may indicate a larger issue with the system. See Clause G.3 for examples.

Perform the setup and waveform capture steps as described in 5.3 and 5.5 under test conditions 125 – 1 000 in Table 2 for both positive and negative polarities using both small and large verification modules, and measuring with the high bandwidth oscilloscope as specified in 4.2.3.1. Refer to Annex G for example flowcharts of the procedures.

If local site test voltage ranges will always be narrower than the range above (for example test conditions 125 – 500), it is permissible to perform the qualification within that narrower range.

5.5.2 Conditions requiring CDM tester qualification/requalification

CDM tester qualification and requalification as described in 5.5 is required in the following situations:

- acceptance testing when the CDM tester is delivered; usually performed by the manufacturer during installation;
- periodic requalification in accordance with the manufacturer's recommendations; the maximum time between requalification tests is one year;
- after service or repair that could affect the waveform.

5.5.3 1 GHz oscilloscope correlation with high bandwidth oscilloscope

During first acceptance testing, the tester manufacturer shall use a high bandwidth oscilloscope as specified in 4.2.3.1 for initial waveform capture. If the test site only has a 1 GHz oscilloscope as specified in 4.2.4.1, the tester manufacturer and end user shall confirm using appropriate bandwidth filtering techniques and comparison with the oscilloscope from the tester manufacturer that the user's oscilloscope measures tester waveforms as defined in Table 1 for quarterly and routine waveform acceptance.

NOTE The Bessel-Thomson software filter option on many oscilloscopes is a recommended high-bandwidth waveform filter as it aligns well with actual 1 GHz oscilloscope data.

Oscilloscope correlation verification shall be repeated if the test site changes 1 GHz oscilloscopes.

5.6 CDM tester quarterly and routine waveform verification procedure

5.6.1 Quarterly waveform verification procedure

Perform the setup and waveform capture steps as described in 5.3 and 5.5 under test conditions 125 – 1 000 in Table 1 using the 1 GHz oscilloscope as specified in 4.2.4.1 or Table 2 using the high-bandwidth oscilloscope as specified in 4.2.3.1. Both verification modules shall be checked at positive and negative polarities. Recommendation is to use the high bandwidth oscilloscope if the option exists. Refer to Annex G for example flowcharts of the procedures.

If local site test voltage ranges will always be narrower than the range above (for example test conditions 125 – 500), it is permissible to perform the qualification within that narrower range.

Tester waveform verification shall be performed at least once per quarter.

5.6.2 Routine waveform verification procedure

5.6.2.1 General

Perform the setup and waveform capture steps as described in 5.3 and 5.5 under test condition 500 in Table 1 (1 GHz oscilloscope) or Table 2 (high-bandwidth oscilloscope) for both positive and negative polarities using the verification module that most closely corresponds to the size package that will be tested. Refer to Annex G for example flowcharts of the procedures.

5.6.2.2 Routine verification frequency

Initially, upon tester qualification or requalification, routine waveform verification should be completed at least once per shift. If CDM stress testing is performed on consecutive shifts, waveform checks at the end of one shift may also serve as the initial check for the following shift.

Longer periods between routine waveform checks may be used if no changes in waveforms are observed for several consecutive checks. The test frequency and method chosen shall be documented. If, at any time, the waveforms no longer meet the specified limits, all ESD stress test data collected subsequent to the previous satisfactory waveform check shall be marked invalid and shall not be used for classification.

5.7 Waveform characteristics

The waveforms shall appear as shown in Figure 2 for both the positive polarity and its inverse for the negative polarity. The average waveform parameters (including I_p) as gathered by the method of 5.4 shall meet the specifications in Table 1 for a 1 GHz oscilloscope and Table 2

for a high-bandwidth oscilloscope. If a high-bandwidth oscilloscope is used for qualification, quarterly and routine waveform verifications, the 1 GHz requirements need not be considered.

Table 1 – CDM waveform characteristics for a 1 GHz bandwidth oscilloscope

1 GHz BW oscilloscope		Test condition									
		TC 125		TC 250		TC 500		TC 750		TC 1000	
Verification module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak current (A)	I_p	1,0 - 1,6	1,9 – 3,2	2,1 – 3,1	4,2 – 6,3	4,4 - 5,9	9,1 - 12,3	6,6 - 8,9	13,7 - 18,5	8,8 - 11,9	18,3 - 24,7
Rise time (ps)	T_r	< 350	< 450	< 350	< 450	< 350	< 450	< 350	< 450	< 350	< 450
Full width at half maximum (ps)	FWHM	325 - 725	500 - 1000	325 - 725	500 - 1000	325 - 725	500 - 1000	325 - 725	500 - 1000	325 - 725	500 - 1000
Undershoot (A, max. 2nd peak)	I_{p2}	<70% I_p	<50% I_p	<70% I_p	<50% I_p	<70% I_p	<50% I_p	<70% I_p	<50% I_p	<70% I_p	<50% I_p

Table 2 – CDM waveform characteristics for a high-bandwidth (≥ 6 GHz) oscilloscope

≥ 6 GHz BW oscilloscope		Test condition									
		TC 125		TC 250		TC 500		TC 750		TC 1000	
Verification Module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak Current (A)	I_p	1,4-2,3	2,3-3,8	2,9-4,3	4,8-7,3	6,1-8,3	10,3-13,9	9,2-12,4	15,5-20,9	12,2-16,5	20,6-27,9
Rise time (ps)	T_r	< 250	< 350	< 250	< 350	< 250	< 350	< 250	< 350	< 250	< 350
Full width at half maximum (ps)	FWHM	250-600	450-900	250-600	450-900	250-600	450-900	250-600	450-900	250-600	450-900
Undershoot (A, max. 2nd peak)	I_{p2}	<70% I_p	<50% I_p	<70% I_p	<50% I_p	<70% I_p	<50% I_p	<70% I_p	<50% I_p	<70% I_p	<50% I_p

NOTE The voltages of the test conditions 125 to 1 000 producing the specified peak current ranges are adjusted from previous classification test voltages of 125 V, 250 V, 500 V, 750 V and 1 000 V, respectively. Informative Annex C describes this relationship between such voltages and ferrite-free tester set voltages. Tester adjusted field plate voltages to achieve these current ranges for the ferrite-free tester platform in this document can vary somewhat between testers. Informative Annex G describes two voltage adjustment methods.

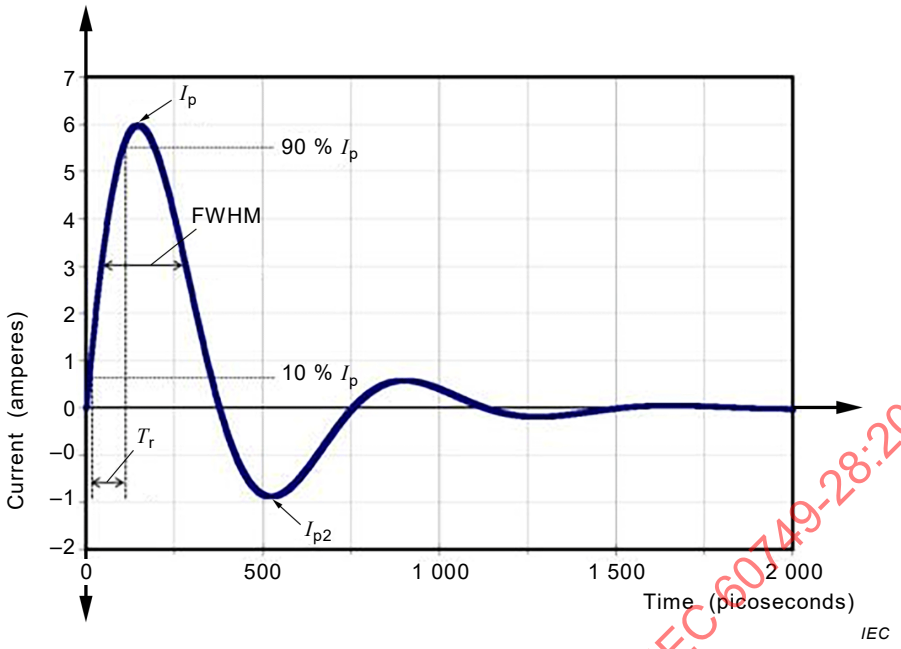


Figure 2 – CDM characteristic waveform and parameters

5.8 Documentation

Retain the waveform records for tester qualification according to internal company policy. For tester requalification, quarterly waveform verification and routine waveform verification, keep the records until the next set of waveforms are collected, or according to internal company policy.

5.9 Procedure for evaluating full CDM tester charging of a device

5.9.1 As defined in 4.1.5, the charging resistor should nominally be 100 MΩ or greater. If the resistor is too large, an added charging delay may be necessary to fully charge the device. To determine if an added delay is needed, follow the procedure in 5.9.2.

5.9.2 Using the large verification module, follow the procedure below.

a) Set the field plate voltage at +250 V (any voltage can be used as the objective is to monitor I_p).

b) With the pre- and post-charge delay both set to 0 ms, collect 10 waveforms and record the I_p from each. Calculate the average I_p of the waveforms.

c) With the pre-charge delay set to 500 ms (and post-charge delay remaining at 0 ms), collect ten waveforms, record the I_p from each. Calculate their average I_p of the waveforms.

d) Compare the average I_p value from the 0 ms charge delay and the 500 ms charge delay. If the average I_p is the same for both measurements, then a device of the same or lower capacitance as the large verification module are receiving a full charge. If the average I_p with 0 ms charge delay and 500 ms charge delay do not match, refer to the informative Annex H for a procedure to determine the appropriate default charge delay to add to the system.

e) Even if the two average I_p values above match, very large packaged devices (larger capacitance than the large verification module) may still require a delay in order to receive a full charge. Since device package technologies vary widely, there are no exact dimensions for how a particular package I_p may compare to the large verification module I_p for the evaluation described above.

f) To determine if a very large packaged device may still require a charge delay, steps a) to d) above can be repeated using the ground pin of a device. If the average I_p with 0 ms charge delay and 500 ms charge delay do not match, refer to the informative Annex H for a procedure to determine the appropriate charge delay.

In addition, where CDM testers have moving parts, care should be taken by personnel to avoid contact with these moving parts during operation.

6 CDM ESD testing requirements and procedures

6.1 Device handling

Devices used for CDM stressing shall not have been used for any prior stress tests.

ESD damage prevention procedures shall be used before, during, and after CDM and post parametric testing.

6.2 Test requirements

6.2.1 Test temperature and humidity

The test shall be carried out at room temperature. Humidity at the test head should not exceed 30 % RH. Heating or cooling the device during CDM testing is not intended.

The tester should be placed in an environment where the temperature is at room temperature.

NOTE Waveform repeatability is strongly dependent on moisture content of the air and having a low relative humidity will result in a more stable waveform.

6.2.2 Device test

6.2.2.1 Pre-stress testing

Prior to ESD stressing, complete static and dynamic testing shall be performed on all submitted devices. Parametric and functional results shall be within the limits specified in the datasheet parameters.

6.2.2.2 Failure criteria

Following ESD stressing, complete static and dynamic testing shall be performed on all stressed devices. A device is considered to have failed if parametric and functional test results are not within the limits specified in the datasheet parameters. A failure may be discounted if proven by failure analysis that it is not CDM–ESD related.

NOTE 1 A change in static leakage (e.g., pin leakage, standby current) is not an adequate criterion to determine pass/fail. It can serve as an indicator for the onset of damage.

NOTE 2 If testing is to be done at multiple temperatures, perform the test first at the lowest temperature, followed by increasing the temperature in sequence (e.g. −40 °C, +25 °C, +85 °C).

6.3 Test procedures

The test procedures are as follows.

a) Unless otherwise specified, obtain a minimum of three samples that have been verified to meet their data specifications.

b) CDM testing should begin at the lowest level in Table 3, but may begin at any level. However, if the initial voltage level is higher than the lowest level in Table 3 and the device fails at the initial voltage, testing shall be restarted with three fresh devices at the next lower level.

c) For each device, apply at least one positive and one negative discharge to each pin. Allow enough time (as specified in 5.9) between discharges for the device to reach the full test voltage level. Stresses may be partitioned by polarity, using a sample size of at least three units per polarity. Pins may also be partitioned into one or more sets of samples, provided that each pin of the device is a member of at least one set. Each set shall have a minimum of three units.

For the field-induced charging method, there are two possible procedures for charging and discharging the device: single and dual. Both procedures produce equivalent results. These procedures are described in the informative Annex F.

6.4 CDM test recording / reporting guidelines

The CDM testing procedure for a particular product shall be recorded and stored per each company's data retention procedure. Product CDM test results (including package information) shall be reported and be made available in the product reliability report. Information regarding tester waveform parameters should be available upon request; refer to Clause G.3 for more information on waveform parameter recording.

7 CDM classification criteria

ESD sensitive (ESDS) devices are classified according to the test procedure described in this document. CDM test results are specific to the particular package type used. The device classification is the highest ESD stress voltage level (both positive and negative polarities) at which a sample of at least three devices has passed full static and dynamic testing as per data sheet parameters following ESD testing. The CDM ESDS device classification levels are presented in Table 3.

Table 3 – CDM ESDS device classification levels

Classification level [a]	Classification test condition (in volts) [b]
C0a	< 125
C0b	125 to < 250
C1	250 to < 500
C2a	500 to < 750
C2b	750 to < 1000
C3	≥ 1000 [c]

[a] Use the "C" prefix to indicate a CDM classification level.

[b] The Classification Test Condition is not equivalent to the actual set voltage of the tester. Please see 5.6.1 and Annex G for further details.

[c] For test conditions above 1 000 V, depending on geometry of the device package, corona effects can limit the actual pre-discharge voltage and discharge current.

Annex A
(normative)

Verification module (metal disc) specifications and cleaning guidelines for verification modules and testers

A.1 Tester verification modules and field plate dielectric

The verification modules (metal discs) shall be made of brass, plated with nickel or gold/nickel, and may optionally have a gold flash coating over the nickel. They shall be manufactured to the dimensions specified in Table A.1 and shall be verified once before the initial use by either the manufacturer or user.

Caution shall be exercised during the manufacture of the discs so that they are free from burrs. If the perimeter of the disc has burrs, arcing may occur which may alter the results.

The field plate dielectric is chosen (see 4.1.4) to result in a capacitance measurement in the range specified in Table A.1.

Table A.1 – Specification for CDM tester verification modules (metal discs)

Disk	Small	Large
Diameter mm (inches)	8,89 ± 0,127 (0,350 ± 0,005)	25,4 ± 0,127 (1,000 ± 0,005)
Thickness mm (inches)	1,27 ± 0,05 (0,05 ± 0,002)	1,27 ± 0,05 (0,050 ± 0,002)
Surface flatness variation mm (inches)	≦ 0,127 (0,005)	≤ 0,127 (0,005)
Capacitance at 1 MHz (pF)	6,8 ± 5%	55 ± 5%

A.2 Care of verification modules

To avoid charge loss in verification modules during charged device model (CDM) evaluation, the verification modules should be cleaned using isopropanol (isopropyl alcohol, IPA) swabs for about 20 s as approved by the local safety organization, and dried in a moderate air stream to prevent charge leakage during test operation. Verification modules should be handled so as to maintain cleanliness.

The capacitance of the small and large verification modules (metal discs) shall be measured according to the procedure in Annex B, and shall conform to the values specified in Table A.1.

The tester should be cleaned periodically with isopropanol to remove any surface contamination that could result in charge loss. Particular attention should be paid to the discharge probe and field plate dielectric on which the device is placed.

Cleaning with isopropyl alcohol swabs can leave the surface moist for some period of time after the cleaning. The moisture can provide an unintended leakage path if present during the test. It is important to dry all surfaces after cleaning either by allowing sufficient time for the surfaces to dry or using forced air flow to evaporate the moisture.

Annex B
(normative)

Capacitance measurement of verification modules (metal discs) sitting on a tester field plate dielectric

a) The capacitance of the verification modules shall be measured in-situ (inside the CDM simulator), but can also be measured outside of the CDM simulator as guidance.

b) The small verification module is placed on the dielectric layer which is in direct contact with the surface of the grounded metallic field plate. Ensure there is no air space between the module and the dielectric layer, and also no air space between the dielectric layer and the metallic field plate.

It is recommended that vacuum be used to ensure the verification module is held in place against the field plate dielectric.

c) Ensure the capacitance meter is “zeroed out” prior to measurement.

d) Connect the two leads from the capacitance meter (CP) as follows. One metallic lead/cable from the CP is connected to an exposed point on the field plate. The second metallic lead/cable from the CP is connected to the top of the verification module (in the centre). Measure the capacitance of the module to the grounded field plate. The capacitance value of the verification module shall be within the value specified in Table A.1.

e) Repeat steps a) to d) using the large verification module on the dielectric.

NOTE Placement of the CP meter leads can cause changes in the measured capacitance. One recommended technique for each verification module is to take a first measurement as outlined in item d) and then take a second measurement with the verification module lead/cable just above, but not touching, the verification module. The second reading is subtracted from the first to result in the true measured value.

It is recommended to use a meter with “guarded leads”.

Annex C
(informative)

CDM test hardware and metrology improvements

The goal of this document is to reduce duplication of effort and confusion by developing a single agreed standard, correcting deficiencies in previous CDM standards whilst maintaining similar stress levels as those previous standards. This required significant hardware and metrology changes to arrive at an improved joint standard. This informative annex describes the motivations for these updates.

The major changes in this test method are listed below.

- Some details of the required waveforms have been modified to better match the high-frequency behaviour of CDM events.
- The test method now requires that the test head not include ferrites or other circuits to modify the high-frequency behaviour of the CDM pulse.
- The test method now requires that tester qualification and requalification be performed with a 6 GHz or faster oscilloscope, and recommends the use of 6 GHz or faster oscilloscopes for quarterly and regular tester verification if a fast oscilloscope is available.
- The tester qualification and verification procedures have been modified to give more flexibility in the field plate voltage settings to arrive at the required peak currents.
- The specification of test levels by voltage has been replaced by a series of test conditions which are related to the previous voltage levels.

When the original CDM test method was developed in the late 1980s, single-shot oscilloscopes with 1 GHz and higher bandwidths were expensive, not readily available and less capable than those available today. The result was that the original waveforms used to develop previous standards had a wider half-width than was characteristic of the actual CDM event. As measurement capability improved and the high frequency behaviour of test heads was improved, tester manufacturers found the peak width at half-height was narrower than allowed previously. In order to meet the peak width at half-height, ferrite beads were often added to the test head to bring the current waveforms into compliance. When oscilloscopes in the 4 GHz to 8 GHz range become readily available, it was found that the ferrite beads, which simply broadened the peak width when measured with a 1 GHz oscilloscope, created undesirable high-frequency harmonics with undesirable consequences. A primary goal in the development of this document was to remove the ferrite beads from the CDM test heads and to modify the waveform requirements to allow this change.

The 1 GHz oscilloscope specified previously is only marginally fast enough to capture CDM events and significantly reduces the measured peak current of the captured waveforms, especially for the small verification module and small integrated circuits. Accurate peak current measurements require the use of a measurement chain with 6 GHz or higher bandwidth, and the new joint standard reflects this requirement for CDM tester qualification. A 1 GHz oscilloscope was considered adequate for routine waveform verification, and that option is still available in the new standard, although the higher bandwidth oscilloscope is recommended if it is available.

The increased flexibility between the required peak current values and the field plate voltage to produce the peak current has been implemented for two reasons: to better match current practice, and to achieve similar stress levels as the legacy standards.

Previous standards specified the CDM tester geometry, as well as the required waveforms at specified field plate voltages. CDM tester manufacturers quickly found that it was often impossible to obtain the required peak current values with the required geometry and the specified field plate voltage. The manufacturers introduced adjustments to the field plate voltage so that the required waveforms were obtained when the specified voltage was

selected in the CDM tester software. This adjustment was reasonable since it is known that it is peak current, not field plate voltage, which damages integrated circuits. The result was that when an integrated circuit passed 500 V, the field plate voltage was often considerably different than 500 V, but the intended current pulse was in fact applied to the device under test.

The removal of the ferrite beads, and the extra impedance which the beads produced, has resulted in higher peak currents than were present in legacy test methods for the same field plate voltage and tester geometry. This creates a second reason to give more flexibility in the setting of the field plate voltage to obtain the required peak currents. Since CDM failure is a result of the peak current during the CDM event, it is therefore more important that different CDM testers create the same peak current for specified test conditions rather than that the field plate voltages are the same. For this reason, the test voltages specified in the earlier standard CDM documents have been replaced by a series of test conditions producing peak currents similar to those at the specified voltages in recent previous standards.

Annex D
(informative)

CDM tester electrical schematic

Figure D.1 represents an electrical model of a CDM tester setup. CDUT is the capacitance between the DUT and the field plate, CDG is the capacitance between the DUT and the ground plane, and CFG is the capacitance between the field plate and the ground plane. The 1 Ω resistance between the pogo pin and the ground plane may be the parallel combination of the resistive probe and the coaxial cable/oscilloscope impedance as described above. The resistance of the spark which forms between the pogo pin and the DUT is assumed to be a variable resistance. The inductance of the pogo pin and spark are lumped together as a single inductor.

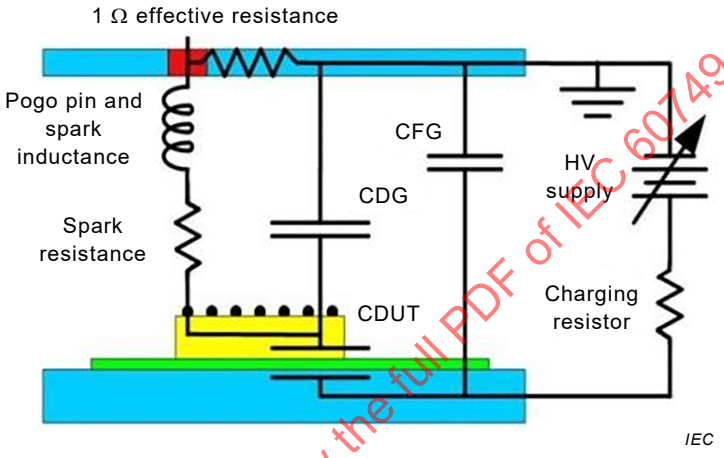


Figure D.1 – Simplified CDM tester electrical schematic

Annex E
(informative)

Sample oscilloscope setup and waveform

E.1 General

The following setup examples are based on measurements of a TC 500 waveform using a 1 GHz and 8 GHz oscilloscope. Other oscilloscopes will have different settings, but this annex should provide basic guidelines that can be used on most oscilloscopes.

E.2 Settings for the 1 GHz bandwidth oscilloscope

Vertical	200 mV/division (small verification module) or 200 mV/division (large verification module)
Timebase	400 ps/division
Trigger	300 mV small verification module or 400 mV large verification module
Impedance	50 Ω

These settings are for an oscilloscope for which the attenuation correction could not be made.

E.3 Settings for the high-bandwidth oscilloscope

Vertical	2 V/division (small verification module) or 2 V/division (large verification module)
Timebase	400 ps/division
Trigger	3 V small verification module or 4 V large verification module
Impedance	50 Ω

These settings are for an oscilloscope for which the attenuation correction was made in the oscilloscope software.

E.4 Setup

Attach the 20 dB attenuator to the oscilloscope. Attach the cable to the end of the attenuator and to the voltage output of the CDM tester.

NOTE The 20 dB attenuator is a 10× attenuator. If the oscilloscope does not automatically compensate for this, the measurements need to be multiplied by 10 to get the correct reading (e.g. from small coin below 532 mV = 5,32 A peak current).

E.5 Sample waveforms from a 1 GHz oscilloscope

Sample waveforms from a 1 GHz oscilloscope are illustrated in Figure E.1 and Figure E.2.

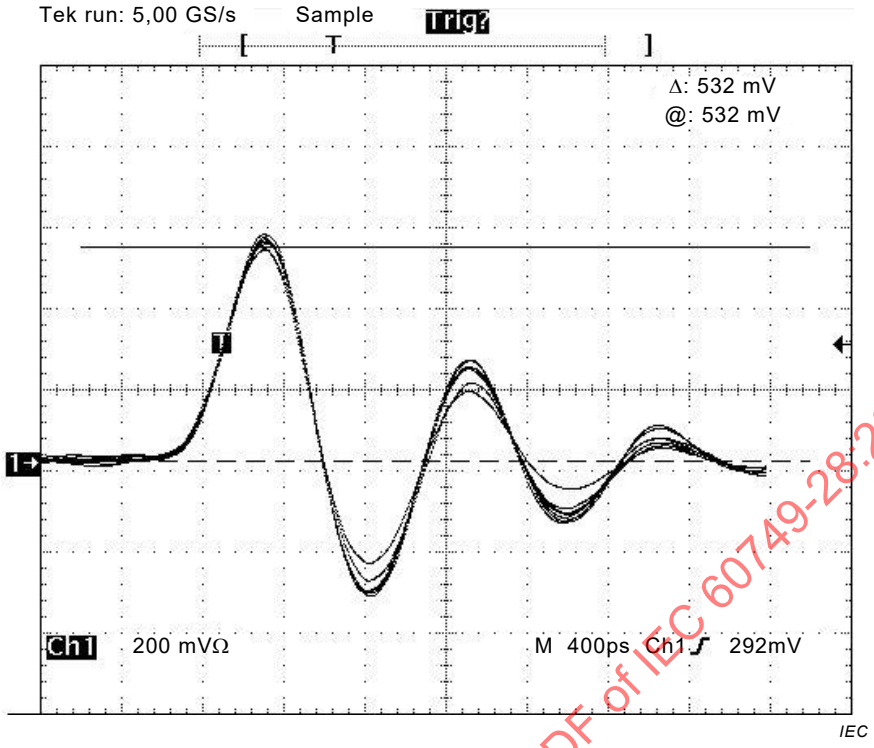


Figure E.1 – 1 GHz TC 500, small verification module

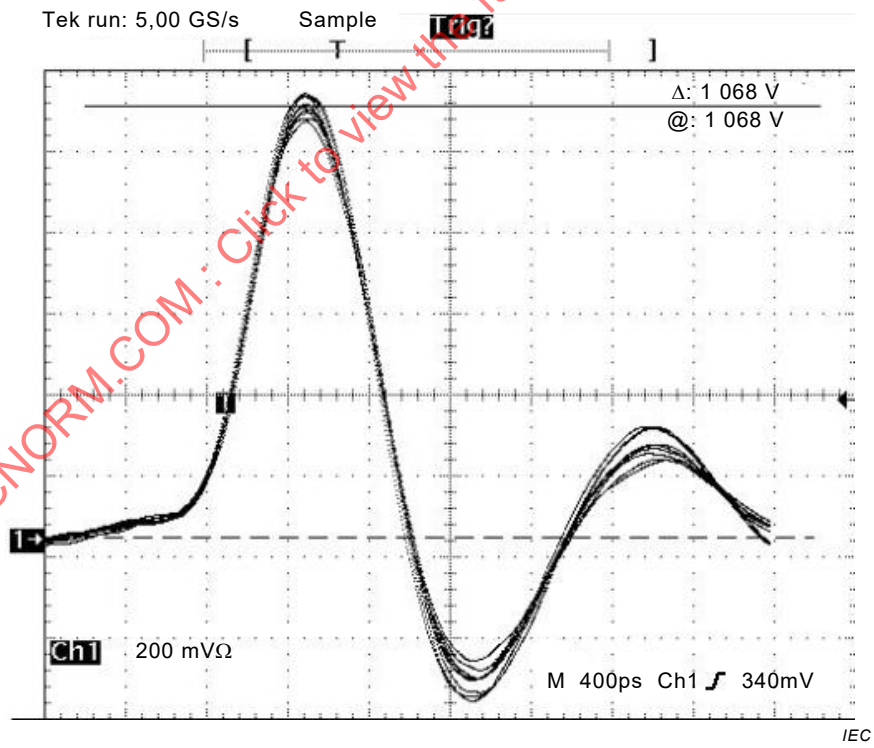


Figure E.2 – 1 GHz TC 500, large verification module

E.6 Sample waveforms from an 8 GHz oscilloscope

Sample waveforms from an 8 GHz oscilloscope are illustrated in Figure E.3 and Figure E.4.

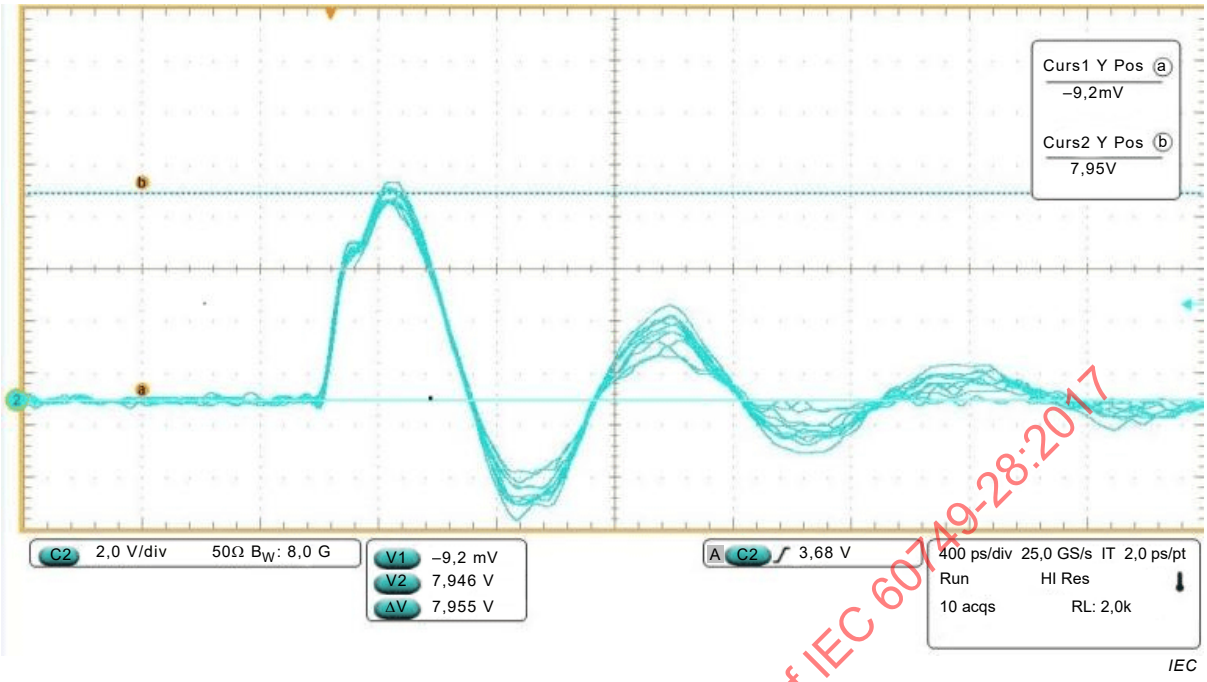


Figure E.3 – 8 GHz TC 500, small verification module (oscilloscope adjusts for attenuation)

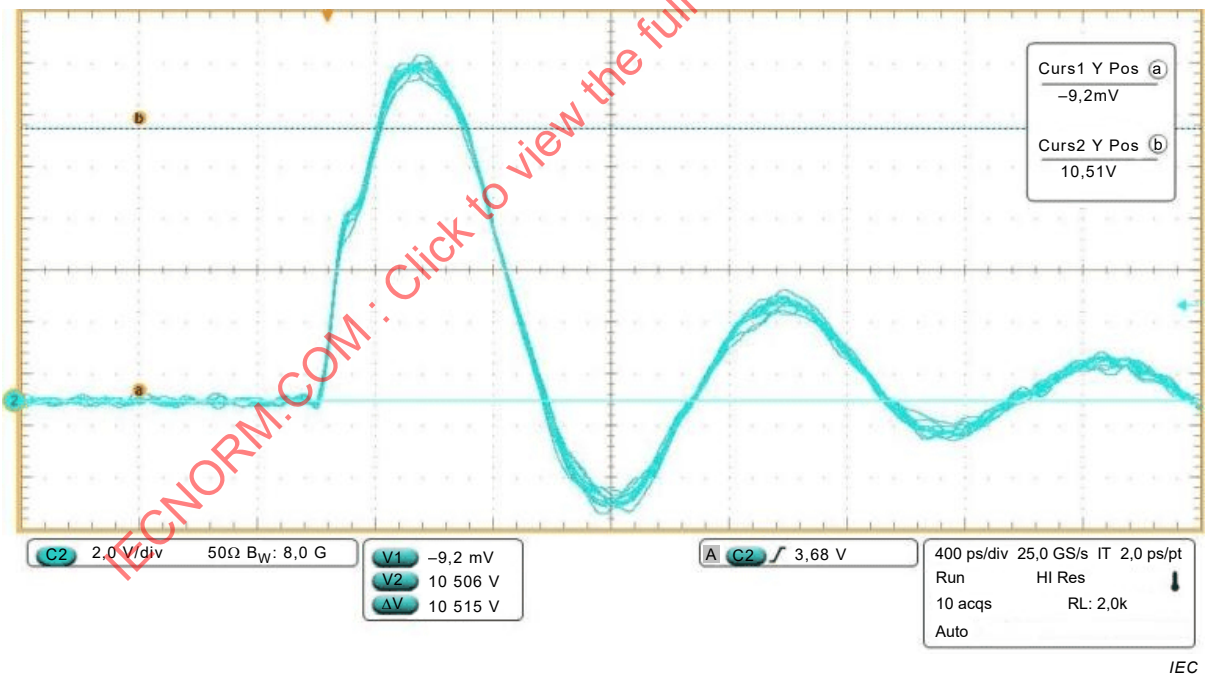


Figure E.4 – GHz TC 500, large verification module (oscilloscope adjusts for attenuation)

Annex F
(informative)

Field-induced CDM tester discharge procedures

F.1 General

Annex F describes the two types of discharge procedures used in field-induced CDM test equipment.

F.2 Single discharge procedure

The single positive and single negative discharges can be applied with two individual discharges using this sequence of steps producing the sequence of charging/discharging events as illustrated in Figure F.1.

a) Place the uncharged DUT on the field plate and align it.

b) The field voltage is established by raising the voltage on the field plate to the specified stress level.

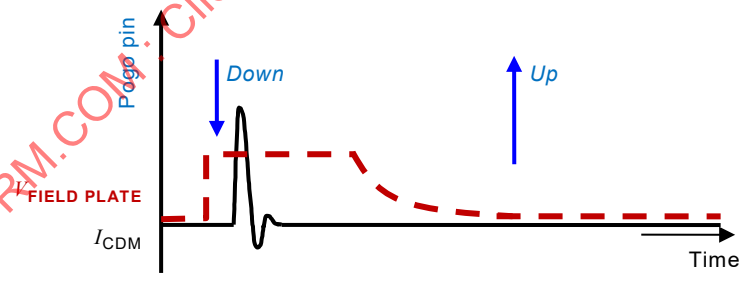
c) The first discharge is made by lowering the pogo pin to the DUT (see Figure F.1).

d) The pogo pin continues to descend until it makes physical contact with the device pin under test (PUT) to ensure full charge transfer and to provide a conduction path to ground.

e) Then the voltage on the field plate is slowly (resistively) returned to zero, which completely removes the charge that was transferred to the DUT during the first CDM discharge.

f) The pogo pin is returned to its starting (separated) position (see Figure F.1) before the voltage of the same or opposite polarity is applied to the field plate for subsequent discharges.

g) Repeat for each pin to be tested.



Field plate ($V_{FIELD\ PLATE}$ dashed line) at High Voltage (+) before DUT is contacted by pogo pin, and at Zero before raising the pogo pin

IEC

Figure F.1 – Single discharge procedure (field charging, I_{CDM} Pulse, and slow discharge)

F.3 Dual discharge procedure

The single positive and single negative discharges can be applied with one pair of alternating polarity discharges using this sequence of steps producing the sequence of charging/discharging events as illustrated in Figure F.2.

a) Place the uncharged DUT on the field plate and align it.

b) The field voltage for the positive stress is established by raising the voltage on the field plate to the specified stress level.

c) The first discharge is made by lowering the pogo pin to the DUT (see Figure F.2).

d) The pogo pin continues to descend until it makes physical contact with the DUT. This is to ensure full charge transfer and to provide a conduction path to ground.

e) The pogo pin is returned to its starting separated position (see Figure F.2), leaving the device with a net charge.

f) The voltage on the field plate is slowly (resistively) returned to zero, which completely removes the charge on the field plate. The DUT will still have a net charge.

g) The pogo pin is lowered (the second down arrow to the right in Figure F.2) a second time for the second discharge, which will be of opposite polarity and the same magnitude.

h) Repeat for each pin to be tested.

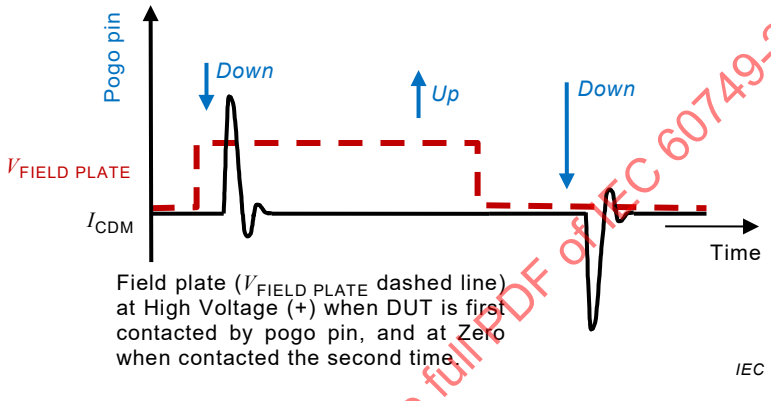


Figure F.2 – Dual discharge procedure (field charging, 1st I_{CDM} pulse, no field, 2nd I_{CDM} pulse)

Annex G
(informative)

Waveform verification procedures

G.1 Factor/offset adjustment method

This procedure aligns the tester for direct software voltage input of the test condition for the full alignment range. This method may not allow for alignment of each test condition with the target mid-range of I_p as shown in Table 1 or Table 2, but it is the easiest to use in a lab environment with multiple testers, as the software voltage entered matches the test condition target level and does not require linear interpolation/extrapolation for test conditions other than the five levels listed in Table 1 or Table 2.

The requirements/details of this method are as follows:

– a single factor/offset is used across the entire test condition range;

– a different factor/offset can be used for each polarity;

– the same factor/offset shall be used for both large and small verification modules.

Figure G.1 below depicts the waveform verification flow for qualification/re-qualification and quarterly checks, while Figure G.2 shows the flow for routine verifications. Table G.1 shows an example of the data that should be recorded.

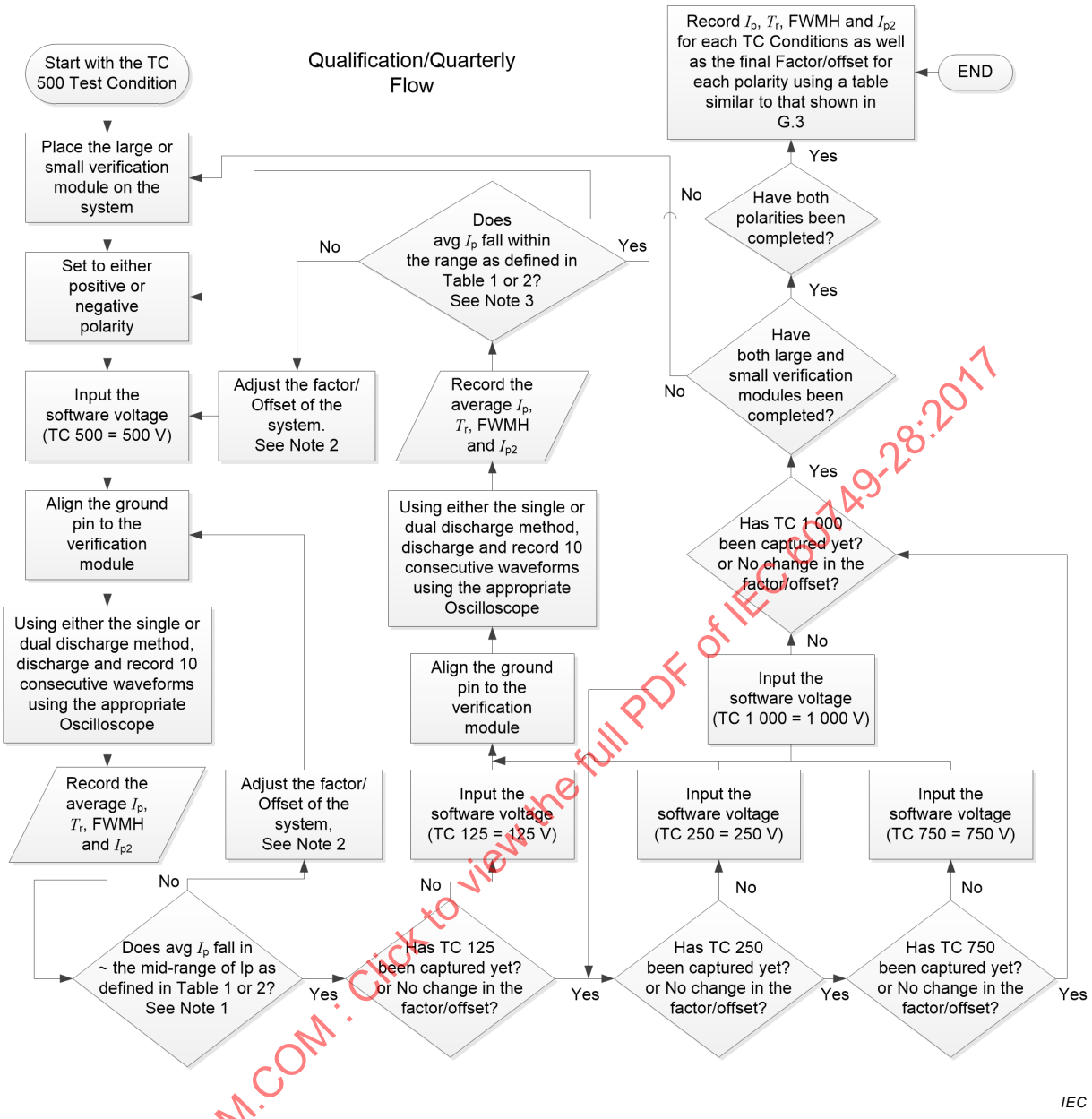


Figure G.1 – An example of a waveform verification flow for qualification and quarterly checks using the factor/offset adjustment method

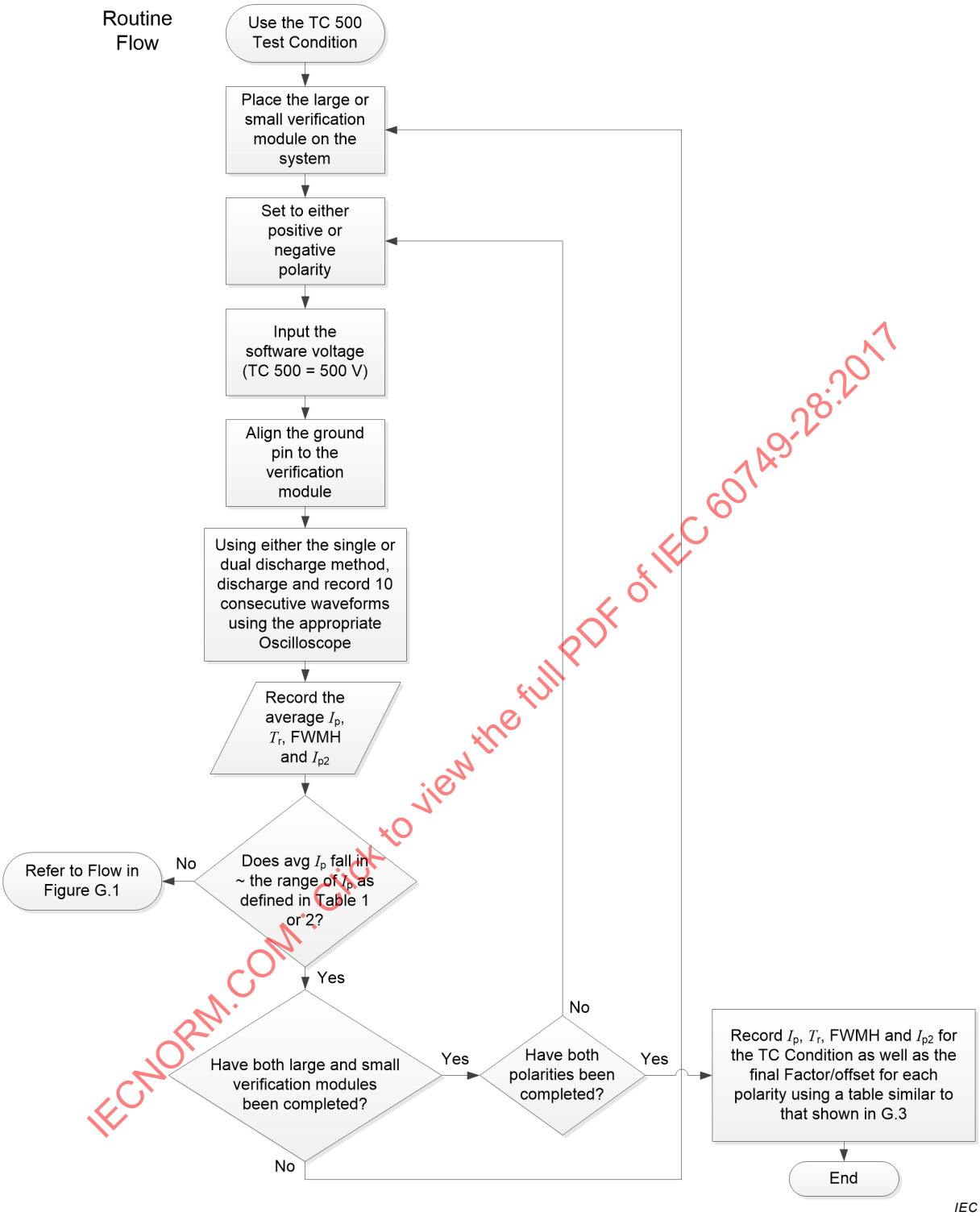


Figure G.2 – An example of a waveform verification flow for the routine checks using the factor/offset adjustment method

NOTE 1 Targeting to the mid-range of TC 500 is a starting point for adjustment of the field plate voltage. Based on the results of the other test conditions (TC 125/250/750/1 000) the I_{peak} can end up higher or lower than the mid-range value on TC 500. As shown in Figure G.3, adjustments in the factor/offset can shift the I_{peak} higher or lower.

NOTE 2 To properly calibrate systems, tester manufacturers have implemented a secondary “adjustment” parameter as an offset from the software voltage setting, either represented as a voltage “multiplier” value or a percentage “offset” value which modifies the field plate voltage. The tester manufacturer can be consulted for more detail.

After several iterations through this loop, if the user finds they cannot meet the I_{peak} range as defined in Table 1 or Table 2 or the factor/offset is outside the typical documented range, the verification modules and ground pin can be cleaned and all connections checked for tightness. If this still does not work, the system vacuum can be checked or the ground pin replaced. The tester manufacturer can be contacted for more information.

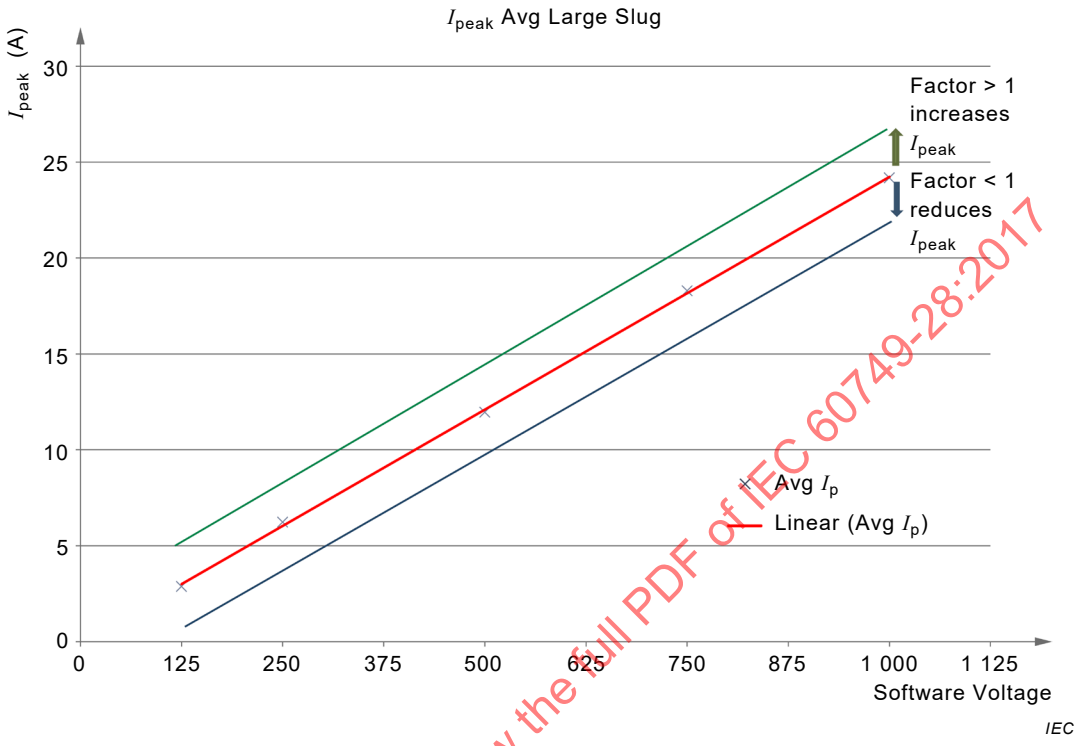


Figure G.3 – Example of average I_{peak} for the large verification module – high bandwidth oscilloscope

G.2 Software voltage adjustment method

This procedure does not adjust the factor/offset but leaves the factor/offset with a value that will not impact the field plate voltage and uses the software voltage entry as the primary adjustment of the field plate voltage. This method will allow for a much more accurate targeting of the midpoint of the I_p range as defined in Table 1 or Table 2, but creates complexity in determining the correct software voltage entry between the five test conditions. Determining software voltage entries, other than the five test condition levels, (which will be determined in this procedure) will require linear interpolation/extrapolation.

The requirements/details of this method are as follows:

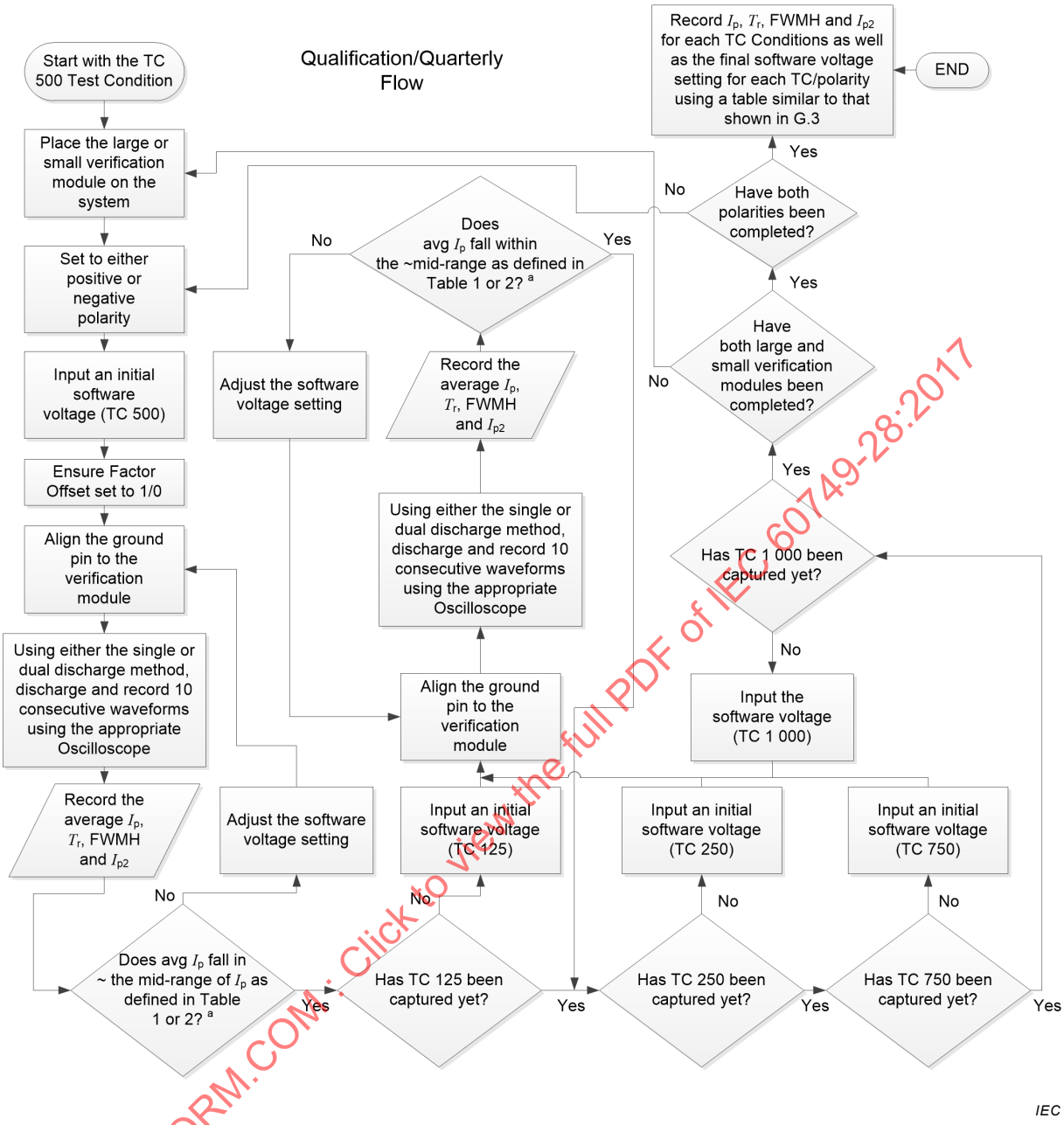
– a unique software voltage setting is determined for each test condition;

– unique voltage settings may be used for each polarity (at each test condition);

– the same software voltage setting shall be used for both large and small verification modules at each test condition;

– testing at levels other than the five test conditions will require a linear interpolation/extrapolation to determine the correct software voltage entry.

Figure G.4 below depicts the waveform verification flow for qualification/re-qualification and quarterly checks while Figure G.5 shows the flow for routine verifications. Table G.2, shows an example of the data which should be recorded.



a After several iterations through this loop, if the user finds they cannot meet the I_{peak} range as defined in Table 1 or Table 2 or that the software voltage setting is well outside the typical documented range, re-clean the verification modules and ground pin and check that all connections are tight. If this still does not work, check the system vacuum or look at replacement of the ground pin. Consult the tester manufacturer for more information.

Figure G.4 – An example of a waveform verification flow for qualification and quarterly checks using the software voltage adjustment method

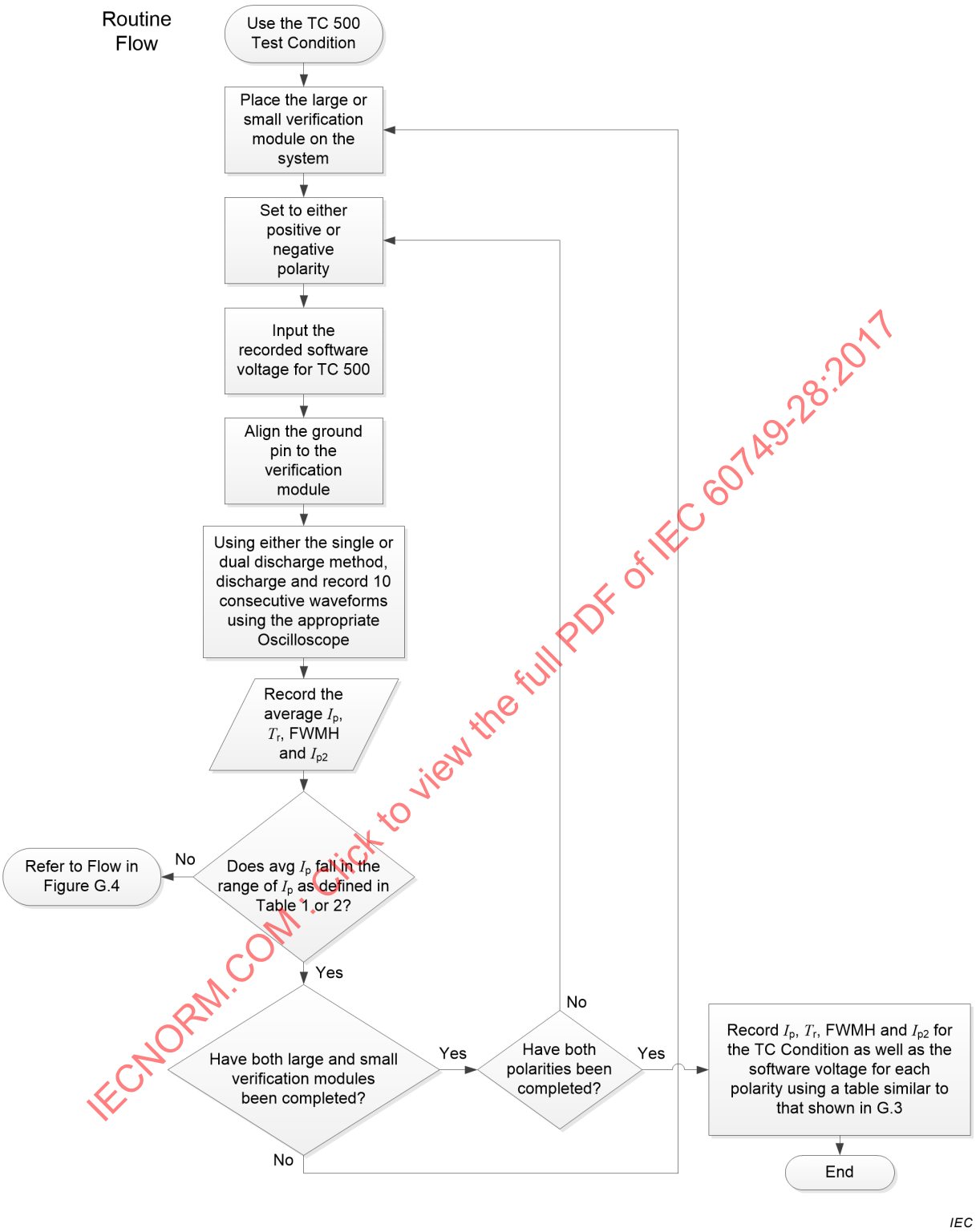


Figure G.5 – An example of a waveform verification flow for the routine checks using the software voltage adjustment method

G.3 Example parameter recording tables

Below is an example table of CDM qualification/quarterly verification waveform parameters to be recorded for the factor/offset adjustment method.

Table G.1 – Example waveform parameter recording table for the factor/offset adjustment method

Tester – System # 1									
Polarity = positive			**Scope bandwidth = 8 GHz**				**Factor/offset final setting = 0,82**		
Module size	**Date**	**% RH**	**Test cond**	**Software voltage**	$I_{P\ AVG}$ (A)	$T_{R\ AVG}$ (ps)	$T_{D\ AVG}$ (ps)	$I_{P2\ AVG}$ (A)	I_{P2} (% I_{P1})
Large	dd/m/yy	*X* %	TC 500	500	12,1	275	610	4,3	36 %
Small	dd/m/yy	*X* %	TC 500	500	7,30	185	400	3,7	51 %
Large	dd/m/yy	*X* %	TC 125	125	2,90	283	611	1,1	38 %
Small	dd/m/yy	*X* %	TC 125	125	1,90	201	395	1,1	58 %
Large	dd/m/yy	*X* %	TC 250	250	6,00	276	609	2,2	37 %
Small	dd/m/yy	*X* %	TC 250	250	3,70	186	397	2,1	57 %
Large	dd/m/yy	*X* %	TC 750	750	18,30	274	611	7,2	39 %
Small	dd/m/yy	*X* %	TC 750	750	11,00	190	398	6,1	55 %
Large	dd/m/yy	*X* %	TC 1 000	1 000	24,40	276	612	9,2	38 %
Small	dd/m/yy	*X* %	TC 1 000	1 000	14,60	187	399	7,4	51 %

Below is an example table of CDM qualification / quarterly verification waveform parameters

Below is an example table of CDM qualification / quarterly verification waveform parameters to be recorded for the software voltage adjustment method.

Table G.2 – Example waveform parameter recording table for the software voltage adjustment method

Tester – System # 2									
Polarity = positive			**Scope bandwidth = 8 GHz**				**Factor/offset final setting = 1/0**		
Module size	**Date**	**% RH**	**Test cond**	**Software voltage**	$I_{P\ AVG}$ (A)	$T_{R\ AVG}$ (ps)	$T_{D\ AVG}$ (ps)	$I_{P2\ AVG}$ (A)	I_{P2} (% I_{P1})
Large	dd/m/yy	*X* %	TC 500	410	12,1	275	610	4,3	36 %
Small	dd/m/yy	*X* %	TC 500	410	7,30	185	400	3,7	51 %
Large	dd/m/yy	*X* %	TC 125	105	2,90	283	611	1,1	38 %
Small	dd/m/yy	*X* %	TC 125	105	1,90	201	395	1,1	58 %
Large	dd/m/yy	*X* %	TC 250	205	6,00	276	609	2,2	37 %
Small	dd/m/yy	*X* %	TC 250	205	3,70	186	397	2,1	57 %
Large	dd/m/yy	*X* %	TC 750	620	18,30	274	611	7,2	39 %
Small	dd/m/yy	*X* %	TC 750	620	11,00	190	398	6,1	55 %
Large	dd/m/yy	*X* %	TC 1 000	840	24,40	276	612	9,2	38 %
Small	dd/m/yy	*X* %	TC 1 000	840	14,60	187	399	7,4	51 %

Annex H
(informative)

Determining the appropriate charge delay for full charging of a large module or device

H.1 General

Annex H describes the procedure for characterizing the charge delay on the CDM tester and determining the appropriate delay (for full charging) as either the default delay for the system (if the initial large verification module checkout fails as described in 5.9) or the delay required for a very large package device.

H.2 Procedure for charge delay determination

Follow the procedure below to determine an appropriate charge delay.

Using the large verification module or the ground pin of a very large package device:

a) Set the field plate voltage at +250 V (any voltage can be used as the objective is to monitor I_p).

b) With the pre-/post-charge delay set to 0 ms, collect 10 waveforms and record the I_p from each. Calculate the average I_p of the waveforms.

c) Increase the pre-charge delay by 50 ms, collect 10 waveforms, record the I_p from each, and calculate their average I_p.

d) Continue incrementing the delay by 50 ms (a larger or smaller step can be chosen) and record the average I_p until a minimum of 500 ms charge delay.

e) Plot the results as shown in Figure H.1.

f) The appropriate charge delay results in a “saturation point” for I_p. As shown below in Figure H.1, I_p for this example saturates at ~300 ms. Adding some guard band to this example would ensure that a pre-charge delay of 400 ms would be sufficient as either the default charge delay on the system (if the large verification module had been used) or as the required charge delay on a specific large package device if a large device had been used as the vehicle for the data collection.

g) For most large devices, it is expected that 500 ms will be sufficient to reach a saturation point. However, if after 500 ms, a saturation point has not been reached, repeat steps d) and e) until this occurs.

h) It is important to note that longer delay times do not “overcharge” the device but would only increase test time.