INTERNATIONAL STANDARD

IEC 60748-23-4

QC 165000-4

First edition
2002-05

Semiconductor devices – Integrated circuits –

Part 23-4: Hybrid integrated circuits and film structures – Manufacturing line certification – Blank detail specification

Dispositifs à semiconducteurs –
Circuits intégrés –

Partie 23-4:
Circuits intégrés hybrides et structures par films –
Certification de la ligne de fabrication –
Spécification particulière cadre

Reference number
IEC 60748-23-4:2002(E)

Publication numbering

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International Electrotechnical Commission
Международная Электротехническая Комиссия

PRICE CODE R

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 23-4: Hybrid integrated circuits and film structures – Manufacturing line certification – Blank detail specification

FOREWORD

1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of the IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested National Committees.
3) The documents produced have the form of recommendations for international use and are published in the form of standards, technical specifications, technical reports or guides and they are accepted by the National Committees in that sense.
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5) The IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with one of its standards.
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International Standard IEC 60748-23-4 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the European standard EN 165000-4 and the following documents:

FDIS	Report on voting
47A/641/FDIS	47A/652/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

IEC 60748-23-4 should be read in conjunction with Parts 23-1, 23-2 and 23-3.

The QC number that appears on the front cover of this publication is the specification number in the IEC Quality Assessment System for Electronic Components (IECQ).

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 23-4: Hybrid integrated circuits and film structures – Manufacturing line certification – Blank detail specification

1 General

1.1 Scope

This part of IEC 60748 serves as a Blank Detail Specification (BDS) for a high quality approval system and contains requirements for style and layout and minimum content of detail specifications. These requirements are applicable when the detail specification is published (e.g. for standard product).

1.2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60748-23-1:2002, *Semiconductor devices – Integrated circuits – Part 23-1: Hybrid integrated circuits and film structures – Manufacturing line certification – Generic specification*

IEC 60748-23-2:2002, *Semiconductor devices – Integrated circuits – Part 23-2: Hybrid integrated circuits and film structures – Manufacturing line certification – Internal visual inspection and special tests*

IEC 60748-23-3:2002, *Semiconductor devices – Integrated circuits – Part 23-3: Hybrid integrated circuits and film structures – Manufacturing line certification – Manufacturers' self audit check list and report*

2 Guidance for preparation of a detail specification

The front page layout is illustrated. When the detail specifications for customer circuits are not published, the layout requirements of the blank detail specification are optional. A suggested front page layout is also illustrated. An example of a Customer Detail Specification (CDS) is also given.

The numbers between square brackets on the front page of the blank detail specification illustrated correspond to the following indications which should be given:

[1] The name of the National Standards Organization under whose authority the detail specification is published and, if applicable, the organization from whom the detail specification is available.

[2] The IECQ number of the detail specification.

[3] The number and issue number of the IEC generic or sectional specification as relevant; also national reference if different.

[4] If different from the IEC number, the national number of the detail specification, date of issue and any further information required by the national system, together with any amendment numbers.

[5] A brief description of the technology and the type or function of the hybrid circuit.

[6] Information on typical construction (where applicable).

[7] An outline drawing with main dimensions which are of importance for interchangeability and/or reference to the appropriate national or international document for outlines. Alternatively, this drawing may be given in an annex to the detail specification.

[8] The product assessment level schedule number covered by the detail specification.

[9] Reference data giving information on the most important properties of the circuit which allow comparison between the various circuit types intended for the same, or for similar applications.

Layout of Blank Detail Specification (BDS)

FRONT PAGE FOR STANDARD CATALOGUE CIRCUITS

<table>
<tr><td>Specification available from: [1]</td><td>IEC 60748-23
Page 1 of</td><td>[2]</td></tr>
<tr><td>Electronic components of assessed quality by Manufacturing Line Certification [2]

Approval in accordance with</td><td colspan="2">[4]</td></tr>
<tr><td rowspan="3">Outline and dimensions – (see table 1) [7]
(first angle projection):

Dimensions in millimetres (see note 1)</td><td colspan="2">Thick/thin film hybrid integrated circuit [5]</td></tr>
<tr><td colspan="2">Encapsulation [6]
(see note 2)</td></tr>
<tr><td colspan="2">Product assessment level No. [8]</td></tr>
</table>

NOTE 1 The non-dimensioned details do not affect the performance of the devices.

NOTE 2 State whether the terminations are (not) suitable for soldering.
State whether the terminations are (not) suitable for printed wiring applications.

Information about manufacturers who have components qualified to this detail specification is available in the current Certified Manufacturing Line Listing.

FRONT PAGE FOR CUSTOMER CIRCUITS

<table>
<tr><td>Customer</td><td rowspan="2">CDS No.
Issue
Date
Page 1 of</td></tr>
<tr><td>Manufacturer</td></tr>
<tr><td>Electronic components of assessed quality by Manufacturing Line Certification Approval in accordance with: [3]</td><td>Type No.</td></tr>
<tr><td rowspan="3">Outline and dimensions – (see table 1) [7]
(first angle projection):

Dimensions in millimetres (see note 1)</td><td>Thick/thin film hybrid integrated circuit [5]</td></tr>
<tr><td>Encapsulation (see note 2) [6]</td></tr>
<tr><td>Product assessment level No. [8]</td></tr>
</table>

NOTE 1 The non-dimensioned details do not affect the performance of the devices.

NOTE 2 State whether the terminations are (not) suitable for soldering.
State whether the terminations are (not) suitable for printed wiring applications.

3 General data (BDS)

3.1 Recommended methods of mounting

The detail specification shall prescribe the method of mounting to be applied for normal use and for the application of the vibration and the bump or shock tests. The design of the circuit may be such that special mounting fixtures are required in its use. In this case the detail specification shall describe the mounting fixtures and they shall be used in the application of the vibration and bump or shock tests.

3.2 Dimensions, characteristics and conditions of use

Table 1 – Reference data [9]

Where a range of products has the same basic function and is made in the same technology and envelope, this table will be used to detail the differences in characteristics.

The detail specification shall contain all information needed to describe adequately:

3.2.1 Performance and design of the circuit

(1) schematic circuit diagram;

(2) resistance and capacitance values, tolerances, matching, tracking, power dissipation, temperature coefficients of resistors/temperature coefficients of capacitors where applicable;

(3) limitations on resistance of conductors where applicable;

(4) test circuit or method and performance limits;

(5) added components (see 6.1.3 of IEC 60748-23-1).

3.2.2 Limiting conditions of use

Examples:

operating temperature range;

storage temperature range;

vibration, shock, bump severities;

climatic category;

maximum voltage.

NOTE Any interrelationship between the details specified in 1.2.1 and 1.2.2 should be stated.

3.2.3 Derating

Where applicable, a derating curve is to be included in this clause.

3.3 Related documents

A list of related documents and issue/date status should be given in this clause.

3.4 Marking

The marking of the circuit and primary package shall be in accordance with the requirements of clause 5 of IEC 60748-23-1.

The details of the marking of the circuit and primary package shall be given in full.

3.5 Ordering information

Orders for circuits covered by this specification shall contain the following information:

1) quantity;
2) number of the detail specification with style reference and product assessment level number;
3) function of the circuit, if appropriate;
4) basic functional characteristics with tolerance, if appropriate.

3.6 Additional information (not for inspection purposes)

The detail specification may include information (which is not normally required to be verified by the inspection procedure) such as circuit diagrams, curves, drawings and notes for the clarification of the detail specification.

3.7 Additional or increased severities or requirements to those specified in the product assessment level schedule

These requirements may be specified in section two of the detail specification, but do not modify the release level.

4 Inspection requirements (BDS)

The detail specification shall prescribe the testing requirements of the initial delivery lot. This shall consist of all tests contained in the product assessment level schedule to which release is required, with the exception of those tests for which structural similarity may be invoked. The tests shall be subdivided into device screening (100 %), device sample testing, design evaluation and additional tests or requirements (see 1.7). Full details shall be given of test condition, pin-outs, mounting methods, etc.

The detail specification shall also prescribe the testing requirements of subsequent delivery lots. These shall consist of the screening tests, device sampling and such of the design evaluation tests as may be agreed between the manufacturer and the customer. For those design evaluation tests which are included the sample size and inspection level shall be as agreed between the manufacturer and the customer.

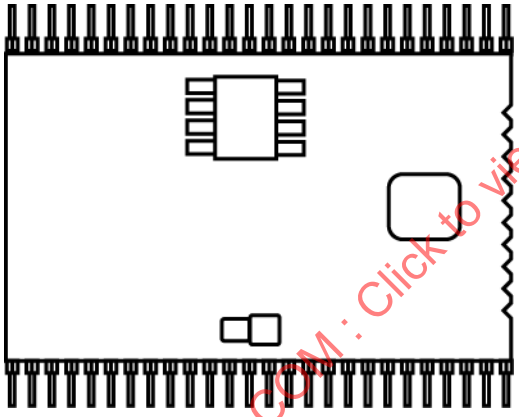
The content of any additional tests shall be as agreed between the manufacturer and the customer.

Annex A
(informative)

Example of a Customer Detail Specification (CDS)

<table>
<tr><td>Customer: Touzac Espace
Avenue Jean Brun
51079 Trouville
FRANCE</td><td rowspan="2">CDS No. 57823
Issue 1
Date 5.6.93
Page 1 of 8</td></tr>
<tr><td>Manufacturer Concise circuits
Electronic Road
Lowtown AX4 2TT, UK</td></tr>
<tr><td>Electronic components of assessed quality by Manufacturing Line Certification Approval in accordance with IEC 60748-23

Generic Specification: Film and hybrid integrated circuits</td><td>Type number
TE1</td></tr>
<tr><td rowspan="3">Outline and dimensions – (see annex 1)
(first angle projection):

 
IEC 1124/02

Dimensions in millimetres (see note)</td><td>Thick/thin film hybrid integrated circuit with leaded and leadless added components. Logarithmic amplifier.</td></tr>
<tr><td>Unencapsulated with solder attached lead frame suitable for soldering and printed wiring applications.</td></tr>
<tr><td>Product assessment level schedule 5.</td></tr>
</table>

NOTE The non-dimensioned details do not affect the performance of the devices.

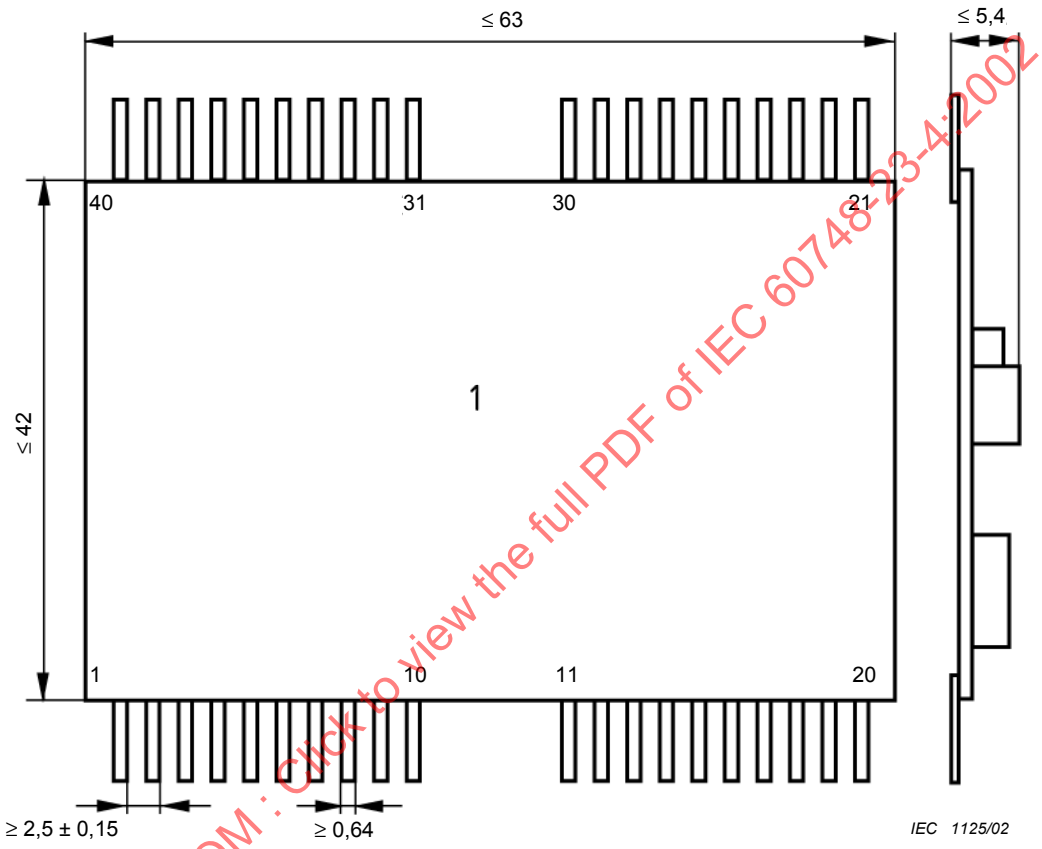
A.1 General data (CDS)

A.1.1 Recommended methods of mounting

Body mounted in Y_1 mode.

A.1.2 Dimensions, characteristics and conditions of use

The dimensions are given in figure A.1.

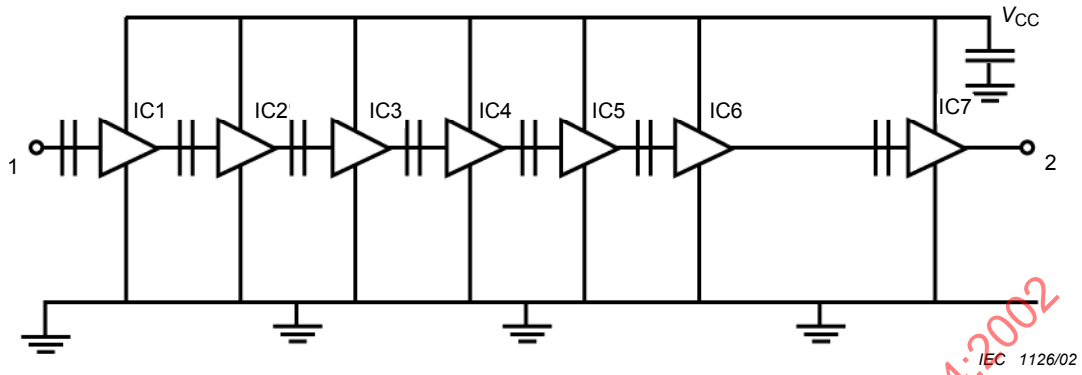


Pin No.	Pin name
1 – 20	Ground
21	Output
22	Ground
23	V_{CC} Positive power supply
24 – 37	Ground
38	Input
39 – 40	Ground

Figure A.1 – Dimensions and pin diagram

A.1.2.1 Performance and design of the circuit

(1) Schematic circuit diagram



Key

1 Signal input
2 Output

Schematic only
Individual resistors and capacitor components are not shown.

Figure A.2 – Schematic circuit diagram

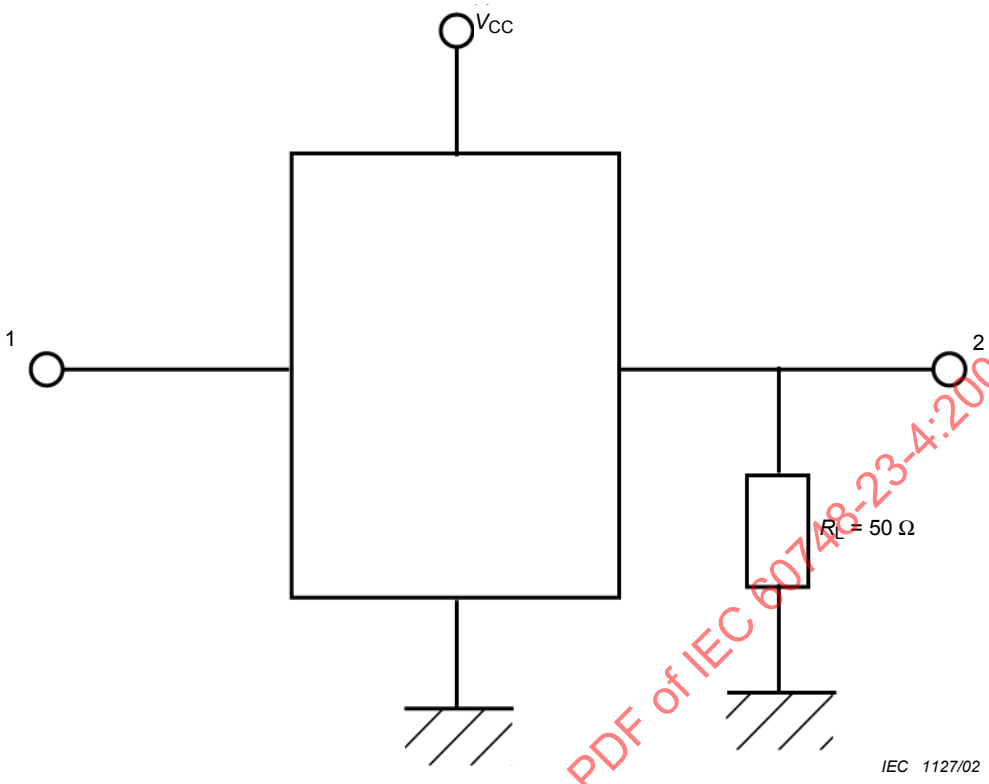
(2) Resistance and capacitance values

i) Resistance: 20-pin chip carrier 15 Ω to 22 Ω
Dual-in-line package 1,2 Ω to 2,2 Ω

ii) Capacitance: Chip capacitor (measured at 10 kHz 18,700 pF to 25,300 pF and 1 V_{rms})

(3) Limitations on resistance of conductors: not applicable

(4) Test circuit



Key

1 Input
2 Output

Operating notes

All supply and ground connections should be as short as possible. High frequency supply decoupling is provided on the hybrid.

Figure A.3 – Test circuit

(5) Added components

i) silicon monolithic integrated circuit SL1613C;
true log amplifier, hermetically sealed in 20-pin leadless chip carrier;

ii) silicon monolithic integrated circuit TI 113 low noise amplifier hermetically sealed in 8-pin flat pack.

A.1.2.2 Limiting conditions of use (not for inspection purposes)

Absolute values (non-simultaneous)

V_{cc} positive supply voltage	–0,5 V to 12 V
Maximum input signal (P_{in}) R_s = 50 Ω	+15 dBm
T_{sub} operating substrate	
Temperature range	–55 °C to 125 °C
T_{stg} storage temperature range	–65 °C to 150 °C
Shock	981 m/s^2, 6 ms
Vibration	20 Hz to 2 000 Hz, 98 m/s^2

This hybrid is static sensitive. Antistatic precautions should be taken.

A.1.2.3 Derating (CDS)

Not applicable.

A.1.3 Related documents

IEC 60748-23-1:2002, *Semiconductor devices – Integrated circuits – Part 23-1: Hybrid integrated circuits and film structures – Manufacturing line certification – Generic specification*

IEC 60748-23-2:2002, *Semiconductor devices – Integrated circuits – Part 23-2: Hybrid integrated circuits and film structures – Manufacturing line certification – Internal visual inspection and special tests*

IEC 60748-23-3:2002, *Semiconductor devices – Integrated circuits – Part 23-3: Hybrid integrated circuits and film structures – Manufacturing line certification – Self audit check list and report for film and hybrid integrated circuit manufacturers*

A.1.4 Marking

i) Each component shall bear the following markings:

   a) date code;
   b) terminal 1 identification;
   c) manufacturer's type number;
   d) factory identification code;
   e) product assessment level schedule number.

   All markings shall be on the lower surface except a) the date code.

ii) Each package containing one or more of these hybrids shall bear all of the above markings and in addition:

   f) quantity;
   g) customer detail specification number;
   h) ESDS warning label.

A.1.5 Ordering information

Orders placed for hybrids circuits to this specification shall include the following:

1. quantity;
2. customer detail specification number, issue number and date;
3. manufacturer's type number;
4. product assessment level schedule number;
5. (CDS).

A.1.6 Additional information (CDS)

The following characteristics (which are not for inspection purposes) describe the function of the circuit.

Characteristic at substrate temperature = 25 °C, V_{cc} = 10 V, f = 64 MHz, P_{in} = –75 dBm, R_L = 50 Ω, unless otherwise stated. Test circuit as in figure A.3.

Table A.1 – Characteristics

Characteristic	Symbol	Min.	Typical	Max.	Units
Supply current	I_{cc}		180	240	mA
Small signal gain	G	65	70	75	dB
Upper 3 dB bandwidth	f_u	120	200		MHz
Lower 3 dB bandwidth	f_l		2		MHz
Output level (P_{in} = –75 dBm)	V_{out}	20	30	5	V_{rms}
Output level (P_{in} = –5 dBm)	V_{out}	230	250	40	V_{rms}
Maximum output level (P_{in} = 4 dBm)	V_{lim}	240	270	270	V_{rms}
Input dynamic range (see note)	D_R	70	73	300	V_{rms} dB
Log accuracy	E	–1		+1	dB
Upper end of dynamic range	P_U	–7	–5	–3	dBm
Lower end of dynamic range	P_L	–77	–75	–73	dBm
Logarithmic slope	S	3	3,2	3,5	mV/dB
Phase variation (P_{in} = –75 dBm to –5 dBm)	P		5	10	degrees
Input VSWR			1,2	1,5	
Output VSWR			1,2	1,5	

NOTE Dynamic range is defined as the input signal range where the logarithmic error is less than 1 dB. See figure 4.