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INTERNATIONAL STANDARD

colour inside

Semiconductor devices – Discrete devices – Part 8: Field-effect transistors

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SEMICONDUCTOR DEVICES – DISCRETE DEVICES –

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FOREWORD

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This consolidated version of the official IEC Standard and its amendment has been prepared for user convenience.

IEC 60747-8 edition 3.1 contains the third edition (2010-12) [documents 47E/398/FDIS and 47E/406/RVD] and its amendment 1 (2021-06) [documents 47E/726/CDV and 47E/744/RVC].

In this Redline version, a vertical line in the margin shows where the technical content is modified by amendment 1. Additions are in green text, deletions are in strikethrough red text. A separate Final version with all changes accepted is available in this publication.

International Standard IEC 60747-8 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This third edition constitutes a technical revision.

The main changes with respect to the previous edition are listed below.

a) ”Clause 3 Classification” was moved and added to Clause 1.
b) “Clause 4 Terminology and letter symbols” was divided into “Clause 3 Terms and definitions” and “Clause 4 Letter symbols” was amended with additions and deletions.
c) Clause 5, 6 and 7 were amended with necessary additions and deletions.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2:.

This Part 8 should be used in conjunction with IEC 60747-1:2006.

A list of all the parts in the IEC 60747 series, under the general title *Semiconductor devices – Discrete devices*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of the base publication and its amendment will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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SEMICONDUCTOR DEVICES – DISCRETE DEVICES –

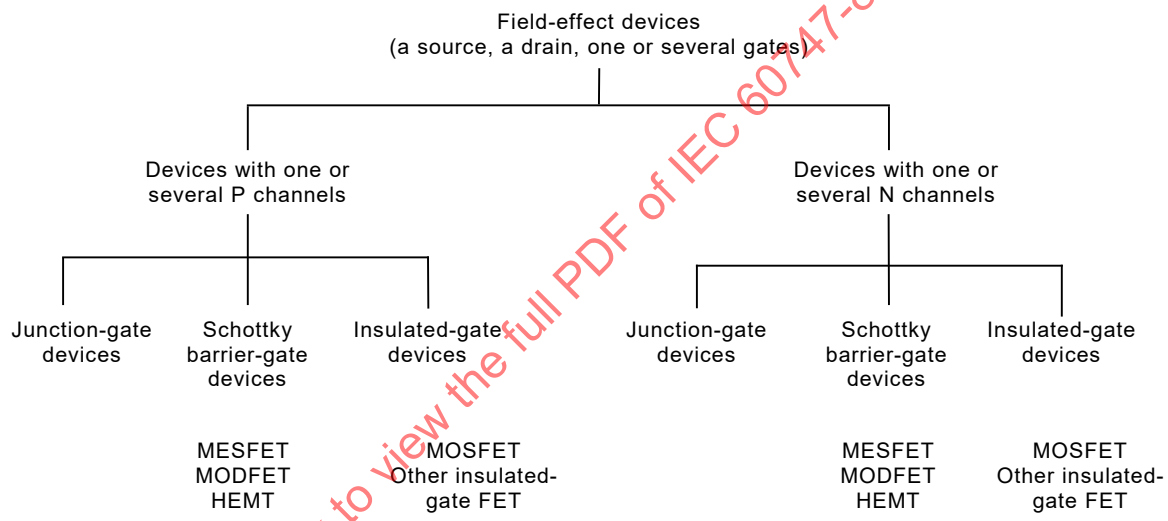
Part 8: Field-effect transistors

1 Scope

This part of IEC 60747 gives standards for the following categories of field-effect transistors:

– type A: junction-gate type;
– type B: insulated-gate depletion (normally on) type;
– type C: insulated-gate enhancement (normally off) type.

Since a field-effect transistor may have one or several gates, the classification shown below results:



NOTE 1 Schottky barrier-gate and insulated gate devices include depletion type devices and enhancement type devices.

NOTE 2 MOSFETs for some applications may not have inverse diode characteristics in the data sheet. Special circuit element structures to eliminate body diode are under development for such applications. MOSFET applications such as motor control equipment need to specify the inverse diode characteristics in the MOSFET to use the inverse diode as a free wheeling diode.

NOTE 3 The graphical symbol only for type C is used in this standard. The standard equally applies for P-channel and for type A and B devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61340 (all parts), *Electrostatics*

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*

IEC 60747-7:2000, *Semiconductor devices – Part 7: Bipolar transistors*

IEC 60749-23:2004, *Semiconductor devices – Mechanical and climatic test methods – Part 23: High temperature operating life*

IEC 60749-34, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling*

3 Terms and definitions

For the purpose of this document, the following terms and definitions apply.

3.1 Types of field-effect transistors

3.1.1
N-channel field-effect transistor
field-effect transistor that has one or more N-type conduction channels

3.1.2
P-channel field-effect transistor
field-effect transistor that has one or more P-type conduction channels

3.1.3
junction-gate field-effect transistor
JFET
field-effect transistor in which

– the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;

– a gate region adjacent to the channel has the opposite conductivity type, thus forming with source, channel and drain region a PN junction

NOTE The gate-source voltage controls the conductivity of the conduction channel in the channel region by controlling the width of the gate space-charge region and hence also the remaining cross-section of the conduction channel.

3.1.4
insulated-gate field-effect transistor
IGFET
field-effect transistor in which

– one or more gate electrodes are electrically insulated from the body;

– the conductivity type of both the source and drain regions is opposite from that of the semiconductor body in which they are located;

– the principal current flows in a channel that is formed by an inversion layer connecting source and drain regions

NOTE The inversion layer is either already present at zero gate-source voltage or produced within the body at sufficiently high forward gate-source voltage by accumulation of the minority charge carriers of the body material. The conductance of the channel is controlled by the gate-source voltage, which controls the electric field between gate electrode and the body and hence the amount of accumulated minority charge carriers.

3.1.5
metal-oxide-semiconductor field-effect transistor
MOSFET
insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material

3.1.6
depletion-type (normally on) field-effect transistor
field-effect transistor in which an inversion layer present at the surface of the active semiconductor region causes an appreciable channel conductance that may be increased (decreased) by applying a forward (reverse) gate-source voltage

3.1.7
enhancement-type (normally off) field-effect transistor
field-effect transistor having substantially zero channel conductance at zero gate-source voltage, and in which a conduction channel may be obtained by applying a sufficiently high forward gate-source voltage, which induces an inversion layer below the gate electrode

3.1.8
single-gate field-effect transistor
field-effect transistor having a gate region, a source region, and a drain region

NOTE The term may be abbreviated to "field-effect transistor", if no ambiguity is likely to occur.

3.1.9
dual-gate field-effect transistor
field-effect transistor having two independent gate regions, a source region, and a drain region

3.1.10
schottky-barrier-gate field-effect transistor
field-effect transistor in which

– the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;
– one or more gate electrodes each form a Schottky-barrier with the channel region;

the gate-source voltage controls the conductance of the conduction channel by varying its cross-section

3.1.11
metal-semiconductor field-effect transistor
MESFET
Schottky-barrier-gate field-effect transistor in which the gate electrodes are metal

3.1.12
modulation-doped field-effect transistor or high electron mobility transistor
MODFET or HEMT
metal-semiconductor field-effect transistor in which a doped material forms a heterojunction with an undoped channel; the doped material supplies electrons to the undoped channel whose high electron mobility results in enhanced channel conductance

NOTE MODFET and HEMT should be used interchangeably.

3.2 General terms

3.2.1 Physical regions (of a field-effect transistor)

3.2.1.1
source (of a field-effect transistor)
physical region that is designed by the manufacturer to contain the supply region under the defined operating conditions to which the specifications refer

3.2.1.2
drain (of a field-effect transistor)
physical region that is designed by the manufacturer to contain the collection region under the defined operating conditions to which the specifications refer

3.2.1.3
gate (of an IGFET)
insulating layer between the gate electrode and the surface of the semiconductor body, below which the channel is or may be formed

3.2.1.4
gate (of an JFET)
region below the gate electrode that is of opposite conductivity type from that of the source, channel and drain regions

3.2.1.5
channel (of a depletion-type IGFET)
inversion layer technologically placed below the gate region

3.2.1.6
channel (of a JFET)
region between source region and drain region that has the same conductivity type as these two regions

3.2.1.7
subchannel (of an IGFET)
region between source region and drain region, excluding the channel region of a depletion-type IGFET and all pertinent transition zones

3.2.1.8
substrate (of a JFET or IGFET)
part of the original material that remains unchanged when the device elements are formed upon or within the original material

NOTE The original material may be a layer of semiconductor material cut from a single crystal, a layer of semiconductor material deposited on a supporting base, or the supporting base itself.

3.2.1.9
substrate (of a JFET or IGFET)
original semiconductor material before being processed

NOTE The intended meaning will become clear from the context in which the term is used. If necessary, distinction could be made between the "original substrate" and the "remaining substrate".

3.2.1.10
substrate (of a thin-film field-effect transistor)
insulator that supports the source and drain electrodes, the insulating gate layer, and the thin semiconductor layer

3.2.2 Functional regions

3.2.2.1
functional source region
supply region that delivers principal-current charge carriers into the channel

3.2.2.2
functional drain region
collection region that acquires principal-current charge carriers from the channel

3.2.2.3
channel (of a IGFET)
functional region through which the principal-current charge carriers pass and in which the carrier concentration is determined by the gate-source voltage, the principal current being the result of the drift field produced by the drain-source voltage

3.2.2.4
channel (of a JFET)
functional region through which the principal-current charge carriers pass and whose cross-section is determined by the applied gate-source voltage, the principal current being the result of the drift field produced by the drain-source voltage

3.2.2.5
subchannel space-charge region (of an IGFET)
space-charge region associated with the transition regions between the subchannel region on one side, and source region, channel region and drain region on the other side

3.2.2.6
functional subchannel region
remaining neutral part of the (physical) subchannel region that is confined by the surrounding subchannel space-charge region

3.3 Terms related to ratings and characteristics

3.3.1
gate cut-off current (of a junction-gate field-effect transistor)
current flowing in the gate terminal of a junction field-effect transistor when the pn junction is biased in the reverse direction

3.3.2
gate leakage current (of an insulated-gate field-effect transistor)
leakage current through the insulated-gate of an insulated-gate field-effect transistor

3.3.3
capacitances

3.3.3.1
(short-circuit) input capacitance
capacitance between the gate and source terminals with the drain terminal short-circuited to the source terminal for a.c. signals

3.3.3.2
(short-circuit) output capacitance
capacitance between the drain and source terminals with the gate terminal short-circuited to the source terminal for a.c. signals

3.3.3.3
reverse transfer capacitance
capacitance between the drain and gate terminals excluding parallel capacitances between drain and source, and gate and source

3.3.4
gate-source resistance
d.c. resistance between gate and source terminals at specified gate-source and drain-source voltages

3.3.5
drain-source on-state resistance
d.c. resistance between the drain and source terminals when the FET is in its on-state

3.3.6
gate charge
charge required to raise the gate-source voltage from zero to a specified value

3.3.6.1
total gate charge
charge that is required to raise the gate-source voltage from zero to a specified value and calculated by the equation below (see Figure 1)

$$Q_G = \int_{t0}^{t4} i_{GG}(t)\mathrm{d}t$$

3.3.6.2
threshold gate charge
charge required to raise gate-source from zero to $V_{GS(th)}$ and calculated by the equation below (see Figure 1)

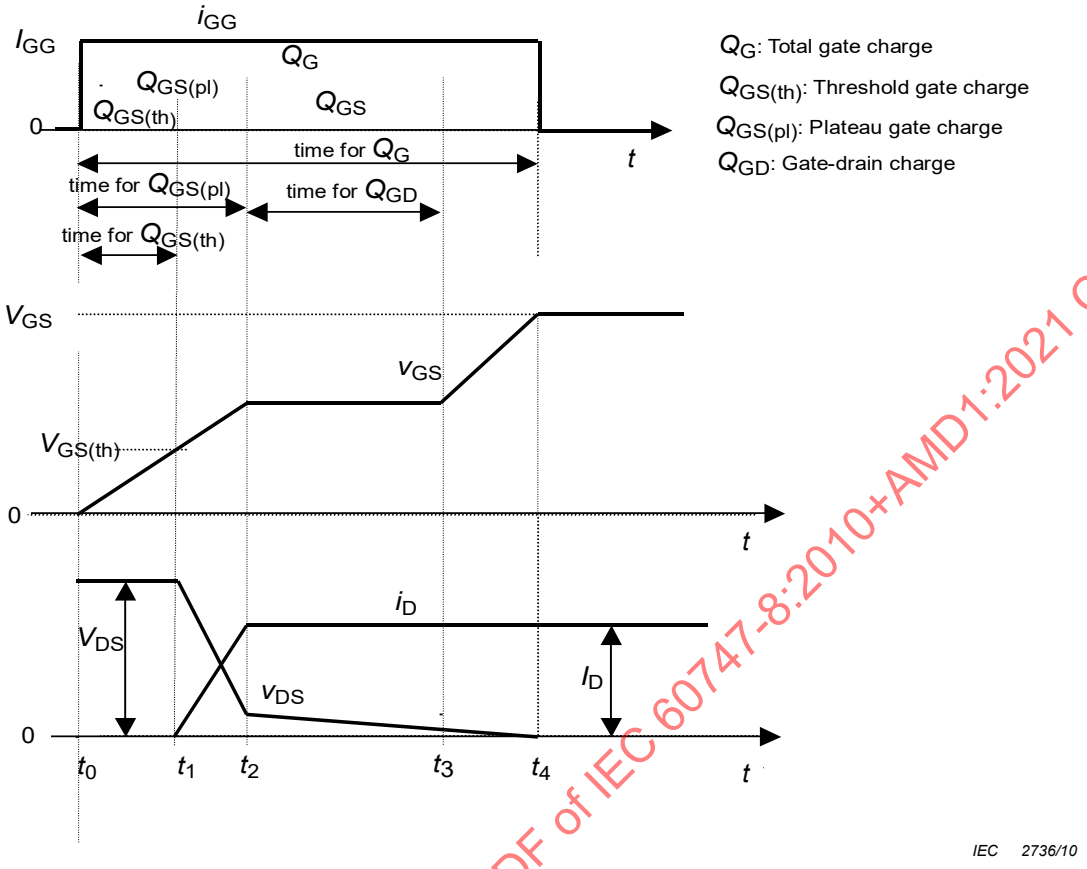
$$Q_{GS(th)} = \int_{t0}^{t1} i_{GG}(t)\mathrm{d}t$$

3.3.6.3
plateau gate charge
charge required to raise gate-source voltage from zero to plateau voltage $V_{GS(pl)}$ and calculated by the equation below (see Figure 1)

$$Q_{GS(pl)} = \int_{t0}^{t2} i_{GG}(t)\mathrm{d}t$$

3.3.6.4
gate drain charge
charge difference between beginning and end of plateau region, required to charge up C_{GD} and calculated by the equation below (see Figure 1)

$$Q_{GD} = \int_{t2}^{t3} i_{GG}(t)\mathrm{d}t$$



NOTE Time intervals indicated by arrow end lines are integral intervals to calculate the gate charges.

Figure 1 – Basic waveforms to specify the gate charges

3.3.7
overall efficiency
ratio of the output power to the sum of the input signal power and the d.c. input power

$$\eta_{tot} = \frac{P_{out}}{P_{in} + P_{(d.c.)}}$$

3.3.8
drain efficiency
ratio of the output power to the d.c. drain power

$$\eta_d = \frac{P_{out}}{P_{d(d.c.)}}$$

3.3.9
power-added efficiency
ratio of the difference between the output power and the input signal power to the d.c. input power

$$\eta_{add} = \frac{P_{out} - P_{in}}{P_{d(d.c.)}}$$

3.3.10
rate of rise of off-state voltage
rate of rise of drain-source off-state voltage induced during reverse recovery period of the inverse diode

3.3.11
reverse-bias safe operating area
drain current versus drain-source voltage region in which the MOSFET is able to turned-off repetitively with clamped inductive load without failure

3.3.12
short circuit safe operating area
drain current versus drain voltage region in which the MOSFET is able to turn on and off non repetitively without failure

3.3.13
avalanche energy (for avalanche devices)
avalanche energy capability during turn-off period

3.3.14
repetitive avalanche energy (for avalanche devices)
repetitive avalanche energy capability during turn-off period

3.3.15
non-repetitive avalanche energy (for avalanche devices)
non-repetitive avalanche capability during turn-off period (single pulse)

3.3.16
drain leakage current
drain current in the off-state

3.3.17
breakdown voltage, drain to source
drain-source breakdown voltage in the off-state

3.3.18
internal gate resistance
short-circuit internal gate resistance (see Figure 32)

3.3.19
switching times
input wave form is the gate to source voltage, and output waveform is the drain current (see IEC 60747-1:2006)

3.3.20
turn-on energy
value of the integral of the product of drain-source voltage V_{DS} and drain current I_D during turn-on described in the following equation: $E_{on} = \int_0^{t_1} i_D \times v_{DS} \times \mathrm{d}t$ (see Figure 2)

3.3.21
turn-off energy
value of the integral of drain-source voltage V_{DS} multiplied by drain current I_D during turn-off described in the following equation: $E_{off} = \int_{t_2}^{t_3} i_D \times v_{DS} \times dt$ (see Figure 2)

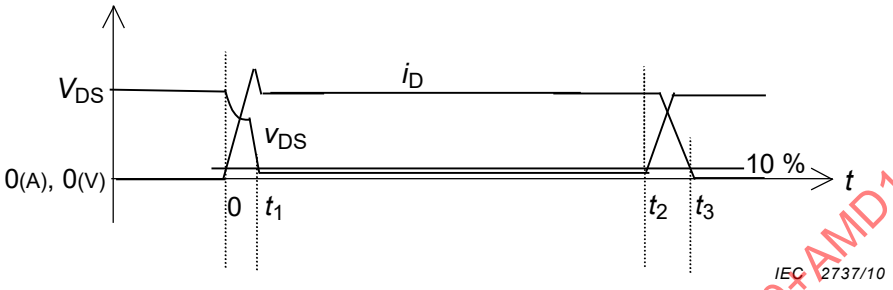


Figure 2 – Integral times for the turn-on energy E_{on} and turn-off energy E_{off}

3.3.22
output capacitance charge
charge required to change the voltage at output capacitance C_{oss} during turn-on and turn-off

3.3.23
gate-source plateau voltage
voltage during turn-on, where V_{GS} is relatively constant (Miller-Plateau) and during which C_{GD} is charged

NOTE See Figure 1.

3.3.24
drain-source reverse voltage
voltage across the MOSFET which results from the flow of current in the reverse direction from source to drain

3.3.25
MOSFET forward recovery current
recovery current of the MOSFET which results from the flow of current in the reverse direction from source to drain

3.3.26
MOSFET forward recovery time
recovery time of the MOSFET which results from the flow of current in the reverse direction from source to drain

3.3.27
MOSFET forward recovery charge
recovery charge of the MOSFET which results from the flow of current in the reverse direction from source to drain

3.3.28
MOSFET forward recovery energy
recovery energy of the MOSFET which results from the flow of current in the reverse direction from source to drain

3.4 Conventional used terms

Table 1 – Terms for MOSFET in this ~~standard~~ document and the conventional used terms for the inverse diode integrated in the MOSFETs for N-channel

Preferred terms	Letter symbol	Deprecated terms for inverse diode with MOSFET in off-state
Drain-source reverse voltage	~~V_{DSR}~~ V_{SD}	Inverse diode forward voltage
MOSFET forward recovery current	I_{fr}	Inverse diode reverse recovery current
MOSFET peak forward recovery current	I_{frm}	Inverse diode peak reverse recovery current
MOSFET forward recovery time	t_{fr}	Inverse diode reverse recovery time
MOSFET forward recovery charge	Q_f	Inverse diode reverse recovery charge
MOSFET forward recovery energy	E_{fr}	Inverse diode reverse recovery energy
Reverse drain current	~~I_{DR}~~ I_S	Inverse diode forward current
Repetitive peak reverse drain current	~~I_{DRM}~~ I_{SRM}	Inverse diode repetitive peak forward current

4 Letter symbols

4.1 General

General letter symbols for MOSFETs are defined in Subclauses 4.4 and 4.5 of IEC 60747-1:2006.

4.2 Additional general subscripts

In addition to the list of recommended general subscripts given in 4.2.3 of IEC 60747-1:2006, the following special subscripts are recommended for field-effect transistors:

D, d = drain
G, g = gate
S, s = source or termination with a short circuit
B, b; U, u = substrate
T; th; (TO) = threshold
O = termination with an open circuit
R = termination with a resistor
X = termination with specified gate source voltage
pl = plateau

4.3 List of letter symbols

Name and designation	Letter symbol	Remarks
4.3.1 Voltage		
Drain-source (d.c.) voltage	V_{DS}	
Gate-source (d.c.) voltage	V_{GS}	
Gate-source cut-off voltage (of a junction field-effect transistor and of a depletion type insulated-gate	$V_{GS(OFF)}$; V_{GSoff}	

Name and designation	Letter symbol	Remarks
field-effect transistor)		
Gate-source threshold voltage (of an enhancement type insulated-gate field-effect transistor)	V_{GST}; $V_{GS(th)}$; $V_{GS(TO)}$	
Forward gate-source (d.c.) voltage	V_{GSF}	
Reverse gate-source (d.c.) voltage	V_{GSR}	
Gate-drain (d.c.) voltage	V_{GD}	
Source-substrate (d.c.) voltage	V_{SB}; V_{SU}	
Drain-substrate (d.c.) voltage	V_{DB}; V_{DU}	
Gate-substrate (d.c.) voltage	V_{GB}; V_{GU}	
Gate-gate voltage (for multi-gate devices)	V_{G1-G2}	
Gate-source breakdown voltage with drain short-circuited to source	$V_{(BR)GSS}$	
Breakdown voltage, drain-source (for type B)	$V_{(BR)DSX}$	
Breakdown voltage, drain-source (for type C)	$V_{(BR)DSS}$	
Drain-source on-state voltage	$V_{DS(on)}$	
Drain-source reverse voltage	V_{DR}	
Gate-source plateau voltage	$V_{GS(pl)}$	
4.3.2 Currents		
Drain (d.c.) current	I_D	
Peak drain current	I_{DM}	
~~Peak reverse drain current~~	~~I_{DRM}~~	
Drain current, at a specified gate-source condition	I_{DSX}	
Drain current, at a specified external gate-source resistance	I_{DSR}	
Drain current, with gate short-circuited to source (V_{GS} = 0)	I_{DSS}	
Source (d.c.) current (for P-channel)	I_S	
Peak source current (for P-channel)	I_{SM}	
Source current, at a specified gate-drain condition (for P-channel)	I_{SDX}	
Source current, with gate short-circuited to drain (V_{GD} = 0) (for P-channel)	I_{SDS}	
~~Gate (d.c.) current~~	~~I_G~~	
Forward gate current	I_{GF}	
Gate cut-off current (of a junction field-effect transistor), with source open-circuited	I_{GDO}	
Gate-cut-off current (of a junction field-effect transistor), with drain open-circuited	I_{GSO}	
Gate cut-off current (of a junction field-effect transistor), with drain short-circuited to source	I_{GSS}	
Gate leakage current (of an insulated-gate field-effect transistor), with drain short-circuited to source	I_{GSS}	
Gate cut-off current (of a junction field-effect transistor), with specified drain-source circuit conditions	I_{GSX}	
Substrate current	I_B; I_U	

Name and designation	Letter symbol	Remarks
4.3.3 Power dissipation		
Total power dissipation	P_{tot}	
4.3.4 Small-signal parameters		
Drain-source resistance Gate-source resistance Gate-drain resistance Gate resistance (with V_{DS} = 0 or v_{ds} = 0)	r_{ds} r_{gs} r_{gd} r_{gss}	
Drain-source on-state resistance	$r_{ds(on)}$	
Drain-source off-state resistance	$r_{ds(off)}$	
Internal gate resistance	R_g	
Open-circuit gate-source capacitance (drain-source and gate-drain open-circuited to a.c.)	C_{gso}	
Open-circuit gate-drain capacitance (drain-source and gate-source open-circuited to a.c.)	C_{gdo}	
Open-circuit drain-source capacitance (gate-drain and gate-source open-circuited to a.c.)	C_{dso}	
Short-circuit input capacitance in common-source configuration; gate-source capacitance (drain-source short-circuited to a.c.)	C_{iss}; C_{11ss}	
Short-circuit output capacitance in common-source configuration; drain-source capacitance (gate-source short-circuited to a.c.)	C_{oss}; C_{22ss}	
Common-source reverse transfer capacitance with input short-circuited to a.c.	C_{rss}; C_{12ss}	
Short-circuit output capacitance in common-drain configuration (gate-drain short-circuited to a.c.)	C_{ods}; C_{22ds}	
Gate-source capacitance (in the π equivalent circuit)	C_{gs}	
Gate-drain capacitance (in the π equivalent circuit)	C_{gd}	
Drain-source capacitance (in the π equivalent circuit)	C_{ds}	
Short-circuit input conductance in common-source configuration	G_{iss}	
Short-circuit output conductance in common-source configuration	G_{oss}	
Gate-source conductance (in the π equivalent circuit)	G_{gs}	
Gate-drain conductance (in the π equivalent circuit)	G_{gd}	
Drain-source conductance (in the π equivalent circuit)	G_{ds}	
Short-circuit input admittance	$y_{is} = Re_{(yis)} + j\omega C_{is}$ $y_{11s} = Re_{(y11s)} + j\omega C_{11s}$	
Short-circuit reverse transfer admittance	$y_{rs} = Re_{(yrs)} + j\omega C_{rs}$ $y_{12s} = Re_{(y12s)} + j\omega C_{12s}$	
Short-circuit forward transfer admittance	$y_{fs} = Re_{(yfs)} + jIm_{yfs}$ $y_{21s} = Re_{(y21s)} + jIm_{y21s}$	
Short-circuit output admittance	$y_{os} = Re_{(yos)} + j\omega C_{os}$ $y_{22s} = Re_{(y22s)} + j\omega C_{22s}$	
Modulus of the short-circuit reverse transfer	$\lvert y_{rs} \rvert$; $\lvert y_{12s} \rvert$	

Name and designation	Letter symbol	Remarks
admittance		
Phase of the short-circuit reverse transfer admittance	φ_{yrs}; φ_{y12s}	
Modulus of the short-circuit forward transfer admittance	$\lvert y_{fs} \rvert$; $\lvert y_{21s} \rvert$	
Phase of the short-circuit forward transfer admittance	φ_{yfs}; φ_{y21s}	
Forward transconductance (in the π equivalent circuit)	g_{ms}; g_m; g_{fs}	
Input reflection coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	 s_{11s} or s_{is} s_{11g} or s_{ig} s_{11d} or s_{id}	
Output reflection coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	 s_{22s} or s_{os} s_{22g} or s_{og} s_{22d} or s_{od}	
Forward transmission coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	 s_{21s} or s_{fs} s_{21g} or s_{fg} s_{21d} or s_{fd}	
Reverse transmission coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	 s_{12s} or s_{rs} s_{12g} or s_{rg} s_{12d} or s_{rd}	
4.3.5 Other parameters		
Total gate charge	Q_G	
Plateau gate charge	$Q_{GS(pl)}$	
Gate-drain charge	Q_{GD}	
Threshold gate charge	$Q_{GS(th)}$	
Power gain	G_P; G_p	
Output power at specified input power	P_o	
Overall efficiency	η_{tot}	
Drain efficiency	η_d	
Power added efficiency	η_{add}	
Cut-off frequency (in the common-source configuration)	f_{yfs}	
Noise voltage	V_n	
Noise figure	F	
Temperature coefficient of drain current	α_{ID}	
Temperature coefficient of drain-source resistance	α_{rds}	
Turn-on delay time	$t_{d(on)}$	Switching times (see Figure 3) $t_{on} = t_{d(on)} + t_r$ $t_{off} = t_{d(off)} + t_f$
Turn-off delay time	$t_{d(off)}$	
Rise time	t_r	
Fall time	t_f	
Turn-on time	t_{on}	
Turn-off time	t_{off}	
Turn-on energy	E_{on}	

Name and designation	Letter symbol	Remarks
Turn-off energy	E_{off}	
Repetitive avalanche energy	E_{AR}	
Non-repetitive single pulse avalanche energy	E_{AS}	
Frequency of unity forward transmission coefficient:		
– in common-source configuration	f_{ss} or f_{iss}	$f_{ss} = f$ for $\lvert s_{21s} \rvert = 1$
– in common-gate configuration	f_{sg} or f_{isg}	$f_{sg} = f$ for $\lvert s_{21g} \rvert = 1$
– in common-drain configuration	f_{sd} or f_{isd}	$f_{sd} = f$ for $\lvert s_{21d} \rvert = 1$

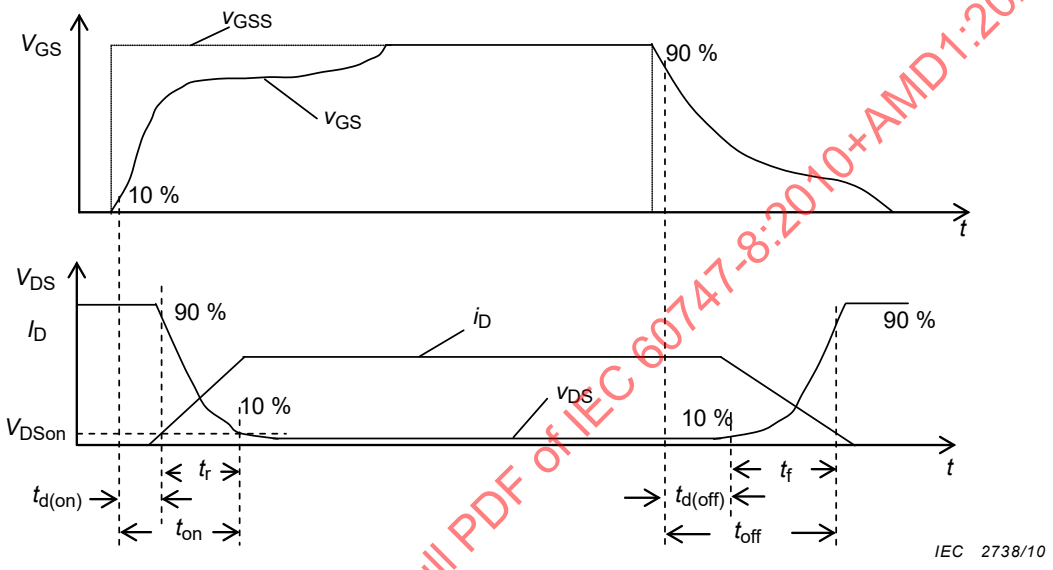


Figure 3 – Switching times

Name and designation	Letter symbol	Remarks
4.3.6 Matched-pair field-effect transistors		
Difference of gate leakage currents (for insulated-gate field-effect transistors) and difference of gate cut-off currents (for junction field-effect transistors)	$I_{G1} - I_{G2}$	The smaller value is subtracted from the larger value
Ratio of drain currents for zero gate-source voltage	I_{DSS1} / I_{DSS2}	The smaller of the two values is taken as the numerator
Difference of small-signal common-source output conductances	$g_{os1} - g_{os2}$	The smaller value is subtracted from the larger value
Ratio of small-signal common-source forward transfer conductances	g_{fs1} / g_{fs2}	The smaller of the two values is taken as the numerator
Difference of gate-source voltages	$V_{GS1} - V_{GS2}$	The smaller value is subtracted from the larger value
Change in difference of gate-source voltages between two temperatures	$\lvert \Delta(V_{GS1} - V_{GS2}) \rvert_{\Delta T}$	
4.3.7 Inverse diodes integrated in MOSFETs for N-channel		
Drain-source reverse voltage	~~V_{DSR}~~ V_{SD}	Forward voltage of the inverse diode
MOSFET forward recovery current	~~I_{FR}~~ I_{fr}	Reverse recovery current of the inverse diode
MOSFET peak forward recovery current	~~I_{FRM}~~ I_{frm}	Peak reverse recovery current of the inverse diode

MOSFET forward recovery time	t_{fr}	Reverse recovery time of the inverse diode
MOSFET forward recovery charge	Q_f	Reverse recovery charge of the inverse diode
MOSFET forward recovery energy	E_{fr}	Reverse recovery energy of the inverse diode
Reverse drain current	~~I_{DR}~~ I_S	Forward current of the inverse diode
Repetitive peak reverse drain current	I_{SRM}	Repetitive peak forward current of the inverse diode

5 Essential ratings and characteristics

5.1 General

5.1.1 Device categories

Field-effect transistors are divided into three categories:

– type A: junction-gate type;
– type B: insulated-gate depletion type;
– type C: insulated-gate enhancement type.

5.1.2 Multiple-gate devices

For multiple-gate devices, the required gate ratings and characteristics shall be given for each gate separately, except where otherwise stated.

5.1.3 Handling precautions

Because of the very high input resistance of field-effect transistors, the gate insulation layer (for insulated-gate types) or the gate junction (for junction-gate types) may be irreversibly damaged if an excessive voltage is allowed to build up, e.g. due to contact with electrostatically charged persons, leakage currents from soldering irons, etc.

The requirements of IEC 60747-1:2006 Clause 8 apply to these devices.

	TYPES		
	A	B	C
5.2 Ratings (limiting values)			
5.2.1 Temperatures			
5.2.1.1 Minimum and maximum storage temperatures (T_{stg})	+	+	+
5.2.1.2 Virtual junction temperature (T_{vj})	+	+	+
Maximum rated value.			
5.2.2 Power dissipation (P_{tot})	+	+	+
Maximum total power dissipation over the specified range of operating temperatures (ambient or case).			
5.2.3 Safe operating area (SOA) for MOSFET only			
Over the specified range of operating temperatures, under specified pulse			

	TYPES		
	A	B	C
conditions.			
5.2.3.1 Forward-bias safe operating area (FBSOA)		+	+
Maximum safe operating area of V_{DS} and I_D in conduction state.			
5.2.3.2 Reverse-bias safe operating area (RBSOA)		+	+
Maximum safe operating area of V_{DS} and I_D during turn-off state.			
5.2.3.3 Short-circuit safe operating area (SCSOA)		+	+
Non-repetitive maximum safe operating area of V_{DS} and I_D during turn-off state from short circuit condition.			
5.2.4 Voltages and currents			
Ratings apply over the operating temperature range unless otherwise specified.			
5.2.4.1 Maximum drain-source voltage	+	+	+
Under specified gate conditions.			
5.2.4.2 Maximum reverse gate-source voltage and, where appropriate, maximum forward gate-source voltage	+	+	+
Under specified drain conditions.			
5.2.4.3 Maximum gate-substrate voltage		+	+
Under specified source conditions;			
For insulated-gate field-effect transistors with separate source and substrate terminals (chopper or analog-switch types)			
5.2.4.4 Maximum drain-substrate voltage		+	+
Under specified gate to source conditions;			
For insulated-gate field-effect transistors with separate source and substrate terminals (chopper or analog-switch types)			
5.2.4.5 Maximum source-substrate voltage		+	+
Under specified gate to drain conditions.			
For insulated-gate field-effect transistors with separate source and substrate terminals (chopper or analog-switch types)			
5.2.4.6 Maximum drain current (I_D)	+	+	+
5.2.4.7 Maximum peak drain current (I_{DM})		+	+
Under specified pulse conditions.			
For MOSFET only.			
5.2.4.8 Maximum continuous (d.c.) reverse drain current (~~I_{DR}~~ I_S) (forward current of the inverse diode)		+	+

	TYPES		
	A	B	C
5.2.4.9 Maximum peak reverse drain current (I_{DRM} I_{SM}) (Maximum peak forward current of the inverse diode)		+	+
Under specified pulse conditions.			
5.2.4.10 Maximum forward gate current	+		
5.3 Characteristics			
Characteristics are to be given at 25 °C, except where otherwise stated and at (at least) one other temperature.			
5.3.1 Characteristics for low-frequency amplifier			
5.3.1.1 Gate cut-off current	+		
Gate leakage current		+	+
Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
Together with:			
Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.1.2 Drain cut-off current	+	+	+
Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.1.3 Drain current at zero gate-source voltage (I_{DSS})	+	+	
Minimum and maximum values, for zero gate-source voltage, at a specified drain-source voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.1.4 Drain current at specified gate-source voltage (I_{DSX})			+
Minimum and maximum values, for specified gate-source and drain-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.1.5 Gate-source cut-off voltage ($V_{GSoff)}$)	+	+	
Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.1.6 Gate-source threshold voltage ($V_{GS(th)}$)			+
Minimum and maximum values, at a specified high value of drain-source			

	TYPES		
	A	B	C
voltage, and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.1.7 Short-circuit input capacitance (C_{iss})	+	+	+
Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the output short-circuited to a.c.			
5.3.1.8 Short-circuit output conductance and, where appropriate, capacitance (g_{oss}, C_{oss})	+	+	+
Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.			
5.3.1.9 Reverse transfer capacitance (where appropriate) (C_{rss})	+	+	+
Maximum small-signal value, in common-source configuration with input open-circuit to a.c., under specified bias conditions and at a specified low frequency.			
5.3.1.10 Forward transconductance (g_{ms}, g_m, g_{fs})	+	+	+
Minimum and maximum values under specified bias conditions and at a specified low frequency.			
5.3.1.11 For low-noise applications, noise voltage and, where appropriate, noise figure (V_n, F)	+	+	+
Maximum value, in common-source configuration, under specified conditions of bias, source resistance, center frequency and power bandwidth.			
5.3.1.12 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-a)}$) or ($R_{th(j-c)}$)	+	+	+
Maximum value.			
5.3.2 Characteristics for high-frequency amplifier			
5.3.2.1 Gate cut-off current	+		
Gate leakage current		+	+
Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
Together with:			
Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.2.2 Drain cut-off current	+	+	+
Maximum value, at specified drain-source and gate-source voltages, other			

	TYPES		
	A	B	C
terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.2.3 Drain current at zero gate-source voltage (I_{DSS})	+	+	
Minimum and maximum values, for zero gate-source voltage and a specified drain-source voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.2.4 Drain current at specified gate-source voltage (I_{DSX})			+
Minimum and maximum values, for specified drain-source voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.2.5 Gate-source cut-off voltage (V_{GSoff})	+	+	
Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.2.6 Gate-source threshold voltage ($V_{GS(th)}$)			+
Minimum and maximum values, at a specified high value of drain-source voltage, and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.2.7 y-parameters			
5.3.2.7.1 For all FETs under specified values of bias and frequency:	+	+	+
y_{is} – real and imaginary parts, maximum values;			
y_{os} – real and imaginary parts, maximum values;			
y_{fs} – real and imaginary parts, minimum and maximum values (see also 5.3.2.7.2);			
y_{rs} – real and imaginary parts, maximum values.			
5.3.2.7.2 For power MOSFET as alternative to y_{fs}, forward transconductance (g_{ms}, g_m, g_{fs}):		+	+
Minimum value with drain-source short circuit to a.c., for specified drain-source voltage and drain current, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.2.8 Output power at specified input power (P_o)	+	+	+
Minimum and typical values under specified circuit and bias conditions			
or: power gain (G_p)	+	+	+

	TYPES		
	A	B	C
Minimum and typical values under specified circuit and bias conditions			
5.3.2.9 Where appropriate, overall efficiency (η_{tot})	+	+	+
Minimum and typical values under specified circuit and bias conditions			
NOTE $\eta_{tot} = \frac{P_{out}}{P_{in} + P_{(d.c.)}}$			
5.3.2.10 Alternatively, collector efficiency (η_d)	+	+	+
Minimum and typical values under specified circuit and bias conditions			
NOTE $\eta_d = \frac{P_{out}}{P_{d(d.c.)}}$			
5.3.2.11 Power added efficiency (η_{add})	+	+	+
Minimum and typical values under specified circuit and bias conditions			
NOTE $\eta_{add} = \frac{P_{out} - P_{in}}{P_{d(d.c.)}}$			
5.3.2.12 Noise figure (F)	+	+	+
Maximum value, under specified conditions of bias, source impedance, centre frequency and power bandwidth. These conditions must be those which provide the lowest value of the noise figure.			
5.3.2.13 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-a)}$) or ($R_{th(j-c)}$)		+	+
Maximum value.			
5.3.3 Characteristics for high and low power switching and chopper			
5.3.3.1 Gate cut-off current	+		
Gate leakage current		+	+
Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
Together with:			
Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.3.2 Drain cut-off current	+	+	+
Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one			

	TYPES		
	A	B	C
other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.3.3 Gate-source cut-off voltage (V_{GSoff}) Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	
5.3.3.4 Gate-source threshold voltage ($V_{GS(th)}$) Minimum and maximum values, at a specified high value of drain-source voltage and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate-voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			+
5.3.3.5 On-state characteristics			
5.3.3.5.1 Drain-source on-state voltage; ($V_{DS(on)}$) **Drain-source saturation voltage** Maximum value, at a specified large value of drain current and gate-source voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	+
or (for MOSFET only):			
5.3.3.5.2 Drain-source on-state resistance ($r_{DS(on)}$) Maximum value, at a specified large value of drain current and gate-source voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.		+	+
5.3.3.5.3 Short-circuit output conductance (g_{oss}) Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.	+	+	+
5.3.3.6 Short-circuit input capacitance (C_{iss}) Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the output short-circuited to a.c.	+	+	+
5.3.3.7 Short-circuit output capacitance (where appropriate) (C_{oss}) Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.	+	+	+
5.3.3.8 Reverse transfer capacitance (where appropriate) (C_{rss}) Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.	+	+	+

	TYPES		
	A	B	C
5.3.3.9 Switching times (see Figure 3)	+	+	+
They are stated under the following conditions:			
a) common-source configuration;			
b) specified condition in which output loading capacitance and resistance shall be included;			
c) input pulse transition times, amplitude and repetition frequency to be specified;			
d) $V_{GS(off\text{-}state)}$ must be greater than or equal to the maximum gate-source cut-off voltage for type A and B devices, or lower than the minimum gate-source threshold voltage for type C devices;			
e) $V_{GS(on\text{-}state)}$ must correspond to a high drain current;			
f)Maximum values of: $t_{d(on)}$, t_r, $t_{d(off)}$ and t_f separately.			
NOTE Where $t_{d(off)}$ is only a small fraction of the total turn-off time (t_{off}), a maximum value for t_{off} alone is adequate.			
5.3.3.10 Characteristics of the inverse diode (for power MOSFET) only			
5.3.3.10.1 Drain-source reverse voltage (~~V_{DSR}~~ V_{SD}) (Forward voltage of the inverse diode)		+	+
Maximum value at specified reverse drain current (~~I_{DR}~~ I_S) (forward current of the inverse diode) and at V_{GS} = 0.			
5.3.3.10.2 Forward recovery time (t_{fr}) (Reverse recovery time of the inverse diode)		+	+
Maximum value under specified conditions.			
5.3.3.10.3 Peak forward recovery current (~~I_{FRM}~~ I_{frm}) (Peak reverse recovery current of the inverse diode)		+	+
Maximum value under specified conditions.			
5.3.3.10.4 Forward recovery energy (E_{fr}) (reverse recovery energy of the inverse diode)		+	+
Maximum value under specified conditions.			
5.3.3.11 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j\text{-}a)}$) or ($R_{th(j\text{-}c)}$)		+	+
Maximum value.			
5.3.3.12 Drain cut-off current or drain-source off-state resistance	+	+	+
Maximum value of drain-source cut-off current (or alternatively, minimum value of drain-source off-state resistance), at specified low values of drain-source voltage for both polarities and at a specified gate-source voltage.			
5.3.3.13 Forward transconductance (g_{ms}, g_m, g_{fs}) (for power MOSFET only)		+	+
Minimum value, for specified drain-source voltage and drain current, at a temperature of 25 °C at one other higher temperature, preferably equal to the maximum virtual junction temperature.			

	TYPES		
	A	B	C
5.3.3.14 Breakdown voltage, drain to source ($V_{(BR)DSX}$) (for type B) Minimum value, at maximum off-state drain current I_{D0} and specified gate-source voltage.		+	
5.3.3.15 Breakdown voltage, drain to source ($V_{(BR)DSS}$) (for type C) Minimum value, at maximum off-state drain current I_{D0} and gate-source shorted.			+
5.3.3.16 Gate-source on-state voltage ($V_{GSM(on)}$) (for type B and C) Maximum value in the on-state		+	+
5.3.3.17 Internal gate resistance (r_g), where appropriate Maximum and/or typical value, under the electrical conditions specified and at specified frequency		+	+
5.3.3.18 Turn-on energy (per pulse) (E_{on}), where appropriate Maximum value under specified conditions: – drain-source voltage before turn-on; – drain peak current after turn-on; – gate-source voltage; – resistance in the gate-source circuit; – case or ambient temperature or virtual junction temperature.		+	+
5.3.3.19 Turn-off energy (per pulse) (E_{off}), where appropriate Maximum value under specified conditions: – drain peak current before turn-off; – drain-source voltage after turn-off; – gate-source voltage; – resistance in the gate-source circuit; – case or ambient temperature or virtual junction temperature.		+	+
5.3.3.20 Gate charges (Q_G, Q_{GD}, $Q_{GD(th)}$, $Q_{GS(pl)}$) Typical values at specified drain current (I_D), drain-source voltage (V_{DS}) and gate current (I_{GG}) (see Figure 1)		+	+
5.3.3.21 Thermal impedance channel-to-ambient or channel-to-case ($Z_{th(j-a)}$) or ($Z_{th(j-c)}$), where appropriate Maximum value.		+	+
5.3.4 Characteristics for low-level amplifier			
5.3.4.1 Gate cut-off current	+		
Gate leakage current Maximum value, at specified gate-source of drain-gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction		+	+

	TYPES		
	A	B	C
temperature. Together with: Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.4.2 Drain cut-off current Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	+
5.3.4.3 Drain current at zero gate-source voltage (I_{DSS}) Minimum and maximum values, at a specified drain-source voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	
5.3.4.4 Drain current at specified gate-source voltage (I_{DSX}) Minimum and maximum values, for specified gate-source and drain-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			+
5.3.4.5 Gate-source cut-off voltage (V_{GSoff}) Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	
5.3.4.6 Gate-source threshold voltage ($V_{GS(th)}$) Minimum and maximum values, at a specified high value of drain-source voltage and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			+
5.3.4.7 Noise voltage (where appropriate) (V_n) Maximum value in common-source configuration, under specified circuit conditions.	+	+	+
5.3.4.8 Small signal forward transconductance (g_{ms}, g_m, g_{fs}) Minimum value, for specified drain-source voltage and drain current, at an operating temperature of 25 °C and, where appropriate, at a specified higher temperature, at a specified frequency.	+	+	+
5.3.4.9 Characteristics of the inverse diode (where appropriate)			
5.3.4.9.1 Reverse drain current (~~I_{DR}~~ I_S) (forward current of the inverse diode)		+	+

	TYPES		
	A	B	C
Maximum value at specified Reverse drain current (~~I_{DR}~~ I_S) and at V_{GS} = 0.			
5.3.4.9.2 Forward recovery time (t_{fr}) (Reverse recovery time of the inverse diode)		+	+
Maximum value under specified conditions.			
5.3.4.10 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-a)}$) or ($R_{th(j-c)}$)		+	+
Maximum value.			
5.3.5 Characteristics for voltage-controlled resistor			
5.3.5.1 Gate cut-off current	+		
Gate leakage current		+	+
Maximum value, at specified gate-source or gate-drain voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.5.2 Small-signal drain-source resistance (r_{ds})	+	+	+
Minimum and maximum small-signal values, at zero drain-source voltage and at two or more specified gate-source voltages, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.5.3 Non-linearity distortion factor of drain-source small-signal resistance, where appropriate	+	+	+
Maximum value (total or individual harmonic contents), at specified drain-source and gate-source voltages and at specified drain-source a.c. signal, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.5.4 Temperature coefficient of the small-signal drain-source resistance	+	+	+
Typical value.			
5.3.5.5 Drain-source capacitance	+	+	+
Maximum small-signal value, at zero drain-source voltage, at a specified gate-source voltage, with the gate short-circuited for a.c. to the source.			
5.3.5.6 Drain-gate capacitance	+	+	+
Maximum small-signal value at zero drain-source voltage, at a specified gate-source voltage.			
5.3.5.7 Gate-source capacitance (where appropriate)	+	+	+
Maximum small-signal value at zero drain-source voltage, at a specified gate-source voltage, with the drain short-circuited for a.c. to the source.			
5.3.5.8 Forward transconductance (g_{ms}, g_m, g_{fs}) (for power MOSFET only)		+	+
Minimum value, for specified drain-source voltage and drain current, at a			

	TYPES		
	A	B	C
temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.5.9 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-a)}$) or ($R_{th(j-c)}$)		+	+
Maximum value.			
5.3.6 Specific characteristics of matched-pair field-effect transistors for low-frequency differential			
5.3.6.1 Difference of gate cut-off currents	+		
Difference of gate leakage currents ($I_{G1} - I_{G2}$)		+	+
Maximum absolute value, at specified drain-gate or drain-source voltage and drain current.			
5.3.6.2 Ratio of drain currents			
5.3.6.2.1 Ratio of drain currents for zero gate-source voltage (I_{DSS1} / I_{DSS2})	+	+	
Minimum value of the ratio of the drain currents, at a specified drain-source voltage and zero gate-source voltage.			
5.3.6.2.2 Ratio of drain currents for specified gate-source voltage			+
Minimum value of the ratio of the drain currents, at specified drain-source and gate-source voltages.			
NOTE This ratio should be stated as the smaller value divided by the larger value.			
5.3.6.3 Difference of small-signal common-source output conductances, where appropriate ($g_{os1} - g_{os2}$)	+	+	+
Maximum absolute value of the difference of the output conductances, at specified drain-gate or drain-source voltage, drain current, and frequency.			
5.3.6.4 Ratio of small-signal common-source forward transconductances ($g_{fs1} - g_{fs2}$)	+	+	+
Minimum value of the ratio of forward transconductances, at specified drain-gate or drain-source voltage, drain current, and frequency			
NOTE This ratio should be stated as the smaller value divided by the larger value.			
5.3.6.5 Difference of gate-source voltages ($V_{GS1} - V_{GS2}$)	+	+	+
Maximum absolute value of the difference of the gate-source voltages, at specified drain-gate or drain-source voltage and drain current.			
5.3.6.6 Change in difference of gate-source voltages between two temperatures ($\lvert\Delta(V_{GS1} - V_{GS2})\rvert_{\Delta T}$)	+	+	+
Maximum absolute value of the change of the difference of the gate-source voltages (as in 5.3.6.5) between two specified temperatures, at the same specified drain-gate or drain-source voltage and drain current.			

6 Measuring methods

6.1 General

The polarities of the power supplies, shown in the circuits in this standard, are applicable to N-channel type devices. However, the circuits can be adapted for P-channel type devices by changing the polarities of the meters and the power supplies.

The general precautions listed in Subclause 6.4 of IEC 60747-1:2006 apply. In addition, special care shall be taken to use low-ripple d.c. supplies and to decouple adequately all bias supply voltages at the frequency of measurement. For four-terminal devices, the fourth terminal shall be connected as specified.

When handling these devices, the handling precautions given in IEC 61340 shall be observed. The entire circuit in the following subclauses shall be placed inside an electrostatic screen.

6.2 Verification of ratings (limiting values)

After the following test, confirm the FET characteristics specified in Table 2.

Table 2 – Acceptance defining characteristics

Characteristics	Acceptance criteria
I_{GSS}	I_{GSS}< USL
I_{DS*}	I_{DS*} < USL
$V_{GS(th)}$ (or $V_{GS(off)}$)	$V_{GS(th)}$ < USL or $V_{GS(th)}$ >LSL
$V_{DS(on)}$	$V_{DS(on)}$ < USL
$r_{DS(on)}$	$r_{DS(on)}$ < USL (only for MOSFET)
USL: upper specified limit LSL: lower specified limit	

6.2.1 Voltages and currents

6.2.1.1 Drain-source voltage (d.c.) (V_{DS*})

NOTE * = O, R, S or X.

– **Purpose**

To verify the drain-source voltage (d.c.) V_{DS*} under specified conditions.

– **Circuit diagram**

See Figure 4 below.

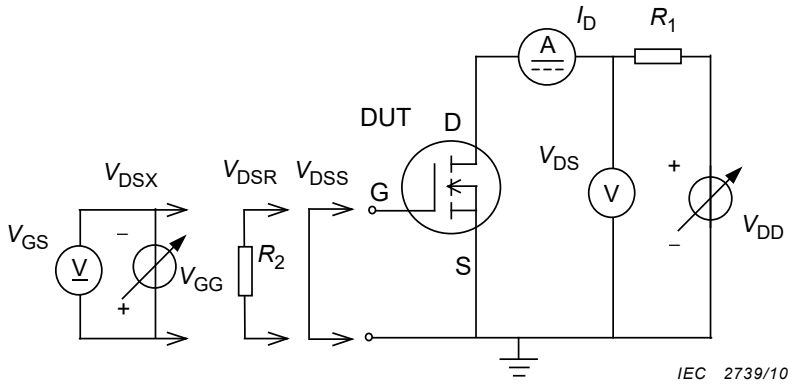


Figure 4 – Circuit diagram for testing of drain-source voltage

– **Circuit description and requirements**

V_{DD} and V_{GG} are the d.c. voltage supply. R_1 is a circuit protection resistor.

– **Testing procedure**

The gate-source is set to specified conditions. V_{DD} is increased until drain-source voltage measured on voltmeter V_{DS} reaches the specified drain-source voltage (d.c.) V_{DS*}. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Gate-source bias conditions
- Drain-source voltage: rated drain-source voltage

6.2.1.2 Gate-source (d.c.) voltage (V_{GS*})

– **Purpose**

To verify the gate-source (d.c.) voltage for both polarities, under specified conditions.

– **Circuit diagram**

See Figure 5 below.

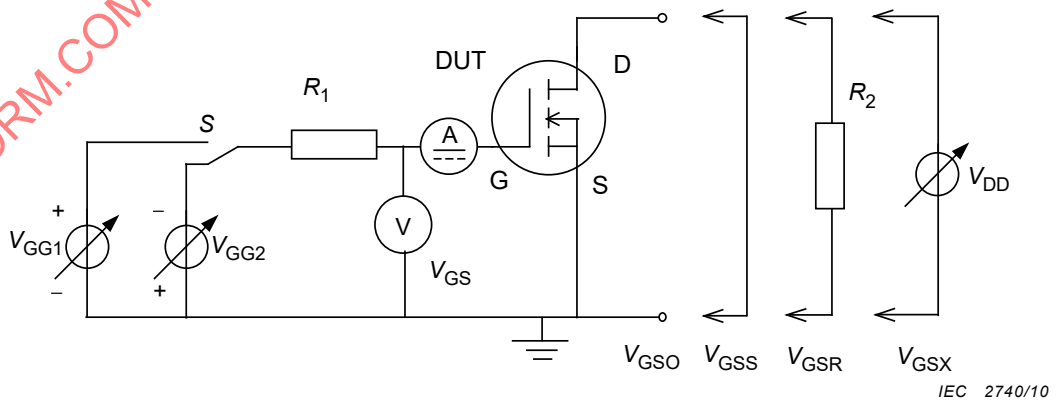


Figure 5 – Circuit diagram for testing of gate-source voltage

– **Circuit description and requirements**

V_{DD}, V_{GG1} and V_{GG2} are the d.c. voltage supply. V_{GSX} is applied only for gate reverse biased condition of V_{GG2}. R_1 is a protective resistor.

– **Testing procedure**

Drain-source voltage is set to specified conditions. V_{GG} is increased until gate-source voltage measured on voltmeter V_{GS} reaches the specified gate-source voltage V_{GS*}. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Reference point or junction temperature T_{vj};
- Drain-source bias conditions;
- Gate-source voltage: rated gate-source voltage.

6.2.1.3 Gate-drain (d.c.) voltage (V_{GD*})

– **Purpose**

To verify the gate-drain (d.c.) voltage for both polarities, under specified conditions.

– **Circuit diagram**

See Figure 6 below.

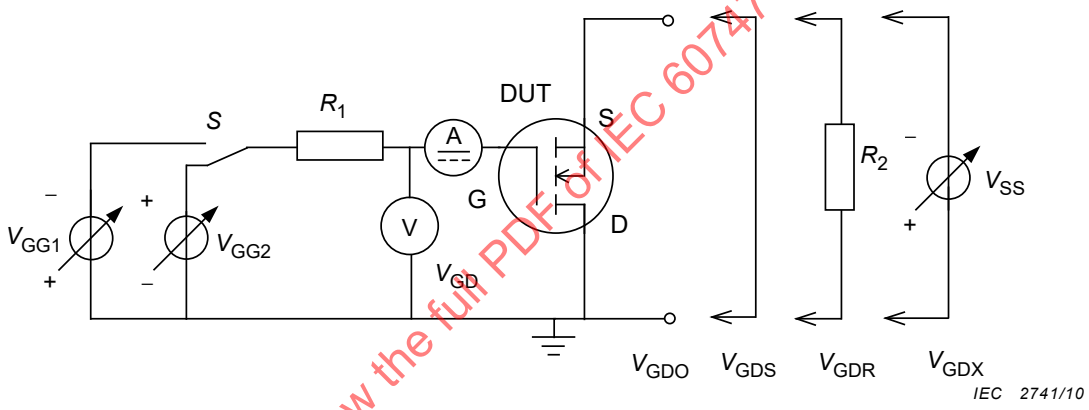


Figure 6 – Circuit diagram for testing of gate-drain voltage

– **Circuit description and requirements**

V_{SS}, V_{GG1} and V_{GG2} are the d.c. voltage supply. V_{GDX} is applied only for gate reverse biased condition of V_{GG2}.

– **Testing procedure**

Source-drain voltage is set to specified conditions. V_{GD} is increased until gate-drain voltage measured on voltmeter V_{DS} reaches the specified gate-drain voltage V_{GD*}. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Reference point or junction temperature T_{vj};
- Drain-source bias conditions;
- Gate-drain voltage: rated gate-drain voltage.

6.2.1.4 Drain current (I_D)

– **Purpose**

To verify that drain current capability of FETs is not less than the maximum rated value I_D under specified conditions.

– **Circuit diagram**

See Figure 7 below.

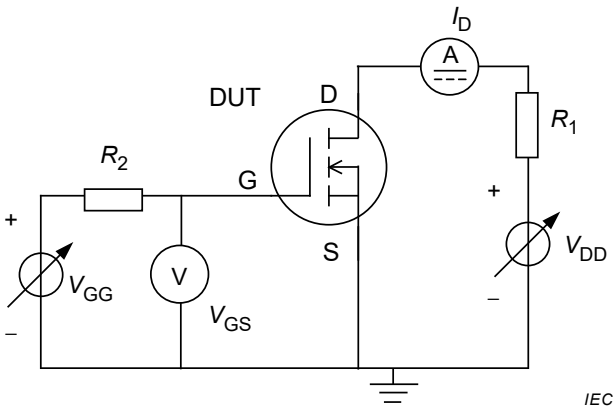


Figure 7 – Basic circuit for the testing of drain current

– **Circuit description and requirements**

V_{DD} and V_{GG} are the d.c. voltage supply. R_1 and R_2 are protective resistors.

– **Testing procedure**

Specified gate-source voltage is applied to the gate. Temperature (T_a or T_c or T_{vj}) and gate-source voltage are set and kept to the specified value. Drain current is supplied at specified conditions. After the above test, confirm the reference-defining characteristics of DUT being normal by the criteria of Table 2. Drain current is supplied at specified conditions until thermal equilibrium is reached.

– **Specified conditions**

- Reference point or junction temperature $T_{vj;}$
- Gate-source voltage V_{GS}.
- Drain current I_D.

6.2.1.5 Peak drain current (I_{DM})

– **Purpose**

To verify the peak drain current under specified conditions.

– **Circuit diagram**

See Figure 8 below.

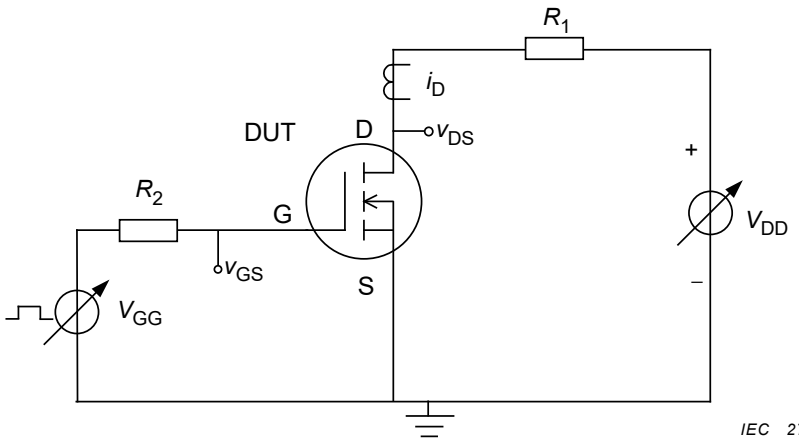


Figure 8 – Circuit diagram for testing of peak drain current

– **Circuit description and requirements**

V_{DD} is the d.c. voltage supply and V_{GG} is the gate pulse generator. R_1 and R_2 are protective resistors.

– **Testing procedure**

A specified gate-source voltage pulse is applied to turn the device on and off. Temperature (T_a or T_c or T_{vj}) is set and kept to the specified value. Peak drain current is conducted at the specified conditions. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Gate-source voltage V_{GS}
- Pulse width and duty cycle
- Peak drain current I_{DM}

6.2.1.6 Reverse drain current (~~I_{DRS}~~ I_{SS}) or (~~I_{DRX}~~ I_{SX})

– **Purpose**

To verify the reverse drain current under specified conditions.

– **Circuit diagram**

See Figure 9 below.

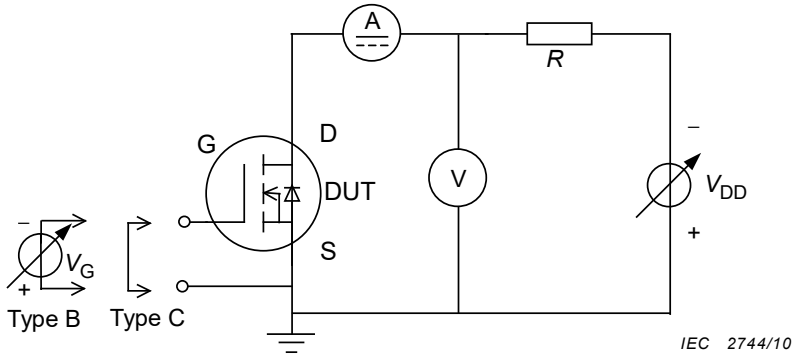


Figure 9 – Basic circuit for the testing of reverse drain current of MOSFETs

– **Circuit description and requirements**

V_{DD} is the d.c. voltage supply. R is a protective resistor.

– **Testing procedure**

Gate-source terminals are shorted (C-type) or supplied with an off-bias (B-type). Temperature (T_a or T_c or T_{vj}) is set and kept to the specified value under specified conditions. Reverse drain current is conducted to DUT with MOSFET in off-state. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- MOSFET in off-state: the gate condition of B type is set to be kept in the off-state.
- Reference point or junction temperature T_{vj}
- Protective resistor R
- Reverse drain current ~~I_{DR}~~ I_S

6.2.1.7 Peak reverse drain current (~~I_{DRM}~~ I_{SM})

– **Purpose**

To verify peak reverse drain current under specified conditions.

– **Circuit diagram**

See Figure 10 below.

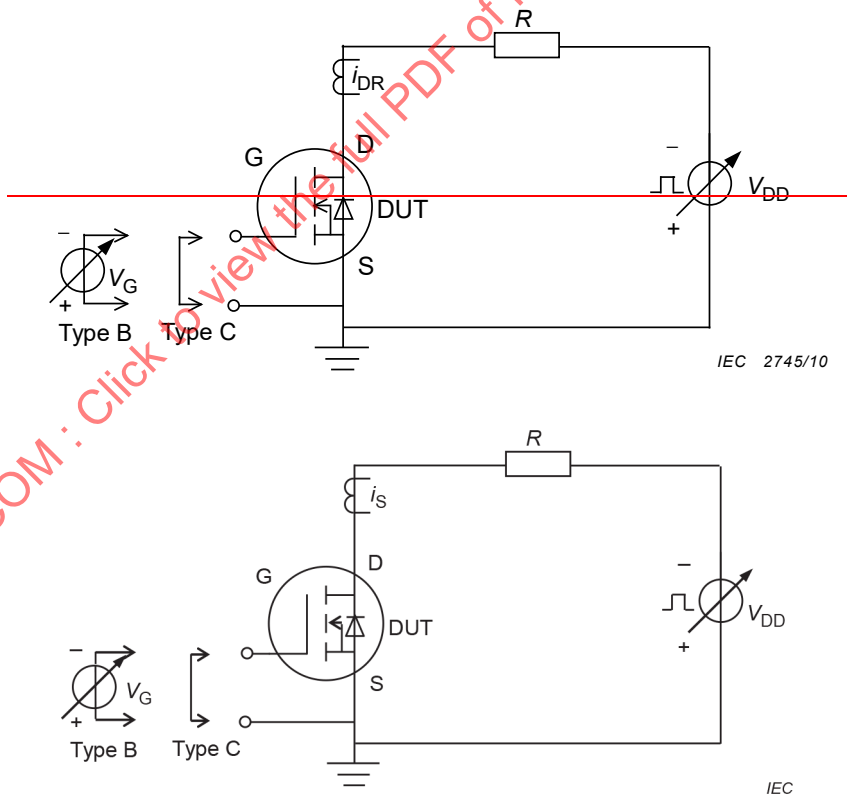


Figure 10 – Basic circuit for the testing of peak reverse drain current of MOSFETs

– **Circuit description and requirements**

V_{DD} is a pulse voltage source with adjustable pulse width and duty cycle control. R is a protective resistor.

– **Testing procedure**

Gate-source terminals are connected as specified. The temperature (T_a or T_c or T_{vj}) is set and kept to the specified value. Peak reverse drain current is conducted to DUT by turning on the V_{DD} with MOSFET in off-state. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- MOSFET in off-state
- Reference point or junction temperature T_{vj}
- Pulse width and duty cycle; setting up by the pulse switching unit
- Peak reverse drain current ~~I_{DRM}~~ I_{SM}

6.2.2 Safe operating area

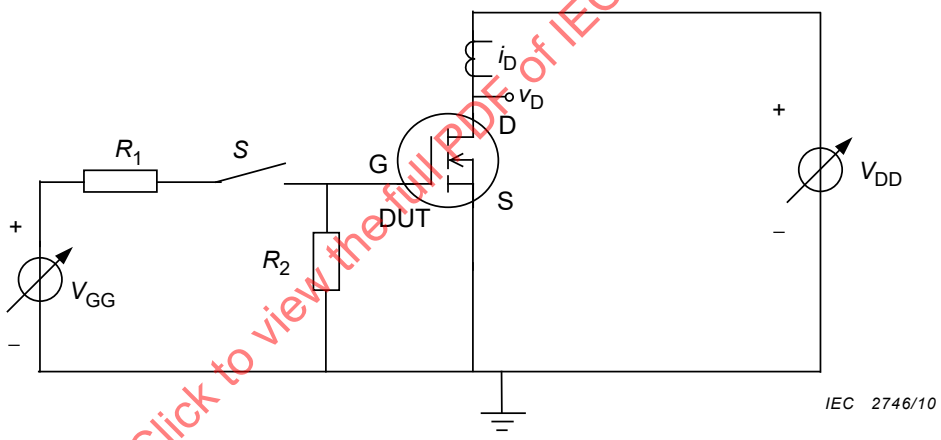
6.2.2.1 Forward-bias safe operating area (FBSOA)

– **Purpose**

To verify the forward-bias safe operating area of a case-rated power field-effect transistor under specified conditions with non-inductive load.

– **Circuit diagram**

See Figure 11 below.



DUT = transistor being measured (MOSFET or JFET)

Figure 11 – Circuit diagram for verifying FBSOA

– **Circuit description and requirements**

V_{GG}, V_{DD} = adjustable voltage sources

R_1, R_2 = 10 kΩ or as specified

S = switch to obtain the specified sequence of current pulse

– **Testing procedure**

The case temperature is set to the specified value. The device is switched on and off with the specified pulse duration and duty cycle. V_{DS} and I_D are monitored. V_{GG} and/or V_{DD} are increased until the specified pulse values for V_{DS} and I_D are reached. Under these operating conditions, the device being measured is operated for the specified duration of the test, or for the specified number of pulses, as appropriate. Verification of the FBSOA rating is obtained from the post-test measurements. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Case temperature T_c
- Drain-source voltage V_{DS}
- Drain current I_D
- As specified, either d.c. operation or repetitive pulse operation, or a combination of these conditions
- Pulse duration t_p and duty factor δ as appropriate
- As specified, either duration of the test or number of test pulses
- R_1, R_2 if other than 10 kΩ
- Post-test measurement limits

6.2.2.2 Reverse-bias safe operation area (RBSOA)

– **Purpose**

To verify the reverse-bias safe operation area under specified conditions with inductive load.

– **Circuit diagram and test waveforms**

See Figure 12 and Figure 13 below.

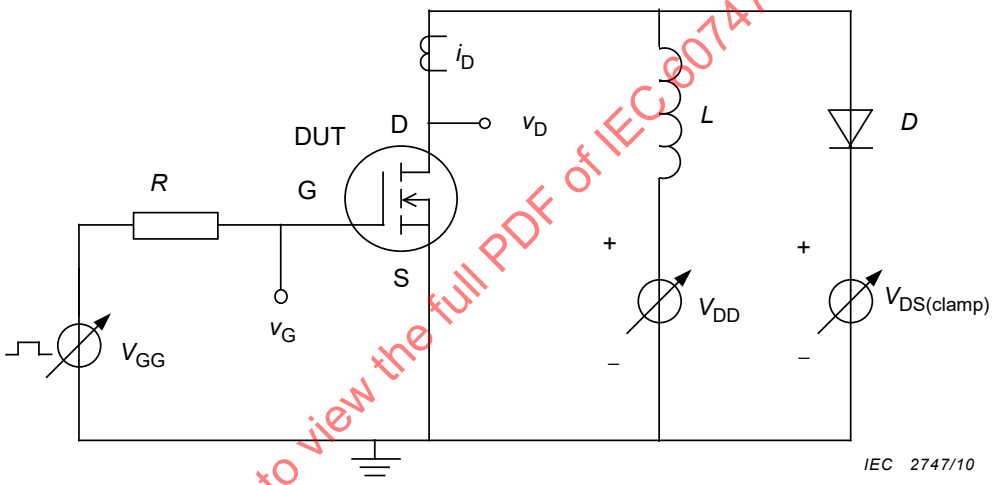


Figure 12 – Circuit diagram for verifying RBSOA

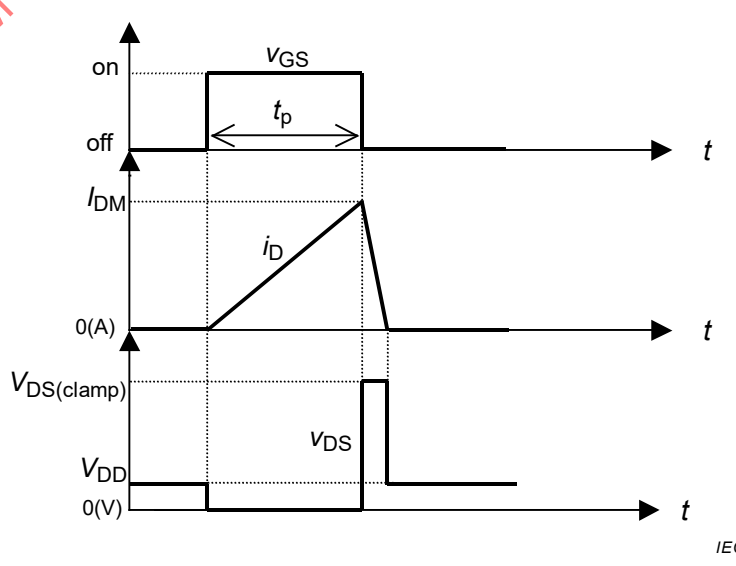


Figure 13 – Test waveforms for verifying RBSOA

– **Circuit description and requirements**

D = clamping diode

L = inductive load

V_{DD} = adjustable voltage sources

$V_{DS(clamp)}$ =adjustable voltage source for the clamping voltage

t_p = gate-source voltage pulse width

V_{GG} = gate pulse generator

R = gate resistor

– **Testing procedure**

~~DUT is turned off at specified I_D. V_{DS} and I_S (I_D) are monitored. The DUT has to turn off I_D and withstand $V_{DS} = V_{DS(clamp)}$.~~

DUT is turned off at specified I_D and V_{DS}. I_D and V_{DS} are monitored. The DUT has to turn off I_D and withstand $V_{DS} = V_{DS(clamp)}$.

NOTE Drain-source peak voltage $V_{DSM} < V_{(BR)DS*}$.

The temperature (*reference point temperature* or T_{vj}) is set and kept to a specified value. Under these operating conditions, DUT is operated for the specified duration of the test, or for the specified number of pulses, as appropriate. Verification of the RBSOA rating is obtained from the post-test measurements. After the above test, confirm the acceptance defining characteristics of DUT being normal by the criteria of Table 2. The device is considered defective if, at any instant during the test, the drain-source voltage collapses or oscillates during the fall of the current pulses.

– **Specified conditions**

- Drain current I_D
- Gate reverse voltage $-V_{GS}$ before and after turn-off
- Drain-source voltage $V_{DS(clamp)}$
- Number of pulses, if greater than one, and pulse width and duty cycle
- Inductance L
- Reference point or virtual junction temperature T_{vj}

– Gate resistor R_G

6.2.2.3 Short-circuit safe operating area (SCSOA)

– **Purpose**

This test is to verify that the MOSFET operates reliably without failure under load-shorted conditions. A short-circuit can occur when the MOSFET is already conducting, or the MOSFET is turned into a short-circuit condition. A test for the latter case is described in the following.

– **Circuit diagram and waveforms**

See Figure 14 and Figure 15 below.

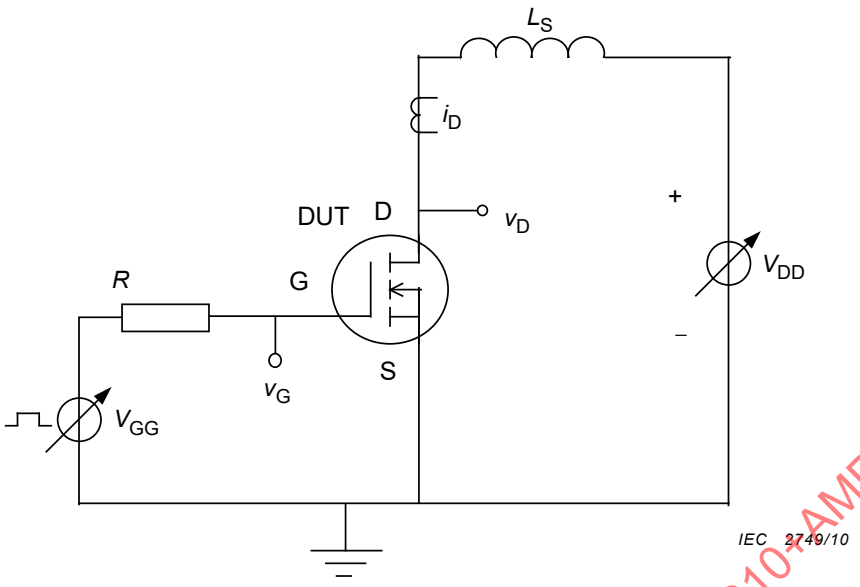


Figure 14 – Circuit for testing safe operating pulse duration at load short circuit

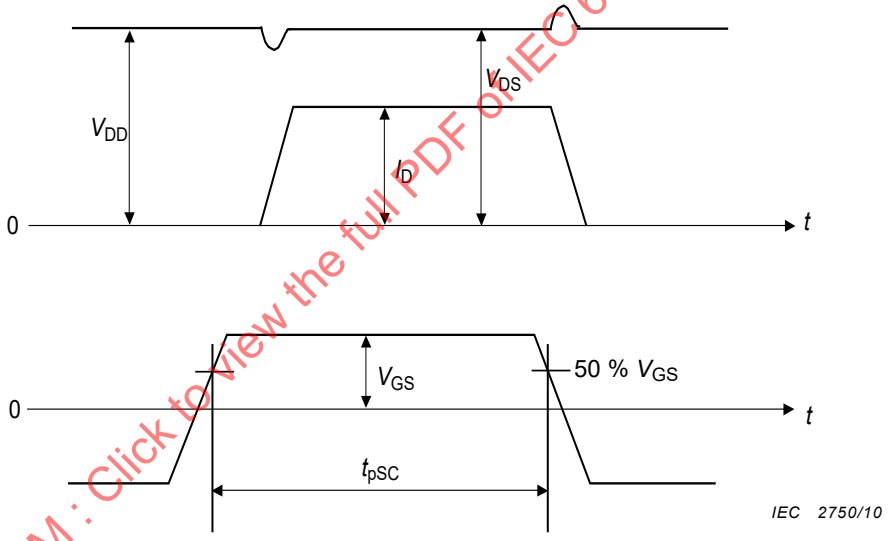


Figure 15 – Waveforms of gate-source voltage V_{GS}, drain current I_D and voltage V_{DS} during load short circuit condition SCSOA

– **Circuit descriptions and requirements**

L_S represents the maximum permitted stray inductance; it must be low enough to ensure that the maximum short circuit current is reached within the first 25% of the gate pulse duration t_{pSC}.

L_S = stray inductance

V_{DD} = adjustable voltage sources

t_{pSC} = gate-source voltage pulse width

V_{GG} = gate pulse generator

R = gate resistor as specified

– **Testing procedure**

Temperature is set to the specified value. Gate-source voltage V_{GS} and pulse duration is set to specified values. Drain-source voltage V_{DS} is set to a specified value. The drain currents I_D and V_{DS} are monitored in order to see whether the MOSFET turns on and turns off correctly. After the above test, confirm the acceptance defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Drain-source voltage $V_{DS} = V_{DD}$
- On and off-state gate source voltages
- Gate pulse duration t_{pSC}
- Gate resistor R
- Value of stray inductance L_S
- Reference point or virtual junction temperature T_{vj}

6.2.3 Avalanche energy

6.2.3.1 Repetitive avalanche energy (E_{AR})

– **Purpose**

To verify the repetitive avalanche energy capability in an unclamped inductive switching circuit.

– **Circuit diagram and waveforms**

See Figure 16 and Figure 17 below.

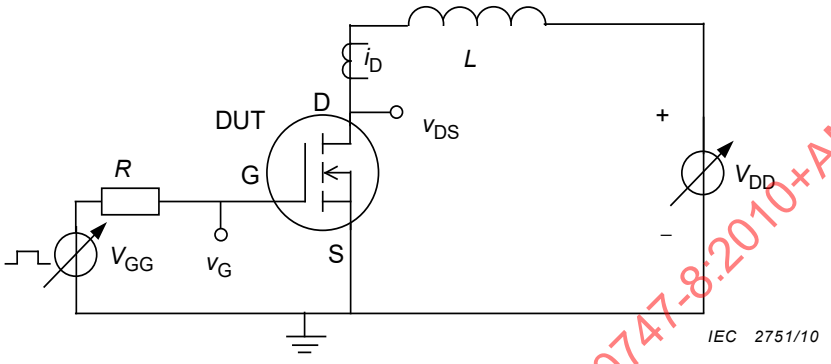


Figure 16 – Circuit for the inductive avalanche switching

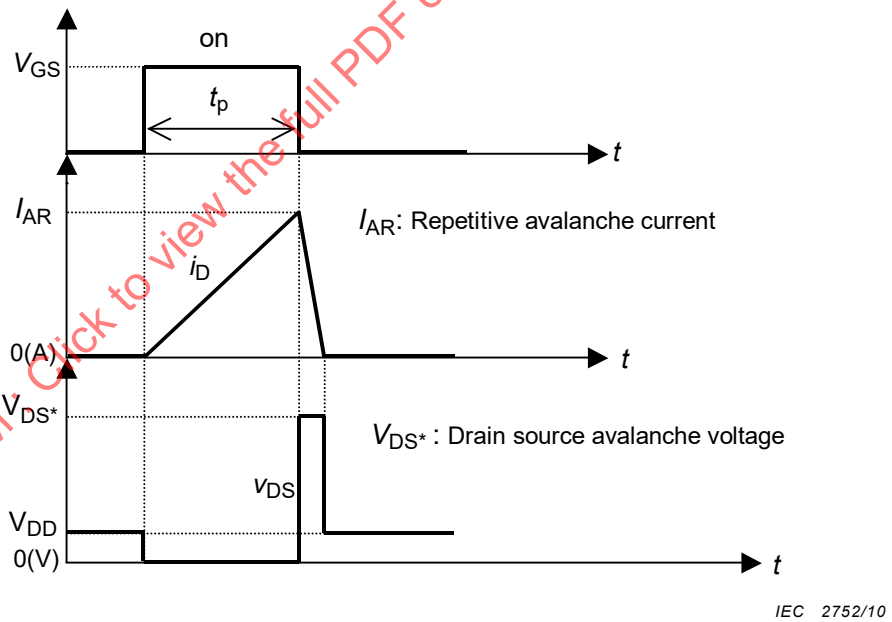


Figure 17 – Waveforms of I_D, V_{DS} and V_{GS} during unclamped inductive switching

– **Circuit descriptions and requirements**

L = inductive load

V_{DD} = adjustable voltage sources

V_{GG} = gate pulse generator

R = gate resistor as specified

– **Test procedure**

Temperature is set to the specified value. The supply voltage (V_{DD}) is set to the specified value. The turn-on time of the MOSFET is adjusted in such a way that the specified avalanche current is reached. Under these operating conditions, the DUT is operated with the specified number of pulses and repetition rate. The energy delivered to the DUT can be calculated as follows:

$$E_{AR} = ½\ L\ I_{AR}^2\ V_{DS*} / (V_{DS*} - V_{DD})$$

After the above test, confirm the acceptance defining characteristics of DUT are normal by the criteria of Table 2. DUT shall be within all specified parameter limits at the completion of the test. The measured value of V_{DS*} shall be greater than or equal to the minimum breakdown voltage $V_{(BR)DS*}$ with the permitted avalanche currents I_{AR}.

NOTE When V_{DD} is set to a smaller value compared with V_{DS*}, E_{AR} is calculated by using the approximate equation of $E_{AR} = ½\ L\ I_{AR}^2$.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DD}
- Gate-source voltage V_{GS}
- Drain current I_D
- Inductance L
- Frequency f

6.2.3.2 Non-repetitive avalanche switching energy (E_{AS})

– **Purpose**

To verify the non-repetitive avalanche switching energy.

– **Circuit diagram and waveforms**

See Figure 18 below.

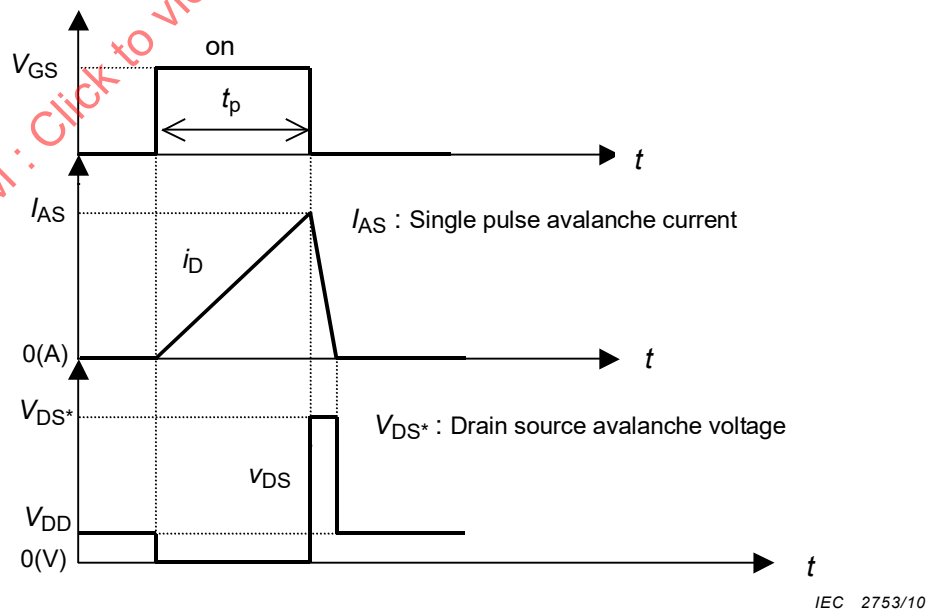


Figure 18 – Waveforms of I_D, V_{DS} and V_{GS} for the non-repetitive avalanche switching

– **Circuit descriptions and requirements**

L = inductive load

V_{DD} = adjustable voltage sources

V_{GG} = gate pulse generator

R_G = gate resistor as specified

– **Testing procedure**

Temperature is set to the specified value. The supply voltage (V_{DD}) is set to the specified value. The turn-on time of the MOSFET is adjusted in such a way that the specified avalanche current is reached. Under these operating conditions, the DUT is operated with the single pulse. The energy delivered to the DUT can be calculated as follows:

$$E_{AS} = ½\ L\ I_{AS}^2\ V_{DS*} / (V_{DS*} - V_{DD})$$

After the above test, confirm the acceptance defining characteristics of DUT are normal by the criteria of Table 2. DUT shall be within all specified parameter limits at the completion of the test. The measured value of V_{DS*} shall be greater than or equal to the minimum breakdown voltage $V_{(BR)DS*}$ with the permitted avalanche currents I_{AS}.

NOTE When V_{DD} is set to a smaller value compared with V_{DS*}, E_{AS} is calculated by using the approximate equation of $E_{AS} = ½\ L\ I_{AS}^2$.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DD}
- Gate-source voltage V_{GS}
- Drain current I_D
- Inductance L
- Single pulse

6.3 Methods of measurement

6.3.1 Breakdown voltage, drain to source ($V_{(BR)DS*}$)

– **Purpose**

To measure the drain to source breakdown voltage under specified conditions.

– **Circuit diagram**

See Figure 19 below.

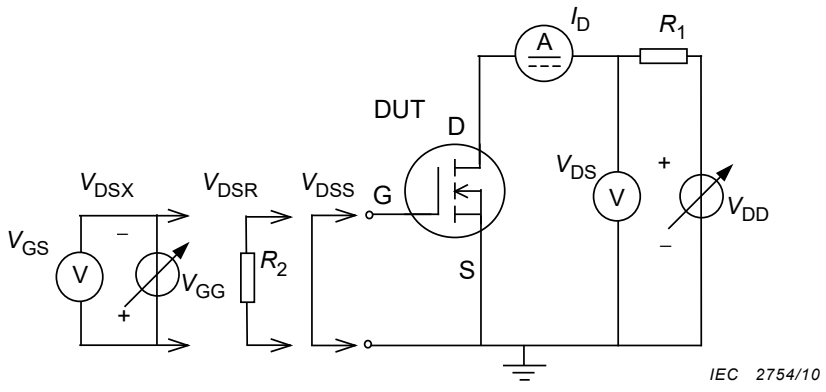


Figure 19 – Circuit diagrams for the measurement drain-source breakdown voltage

– **Circuit description and requirements**

V_{DD} and V_{GG} are the d.c. voltage supply. R_1 is a circuit protection resistor.

– **Measurement procedure**

The gate-source is set to specified conditions. V_{DD} is increased until the drain off-state current measured by ammeter A reaches the specified value I_{DS}. The breakdown voltage is measured on the voltmeter V_{DS}.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Gate-source bias conditions

SX : gate-source voltage is applied;

SR : the resistance is connected between gate and source (R_2 value);

SS : gate-source is shorted;

- Maximum drain off-state current $I_{DS*,max}$

6.3.2 Gate-source off-state voltage ($V_{GS(off)}$) (type A and B), gate source threshold voltage ($V_{GS(th)}$) (type C)

– **Purpose**

To measure the gate-source off-state voltage, under specified conditions.

– **Circuit diagram**

See Figure 20 below.

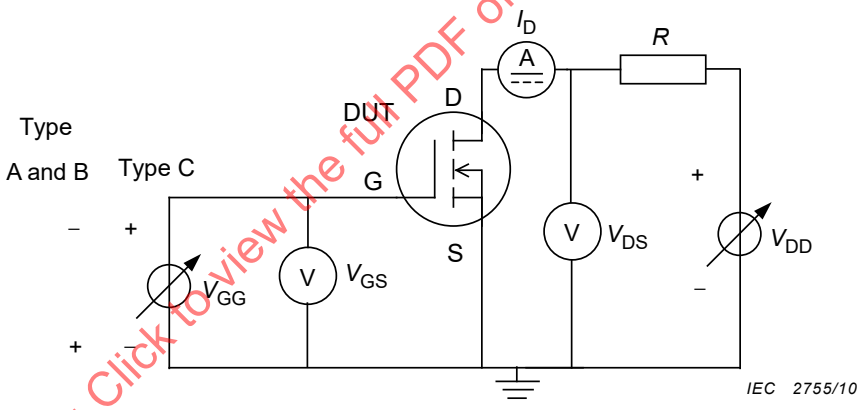


Figure 20 – Circuit diagram for measurement of gate-source off-state voltage and gate-source threshold voltage

– **Circuit description and requirements**

V_{DD} and V_{GG} are the d.c. voltage supply. R is a circuit protection resistor.

– **Measurement procedure**

The specified drain-source voltage is applied. The gate source voltage is adjusted to the value at which the drain current equals the specified value. The voltage measured by V_{GS} is the gate-source off-state voltage (type A and B) respectively the gate-source threshold voltage (type C).

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DS}
- Drain current I_D

6.3.3 Drain leakage current (d.c.) (I_{DS*})(type C), Drain cut-off current (d.c.) (I_{DSX}) (type A and B)

– **Purpose**

To measure the drain leakage (or off-state) current (d.c.) I_{DS*} under specified conditions or the drain cut-off current (d.c.) I_{DSX} under the gate-source voltage.

NOTE * = R, S or X.

– **Circuit diagram**

See Figure 21 below.

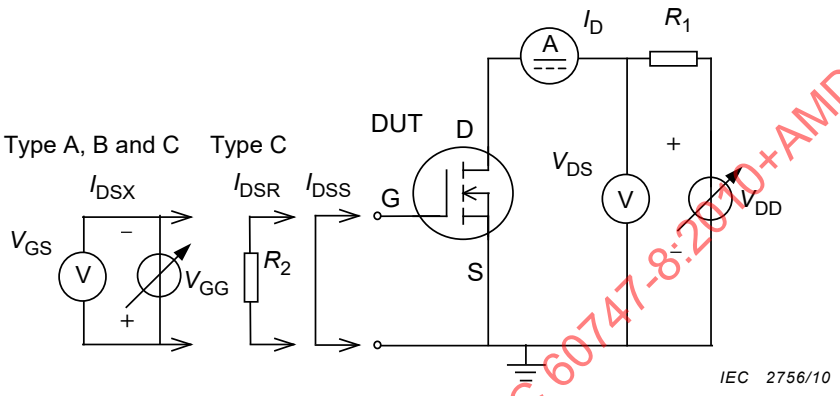


Figure 21 – Circuit diagram for drain leakage (or off-state) current or drain cut-off current measurement

– **Circuit description and requirements**

V_{DS} and V_{GG} are the d.c. voltage supply. R_1 is a circuit protection resistor.

– **Measurement procedure**

The gate-source is set to the specified bias conditions. V_{DD} is increased until the drain-source voltage measured by voltmeter V_{DS} reaches the specified value. The drain leakage (or off-state) current I_D is measured on the ammeter. If required, $r_{DS(off)}$ is calculated from the formula $r_{DS(off)} = V_{DS}/I_{Dx}$.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Gate-source bias conditions

$_{SX}$: gate-source voltage is applied;

$_{SR}$: the resistance is connected between gate and source (R_2 value);

$_{SS}$: gate-source is shorted;

- Drain-source voltage: the value is not greater than the breakdown voltage

6.3.4 Gate cut-off current (I_{GS*})(type A), Gate-leakage current (I_{GS*})(type B and C)

– **Purpose**

To measure the gate cut-off current or gate leakage current under specified conditions.

– **Circuit diagram**

See Figure 22 below.

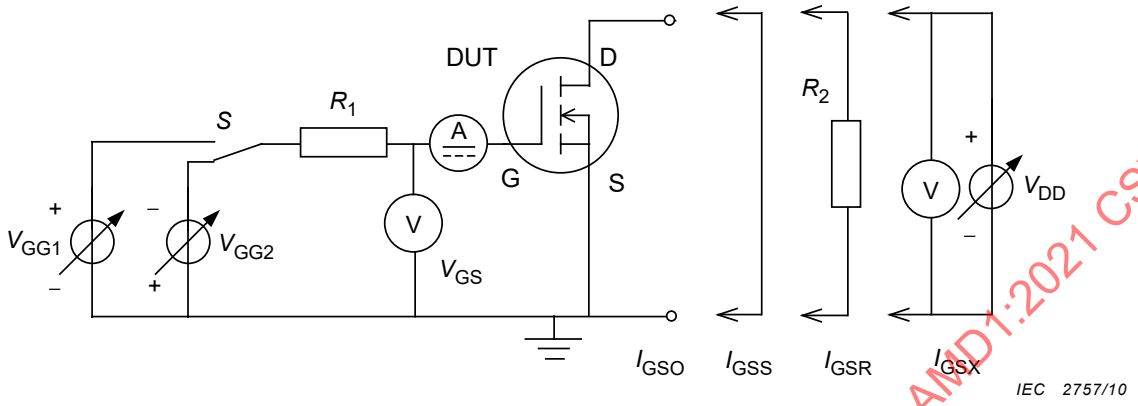


Figure 22 – Circuit diagram for measuring of gate cut-off current or gate leakage current

– **Circuit description and requirements**

The entire circuit shall be placed inside an electrostatic screen. The voltage drop of the ammeter A to depend on the internal resistance and the value of I_{GS} shall be smaller than 1 % of the value of V_{GS}.

– **Measurement procedure**

Set the drain-source to the specified bias conditions. Increase V_{GG} until gate-source voltage measured on voltmeter V_{GS} reaches the specified gate-source voltage V_{GS*}. The gate cut-off current or gate leakage current is measured on ammeter A.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source bias conditions
- I_{GSX} conditions in case of type B and C are applied just for reverse biased V_{GG2}
- Gate-source voltage: Type A is applied just for reverse biased V_{GG2}

6.3.5 (Static) drain-source on-state resistance ($r_{DS(on)}$) or drain-source on-state voltage ($V_{DS(on)}$)

– **Purpose**

To measure drain-source on-state resistance or drain-source on-state voltage under specified negligible dissipation conditions.

– **Circuit diagram**

See Figure 23 below.

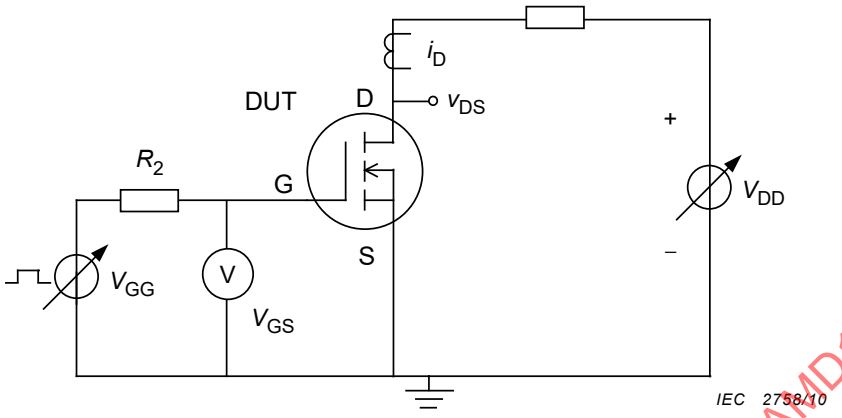


Figure 23 – Basic circuit of measurement for on-state resistance

– **Circuit description and requirements**

V_{GG} is a gate pulse generator. V_{DD} is a variable voltage source to supply the drain-source current. R_1 is a protective resistor.

– **Measurement procedure**

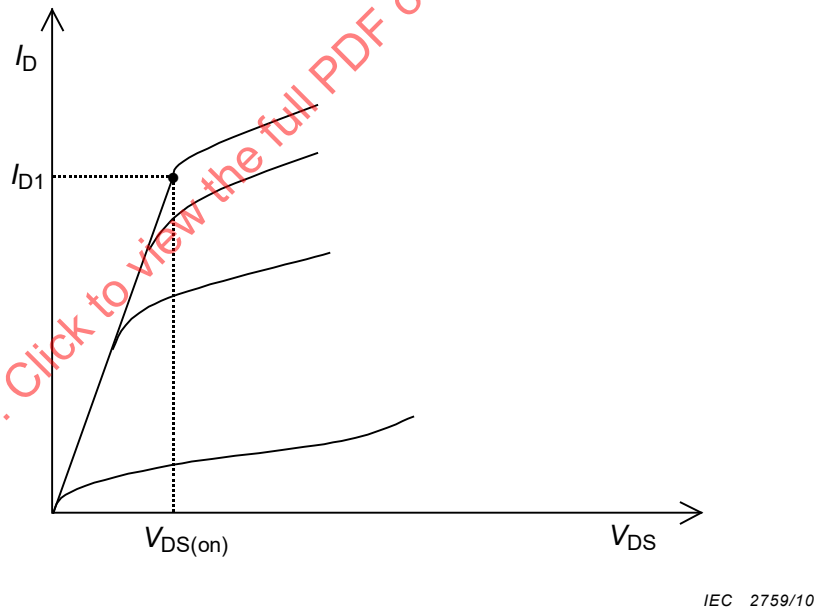


Figure 24 – On-state resistance

Adjust the temperature to the specified value. Set the V_{GS} to the specified value. Apply a drain current I_D pulse in the range of the linear part of the on-state drain current–voltage curve (see Figure 25). Measure the values of I_{D1} and $V_{DS(on)}$. Calculate $r_{DS(on)}$ from the formula $r_{DS(on)} = V_{DS(on)}/I_{D1}$.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage or drain current
- Gate-source voltage

6.3.6 Switching times ($t_{d(on)}$, t_r, $t_{d(off)}$, and t_f)

– **Purpose**

To measure the switching time during turn-on and turn-off under specified conditions.

– **Circuit diagram and waveforms**

See Figure 25 and Figure 26 below.

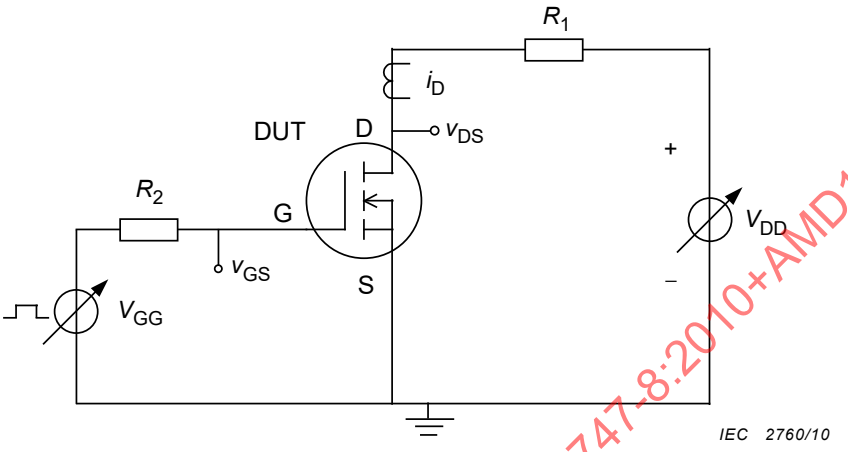


Figure 25 – Circuit diagram for switching time

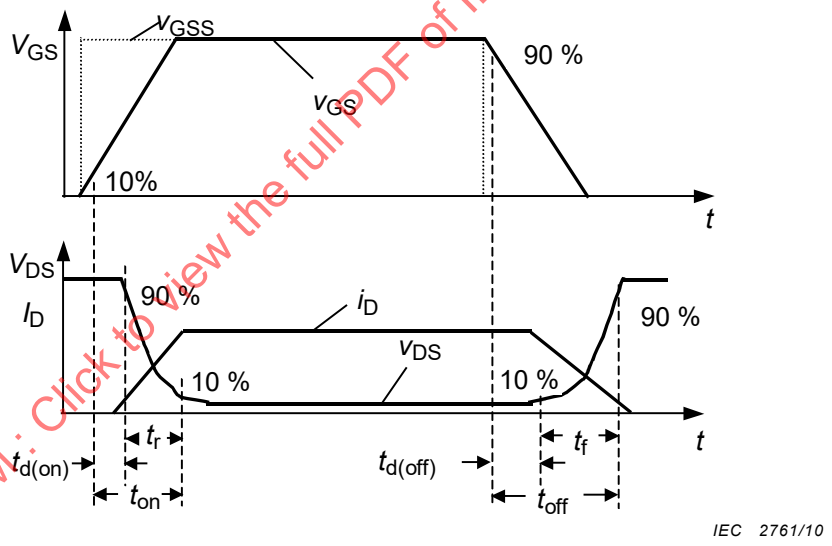


Figure 26 – Schematic switching waveforms and times

– **Circuit description and requirements**

V_{GG} is a generator for rectangular pulses having an internal resistance that is small compared to the gate resistance R_2. The rise time and the fall time of the pulses at the generator output shall be smaller than the switching time of the DUT. R_1 is a load resistor. In the practical layout, parasitic stray inductance shall be minimized. Unless otherwise specified, the common-source configuration is used.

– **Measurement procedure**

The gate voltage pulse amplitude V_{GG} and the drain-source supply voltage V_{DD} are set to the specified values. R_1 is adjusted to set the specified drain current I_D. The waveforms of the

drain-source voltage v_{DS} and the gate-source voltage v_{GS} are monitored and the turn-on and the turn-off times are measured in accordance with Figure 26.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain -source voltage V_{DS}
- Pulse shape of gate source voltage V_{GS} after turn-on and turn-off:
- Gate pulse width, pulse rise and pulse fall times, repetition rate
- Resistor R_1, R_2
- Drain current I_D

6.3.7 Turn-on power dissipation (P_{on}), turn-on energy (per pulse) (E_{on})

– **Purpose**

To measure the turn-on power dissipation and / or the turn-on energy per pulse of the DUT under specified conditions at inductive load.

– **Circuit diagram**

See Figure 27 below.

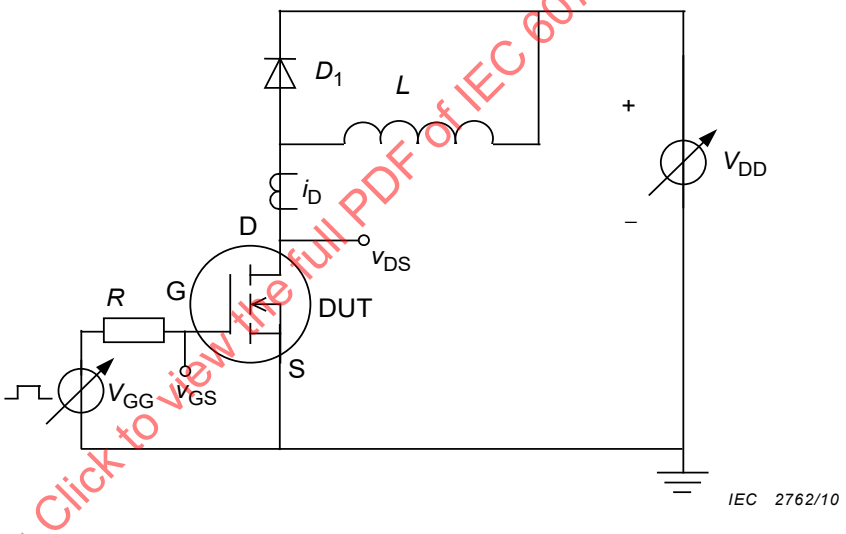


Figure 27 – Circuit for determining the turn-on and turn-off power dissipation and/or energy

– **Circuit description and requirements**

V_{GG} is a generator for rectangular pulses having an internal resistance that is small compared to the gate resistance R. The rise time of the pulses at the generator output shall be smaller than the switching time of the DUT. D_1 is a specified free-wheeling diode and L is a load inductance. In the practical layout, parasitic stray inductance shall be minimized.

– **Measurement procedure**

The gate voltage pulse amplitude V_{GG} and the drain-source supply voltage V_{DD} are set to the specified values. The waveforms of the drain current I_D and the drain-source voltage V_{DS} are monitored. The turn-on energy per pulse is then the integral of the product of the two magnitudes over the time. The turn-on power dissipation at any repetition frequency is the product of this frequency and the turn-on energy per pulse as determined by the integration (see 3.3.21).

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage before turn-on V_{DS}
- Drain current I_D after turn-on
- Gate resistor R
- Gate-source voltage pulse shape: amplitude, rise time, duration
- Characteristics of free wheeling diode D_1 (type number of free-wheeling diode)

6.3.8 Turn-off power dissipation (P_{off}), turn-off energy (per pulse) (E_{off})

– **Purpose**

To measure the turn-off power dissipation and / or the turn-off energy per pulse of the DUT under specified conditions at inductive load.

– **Circuit diagram**

See Figure 27 above.

– **Circuit description and requirements**

V_{GG} is a generator for rectangular pulses having an internal resistance that is small compared to the gate resistance R. The rise time and the fall time of the pulses at the generator output shall be smaller than the switching time of the DUT. D_1 is a specified free-wheeling diode and L is a load inductance. In the practical layout, parasitic inductance shall be minimized.

– **Measurement procedure**

The gate voltage amplitude V_{GG} and the drain-source supply voltage V_{DD} are set to the specified values. The waveforms of drain current I_D and drain-source voltage V_{DS} are monitored as shown in Figure 2. The turn-off energy per pulse is then the integral of the product of the two magnitudes over the time. The turn-off power dissipation at any repetition frequency is the product of this frequency and the turn-off energy per pulse as determined by the integration (see 3.3.22).

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain peak current I_D before turn-off
- Drain-source voltage V_{DS} after turn-off
- Load inductance L
- Resistor R in the gate-source circuit
- Gate voltage pulse: amplitude, rise time, duration

6.3.9 Gate charges (Q_G, Q_{GD}, $Q_{GS(th)}$, $Q_{GS(pl)}$)

– **Purpose**

To measure gate charges of the DUT under specified conditions.

– **Circuit diagram**

See Figure 28 below.

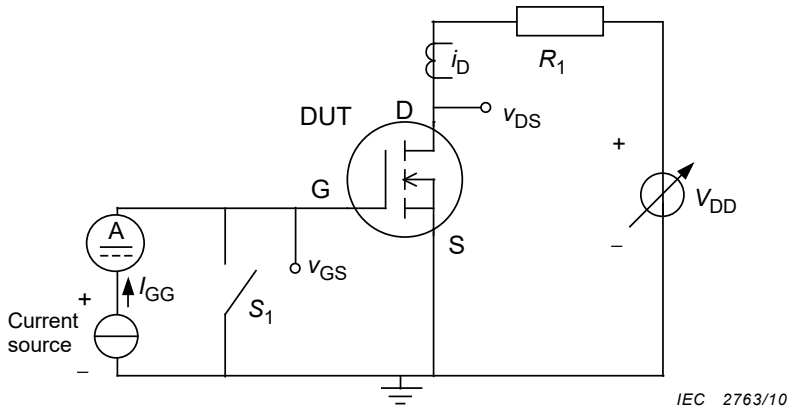


Figure 28 – Circuit diagrams for the measurement gate charges

– **Circuit description and requirements**

I_{GG} is a constant current source. S_1 is a switch to control the time of gate current pulse width. R_1 is a load resistor to limit the drain current.

– **Measurement procedure**

The waveforms are shown in Figure 1. Switch S_1 is opened at t_0 and the gate is fed with a constant current until a specified gate-source voltage reaches a constant final value, when switch S_1 is closed. Then, the total gate charge, gate-source charge and gate-drain charge can be calculated by using the expressions defined in Subclauses 3.3.7.1 to 3.3.7.4.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain current I_D
- Drain source voltage V_{DS}
- Gate current I_{GG}

6.3.10 Common source short-circuit input capacitance (C_{iss})

– **Purpose**

To measure the input capacitance of the DUT, under specified conditions.

– **Circuit diagram**

See Figure 29 below.

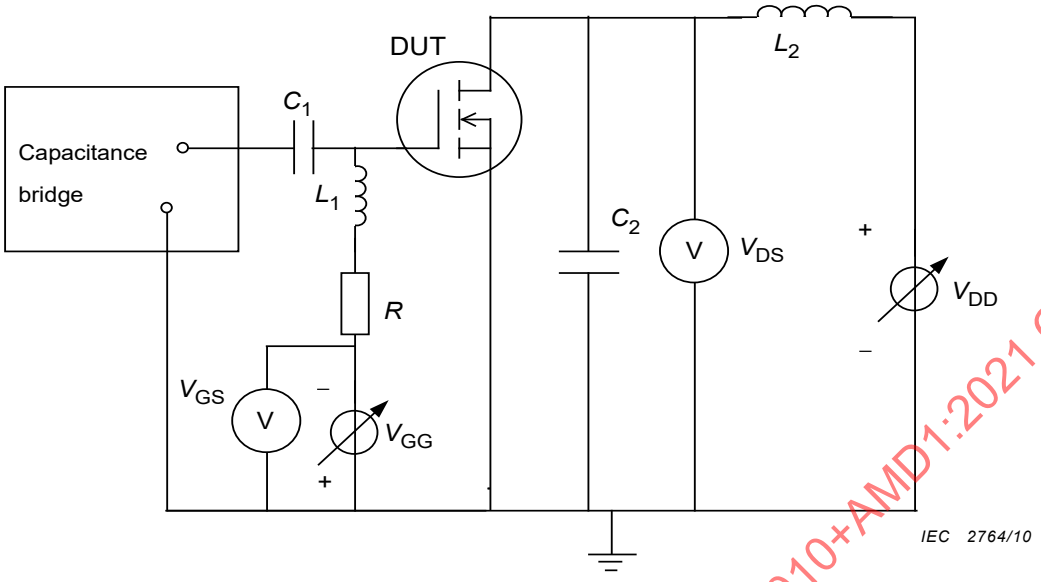


Figure 29 – Basic for the measurement of short-circuit input capacitance

– **Circuit description and requirements**

Capacitance C_1 and C_2 shall present short circuits at the measurement frequency, satisfying the following conditions. The impedance of L_1 and R shall be sufficiently large at the measurement frequency not to affect the measurement value:

$$|y_{is}| \gg 1/\omega L_1 \text{ and } \omega C_1 \gg |y_{is}|$$

$$|y_{os}| \gg 1/\omega L_2 \text{ and } \omega C_2 \gg |y_{os}|$$

– **Measurement procedure**

Without the DUT, zero adjustments of the capacitance bridge are made. And then, after the DUT is set, V_{DS} and V_{GS} are adjusted to the specified values. The bridge is re-balanced; the difference of the capacitance readings of this adjustment and that without the DUT in the measurement circuit yields the value of C_{iss}.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DS}
- Gate-source voltage V_{GS}
- Frequency of measurement f

6.3.11 Common source short-circuit output capacitance (C_{oss})

– **Purpose**

To measure the short-circuit output capacitance, under specified conditions.

– **Circuit diagram**

See Figure 30 below.

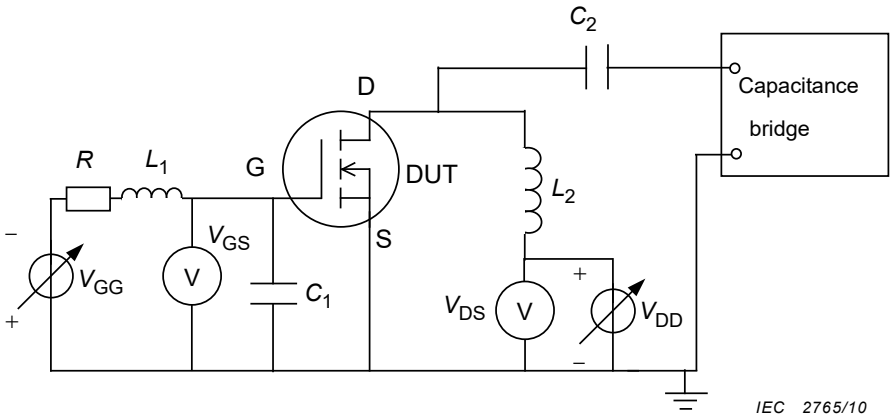


Figure 30 – Basic circuit for measurement of short-circuit output capacitance (C_{oss})

– **Circuit description and requirements**

A capacitance bridge is used, thus making it possible to apply a null method. C_2 shall be much larger than C_{oss}, and ωC_1 much larger than $|y_{is}|$. The impedance of L_1, L_2 shall be sufficiently high, so that it is possible to compensate it by the bridge adjustments.

$$|y_{is}| \gg 1/\omega L_1 \text{ and } \omega C_1 \gg |y_{is}|$$

$$|y_{os}| \gg 1/\omega L_2 \text{ and } \omega C_2 \gg |y_{os}|$$

– **Measurement procedure**

First without the DUT, zero adjustments of the capacitance bridge are made. The DUT to be measured is then set into the measurement circuit, V_{DS}, and V_{GS} (or I_D) is adjusted to the specified values. The bridge is re-balanced; the difference of the capacitance readings of this adjustment and that without the DUT in the measurement circuit yields the value of C_{oss}.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DS}
- Gate-source voltage V_{GS}
- Frequency of measurement f

6.3.12 Common source short-circuit reverse transfer capacitance (C_{rss})

– **Purpose**

To measure reverse transfer capacitance, under specified conditions.

– **Circuit diagram**

See Figure 31 below.

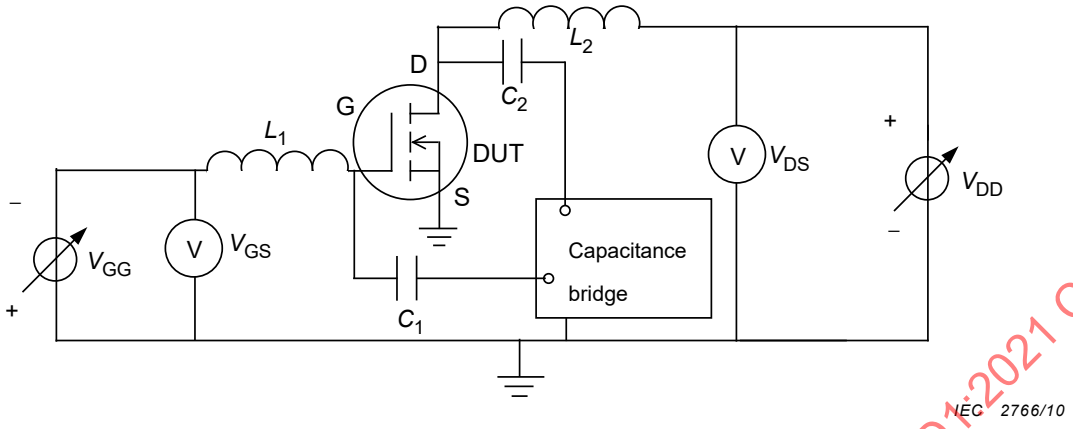


Figure 31 – Circuit for measurement of reverse transfer capacitance C_{rss}

– **Circuit description and requirements**

The values of C_1, C_2, L_1 and L_2 shall be sufficiently large so that they do not affect the measurement. The capacitance bridge shall be capable of measuring the capacitance independently of any impedance present between either measuring terminal and ground.

– **Measurement procedure**

First without the DUT, zero adjustments of the capacitance bridge are made. The DUT to be measured is then set into the measurement circuit, V_{DS}, and V_{GS} (or I_D) is adjusted to the specified values. The bridge is re-balanced; the difference of the capacitance readings of this adjustment and that without the DUT in the measurement circuit yields the value of C_{rss}.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DS}
- Gate-source voltage V_{GS}
- Frequency of measurement f

6.3.13 Internal gate resistance (r_g)

– **Purpose**

To measure the internal gate resistance of the DUT, under specified conditions.

– **Circuit diagram**

See Figure 32 below.

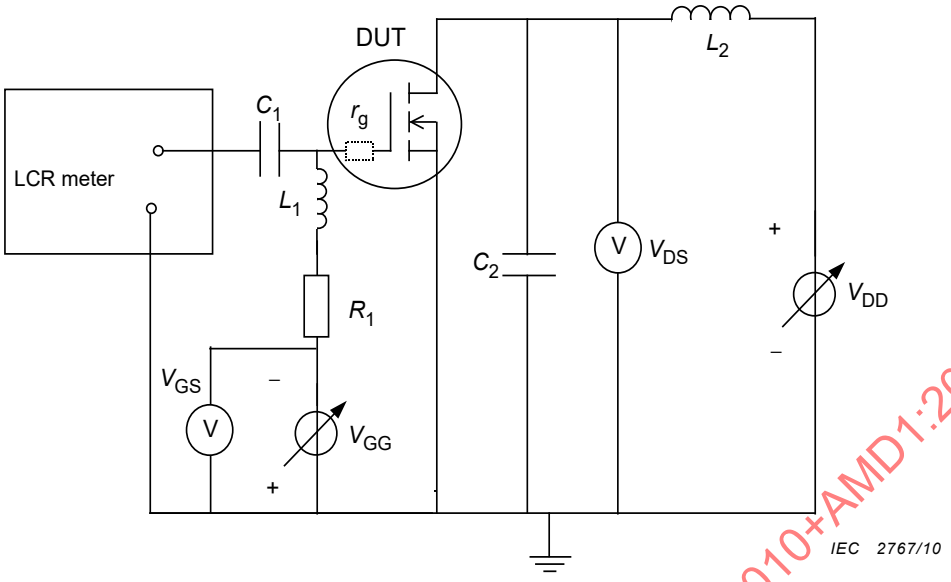


Figure 32 – Circuit for measurement of internal gate resistance

– **Circuit description and requirements**

An LCR meter is used, thus making it possible to apply a null method. C_2 shall be much larger than C_{oss}, and ωC_1 much larger than $|y_{is}|$. The impedance of L_1, L_2 shall be sufficiently high so that it is possible to compensate it by the bridge adjustments.

$$|y_{is}| \gg 1/\omega L_1 \text{ and } \omega C_1 \gg |y_{is}|$$

$$|y_{os}| \gg 1/\omega L_2 \text{ and } \omega C_2 \gg |y_{os}|$$

– **Measurement procedure**

Drain-source voltage V_{DS} and gate-source voltage V_{GS} of DUT are set to specified values and then internal gate resistance r_g is measured by LCR meter adjusted in a series mode connection of gate capacitance of DUT and resistance r_g.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DS}
- Gate-source voltage V_{GS}
- Frequency of measurement f

6.3.14 MOSFET forward recovery time (t_{fr}) and MOSFET forward recovered charge (Q_f)

– **Purpose**

To measure the MOSFET forward recovery time t_{fr} and MOSFET forward recovered charge Q_f under specified conditions.

Method 1

– **Circuit diagram and waveform**

See Figure 33 and Figure 34 below.

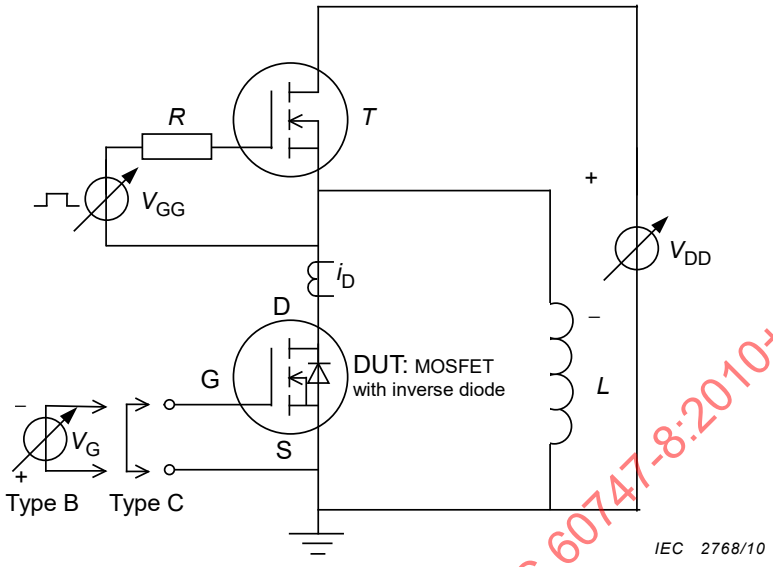
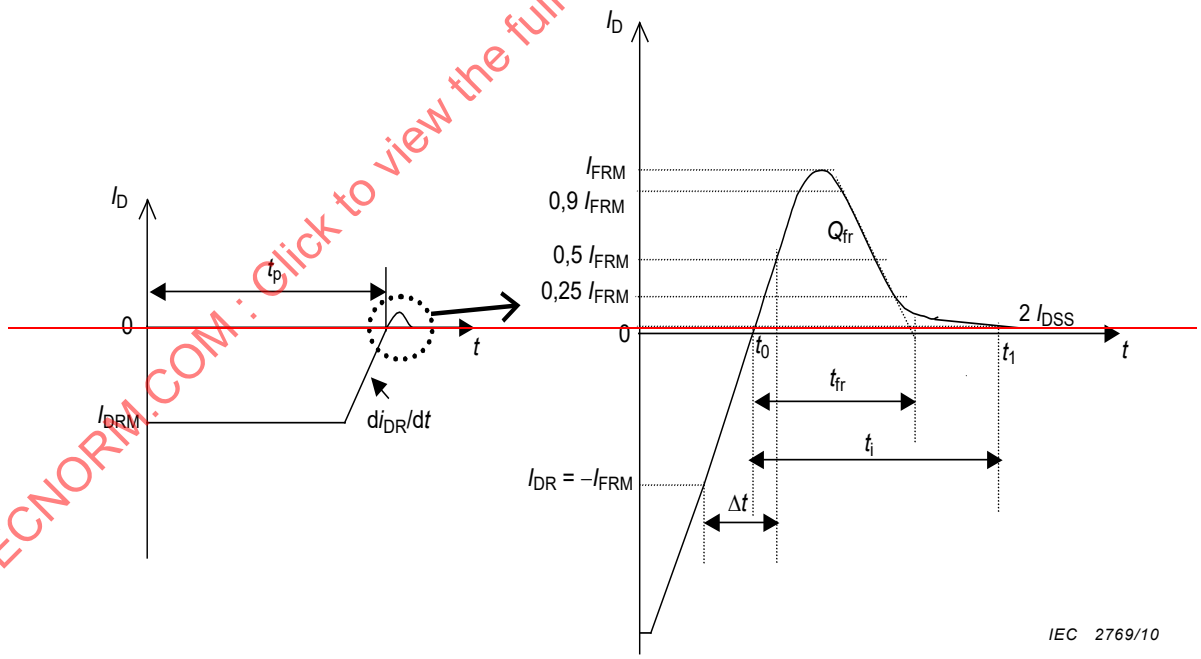


Figure 33 – Circuit diagram for MOSFET forward recovery time and recovered charge (Method 1)



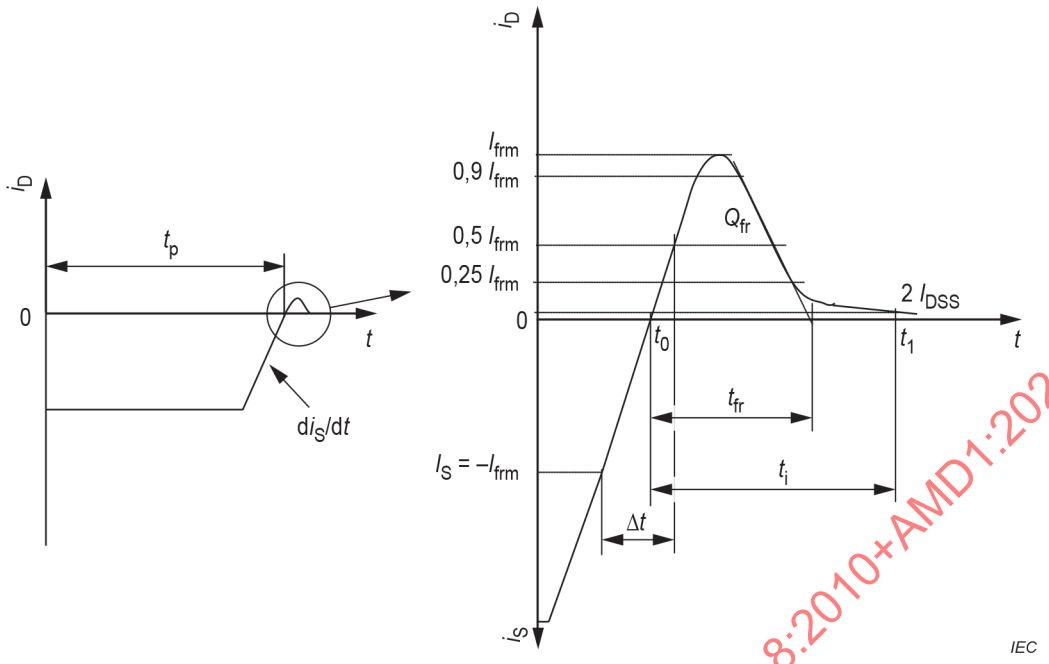


Figure 34 – Current waveform through MOSFET (Method 1)

– **Circuit description and requirements**

V_{DD} is the d.c. voltage supply and V_{GG} is the gate pulse generator to turn-on and turn-off the MOSFET ~~T~~ *T*. *L* is a load inductance. Inverse diode is integrated in the DUT. The rate of change of reverse drain current ~~$-di_{DR}/dt$~~ di_S/dt of the DUT can be controlled by the values of the gate voltage V_{GG} and/or *R*.

– **Measurement procedure**

MOSFET ~~T~~ *T* is turned on and turned off twice, and then the second turn-on is observed. Waveforms of the current ~~I_D~~ I_S are monitored. The recovered charge is measured as

~~$$Q_f = \int_{t_0}^{t_0+t_i} i_D \cdot dt$$~~

$$Q_f = \int_{t_0}^{t_0+t_i} i_S \cdot dt$$

where

t_0 is the instant when the current passes through zero;

t_i is the integration time.

~~Integral end time t_1 is the time when forward drain current reaches $2 \times I_{DSS}$, preferably equal to the specified maximum value of t_{fr}. Δt can be adjusted by MOSFET *T* driving conditions, such as V_G and/or *R*. The forward recovery time t_{fr} is measured as the interval between the time of t_0 when the drain current passes through zero and the time when, for decreasing values of I_D, a line through the points for 0,9 I_{FRM} and 0,25 I_{FRM} crosses the zero current axis.~~

Integral end time t_1 is the time when forward drain current reaches $2 \times I_{DSS}$, preferably equal to the specified maximum value of t_{fr}. Δt can be adjusted by MOSFET *T* driving conditions, such as V_G and/or *R*. The forward recovery time t_{fr} is measured as the interval between the time of t_0 when the drain current passes through zero and the time when, for decreasing values of I_D, a line through the points for 0,9 I_{frm} and 0,25 I_{frm} crosses the zero current axis.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- ~~Reverse drain current I_{DR}~~
- Peak reverse drain current I_{SM}
- Rate of change of drain current ~~$-di_{DR}/dt$~~ di_S/dt
- Integration time t_i (for the recovered charge measurement)
- T shall be off-state by gate-source shorted or reverse biased

Method 2

– **Circuit diagram and waveform**

See Figure 35 and Figure 36 below.

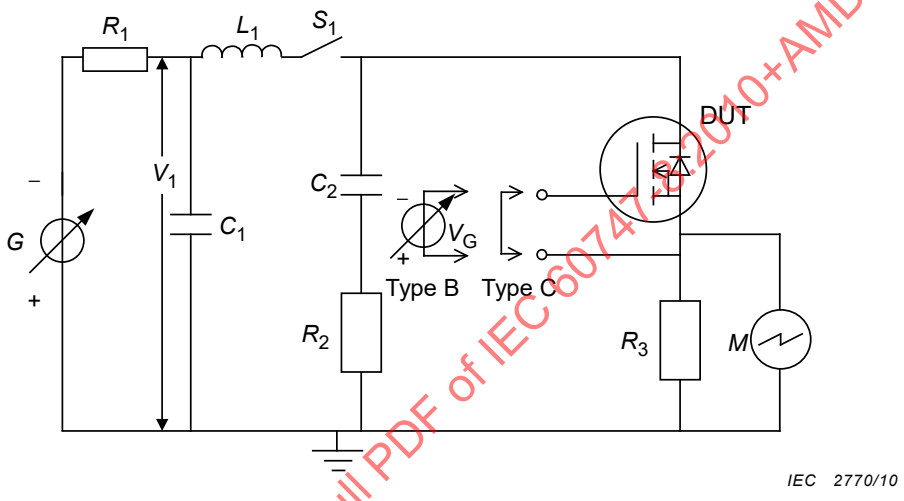
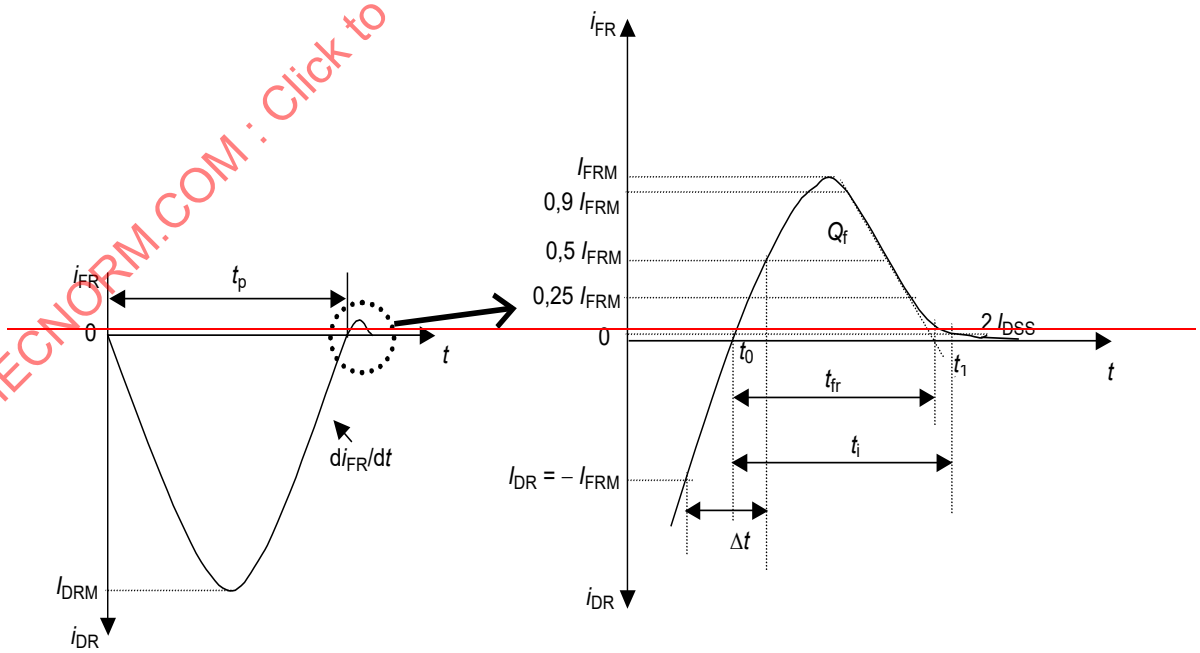


Figure 35 – Circuit diagram for MOSFET forward recovery time and recovered charge (Method 2)



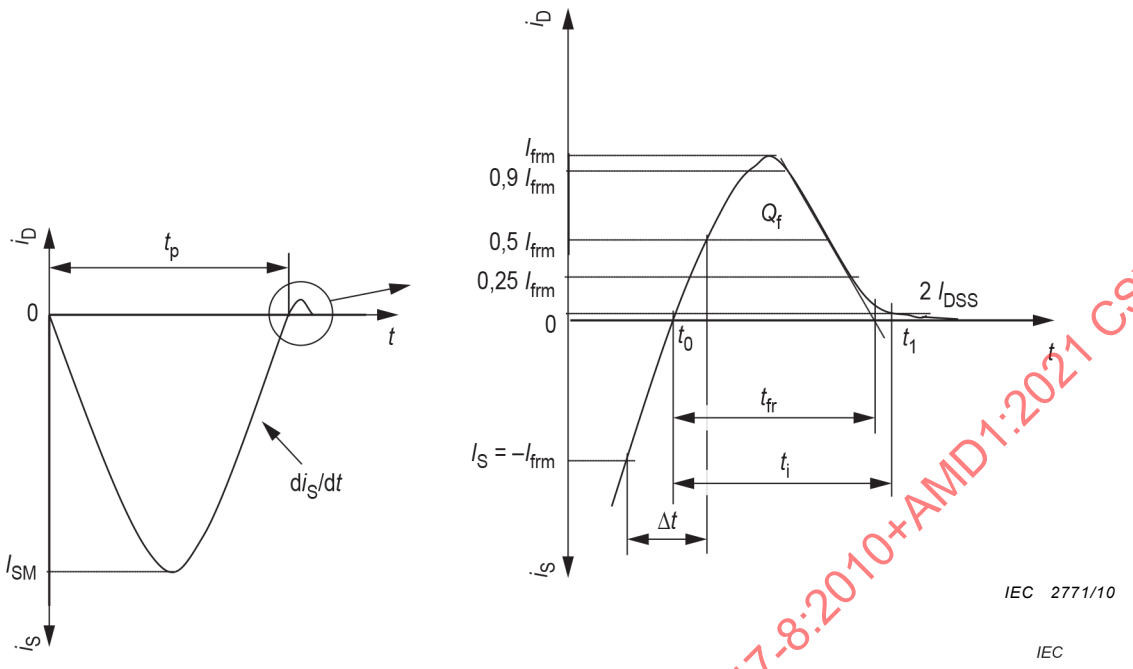


Figure 36 – Current waveform through MOSFET (Method 2)

– **Circuit description and requirements**

G Voltage generator to charge C_1

R_1 Resistor to prevent generator G from damping of the resonant circuit

C_1 & L_1 Resonant circuit supplying the reverse and forward currents

Approximately $t_p = \pi\sqrt{L_1 C_1}$ and $V_1 = I_{DRM}\sqrt{L_1/C_1}$ provided that $\sqrt{L_1/C_1} \rangle\rangle 2(r_{ds(on)} + R_3)$

S_1 Switch (e.g. MOSFET with inverse (antiparallel) diode)

C_2 & R_2 Circuit to limit the applied forward off-state drain voltage (alternatively the DUT may be switched on as the forward voltage rises towards the break-over voltage)

R_3 Current sensing resistor

M Measuring instrument (e.g. oscilloscope)

V_G Gate off-state voltage for type B devices

– **Measurement procedure**

The DUT gate is biased to the off-state. With S_1 open, generator G charges capacitor C_1 to the voltage required to produce the specified peak reverse drain current ~~I_{DRM}~~ I_{SM} through the DUT. Switch S_1 is closed and the resonant circuit L_1 C_1 discharges through the DUT. The pulse duration (t_p) and the rate of change of reverse drain current ~~$-di_{DR}/dt$~~ di_S/dt shall be in accordance with the specified conditions. The forward recovery time t_{fr} is measured as the interval between the time when the drain current passes through zero and time when, for decreasing values of I_D, a line through the points for 0,9 ~~I_{FRM}~~ I_{frm} and 0,25 ~~I_{FRM}~~ I_{frm} crosses the zero current axis.

The forward recovered charge is measured as $Q_f = \int_{t_0}^{t_0+t_i} i_D \cdot dt$

Where t_0 is the instant when the current passes through zero, t_i is the integration time.

Integral end time t_1 is the time when forward drain current reaches 2 × I_{DSS}.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Peak drain reverse current ~~I_{FRM}~~ I_{frm}
- Rate of change of drain current ~~$-di_{DR}/dt$~~ di_S/dt
- Integration time (t_i) (for the recovered charge measurement)

NOTE The rate of change of drain current is measured at zero crossing current, for example over time Δt, between current values of ~~I_{DR}~~ $I_S = -I_{DM}$ and ~~I_{DR}~~ $I_S = 0{,}5\ I_{DM}$.

6.3.15 Drain-source reverse voltage (~~V_{DSR}~~ V_{SD})

– **Purpose**

To measure the drain-source reverse voltage ~~V_{DSR}~~ V_{SD} under specified conditions.

– **Circuit diagram**

See Figure 37 below.

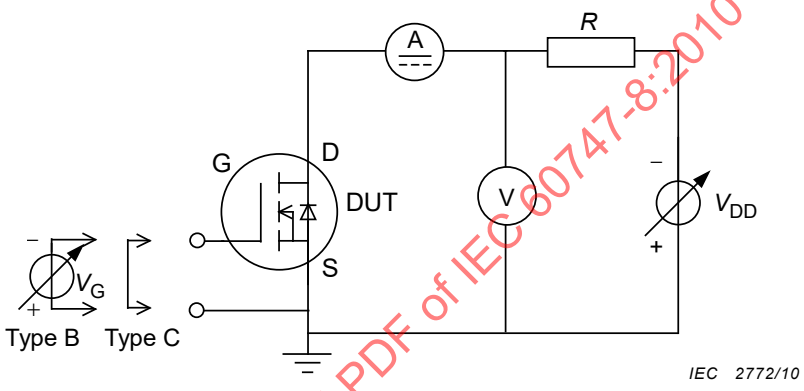


Figure 37 – Circuit diagram for the measurement of drain-source reverse voltage

– **Circuit description and requirements**

V_{DD} is a low voltage supply. R is a current limiting resistor.

– **Measurement procedure**

Gate-source terminals are connected as specified. Adjust the voltage V_{DD} to supply the specified value of reverse drain current. Measure the drain-source reverse voltage on voltmeter V.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Reverse drain current ~~I_{DR}~~ I_S

6.3.16 Small-signal short-circuit output conductance (type A, B and C) (g_{oss})

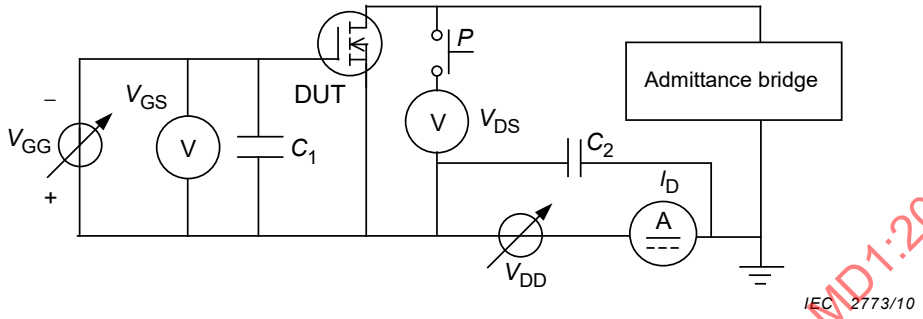
– **Purpose**

To measure the small-signal output conductance, under specified conditions.

Method 1: Null method

– **Circuit diagram**

See Figure 38 below.



P = push-button

Figure 38 – Basic circuit for the measurement of the output conductance g_{oss} (method 1: null method)

– **Circuit description and requirements**

The admittance bridge is used for this measurement. Capacitances C_1 and C_2 shall present short circuits at the measurement frequency, satisfying the following conditions:

$$\omega C_1 \gg |y_{is}|$$
$$\omega C_2 \gg |y_{os}|$$

This method requires an admittance bridge but has the advantage that g_{oss} may be measured at high and low frequencies, and that both g_{oss} and C_{oss} may be measured simultaneously.

– **Measurement procedure**

Without the DUT in the measurement socket, the zero adjustments of the bridge are made. The device to be measured is then set into the measurement circuit; the drain-source voltage V_{DS} and the gate-source voltage V_{GS} are adjusted to obtain the specified bias conditions with the push-button *P* closed. With the push-button *P* open, the bridge is rebalanced, and the values of g_{oss} or Re y_{os} and Im y_{os}, if needed, are then read.

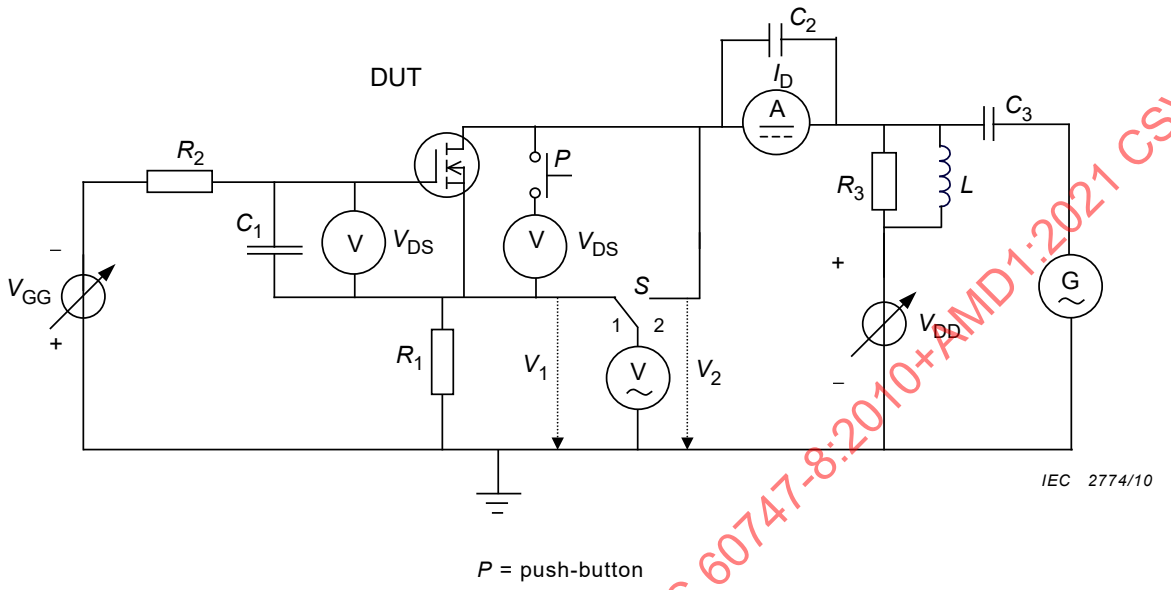
– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DS}
- Gate-source voltage V_{GS} or drain current I_D
- Frequency of measurement *f*

Method 2: Two-voltmeter method

– **Circuit diagram**

See Figure 39 below.



P = push-button

Figure 39 – Basic circuit for the measurement of the output conductance g_{oss} (method 2: two-voltmeter method)

– **Circuit description and requirements**

All bias voltages applied shall be adequately decoupled at the frequency of measurement. The value of ωC_1 shall be much larger than $|y_{is}|$; the value ωC_2 shall be high. Inductance L is optional; its use facilitates the adjustment of the specified operating point. Resistor R_1 shall be sufficiently low with respect to $\frac{1}{g_{oss}}$; practically, a value of 10 Ω to 100 Ω will be used, in accordance with the voltmeter sensitivity. The a.c. voltmeter shall have sufficient sensitivity; for the measurement or low conductances, it shall preferably be a selective instrument. This method simply measures the modulus of $y_{os} = g_{oss} + j\omega C_{oss}$ which is identical with g_{oss} for sufficiently low frequency.

– **Measurement procedure**

The DUT to be measured set into the measurement circuit; the drain-source voltage V_{DS} and the gate-source voltage V_{GS} are adjusted to obtain the specified bias conditions with the push-button P closed. With the switch S in position 1, the value $V_1 = I_D R_1$ is measured, while with the switch S in position 2, the value $V_2 = V_{DS} + I_D R_1$ is measured.

Thus:

$$V_2 - V_1 = V_{DS}$$

$$I_D = \frac{V_1}{R_1}$$

$$|y_{os}| = \frac{V_1}{R_1 (V_2 - V_1)} \simeq \frac{V_1}{R_1 V_2} \quad \text{(for } V_2 \gg V_1\text{)}$$

For sufficiently low frequencies: $|y_{os}| \simeq g_{oss}$.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DS}
- Gate-source voltage V_{GS} or drain current I_D
- Frequency of measurement f

6.3.17 Small-signal short-circuit forward transconductance (types A, B and C)

– **Purpose**

To measure the small-signal short-circuit forward transconductance, under specified conditions.

Method 1: Null method

– **Circuit diagram**

See Figure 40 below.

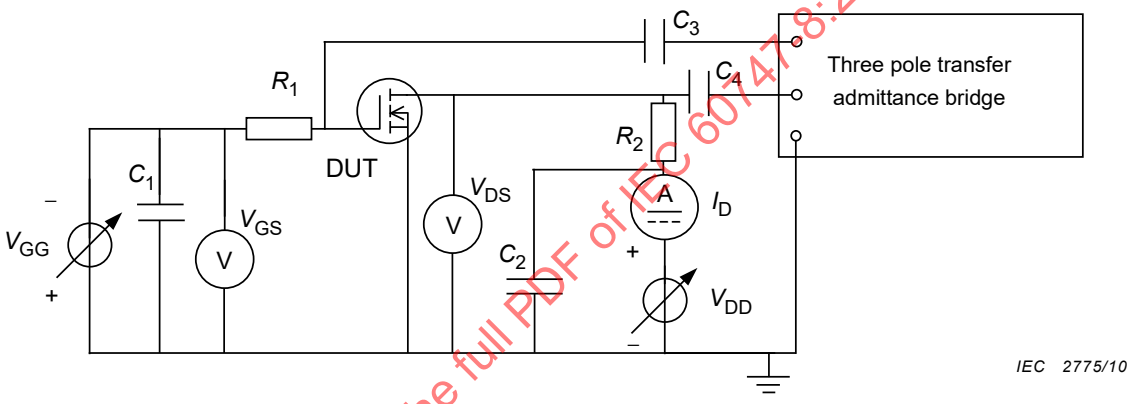


Figure 40 – Circuit for the measurement of short-circuit forward transconductance g_{fs} (Method 1: Null method)

– **Circuit description and requirements**

All bias supply voltages applied shall be adequately decoupled at the frequency of measurement. The value of ωC_1 shall be much larger than $|y_{is}|$ and the value of ωC_2 shall be much larger than $|y_{os}|$. R_1 shall be much larger than the internal impedance of the bridge, in order not to affect the measurement accuracy. R_2 shall be much larger than the internal resistance of the detector, but nevertheless sufficiently lower than $1/y_{fs}$, in order not to affect the measurement sensitivity. The values of ωC_3 and ωC_4 shall be much larger than $|y_{fs}|$ to be measured. The internal resistance of the voltmeter V_{DS} shall be much larger than V_{DS}/I_D. This method needs a three-pole transfer admittance bridge, but has the advantage that g_{fs} may be measured at low frequencies, as well as $y_{fs} = g_{fs} + jb_{fs}$ at high frequencies. Furthermore, it guarantees a real short circuit at the output.

– **Measurement procedure**

Without the DUT in the measurement circuit, the zero adjustments of the bridge are made. The device to be measured is then set into the measurement circuit; V_{DS} and V_{GS} (or I_D) are adjusted to the specified values. The bridge is rebalanced, and the values of g_{fs}, or Re (y_{fs}) and Im (y_{fs}) if needed, are then read.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DS}

- Gate-source voltage V_{GS} or drain current I_D
- Frequency of measurement f

Method 2: Two-voltmeter method

– **Circuit diagram**

See Figure 41 below.

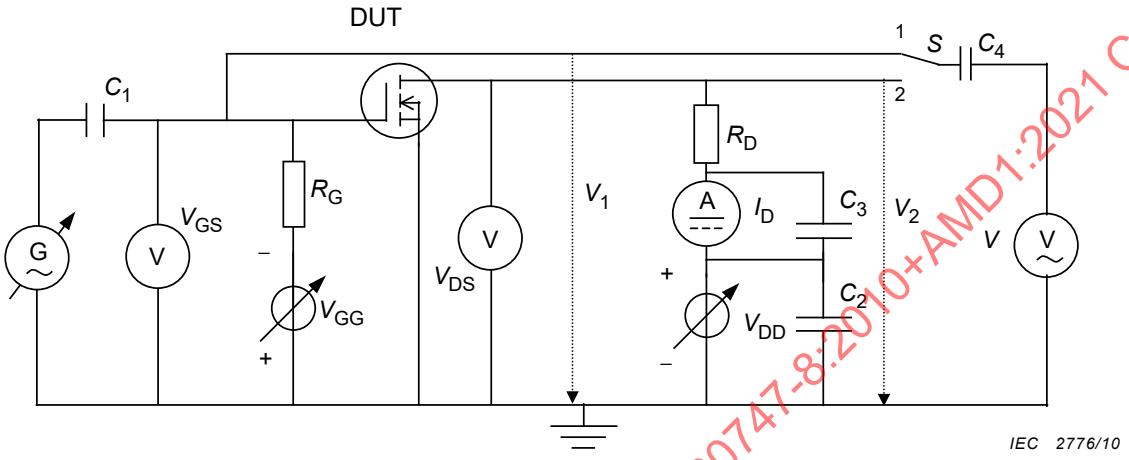


Figure 41 – Circuit for the measurement of forward transconductance g_{fs} (method 2: two-voltmeter method)

– **Circuit description and requirements**

A suitable oscillator shall be used, the frequency of which shall be sufficiently low. The value of resistor ωC_3 and ωC_2 shall be much greater than $1/R_D$. The value of ωC_1 shall be high. The value of resistor R_G is not critical; it shall preferably not be too high. Resistance R_D must be low compared with $\left|\frac{1}{y_{os}}\right|$. Voltmeter V shall have sufficient sensitivity; for the measurement of low values of g_{fs}, it shall preferably be a selective instrument. This method simply measures the modulus of y_{fs}, which is identical with g_{fs} for sufficiently low frequencies.

– **Measurement procedure**

The DUT to be measured is set into the measurement circuit; V_{DS} and V_{GS} (or I_D) are adjusted to the specified values. With the switch S in position 1, the value $V_1 = V_{gs}$ is measured, while with the switch S in position 2, the value $V_2 = I_D R_D$ is measured.

Thus:

$$|y_{fs}| \approx \frac{I_D}{V_{GS}} = \frac{V_2}{V_1 R_D}$$

For sufficiently low frequencies: $|y_{fs}| \simeq g_{fs}$.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DS}
- Gate-source voltage V_{GS} or drain current I_D
- Frequency of measurement f

6.3.18 Noise (types A, B and C) (F, Vn)

– **Purpose**

To measure the equivalent input noise voltage or noise factor, under specified conditions.

6.3.18.1 Equivalent input noise voltage

– **Circuit diagram**

A circuit in accordance with the block diagram shown in Figure 42 shall be used.

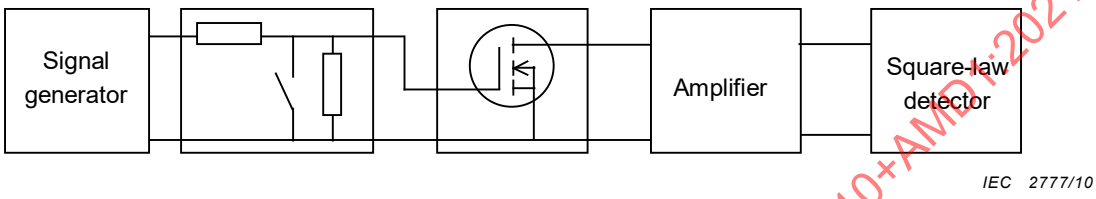
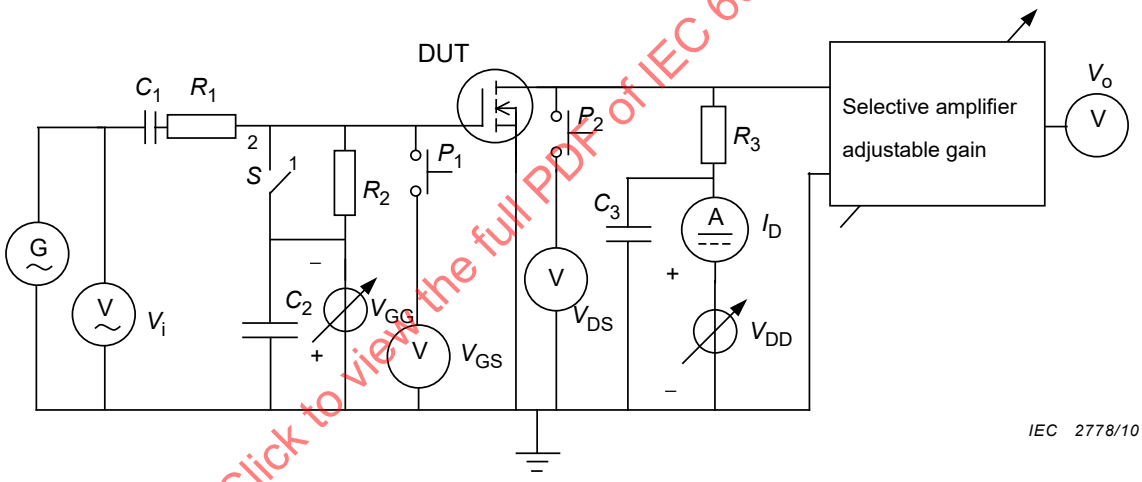


Figure 42 – Block diagram for the measurement of equivalent input noise voltage

Figure 43 shows an example of a circuit in accordance with that block diagram.



P_1, P_2 = push-buttons

Figure 43 – Circuit for the measurement of equivalent input noise voltage

– **Circuit description and requirements**

The frequency of the generator shall be adjusted to be the center frequency of the selective amplifier. The output voltage shall be adjusted in such a way that the input voltage to the transistor is high compared with the noise voltage, but low enough to avoid overloading of the device. The voltage-dividing ratio of the voltage divider (R_2, R_1) shall be known. For the bias source, special care shall be taken to achieve low-noise biasing (especially important for the gate bias). All resistors that might deliver noise to the circuit shall be of a low-noise type (e.g. metallic film resistors). A neutralization network shall be used, when appropriate. Adequate shielding to minimize the influence of external electromagnetic fields shall be provided, when appropriate. The amplifier shall be linear up to a level of at least 20 dB higher than the r.m.s. noise value, so that noise peaks are correctly amplified. The second stage noise shall be as low as possible. The noise level measured with the device removed from the circuit shall be at least 15 dB lower than that measured with the device in the circuit. The output voltmeter shall measure the true r.m.s. value. The equivalent noise bandwidth shall be accurately known. ωC_3 shall be much larger than $1/R_3$ and ωC_2 much larger than $1/R_2$.

– **Measurement procedure**

The DUT is set into the measurement circuit and the operating point is adjusted to the specified values of V_{DS} and V_{GS} (or I_D). The input voltage V_i is adjusted to a suitable value (e.g. 0,1 V). With switch S in position 1, the output voltage V_{o1} is measured, after proper adjustment of the gain of the amplifier. With switch S in position 2, the output voltage V_{o2} is measured.

The noise voltage is given by

$$V_n = \frac{V_{o2}}{V_{o1}} V_i \frac{R_2}{R_1 + R_2}$$

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Values of resistors R_1 and R_2
- Drain-source voltage V_{DS}
- Gate-source voltage V_{GS} or drain current I_D
- Frequency of measurement f and bandwidth

6.3.18.2 Noise factor

All methods of measurement for bipolar transistors (see 6.3.14 of IEC 60747-7:2000) are applicable for field-effects transistors.

6.3.19 On-state drain-source resistance (under small-signal conditions) ($r_{ds(on)}$)

– **Purpose**

To measure the on-state drain-source resistance, by means of a low-frequency bridge.

– **Circuit diagram**

See Figure 44 below.

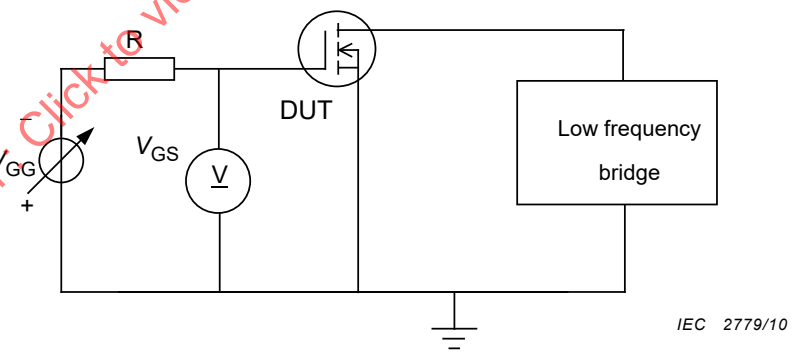


Figure 44 – Circuit diagram for the measurement of on-state drain-source resistance

– **Circuit description and requirements**

The bridge shall be able to pass d.c. For type B and C devices, the case and/or substrate shall be connected to the source.

– **Measurement procedure**

The bridge is first balanced without the DUT. The DUT is then set into the measurement circuit and the gate-source voltage is adjusted to the specified value. The bridge is rebalanced, and the value of the on-state resistance is read from the bridge.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage (equal to zero) V_{DS}
- Gate-source voltage V_{GS}
- Frequency (1 kHz, unless otherwise specified) f

NOTE The bridge may be replaced by an a.c. voltmeter, a.c. ammeter and signal generator, if desired.

6.3.20 Channel-case transient thermal impedance ($Z_{th(j-c)}$) and thermal resistance ($R_{th(j-c)}$) of a field-effect transistor

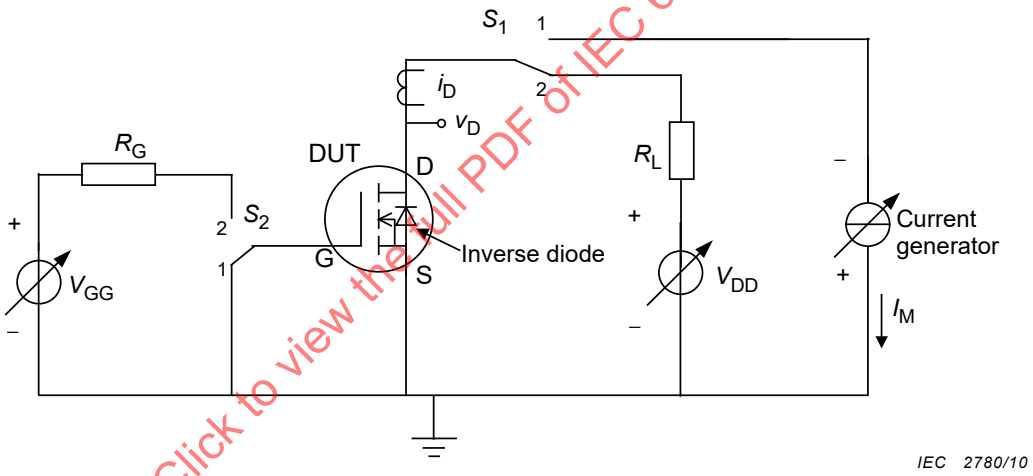
– **Purpose**

To measure the channel-case transient thermal impedance and channel-case thermal resistance of a field-effect transistor.

This method cannot be used if an isolation material is used having a varying temperature coefficient, e.g. beryllium oxide.

Method 1: Cooling method

– **Circuit diagram**



DUT = transistor being measured (MOSFET or JFET)
(Example: *n*-channel enhancement MOSFET)

Figure 45 – Circuit diagram

– **Circuit description and requirements**

V_{GG} = adjustable voltage source
V_{DD} = adjustable voltage source } set to obtain the intended heating power P(H)
I_M = reference (direct) current generator
S_1, S_2 = synchronous switches
R_L = limiting resistors for drain current I_D
R_G = protective resistor

As a temperature-sensitive characteristic, the forward voltage of the inverse diode (V_{SD} in Figure 45) is chosen to be measured at a fixed reference current (I_M in Figure 45). After a heating current has been applied and thermal equilibrium is established, the heating current is switched off. During the following cooling period, V_{SD} and the case temperature are recorded

as a function of time. From the recorded values and the initial heating power, the values of $Z_{th(j-c)}$ and $R_{th(j-c)}$ are determined by means of a calibration curve. Care must be taken that the drain-source channel is not conducting when the forward voltage of the inverse diode is measured. In the example, this is reached by setting V_{GS} equal to zero. Make sure that switch S_2 is in position 1 before S_1 is switched to position 1. The change-over time of switches S_1, S_2 shall be short enough so that $Z_{th(j-c)}$ can (at least by interpolation back to t = 0) be measured for the shortest required cooling period t_c. I_M shall be sufficiently small so that the corresponding power $P(M) = I_M \cdot V_{SD}$ is relatively small compared to the heating power $P(H) = I_D \cdot V_{DS}$ or may even be neglected (see equation (1) below).

– **Measurement procedure**

A thermosensor is fixed at the reference point of the transistor being measured to measure its case temperature T_c. A calibration curve is established as follows: the transistor is externally heated to rising step values of case temperature T_c*. At each step, after thermal equilibrium has been reached, the forward voltage of the inverse diode V_{SD} is measured. From the measured values, the calibration curve $T_c^* = f(V_{SD})$ is established. With the switches in position 2, the heating power $P(H) = I_D \cdot V_{DS}$ is set to the intended value, and this setting is subsequently maintained. $P(H)$ is recorded. After thermal equilibrium has been reached, the case temperature $T_c(0)$ and the forward voltage of the inverse diode $V_{SD}(0)$ are recorded. Switching back to position 1, the heating process is interrupted, and the courses $V_{SD}(t)$ and $T_c(t)$ during the cooling process are recorded. By means of the calibration curve, the recorded values of $V_{SD}(0)$ and $V_{SD}(t)$ are converted to the corresponding values of $T_c^*(0)$ and $T_c^*(t)$ respectively. The channel-case transient thermal impedance after a particular cooling period t_c is calculated as

$$Z_{th(j-c)}(t_c) = \frac{[T_c^*(0) - T_c^*(t_c)] - [T_c(0) - T_c(t_c)]}{P(H) - P(M)} \quad (1)$$

where

$T_c^*(0)$, $T_c^*(t_c)$ are the values taken from the calibration curve for $V_{SD}(0)$ and $V_{SD}(t_c)$;

$T_c(0)$, $T_c(t_c)$ are the values of T_c at t = 0 and $t = t_c$ respectively;

$P(H) = I_D \cdot V_{DS}$ is the heating power in position 2;

$P(M) = I_M \cdot V_{SD}$ is the measuring power in position 1.

The channel-case thermal resistance $R_{th(j-c)}$ is the value finally reached of $Z_{th(j-c)}$ after the cooling period is settled, i.e. thermal equilibrium has again been reached.

Method 2: Heating method

– **Circuit diagram**

Same as in Method 1 above.

– **Circuit description and requirements**

Same as in Method 1 above.

As a temperature-sensitive characteristic, the forward voltage of the inverse diode (VS_D in Figure 45) is chosen to be measured at a fixed reference current (I_M in Figure 45). Starting from thermal equilibrium at heating current zero, a heating current is applied to specified values of heating power and duration. The values of V_{SD} and of the case temperature are measured just before and after the application of heating current. From the measured values of V_{SD}, the channel temperature may be determined from the calibration curve. The values of $Z_{th(j-c)}$ and $R_{th(j-c)}$ may then be calculated using the values of heating power, channel temperature and reference-point temperature.

– **Measurement procedure**

A thermosensor is fixed at the reference point of the transistor being measured to measure its case temperature T_c. With the switches in position 2, the heating power $P(H) = I_D \cdot V_{DS}$ is set to the intended value and this setting is subsequently maintained. $P(H)$ is recorded. The heating power is switched off by switching back to position 1. When thermal equilibrium has been reached, the case temperature $T_c(0)$ and the forward voltage of the inverse diode $V_{SD}(0)$ are recorded. By switching first to position 2 and then back to position 1, the heating power is applied for the intended heating period t_h. Immediately after having switched back to position 1, the case temperature $T_c(t_h)$ and the forward voltage of the inverse diode $V_{SD}(t_h)$ are recorded. By means of the calibration curve, the recorded values of $V_{SD}(0)$ and $V_{SD}(t_h)$ are converted to the corresponding values $T_c^*(0)$ and $T_c^*(t_h)$ respectively. The channel-case transient thermal impedance for the heating pulse duration t_h is calculated as

$$Z_{th(j\text{-}c)}(t_h) = \frac{[T_c^*(t_h) - T_c^*(0)] - [T_c(t_h) - T_c(0)]}{P(H) - P(M)} \quad (2)$$

where

$T_c^*(t_h)$, $T_c^*(0)$ are the values taken from the calibration curve for $V_{SD}(t_h)$ and $V_{SD}(0)$ respectively;

$T_c(t_h)$, $T_c(0)$ are the values at $t = t_h$ and $t = 0$ respectively;

$P(H) = I_D \cdot V_{DS}$ is the heating power in position 2;

$P(M) = I_M \cdot V_{SD}$ is the dissipation in position 1.

The channel-case thermal resistance $R_{th(j\text{-}c)}$ is the value finally reached of $Z_{th(j\text{-}c)}$ when the pulse duration is long enough to reach the new thermal equilibrium.

7 Acceptance and reliability

7.1 General requirements

Clause 7 of IEC 60747-1:2006 applies. The testing times of the endurance tests shall be introduced in the data sheet.

7.2 Acceptance-defining characteristics

Acceptance-defining characteristics, their criteria and measurement conditions are listed in Table 2.

NOTE Characteristics should be measured in the sequence in which they are listed in Table 3, because the changes in characteristics caused by some failure mechanisms may be wholly or partially masked by the influence of other measurements.

Table 3 – Acceptance-defining characteristics for endurance and reliability tests

Characteristics	Criteria (see note)	Measurement conditions
I_{DSS} or I_{DSX}	< USL	Specified V_{DS} and gate condition
I_{GSS}	< USL	Specified V_{GS}
$V_{GS(off)}$ or $V_{GS(th)}$	> LSL < USL	Specified V_{DS} and I_D
$R_{DS(on)}$	< USL	Specified V_{GS} and I_D
R_{th}	< USL	
USL: upper specification limit LSL: lower specification limit		

7.3 Endurance and reliability tests

7.3.1 High-temperature blocking (HTRB)

The test is performed as specified in IEC 60749-23:2004, Subclause 5.2.3.3.

– **Operating conditions**

- Voltage: preferably 80 % of V_{DSSmax} or V_{DSXmax}
- Temperature: preferably maximum virtual junction temperature $T_{vj(max)}$ or $T_c = T_{stg(max)} – 5$ °C as specified

– **Test circuit**

R is the current limiting resistor in Figure 46.

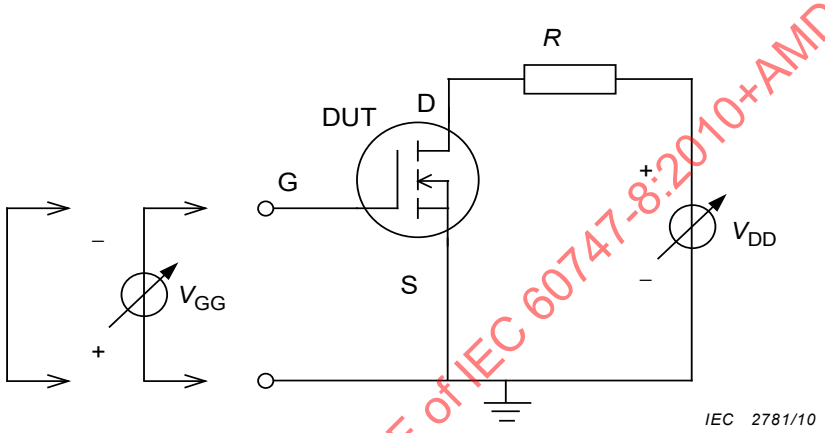


Figure 46 – Circuit for high-temperature blockings

7.3.2 High-temperature gate bias

The test is performed as specified in IEC 60749-23:2004, Subclause 5.2.3.4.

– **Operating conditions**

- Voltage: preferably 80 % of specified continuous V_{GSSmax}
- Temperature: preferably $T_{vj\ (max)}$ or $T_c = T_{stg\ (max)} – 5$ °C

– **Test circuit**

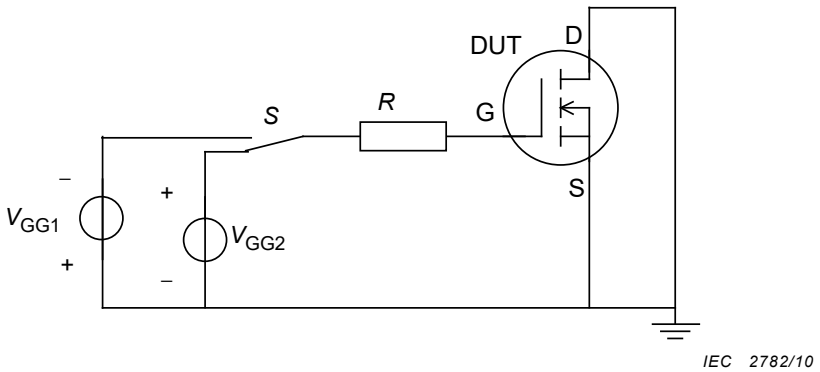


Figure 47 – Circuit for high-temperature gate bias

7.3.3 Intermittent operating life (load cycles)

The test is performed as specified in IEC 60749-34.

– **Operating conditions**

- Current: specified value
- Temperature: ΔT_{vj} as specified
- Gate voltage V_{GS} : specified value
- Case temperature
- Method 1: T_c = constant
- Method 2: T_c = variable with T_{vj}
- On-time t_p and off-time ($t_c - t_p$) specified

NOTE Mechanical stress in the device under test by method 1 concentrates on the wire-bonded emitter portions of dies of the module type devices. Mechanical stress in the device under test by method 2 concentrates mainly on the soldering material portion or the pressure contact portion of dies of the devices.

– **Test circuits**

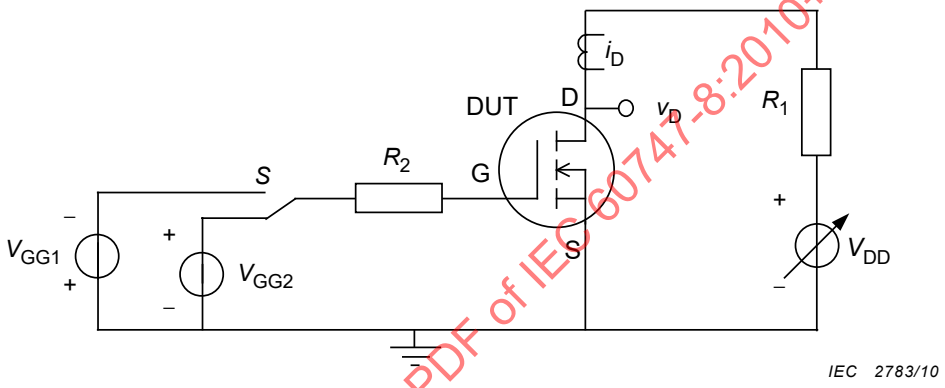


Figure 48 – Circuit for intermittent operating life

7.4 Type tests and routine tests

7.4.1 Type tests

Type tests are carried out on new products on a sample basis, in order to confirm the electrical and thermal ratings (limiting values) and characteristics to be given in the data sheet and to be referenced to the test limits for future routine tests.

Some or all of the type tests may be repeated from time to time on samples drawn from current production or deliveries, so as to confirm that the quality of the product continuously meets the specified requirements.

The minimum items of type tests to be carried out on FETs are listed in Table 3. Some of the type tests are destructive.

7.4.2 Routine tests

The routine tests are carried out on the current production or deliveries normally on a 100 % basis, in order to verify that the ratings (limiting values) and characteristics specified in the data sheet are met by each specimen. Routine tests may comprise distribution of the devices into groups. The minimum items of routine tests to be carried out on FETs are listed in Table 4, unless otherwise agreed between supplier and purchaser.

Table 4 – Minimum type and routine tests for FETs when applicable

Subclause		Type test	Routine test
Verification of ratings			
6.1.1.1	Drain-source voltage V_{DS*}	X	X
6.1.1.2	Gate-source voltage $\pm V_{GS*}$	X	
6.1.1.3	Gate-drain (d.c.) voltage (V_{GD*}) [b]	X	
6.1.1.4	Drain current (I_D)	X	
6.1.1.5	Pulse drain current I_{DM}	X	
6.1.1.6	Reverse drain current (~~I_{DRS}~~ I_{SS}) or (~~I_{DRX}~~ I_{SX})	X	
6.1.1.7	Peak reverse drain current (~~I_{DRM}~~ I_{SM})	X	X
6.1.1.1	Forward-bias safe operating area (FBSOA) [b]	X	X
6.1.1.2	Reverse biased safe operating area (RBSOA)	X	
6.1.1.3	Short circuit safe operating area (SCSOA)	X	
6.1.1.1	Repetitive avalanche energy (E_{AR}) [a]	X	X
6.1.1.2	Non-repetitive avalanche energy (E_{AS}) [a]	X	
Electrical characteristics			
6.2.1	Breakdown voltage, drain to source ($V_{(BR)DS*}$)	X	X
6.2.3	Drain leakage current (d.c.) (I_{DSS}, I_{DSR}, I_{DSX})	X	X
6.2.4	Gate leakage current (I_{GSS})	X	X
6.2.2	Gate-source off-state voltage $V_{GS(off)}$ (for type B)	X	X
6.2.2	Gate-source threshold voltage $V_{GS(th)}$ (for type C)	X	X
6.2.5	Drain-source on-state resistance ($r_{DS(on)}$)	X	X
6.2.15	Drain-source reverse voltage (~~V_{DSR}~~ V_{SD})	X	
6.2.6	Switching times ($t_{d(on)}$, t_r, $t_{d(off)}$, and t_f)	X	
6.2.10	Common source short-circuit input capacitance C_{iss}	X	
6.2.13	Internal gate resistance r_g	X	
Electrical characteristics			
6.2.11	Common source short-circuit output capacitance C_{oss}	X	
6.2.12	Common source short-circuit reverse transfer capacitance C_{rss}	X	
6.2.17	Forward transconductance g_{fs}	X	
6.2.9	Total gate charge Q_G	X	
	Threshold gate charge $Q_{GS(th)}$ [b]	X	
	Plateau gate charge $Q_{GS(pl)}$ [b]	X	
	Gate drain charge Q_{GD} [b]	X	
6.2.14	MOSFET forward recovery time (t_{fr}) and MOSFET forward recovery charge (Q_f)	X	X
6.2.20	Thermal resistance junction to case ($R_{th(j-c)}$)	X	
6.2.20	Transient thermal impedance junction to case ($Z_{th(j-c)}$) [b]	X	X
Electrical endurance tests			
7.3.1	High temperature blocking (HTRB)	X	
7.3.2	High temperature gate bias (HTGB)	X	
7.3.3	Intermittent operating life	X	

[a] Terms are applied for avalanche type MOSFETs only.

[b] Terms are applied where appropriate.

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IEC 60747-2:2000, *Semiconductor devices – Discrete devices and integrated circuits – Part 2: Rectifier diodes*

IEC 60747-8

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FINAL VERSION

Semiconductor devices – Discrete devices – Part 8: Field-effect transistors

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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SEMICONDUCTOR DEVICES – DISCRETE DEVICES –

Part 8: Field-effect transistors

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This consolidated version of the official IEC Standard and its amendment has been prepared for user convenience.

IEC 60747-8 edition 3.1 contains the third edition (2010-12) [documents 47E/398/FDIS and 47E/406/RVD] and its amendment 1 (2021-06) [documents 47E/726/CDV and 47E/744/RVC].

This Final version does not show where the technical content is modified by amendment 1. A separate Redline version with all changes highlighted is available in this publication.

International Standard IEC 60747-8 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This third edition constitutes a technical revision.

The main changes with respect to the previous edition are listed below.

a) ”Clause 3 Classification” was moved and added to Clause 1.
b) “Clause 4 Terminology and letter symbols” was divided into “Clause 3 Terms and definitions” and “Clause 4 Letter symbols” was amended with additions and deletions.
c) Clause 5, 6 and 7 were amended with necessary additions and deletions.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2:.

This Part 8 should be used in conjunction with IEC 60747-1:2006.

A list of all the parts in the IEC 60747 series, under the general title *Semiconductor devices – Discrete devices*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of the base publication and its amendment will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

SEMICONDUCTOR DEVICES – DISCRETE DEVICES –

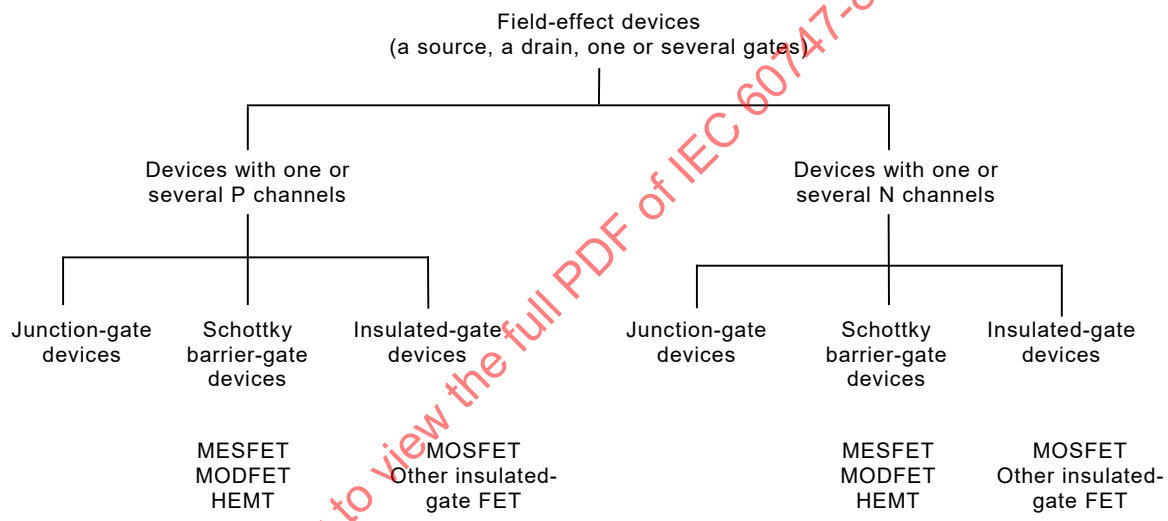
Part 8: Field-effect transistors

1 Scope

This part of IEC 60747 gives standards for the following categories of field-effect transistors:

– type A: junction-gate type;
– type B: insulated-gate depletion (normally on) type;
– type C: insulated-gate enhancement (normally off) type.

Since a field-effect transistor may have one or several gates, the classification shown below results:



NOTE 1 Schottky barrier-gate and insulated gate devices include depletion type devices and enhancement type devices.

NOTE 2 MOSFETs for some applications may not have inverse diode characteristics in the data sheet. Special circuit element structures to eliminate body diode are under development for such applications. MOSFET applications such as motor control equipment need to specify the inverse diode characteristics in the MOSFET to use the inverse diode as a free wheeling diode.

NOTE 3 The graphical symbol only for type C is used in this standard. The standard equally applies for P-channel and for type A and B devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61340 (all parts), *Electrostatics*

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*

IEC 60747-7:2000, *Semiconductor devices – Part 7: Bipolar transistors*

IEC 60749-23:2004, *Semiconductor devices – Mechanical and climatic test methods – Part 23: High temperature operating life*

IEC 60749-34, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling*

3 Terms and definitions

For the purpose of this document, the following terms and definitions apply.

3.1 Types of field-effect transistors

3.1.1
N-channel field-effect transistor
field-effect transistor that has one or more N-type conduction channels

3.1.2
P-channel field-effect transistor
field-effect transistor that has one or more P-type conduction channels

3.1.3
junction-gate field-effect transistor
JFET
field-effect transistor in which

– the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;

– a gate region adjacent to the channel has the opposite conductivity type, thus forming with source, channel and drain region a PN junction

NOTE The gate-source voltage controls the conductivity of the conduction channel in the channel region by controlling the width of the gate space-charge region and hence also the remaining cross-section of the conduction channel.

3.1.4
insulated-gate field-effect transistor
IGFET
field-effect transistor in which

– one or more gate electrodes are electrically insulated from the body;

– the conductivity type of both the source and drain regions is opposite from that of the semiconductor body in which they are located;

– the principal current flows in a channel that is formed by an inversion layer connecting source and drain regions

NOTE The inversion layer is either already present at zero gate-source voltage or produced within the body at sufficiently high forward gate-source voltage by accumulation of the minority charge carriers of the body material. The conductance of the channel is controlled by the gate-source voltage, which controls the electric field between gate electrode and the body and hence the amount of accumulated minority charge carriers.

3.1.5
metal-oxide-semiconductor field-effect transistor
MOSFET
insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material

3.1.6
depletion-type (normally on) field-effect transistor
field-effect transistor in which an inversion layer present at the surface of the active semiconductor region causes an appreciable channel conductance that may be increased (decreased) by applying a forward (reverse) gate-source voltage

3.1.7
enhancement-type (normally off) field-effect transistor
field-effect transistor having substantially zero channel conductance at zero gate-source voltage, and in which a conduction channel may be obtained by applying a sufficiently high forward gate-source voltage, which induces an inversion layer below the gate electrode

3.1.8
single-gate field-effect transistor
field-effect transistor having a gate region, a source region, and a drain region

NOTE The term may be abbreviated to "field-effect transistor", if no ambiguity is likely to occur.

3.1.9
dual-gate field-effect transistor
field-effect transistor having two independent gate regions, a source region, and a drain region

3.1.10
schottky-barrier-gate field-effect transistor
field-effect transistor in which

– the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;
– one or more gate electrodes each form a Schottky-barrier with the channel region;

the gate-source voltage controls the conductance of the conduction channel by varying its cross-section

3.1.11
metal-semiconductor field-effect transistor
MESFET
Schottky-barrier-gate field-effect transistor in which the gate electrodes are metal

3.1.12
modulation-doped field-effect transistor or high electron mobility transistor
MODFET or HEMT
metal-semiconductor field-effect transistor in which a doped material forms a heterojunction with an undoped channel; the doped material supplies electrons to the undoped channel whose high electron mobility results in enhanced channel conductance

NOTE MODFET and HEMT should be used interchangeably.

3.2 General terms

3.2.1 Physical regions (of a field-effect transistor)

3.2.1.1
source (of a field-effect transistor)
physical region that is designed by the manufacturer to contain the supply region under the defined operating conditions to which the specifications refer

3.2.1.2
drain (of a field-effect transistor)
physical region that is designed by the manufacturer to contain the collection region under the defined operating conditions to which the specifications refer

3.2.1.3
gate (of an IGFET)
insulating layer between the gate electrode and the surface of the semiconductor body, below which the channel is or may be formed

3.2.1.4
gate (of an JFET)
region below the gate electrode that is of opposite conductivity type from that of the source, channel and drain regions

3.2.1.5
channel (of a depletion-type IGFET)
inversion layer technologically placed below the gate region

3.2.1.6
channel (of a JFET)
region between source region and drain region that has the same conductivity type as these two regions

3.2.1.7
subchannel (of an IGFET)
region between source region and drain region, excluding the channel region of a depletion-type IGFET and all pertinent transition zones

3.2.1.8
substrate (of a JFET or IGFET)
part of the original material that remains unchanged when the device elements are formed upon or within the original material

NOTE The original material may be a layer of semiconductor material cut from a single crystal, a layer of semiconductor material deposited on a supporting base, or the supporting base itself.

3.2.1.9
substrate (of a JFET or IGFET)
original semiconductor material before being processed

NOTE The intended meaning will become clear from the context in which the term is used. If necessary, distinction could be made between the "original substrate" and the "remaining substrate".

3.2.1.10
substrate (of a thin-film field-effect transistor)
insulator that supports the source and drain electrodes, the insulating gate layer, and the thin semiconductor layer

3.2.2 Functional regions

3.2.2.1
functional source region
supply region that delivers principal-current charge carriers into the channel

3.2.2.2
functional drain region
collection region that acquires principal-current charge carriers from the channel

3.2.2.3
channel (of a IGFET)
functional region through which the principal-current charge carriers pass and in which the carrier concentration is determined by the gate-source voltage, the principal current being the result of the drift field produced by the drain-source voltage

3.2.2.4
channel (of a JFET)
functional region through which the principal-current charge carriers pass and whose cross-section is determined by the applied gate-source voltage, the principal current being the result of the drift field produced by the drain-source voltage

3.2.2.5
subchannel space-charge region (of an IGFET)
space-charge region associated with the transition regions between the subchannel region on one side, and source region, channel region and drain region on the other side

3.2.2.6
functional subchannel region
remaining neutral part of the (physical) subchannel region that is confined by the surrounding subchannel space-charge region

3.3 Terms related to ratings and characteristics

3.3.1
gate cut-off current (of a junction-gate field-effect transistor)
current flowing in the gate terminal of a junction field-effect transistor when the pn junction is biased in the reverse direction

3.3.2
gate leakage current (of an insulated-gate field-effect transistor)
leakage current through the insulated-gate of an insulated-gate field-effect transistor

3.3.3
capacitances

3.3.3.1
(short-circuit) input capacitance
capacitance between the gate and source terminals with the drain terminal short-circuited to the source terminal for a.c. signals

3.3.3.2
(short-circuit) output capacitance
capacitance between the drain and source terminals with the gate terminal short-circuited to the source terminal for a.c. signals

3.3.3.3
reverse transfer capacitance
capacitance between the drain and gate terminals excluding parallel capacitances between drain and source, and gate and source

3.3.4
gate-source resistance
d.c. resistance between gate and source terminals at specified gate-source and drain-source voltages

3.3.5
drain-source on-state resistance
d.c. resistance between the drain and source terminals when the FET is in its on-state

3.3.6
gate charge
charge required to raise the gate-source voltage from zero to a specified value

3.3.6.1
total gate charge
charge that is required to raise the gate-source voltage from zero to a specified value and calculated by the equation below (see Figure 1)

$$Q_G = \int_{t0}^{t4} i_{GG}(t)\mathrm{d}t$$

3.3.6.2
threshold gate charge
charge required to raise gate-source from zero to $V_{GS(th)}$ and calculated by the equation below (see Figure 1)

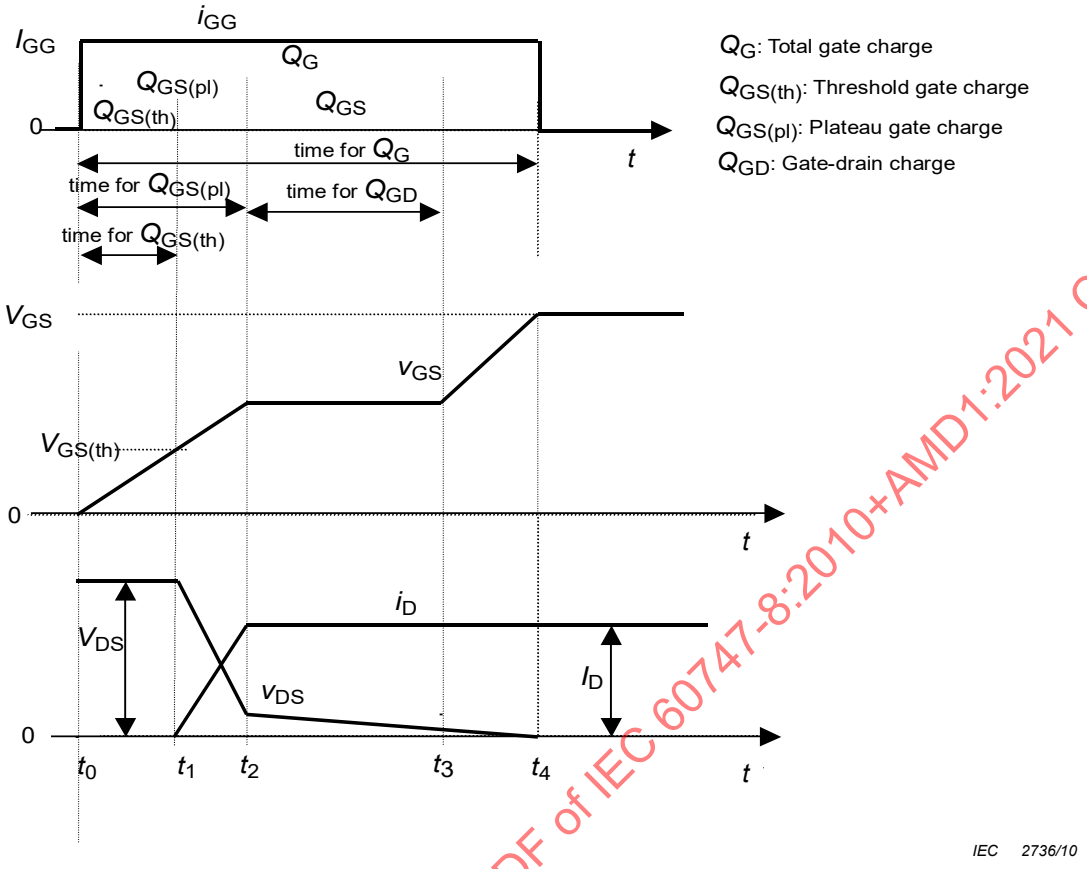
$$Q_{GS(th)} = \int_{t0}^{t1} i_{GG}(t)\mathrm{d}t$$

3.3.6.3
plateau gate charge
charge required to raise gate-source voltage from zero to plateau voltage $V_{GS(pl)}$ and calculated by the equation below (see Figure 1)

$$Q_{GS(pl)} = \int_{t0}^{t2} i_{GG}(t)\mathrm{d}t$$

3.3.6.4
gate drain charge
charge difference between beginning and end of plateau region, required to charge up C_{GD} and calculated by the equation below (see Figure 1)

$$Q_{GD} = \int_{t2}^{t3} i_{GG}(t)\mathrm{d}t$$



NOTE Time intervals indicated by arrow end lines are integral intervals to calculate the gate charges.

Figure 1 – Basic waveforms to specify the gate charges

3.3.7
overall efficiency
ratio of the output power to the sum of the input signal power and the d.c. input power

$$\eta_{tot} = \frac{P_{out}}{P_{in} + P_{(d.c.)}}$$

3.3.8
drain efficiency
ratio of the output power to the d.c. drain power

$$\eta_d = \frac{P_{out}}{P_{d(d.c.)}}$$

3.3.9
power-added efficiency
ratio of the difference between the output power and the input signal power to the d.c. input power

$$\eta_{add} = \frac{P_{out} - P_{in}}{P_{d(d.c.)}}$$

3.3.10
rate of rise of off-state voltage
rate of rise of drain-source off-state voltage induced during reverse recovery period of the inverse diode

3.3.11
reverse-bias safe operating area
drain current versus drain-source voltage region in which the MOSFET is able to turned-off repetitively with clamped inductive load without failure

3.3.12
short circuit safe operating area
drain current versus drain voltage region in which the MOSFET is able to turn on and off non repetitively without failure

3.3.13
avalanche energy (for avalanche devices)
avalanche energy capability during turn-off period

3.3.14
repetitive avalanche energy (for avalanche devices)
repetitive avalanche energy capability during turn-off period

3.3.15
non-repetitive avalanche energy (for avalanche devices)
non-repetitive avalanche capability during turn-off period (single pulse)

3.3.16
drain leakage current
drain current in the off-state

3.3.17
breakdown voltage, drain to source
drain-source breakdown voltage in the off-state

3.3.18
internal gate resistance
short-circuit internal gate resistance (see Figure 32)

3.3.19
switching times
input wave form is the gate to source voltage, and output waveform is the drain current (see IEC 60747-1:2006)

3.3.20
turn-on energy
value of the integral of the product of drain-source voltage V_{DS} and drain current I_D during turn-on described in the following equation: $E_{on} = \int_0^{t_1} i_D \times v_{DS} \times \mathrm{d}t$ (see Figure 2)

3.3.21
turn-off energy
value of the integral of drain-source voltage V_{DS} multiplied by drain current I_D during turn-off described in the following equation: $E_{off} = \int_{t_2}^{t_3} i_D \times v_{DS} \times dt$ (see Figure 2)

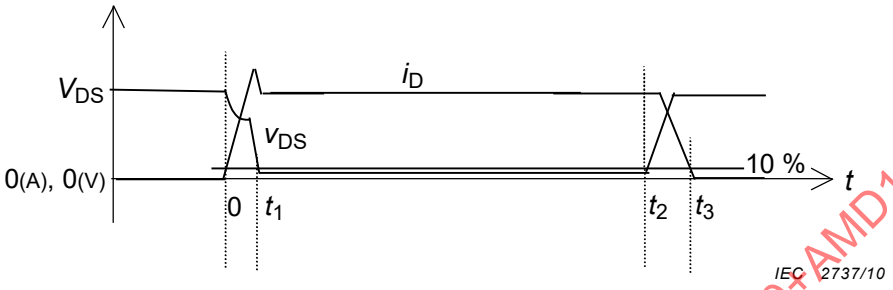


Figure 2 – Integral times for the turn-on energy E_{on} and turn-off energy E_{off}

3.3.22
output capacitance charge
charge required to change the voltage at output capacitance C_{oss} during turn-on and turn-off

3.3.23
gate-source plateau voltage
voltage during turn-on, where V_{GS} is relatively constant (Miller-Plateau) and during which C_{GD} is charged

NOTE See Figure 1.

3.3.24
drain-source reverse voltage
voltage across the MOSFET which results from the flow of current in the reverse direction from source to drain

3.3.25
MOSFET forward recovery current
recovery current of the MOSFET which results from the flow of current in the reverse direction from source to drain

3.3.26
MOSFET forward recovery time
recovery time of the MOSFET which results from the flow of current in the reverse direction from source to drain

3.3.27
MOSFET forward recovery charge
recovery charge of the MOSFET which results from the flow of current in the reverse direction from source to drain

3.3.28
MOSFET forward recovery energy
recovery energy of the MOSFET which results from the flow of current in the reverse direction from source to drain

3.4 Conventional used terms

Table 1 – Terms for MOSFET in this document and the conventional used terms for the inverse diode integrated in the MOSFETs for N-channel

Preferred terms	Letter symbol	Deprecated terms for inverse diode with MOSFET in off-state
Drain-source reverse voltage	V_{SD}	Inverse diode forward voltage
MOSFET forward recovery current	I_{fr}	Inverse diode reverse recovery current
MOSFET peak forward recovery current	I_{frm}	Inverse diode peak reverse recovery current
MOSFET forward recovery time	t_{fr}	Inverse diode reverse recovery time
MOSFET forward recovery charge	Q_f	Inverse diode reverse recovery charge
MOSFET forward recovery energy	E_{fr}	Inverse diode reverse recovery energy
Reverse drain current	I_S	Inverse diode forward current
Repetitive peak reverse drain current	I_{SRM}	Inverse diode repetitive peak forward current

4 Letter symbols

4.1 General

General letter symbols for MOSFETs are defined in Subclauses 4.4 and 4.5 of IEC 60747-1:2006.

4.2 Additional general subscripts

In addition to the list of recommended general subscripts given in 4.2.3 of IEC 60747-1:2006, the following special subscripts are recommended for field-effect transistors:

D, d = drain
G, g = gate
S, s = source or termination with a short circuit
B, b; U, u = substrate
T; th; (TO) = threshold
O = termination with an open circuit
R = termination with a resistor
X = termination with specified gate source voltage
pl = plateau

4.3 List of letter symbols

Name and designation	Letter symbol	Remarks
4.3.1 Voltage		
Drain-source (d.c.) voltage	V_{DS}	
Gate-source (d.c.) voltage	V_{GS}	
Gate-source cut-off voltage (of a junction field-effect transistor and of a depletion type insulated-gate field-effect transistor)	$V_{GS(OFF)}$; V_{GSoff}	
Gate-source threshold voltage (of an enhancement type insulated-gate field-effect transistor)	V_{GST}; $V_{GS(th)}$; $V_{GS(TO)}$	
Forward gate-source (d.c.) voltage	V_{GSF}	

Name and designation	Letter symbol	Remarks
Reverse gate-source (d.c.) voltage	V_{GSR}	
Gate-drain (d.c.) voltage	V_{GD}	
Source-substrate (d.c.) voltage	V_{SB}; V_{SU}	
Drain-substrate (d.c.) voltage	V_{DB}; V_{DU}	
Gate-substrate (d.c.) voltage	V_{GB}; V_{GU}	
Gate-gate voltage (for multi-gate devices)	$V_{G1 - G2}$	
Gate-source breakdown voltage with drain short-circuited to source	$V_{(BR)GSS}$	
Breakdown voltage, drain-source (for type B)	$V_{(BR)DSX}$	
Breakdown voltage, drain-source (for type C)	$V_{(BR)DSS}$	
Drain-source on-state voltage	$V_{DS(on)}$	
Drain-source reverse voltage	V_{DR}	
Gate-source plateau voltage	$V_{GS(pl)}$	
4.3.2 Currents		
Drain (d.c.) current	I_D	
Peak drain current	I_{DM}	
Drain current, at a specified gate-source condition	I_{DSX}	
Drain current, at a specified external gate-source resistance	I_{DSR}	
Drain current, with gate short-circuited to source (V_{GS} = 0)	I_{DSS}	
Source (d.c.) current (for P-channel)	I_S	
Peak source current (for P-channel)	I_{SM}	
Source current, at a specified gate-drain condition (for P-channel)	I_{SDX}	
Source current, with gate short-circuited to drain (V_{GD} = 0) (for P-channel)	I_{SDS}	
Forward gate current	I_{GF}	
Gate cut-off current (of a junction field-effect transistor), with source open-circuited	I_{GDO}	
Gate-cut-off current (of a junction field-effect transistor), with drain open-circuited	I_{GSO}	
Gate cut-off current (of a junction field-effect transistor), with drain short-circuited to source	I_{GSS}	
Gate leakage current (of an insulated-gate field-effect transistor), with drain short-circuited to source	I_{GSS}	
Gate cut-off current (of a junction field-effect transistor), with specified drain-source circuit conditions	I_{GSX}	
Substrate current	I_B; I_U	
4.3.3 Power dissipation		
Total power dissipation	P_{tot}	
4.3.4 Small-signal parameters		
Drain-source resistance	r_{ds}	
Gate-source resistance	r_{gs}	
Gate-drain resistance	r_{gd}	

Name and designation	Letter symbol	Remarks
Gate resistance (with V_{DS} = 0 or v_{ds} = 0)	r_{gss}	
Drain-source on-state resistance	$r_{ds(on)}$	
Drain-source off-state resistance	$r_{ds(off)}$	
Internal gate resistance	R_g	
Open-circuit gate-source capacitance (drain-source and gate-drain open-circuited to a.c.)	C_{gso}	
Open-circuit gate-drain capacitance (drain-source and gate-source open-circuited to a.c.)	C_{gdo}	
Open-circuit drain-source capacitance (gate-drain and gate-source open-circuited to a.c.)	C_{dso}	
Short-circuit input capacitance in common-source configuration; gate-source capacitance (drain-source short-circuited to a.c.)	C_{iss}; C_{11ss}	
Short-circuit output capacitance in common-source configuration; drain-source capacitance (gate-source short-circuited to a.c.)	C_{oss}; C_{22ss}	
Common-source reverse transfer capacitance with input short-circuited to a.c.	C_{rss}; C_{12ss}	
Short-circuit output capacitance in common-drain configuration (gate-drain short-circuited to a.c.)	C_{ods}; C_{22ds}	
Gate-source capacitance (in the π equivalent circuit)	C_{gs}	
Gate-drain capacitance (in the π equivalent circuit)	C_{gd}	
Drain-source capacitance (in the π equivalent circuit)	C_{ds}	
Short-circuit input conductance in common-source configuration	G_{iss}	
Short-circuit output conductance in common-source configuration	G_{oss}	
Gate-source conductance (in the π equivalent circuit)	G_{gs}	
Gate-drain conductance (in the π equivalent circuit)	G_{gd}	
Drain-source conductance (in the π equivalent circuit)	G_{ds}	
Short-circuit input admittance	$y_{is} = Re_{(yis)} + j\omega C_{is}$ $y_{11s} = Re_{(y11s)} + j\omega C_{11s}$	
Short-circuit reverse transfer admittance	$y_{rs} = Re_{(yrs)} + j\omega C_{rs}$ $y_{12s} = Re_{(y12s)} + j\omega C_{12s}$	
Short-circuit forward transfer admittance	$y_{fs} = Re_{(yfs)} + jIm_{yfs}$ $y_{21s} = Re_{(y21s)} + jIm_{y21s}$	
Short-circuit output admittance	$y_{os} = Re_{(yos)} + j\omega C_{os}$ $y_{22s} = Re_{(y22s)} + j\omega C_{22s}$	
Modulus of the short-circuit reverse transfer admittance	$\lvert y_{rs} \rvert$; $\lvert y_{12s} \rvert$	
Phase of the short-circuit reverse transfer admittance	φ_{yrs}; φ_{y12s}	
Modulus of the short-circuit forward transfer admittance	$\lvert y_{fs} \rvert$; $\lvert y_{21s} \rvert$	
Phase of the short-circuit forward transfer admittance	φ_{yfs}; φ_{y21s}	
Forward transconductance (in the π equivalent circuit)	g_{ms}; g_m; g_{fs}	

Name and designation	Letter symbol	Remarks
Input reflection coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	 s_{11s} or s_{is} s_{11g} or s_{ig} s_{11d} or s_{id}	
Output reflection coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	 s_{22s} or s_{os} s_{22g} or s_{og} s_{22d} or s_{od}	
Forward transmission coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	 s_{21s} or s_{fs} s_{21g} or s_{fg} s_{21d} or s_{fd}	
Reverse transmission coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	 s_{12s} or s_{rs} s_{12g} or s_{rg} s_{12d} or s_{rd}	
4.3.5 Other parameters		
Total gate charge	Q_G	
Plateau gate charge	$Q_{GS(pl)}$	
Gate-drain charge	Q_{GD}	
Threshold gate charge	$Q_{GS(th)}$	
Power gain	G_P; G_p	
Output power at specified input power	P_o	
Overall efficiency	η_{tot}	
Drain efficiency	η_d	
Power added efficiency	η_{add}	
Cut-off frequency (in the common-source configuration)	f_{yfs}	
Noise voltage	V_n	
Noise figure	F	
Temperature coefficient of drain current	α_{ID}	
Temperature coefficient of drain-source resistance	α_{rds}	
Turn-on delay time	$t_{d(on)}$	Switching times (see Figure 3)
Turn-off delay time	$t_{d(off)}$	
Rise time	t_r	
Fall time	t_f	
Turn-on time	t_{on}	$t_{on} = t_{d(on)} + t_r$
Turn-off time	t_{off}	$t_{off} = t_{d(off)} + t_f$
Turn-on energy	E_{on}	
Turn-off energy	E_{off}	
Repetitive avalanche energy	E_{AR}	
Non-repetitive single pulse avalanche energy	E_{AS}	
Frequency of unity forward transmission coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	 f_{ss} or f_{iss} f_{sg} or f_{isg} f_{sd} or f_{isd}	 $f_{ss} = f$ for $\lvert s_{21s} \rvert = 1$ $f_{sg} = f$ for $\lvert s_{21g} \rvert = 1$ $f_{sd} = f$ for $\lvert s_{21d} \rvert = 1$

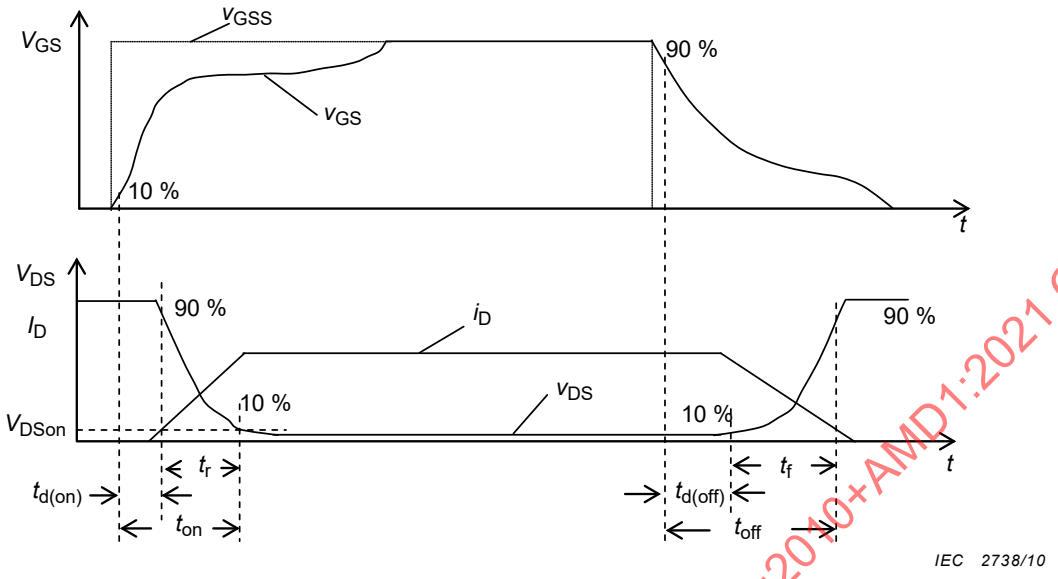


Figure 3 – Switching times

Name and designation	Letter symbol	Remarks
4.3.6 Matched-pair field-effect transistors		
Difference of gate leakage currents (for insulated-gate field-effect transistors) and difference of gate cut-off currents (for junction field-effect transistors)	$I_{G1} - I_{G2}$	The smaller value is subtracted from the larger value
Ratio of drain currents for zero gate-source voltage	I_{DSS1} / I_{DSS2}	The smaller of the two values is taken as the numerator
Difference of small-signal common-source output conductances	$g_{os1} - g_{os2}$	The smaller value is subtracted from the larger value
Ratio of small-signal common-source forward transfer conductances	g_{fs1} / g_{fs2}	The smaller of the two values is taken as the numerator
Difference of gate-source voltages	$V_{GS1} - V_{GS2}$	The smaller value is subtracted from the larger value
Change in difference of gate-source voltages between two temperatures	$\lvert\Delta(V_{GS1} - V_{GS2})\rvert_{\Delta T}$	
4.3.7 Inverse diodes integrated in MOSFETs for N-channel		
Drain-source reverse voltage	V_{SD}	Forward voltage of the inverse diode
MOSFET forward recovery current	I_{fr}	Reverse recovery current of the inverse diode
MOSFET peak forward recovery current	I_{frm}	Peak reverse recovery current of the inverse diode
MOSFET forward recovery time	t_{fr}	Reverse recovery time of the inverse diode
MOSFET forward recovery charge	Q_f	Reverse recovery charge of the inverse diode
MOSFET forward recovery energy	E_{fr}	Reverse recovery energy of the inverse diode
Reverse drain current	I_S	Forward current of the inverse diode
Repetitive peak reverse drain current	I_{SRM}	Repetitive peak forward current of the inverse diode

5 Essential ratings and characteristics

5.1 General

5.1.1 Device categories

Field-effect transistors are divided into three categories:

– type A: junction-gate type;
– type B: insulated-gate depletion type;
– type C: insulated-gate enhancement type.

5.1.2 Multiple-gate devices

For multiple-gate devices, the required gate ratings and characteristics shall be given for each gate separately, except where otherwise stated.

5.1.3 Handling precautions

Because of the very high input resistance of field-effect transistors, the gate insulation layer (for insulated-gate types) or the gate junction (for junction-gate types) may be irreversibly damaged if an excessive voltage is allowed to build up, e.g. due to contact with electrostatically charged persons, leakage currents from soldering irons, etc.

The requirements of IEC 60747-1:2006 Clause 8 apply to these devices.

	TYPES		
	A	B	C
5.2 Ratings (limiting values)			
5.2.1 Temperatures			
5.2.1.1 Minimum and maximum storage temperatures (T_{stg})	+	+	+
5.2.1.2 Virtual junction temperature (T_{vj})	+	+	+
Maximum rated value.			
5.2.2 Power dissipation (P_{tot})	+	+	+
Maximum total power dissipation over the specified range of operating temperatures (ambient or case).			
5.2.3 Safe operating area (SOA) for MOSFET only			
Over the specified range of operating temperatures, under specified pulse conditions.			
5.2.3.1 Forward-bias safe operating area (FBSOA)		+	+
Maximum safe operating area of V_{DS} and I_D in conduction state.			
5.2.3.2 Reverse-bias safe operating area (RBSOA)		+	+
Maximum safe operating area of V_{DS} and I_D during turn-off state.			
5.2.3.3 Short-circuit safe operating area (SCSOA)		+	+
Non-repetitive maximum safe operating area of V_{DS} and I_D during turn-off			

	TYPES		
	A	B	C
state from short circuit condition.			
5.2.4 Voltages and currents			
Ratings apply over the operating temperature range unless otherwise specified.			
5.2.4.1 Maximum drain-source voltage	+	+	+
Under specified gate conditions.			
5.2.4.2 Maximum reverse gate-source voltage and, where appropriate, maximum forward gate-source voltage	+	+	+
Under specified drain conditions.			
5.2.4.3 Maximum gate-substrate voltage		+	+
Under specified source conditions;			
For insulated-gate field-effect transistors with separate source and substrate terminals (chopper or analog-switch types)			
5.2.4.4 Maximum drain-substrate voltage		+	+
Under specified gate to source conditions;			
For insulated-gate field-effect transistors with separate source and substrate terminals (chopper or analog-switch types)			
5.2.4.5 Maximum source-substrate voltage		+	+
Under specified gate to drain conditions.			
For insulated-gate field-effect transistors with separate source and substrate terminals (chopper or analog-switch types)			
5.2.4.6 Maximum drain current (I_D)	+	+	+
5.2.4.7 Maximum peak drain current (I_{DM})		+	+
Under specified pulse conditions.			
For MOSFET only.			
5.2.4.8 Maximum continuous (d.c.) reverse drain current (I_S) (forward current of the inverse diode)		+	+
5.2.4.9 Maximum peak reverse drain current (I_{SM}) (Maximum peak forward current of the inverse diode)		+	+
Under specified pulse conditions.			
5.2.4.10 Maximum forward gate current	+		
5.3 Characteristics			
Characteristics are to be given at 25 °C, except where otherwise stated and at (at least) one other temperature.			
5.3.1 Characteristics for low-frequency amplifier			

	TYPES		
	A	B	C
5.3.1.1 Gate cut-off current	+		
Gate leakage current Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature. Together with: Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.		+	+
5.3.1.2 Drain cut-off current Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	+
5.3.1.3 Drain current at zero gate-source voltage (I_{DSS}) Minimum and maximum values, for zero gate-source voltage, at a specified drain-source voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	
5.3.1.4 Drain current at specified gate-source voltage (I_{DSX}) Minimum and maximum values, for specified gate-source and drain-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			+
5.3.1.5 Gate-source cut-off voltage ($V_{GSoff)}$) Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	
5.3.1.6 Gate-source threshold voltage ($V_{GS(th)}$) Minimum and maximum values, at a specified high value of drain-source voltage, and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			+
5.3.1.7 Short-circuit input capacitance (C_{iss}) Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the output short-circuited to a.c.	+	+	+
5.3.1.8 Short-circuit output conductance and, where appropriate, capacitance (g_{oss}, C_{oss})	+	+	+

	TYPES		
	A	B	C
Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.			
5.3.1.9 Reverse transfer capacitance (where appropriate) (C_{rss})	+	+	+
Maximum small-signal value, in common-source configuration with input open-circuit to a.c., under specified bias conditions and at a specified low frequency.			
5.3.1.10 Forward transconductance (g_{ms}, g_m, g_{fs})	+	+	+
Minimum and maximum values under specified bias conditions and at a specified low frequency.			
5.3.1.11 For low-noise applications, noise voltage and, where appropriate, noise figure (V_n, F)	+	+	+
Maximum value, in common-source configuration, under specified conditions of bias, source resistance, center frequency and power bandwidth.			
5.3.1.12 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-a)}$) or ($R_{th(j-c)}$)	+	+	+
Maximum value.			
5.3.2 Characteristics for high-frequency amplifier			
5.3.2.1 Gate cut-off current	+		
Gate leakage current		+	+
Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
Together with:			
Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.2.2 Drain cut-off current	+	+	+
Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.2.3 Drain current at zero gate-source voltage (I_{DSS})	+	+	
Minimum and maximum values, for zero gate-source voltage and a specified drain-source voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.2.4 Drain current at specified gate-source voltage (I_{DSX})			+
Minimum and maximum values, for specified drain-source voltage, other terminal connections being specified, at a temperature of 25 °C or at one			

	TYPES		
	A	B	C
other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.2.5 Gate-source cut-off voltage (V_{GSoff}) Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	
5.3.2.6 Gate-source threshold voltage ($V_{GS(th)}$) Minimum and maximum values, at a specified high value of drain-source voltage, and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			+
5.3.2.7 y-parameters			
5.3.2.7.1 For all FETs under specified values of bias and frequency:	+	+	+
y_{is} – real and imaginary parts, maximum values;			
y_{os} – real and imaginary parts, maximum values;			
y_{fs} – real and imaginary parts, minimum and maximum values (see also 5.3.2.7.2);			
y_{rs} – real and imaginary parts, maximum values.			
5.3.2.7.2 For power MOSFET as alternative to y_{fs}, forward transconductance (g_{ms}, g_m, g_{fs}): Minimum value with drain-source short circuit to a.c., for specified drain-source voltage and drain current, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.		+	+
5.3.2.8 Output power at specified input power (P_o) Minimum and typical values under specified circuit and bias conditions	+	+	+
or: power gain (G_p) Minimum and typical values under specified circuit and bias conditions	+	+	+
5.3.2.9 Where appropriate, overall efficiency (η_{tot}) Minimum and typical values under specified circuit and bias conditions	+	+	+

NOTE $\eta_{tot} = \dfrac{P_{out}}{P_{in} + P_{(d.c.)}}$

	TYPES		
	A	B	C
5.3.2.10 Alternatively, collector efficiency (η_d)	+	+	+
Minimum and typical values under specified circuit and bias conditions			
NOTE $\eta_d = \frac{P_{out}}{P_{d(d.c.)}}$			
5.3.2.11 Power added efficiency (η_{add})	+	+	+
Minimum and typical values under specified circuit and bias conditions			
NOTE $\eta_{add} = \frac{P_{out} - P_{in}}{P_{d(d.c.)}}$			
5.3.2.12 Noise figure (F)	+	+	+
Maximum value, under specified conditions of bias, source impedance, centre frequency and power bandwidth. These conditions must be those which provide the lowest value of the noise figure.			
5.3.2.13 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-a)}$) or ($R_{th(j-c)}$)		+	+
Maximum value.			
5.3.3 Characteristics for high and low power switching and chopper			
5.3.3.1 Gate cut-off current	+		
Gate leakage current		+	+
Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
Together with:			
Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.3.2 Drain cut-off current	+	+	+
Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.3.3 Gate-source cut-off voltage (V_{GSoff})	+	+	
Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			

	TYPES		
	A	B	C
5.3.3.4 Gate-source threshold voltage ($V_{GS(th)}$) Minimum and maximum values, at a specified high value of drain-source voltage and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate-voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			+
5.3.3.5 On-state characteristics			
5.3.3.5.1 Drain-source on-state voltage; ($V_{DS(on)}$) **Drain-source saturation voltage** Maximum value, at a specified large value of drain current and gate-source voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature. or (for MOSFET only):	+	+	+
5.3.3.5.2 Drain-source on-state resistance ($r_{DS(on)}$) Maximum value, at a specified large value of drain current and gate-source voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.		+	+
5.3.3.5.3 Short-circuit output conductance (g_{oss}) Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.	+	+	+
5.3.3.6 Short-circuit input capacitance (C_{iss}) Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the output short-circuited to a.c.	+	+	+
5.3.3.7 Short-circuit output capacitance (where appropriate) (C_{oss}) Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.	+	+	+
5.3.3.8 Reverse transfer capacitance (where appropriate) (C_{rss}) Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.	+	+	+
5.3.3.9 Switching times (see Figure 3) They are stated under the following conditions: a) common-source configuration; b) specified condition in which output loading capacitance and resistance shall be included; c) input pulse transition times, amplitude and repetition frequency to be specified;	+	+	+

	TYPES		
	A	B	C
d) $V_{GS(off\text{-}state)}$ must be greater than or equal to the maximum gate-source cut-off voltage for type A and B devices, or lower than the minimum gate-source threshold voltage for type C devices;			
e) $V_{GS(on\text{-}state)}$ must correspond to a high drain current;			
f)Maximum values of: $t_{d(on)}$, t_r, $t_{d(off)}$ and t_f separately.			
NOTE Where $t_{d(off)}$ is only a small fraction of the total turn-off time (t_{off}), a maximum value for t_{off} alone is adequate.			
5.3.3.10 Characteristics of the inverse diode (for power MOSFET) only			
5.3.3.10.1 Drain-source reverse voltage (V_{SD}) (Forward voltage of the inverse diode)		+	+
Maximum value at specified reverse drain current (I_S) (forward current of the inverse diode) and at V_{GS} = 0.			
5.3.3.10.2 Forward recovery time (t_{fr}) (Reverse recovery time of the inverse diode)		+	+
Maximum value under specified conditions.			
5.3.3.10.3 Peak forward recovery current (I_{frm}) (Peak reverse recovery current of the inverse diode)		+	+
Maximum value under specified conditions.			
5.3.3.10.4 Forward recovery energy (E_{fr}) (reverse recovery energy of the inverse diode)		+	+
Maximum value under specified conditions.			
5.3.3.11 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j\text{-}a)}$) or ($R_{th(j\text{-}c)}$)		+	+
Maximum value.			
5.3.3.12 Drain cut-off current or drain-source off-state resistance	+	+	+
Maximum value of drain-source cut-off current (or alternatively, minimum value of drain-source off-state resistance), at specified low values of drain-source voltage for both polarities and at a specified gate-source voltage.			
5.3.3.13 Forward transconductance (g_{ms}, g_m, g_{fs}) (for power MOSFET only)		+	+
Minimum value, for specified drain-source voltage and drain current, at a temperature of 25 °C at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.3.14 Breakdown voltage, drain to source ($V_{(BR)DSX}$) (for type B)		+	
Minimum value, at maximum off-state drain current I_{D0} and specified gate-source voltage.			
5.3.3.15 Breakdown voltage, drain to source ($V_{(BR)DSS}$) (for type C)			+
Minimum value, at maximum off-state drain current I_{D0} and gate-source shorted.			

	TYPES		
	A	B	C
5.3.3.16 Gate-source on-state voltage ($V_{GSM(on)}$) (for type B and C) Maximum value in the on-state		+	+
5.3.3.17 Internal gate resistance (r_g), where appropriate Maximum and/or typical value, under the electrical conditions specified and at specified frequency		+	+
5.3.3.18 Turn-on energy (per pulse) (E_{on}), where appropriate Maximum value under specified conditions: – drain-source voltage before turn-on; – drain peak current after turn-on; – gate-source voltage; – resistance in the gate-source circuit; – case or ambient temperature or virtual junction temperature.		+	+
5.3.3.19 Turn-off energy (per pulse) (E_{off}), where appropriate Maximum value under specified conditions: – drain peak current before turn-off; – drain-source voltage after turn-off; – gate-source voltage; – resistance in the gate-source circuit; – case or ambient temperature or virtual junction temperature.		+	+
5.3.3.20 Gate charges (Q_G, Q_{GD}, $Q_{GD(th)}$, $Q_{GS(pl)}$) Typical values at specified drain current (I_D), drain-source voltage (V_{DS}) and gate current (I_{GG}) (see Figure 1)		+	+
5.3.3.21 Thermal impedance channel-to-ambient or channel-to-case ($Z_{th(j-a)}$) or ($Z_{th(j-c)}$), where appropriate Maximum value.		+	+
5.3.4 Characteristics for low-level amplifier			
5.3.4.1 Gate cut-off current	+		
Gate leakage current Maximum value, at specified gate-source of drain-gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature. Together with: Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.		+	+

	TYPES		
	A	B	C
5.3.4.2 Drain cut-off current Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	+
5.3.4.3 Drain current at zero gate-source voltage (I_{DSS}) Minimum and maximum values, at a specified drain-source voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	
5.3.4.4 Drain current at specified gate-source voltage (I_{DSX}) Minimum and maximum values, for specified gate-source and drain-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			+
5.3.4.5 Gate-source cut-off voltage (V_{GSoff}) Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	
5.3.4.6 Gate-source threshold voltage ($V_{GS(th)}$) Minimum and maximum values, at a specified high value of drain-source voltage and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			+
5.3.4.7 Noise voltage (where appropriate) (V_n) Maximum value in common-source configuration, under specified circuit conditions.	+	+	+
5.3.4.8 Small signal forward transconductance (g_{ms}, g_m, g_{fs}) Minimum value, for specified drain-source voltage and drain current, at an operating temperature of 25 °C and, where appropriate, at a specified higher temperature, at a specified frequency.	+	+	+
5.3.4.9 Characteristics of the inverse diode (where appropriate)			
5.3.4.9.1 Reverse drain current (I_S) (forward current of the inverse diode) Maximum value at specified Reverse drain current (I_S) and at V_{GS} = 0.		+	+
5.3.4.9.2 Forward recovery time (t_{fr}) (Reverse recovery time of the inverse diode) Maximum value under specified conditions.		+	+

	TYPES		
	A	B	C
5.3.4.10 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-a)}$) or ($R_{th(j-c)}$) Maximum value.		+	+
5.3.5 Characteristics for voltage-controlled resistor			
5.3.5.1 Gate cut-off current	+		
Gate leakage current Maximum value, at specified gate-source or gate-drain voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.		+	+
5.3.5.2 Small-signal drain-source resistance (r_{ds}) Minimum and maximum small-signal values, at zero drain-source voltage and at two or more specified gate-source voltages, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	+
5.3.5.3 Non-linearity distortion factor of drain-source small-signal resistance, where appropriate Maximum value (total or individual harmonic contents), at specified drain-source and gate-source voltages and at specified drain-source a.c. signal, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	+
5.3.5.4 Temperature coefficient of the small-signal drain-source resistance Typical value.	+	+	+
5.3.5.5 Drain-source capacitance Maximum small-signal value, at zero drain-source voltage, at a specified gate-source voltage, with the gate short-circuited for a.c. to the source.	+	+	+
5.3.5.6 Drain-gate capacitance Maximum small-signal value at zero drain-source voltage, at a specified gate-source voltage.	+	+	+
5.3.5.7 Gate-source capacitance (where appropriate) Maximum small-signal value at zero drain-source voltage, at a specified gate-source voltage, with the drain short-circuited for a.c. to the source.	+	+	+
5.3.5.8 Forward transconductance (g_{ms}, g_m, g_{fs}) (for power MOSFET only) Minimum value, for specified drain-source voltage and drain current, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.		+	+

	TYPES		
	A	B	C
5.3.5.9 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-a)}$) or ($R_{th(j-c)}$) Maximum value.		+	+
5.3.6 Specific characteristics of matched-pair field-effect transistors for low-frequency differential			
5.3.6.1 Difference of gate cut-off currents	+		
Difference of gate leakage currents ($I_{G1} - I_{G2}$) Maximum absolute value, at specified drain-gate or drain-source voltage and drain current.		+	+
5.3.6.2 Ratio of drain currents			
5.3.6.2.1 Ratio of drain currents for zero gate-source voltage (I_{DSS1} / I_{DSS2}) Minimum value of the ratio of the drain currents, at a specified drain-source voltage and zero gate-source voltage.	+	+	
5.3.6.2.2 Ratio of drain currents for specified gate-source voltage Minimum value of the ratio of the drain currents, at specified drain-source and gate-source voltages. NOTE This ratio should be stated as the smaller value divided by the larger value.			+
5.3.6.3 Difference of small-signal common-source output conductances, where appropriate ($g_{os1} - g_{os2}$) Maximum absolute value of the difference of the output conductances, at specified drain-gate or drain-source voltage, drain current, and frequency.	+	+	+
5.3.6.4 Ratio of small-signal common-source forward transconductances ($g_{fs1} - g_{fs2}$) Minimum value of the ratio of forward transconductances, at specified drain-gate or drain-source voltage, drain current, and frequency NOTE This ratio should be stated as the smaller value divided by the larger value.	+	+	+
5.3.6.5 Difference of gate-source voltages ($V_{GS1} - V_{GS2}$) Maximum absolute value of the difference of the gate-source voltages, at specified drain-gate or drain-source voltage and drain current.	+	+	+
5.3.6.6 Change in difference of gate-source voltages between two temperatures ($\lvert\Delta(V_{GS1} - V_{GS2})\rvert_{\Delta T}$) Maximum absolute value of the change of the difference of the gate-source voltages (as in 5.3.6.5) between two specified temperatures, at the same specified drain-gate or drain-source voltage and drain current.	+	+	+

6 Measuring methods

6.1 General

The polarities of the power supplies, shown in the circuits in this standard, are applicable to N-channel type devices. However, the circuits can be adapted for P-channel type devices by changing the polarities of the meters and the power supplies.

The general precautions listed in Subclause 6.4 of IEC 60747-1:2006 apply. In addition, special care shall be taken to use low-ripple d.c. supplies and to decouple adequately all bias supply voltages at the frequency of measurement. For four-terminal devices, the fourth terminal shall be connected as specified.

When handling these devices, the handling precautions given in IEC 61340 shall be observed. The entire circuit in the following subclauses shall be placed inside an electrostatic screen.

6.2 Verification of ratings (limiting values)

After the following test, confirm the FET characteristics specified in Table 2.

Table 2 – Acceptance defining characteristics

Characteristics	Acceptance criteria
I_{GSS}	I_{GSS}< USL
I_{DS*}	I_{DS*} < USL
$V_{GS(th)}$ (or $V_{GS(off)}$)	$V_{GS(th)}$ < USL or $V_{GS(th)}$ >LSL
$V_{DS(on)}$	$V_{DS(on)}$ < USL
$r_{DS(on)}$	$r_{DS(on)}$ < USL (only for MOSFET)
USL: upper specified limit LSL: lower specified limit	

6.2.1 Voltages and currents

6.2.1.1 Drain-source voltage (d.c.) (V_{DS*})

NOTE * = O, R, S or X.

– **Purpose**

To verify the drain-source voltage (d.c.) V_{DS*} under specified conditions.

– **Circuit diagram**

See Figure 4 below.

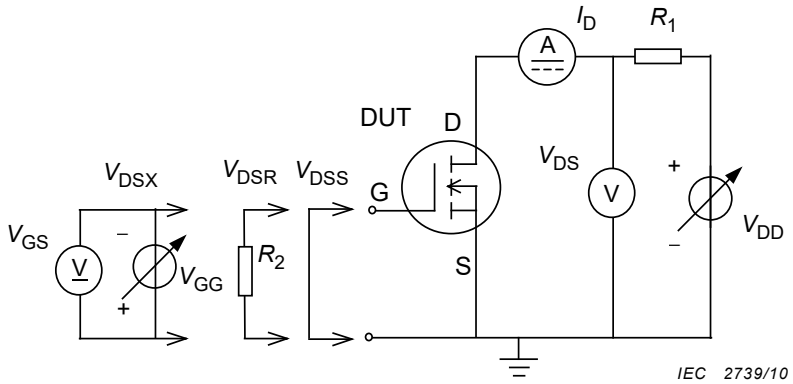


Figure 4 – Circuit diagram for testing of drain-source voltage

– **Circuit description and requirements**

V_{DD} and V_{GG} are the d.c. voltage supply. R_1 is a circuit protection resistor.

– **Testing procedure**

The gate-source is set to specified conditions. V_{DD} is increased until drain-source voltage measured on voltmeter V_{DS} reaches the specified drain-source voltage (d.c.) V_{DS*}. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Gate-source bias conditions
- Drain-source voltage: rated drain-source voltage

6.2.1.2 Gate-source (d.c.) voltage (V_{GS*})

– **Purpose**

To verify the gate-source (d.c.) voltage for both polarities, under specified conditions.

– **Circuit diagram**

See Figure 5 below.

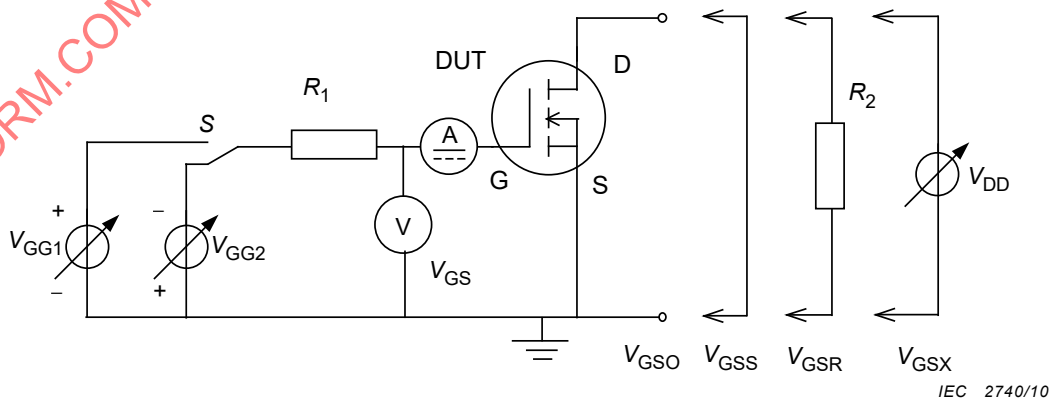


Figure 5 – Circuit diagram for testing of gate-source voltage

– **Circuit description and requirements**

V_{DD}, V_{GG1} and V_{GG2} are the d.c. voltage supply. V_{GSX} is applied only for gate reverse biased condition of V_{GG2}. R_1 is a protective resistor.

– **Testing procedure**

Drain-source voltage is set to specified conditions. V_{GG} is increased until gate-source voltage measured on voltmeter V_{GS} reaches the specified gate-source voltage V_{GS*}. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Reference point or junction temperature T_{vj};
- Drain-source bias conditions;
- Gate-source voltage: rated gate-source voltage.

6.2.1.3 Gate-drain (d.c.) voltage (V_{GD*})

– **Purpose**

To verify the gate-drain (d.c.) voltage for both polarities, under specified conditions.

– **Circuit diagram**

See Figure 6 below.

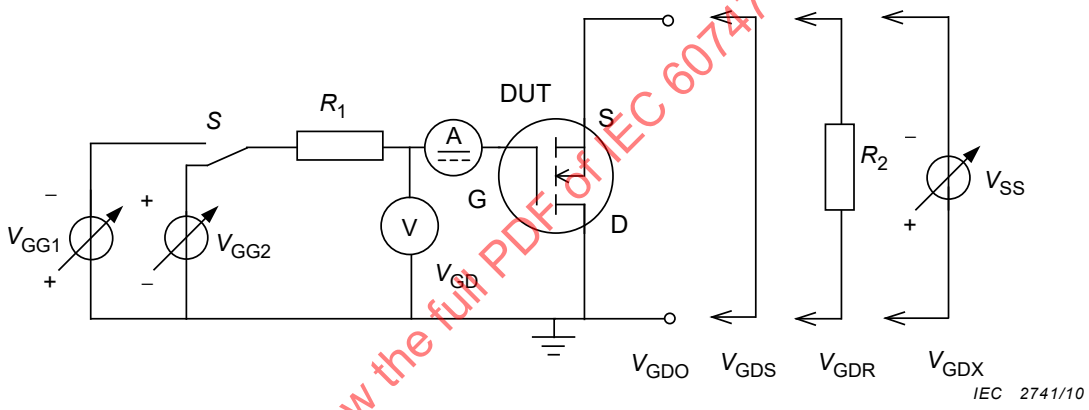


Figure 6 – Circuit diagram for testing of gate-drain voltage

– **Circuit description and requirements**

V_{SS}, V_{GG1} and V_{GG2} are the d.c. voltage supply. V_{GDX} is applied only for gate reverse biased condition of V_{GG2}.

– **Testing procedure**

Source-drain voltage is set to specified conditions. V_{GD} is increased until gate-drain voltage measured on voltmeter V_{DS} reaches the specified gate-drain voltage V_{GD*}. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Reference point or junction temperature T_{vj};
- Drain-source bias conditions;
- Gate-drain voltage: rated gate-drain voltage.

6.2.1.4 Drain current (I_D)

– **Purpose**

To verify that drain current capability of FETs is not less than the maximum rated value I_D under specified conditions.

– **Circuit diagram**

See Figure 7 below.

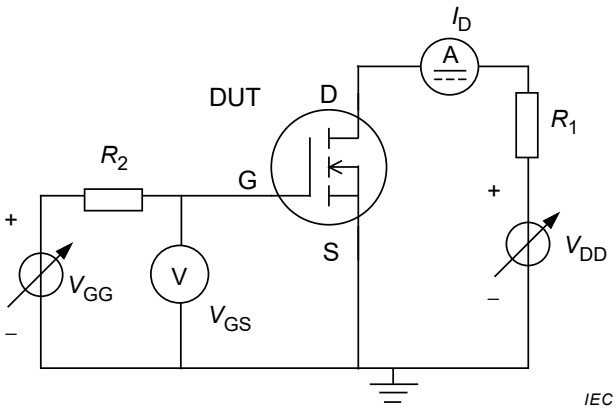


Figure 7 – Basic circuit for the testing of drain current

– **Circuit description and requirements**

V_{DD} and V_{GG} are the d.c. voltage supply. R_1 and R_2 are protective resistors.

– **Testing procedure**

Specified gate-source voltage is applied to the gate. Temperature (T_a or T_c or T_{vj}) and gate-source voltage are set and kept to the specified value. Drain current is supplied at specified conditions. After the above test, confirm the reference-defining characteristics of DUT being normal by the criteria of Table 2. Drain current is supplied at specified conditions until thermal equilibrium is reached.

– **Specified conditions**

- Reference point or junction temperature $T_{vj;}$
- Gate-source voltage V_{GS}.
- Drain current I_D.

6.2.1.5 Peak drain current (I_{DM})

– **Purpose**

To verify the peak drain current under specified conditions.

– **Circuit diagram**

See Figure 8 below.

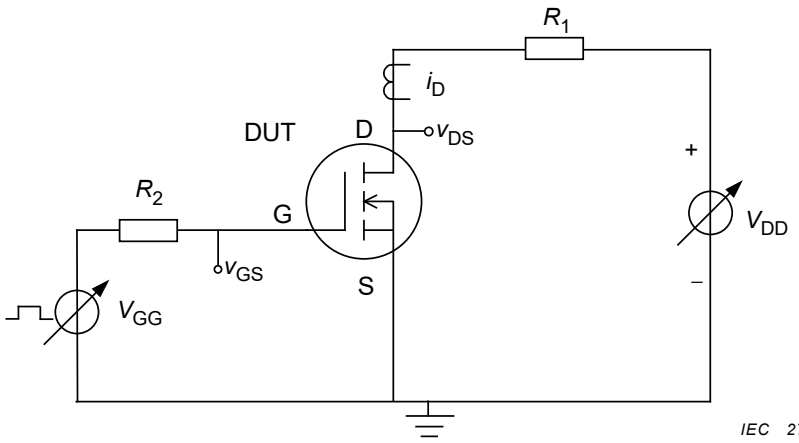


Figure 8 – Circuit diagram for testing of peak drain current

– **Circuit description and requirements**

V_{DD} is the d.c. voltage supply and V_{GG} is the gate pulse generator. R_1 and R_2 are protective resistors.

– **Testing procedure**

A specified gate-source voltage pulse is applied to turn the device on and off. Temperature (T_a or T_c or T_{vj}) is set and kept to the specified value. Peak drain current is conducted at the specified conditions. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Gate-source voltage V_{GS}
- Pulse width and duty cycle
- Peak drain current I_{DM}

6.2.1.6 Reverse drain current (I_{SS}) or (I_{SX})

– **Purpose**

To verify the reverse drain current under specified conditions.

– **Circuit diagram**

See Figure 9 below.

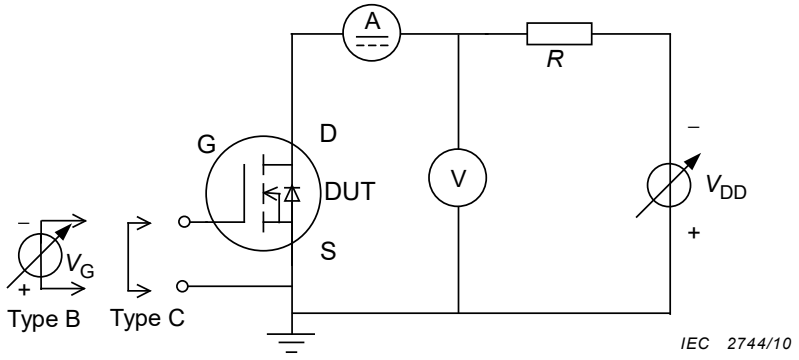


Figure 9 – Basic circuit for the testing of reverse drain current of MOSFETs

– **Circuit description and requirements**

V_{DD} is the d.c. voltage supply. R is a protective resistor.

– **Testing procedure**

Gate-source terminals are shorted (C-type) or supplied with an off-bias (B-type). Temperature (T_a or T_c or T_{vj}) is set and kept to the specified value under specified conditions. Reverse drain current is conducted to DUT with MOSFET in off-state. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- MOSFET in off-state: the gate condition of B type is set to be kept in the off-state.
- Reference point or junction temperature T_{vj}
- Protective resistor R
- Reverse drain current I_S

6.2.1.7 Peak reverse drain current (I_{SM})

– **Purpose**

To verify peak reverse drain current under specified conditions.

– **Circuit diagram**

See Figure 10 below.

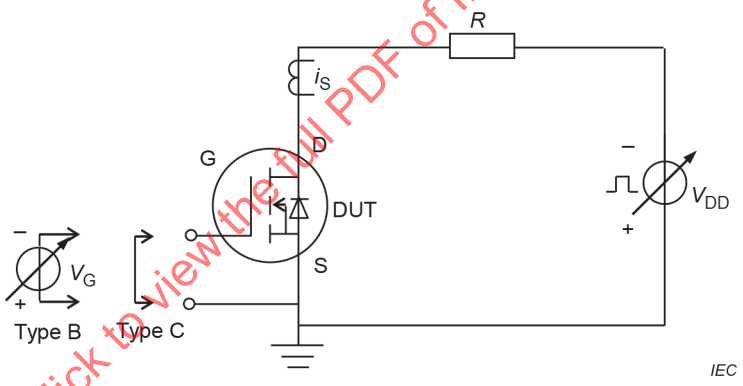


Figure 10 – Basic circuit for the testing of peak reverse drain current of MOSFETs

– **Circuit description and requirements**

V_{DD} is a pulse voltage source with adjustable pulse width and duty cycle control. R is a protective resistor.

– **Testing procedure**

Gate-source terminals are connected as specified. The temperature (T_a or T_c or T_{vj}) is set and kept to the specified value. Peak reverse drain current is conducted to DUT by turning on the V_{DD} with MOSFET in off-state. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- MOSFET in off-state
- Reference point or junction temperature T_{vj}
- Pulse width and duty cycle; setting up by the pulse switching unit
- Peak reverse drain current I_{SM}

6.2.2 Safe operating area

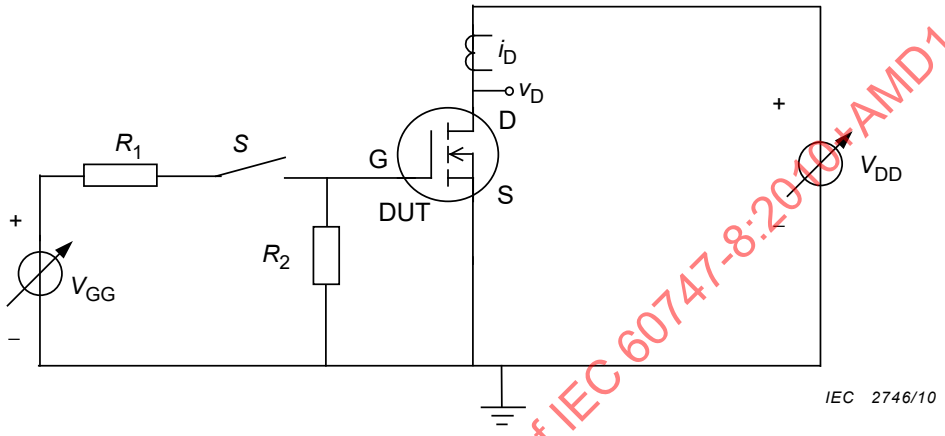
6.2.2.1 Forward-bias safe operating area (FBSOA)

– **Purpose**

To verify the forward-bias safe operating area of a case-rated power field-effect transistor under specified conditions with non-inductive load.

– **Circuit diagram**

See Figure 11 below.



DUT = transistor being measured (MOSFET or JFET)

Figure 11 – Circuit diagram for verifying FBSOA

– **Circuit description and requirements**

V_{GG}, V_{DD} = adjustable voltage sources

R_1, R_2 = 10 kΩ or as specified

S = switch to obtain the specified sequence of current pulse

– **Testing procedure**

The case temperature is set to the specified value. The device is switched on and off with the specified pulse duration and duty cycle. V_{DS} and I_D are monitored. V_{GG} and/or V_{DD} are increased until the specified pulse values for V_{DS} and I_D are reached. Under these operating conditions, the device being measured is operated for the specified duration of the test, or for the specified number of pulses, as appropriate. Verification of the FBSOA rating is obtained from the post-test measurements. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Case temperature T_c
- Drain-source voltage V_{DS}
- Drain current I_D
- As specified, either d.c. operation or repetitive pulse operation, or a combination of these conditions
- Pulse duration t_p and duty factor δ as appropriate
- As specified, either duration of the test or number of test pulses
- R_1, R_2 if other than 10 kΩ

- Post-test measurement limits

6.2.2.2 Reverse-bias safe operation area (RBSOA)

– **Purpose**

To verify the reverse-bias safe operation area under specified conditions with inductive load.

– **Circuit diagram and test waveforms**

See Figure 12 and Figure 13 below.

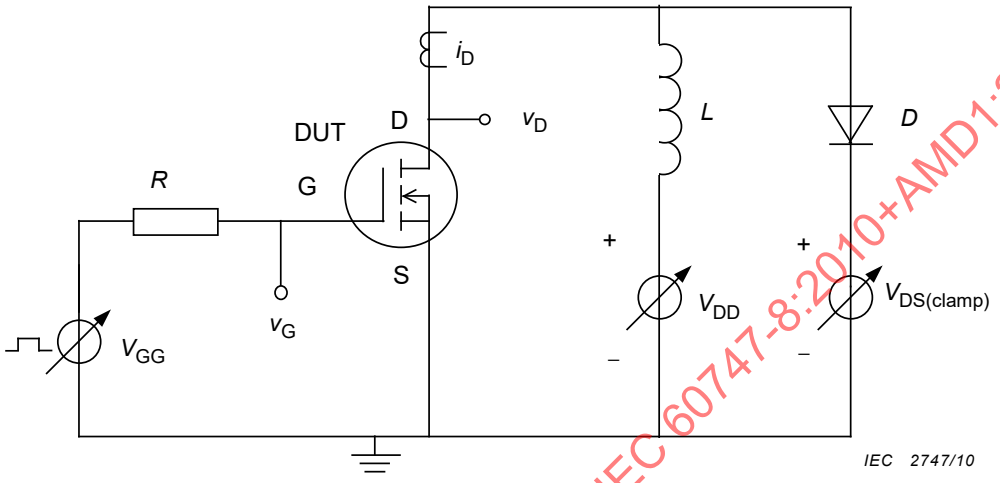


Figure 12 – Circuit diagram for verifying RBSOA

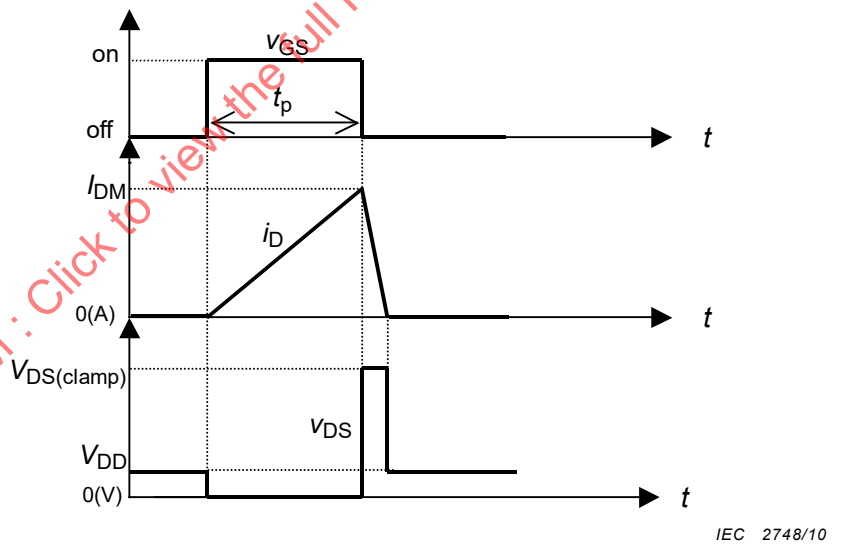


Figure 13 – Test waveforms for verifying RBSOA

– **Circuit description and requirements**

D = clamping diode

L = inductive load

V_{DD} = adjustable voltage sources

$V_{DS(clamp)}$ =adjustable voltage source for the clamping voltage

t_p = gate-source voltage pulse width

V_{GG} = gate pulse generator

R = gate resistor

– **Testing procedure**

DUT is turned off at specified I_D and V_{DS}. I_D and V_{DS} are monitored. The DUT has to turn off I_D and withstand V_{DS} = $V_{DS(clamp)}$.

NOTE Drain-source peak voltage $V_{DSM} < V_{(BR)DS}$.

The temperature (*reference point temperature* or T_{vj}) is set and kept to a specified value. Under these operating conditions, DUT is operated for the specified duration of the test, or for the specified number of pulses, as appropriate. Verification of the RBSOA rating is obtained from the post-test measurements. After the above test, confirm the acceptance defining characteristics of DUT being normal by the criteria of Table 2. The device is considered defective if, at any instant during the test, the drain-source voltage collapses or oscillates during the fall of the current pulses.

– **Specified conditions**

- Drain current I_D
- Gate reverse voltage -V_{GS} before and after turn-off
- Drain-source voltage $V_{DS(clamp)}$
- Number of pulses, if greater than one, and pulse width and duty cycle
- Inductance L
- Reference point or virtual junction temperature T_{vj}

– Gate resistor R_G

6.2.2.3 Short-circuit safe operating area (SCSOA)

– **Purpose**

This test is to verify that the MOSFET operates reliably without failure under load-shorted conditions. A short-circuit can occur when the MOSFET is already conducting, or the MOSFET is turned into a short-circuit condition. A test for the latter case is described in the following.

– **Circuit diagram and waveforms**

See Figure 14 and Figure 15 below.

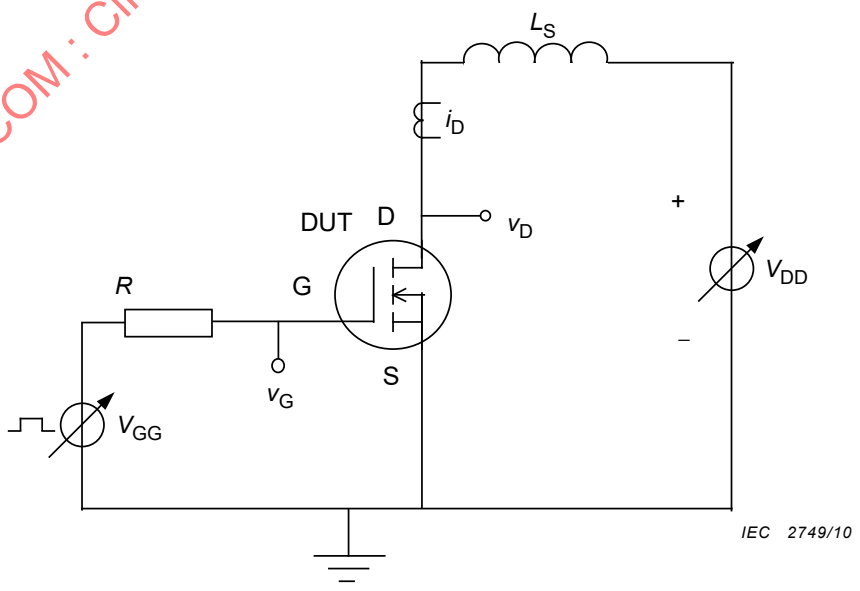


Figure 14 – Circuit for testing safe operating pulse duration at load short circuit

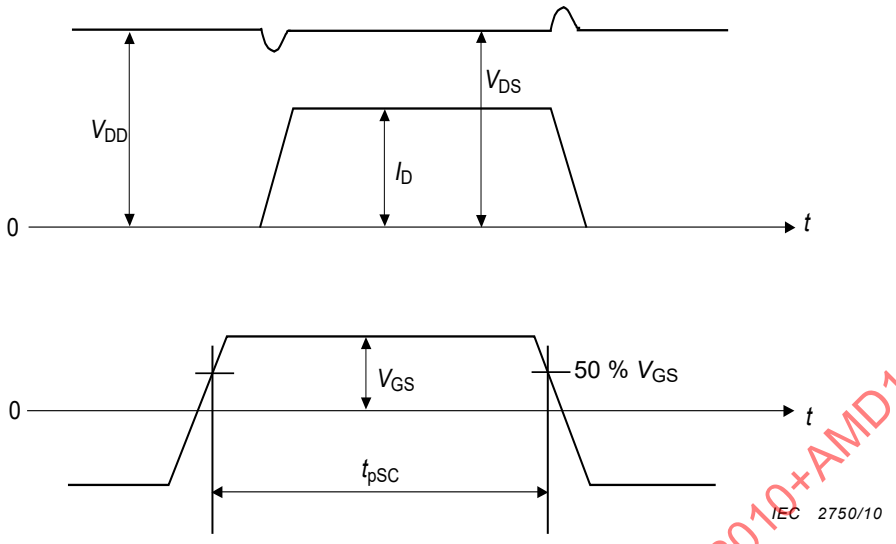


Figure 15 – Waveforms of gate-source voltage V_{GS}, drain current I_D and voltage V_{DS} during load short circuit condition SCSOA

– **Circuit descriptions and requirements**

L_S represents the maximum permitted stray inductance; it must be low enough to ensure that the maximum short circuit current is reached within the first 25% of the gate pulse duration t_{pSC}.

L_S = stray inductance

V_{DD} = adjustable voltage sources

t_{pSC} = gate-source voltage pulse width

V_{GG} = gate pulse generator

R = gate resistor as specified

– **Testing procedure**

Temperature is set to the specified value. Gate-source voltage V_{GS} and pulse duration is set to specified values. Drain-source voltage V_{DS} is set to a specified value. The drain currents I_D and V_{DS} are monitored in order to see whether the MOSFET turns on and turns off correctly. After the above test, confirm the acceptance defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Drain-source voltage V_{DS} = V_{DD}
- On and off-state gate source voltages
- Gate pulse duration t_{pSC}
- Gate resistor R
- Value of stray inductance L_S
- Reference point or virtual junction temperature T_{vj}

6.2.3 Avalanche energy

6.2.3.1 Repetitive avalanche energy (E_{AR})

– **Purpose**

To verify the repetitive avalanche energy capability in an unclamped inductive switching circuit.

– **Circuit diagram and waveforms**

See Figure 16 and Figure 17 below.

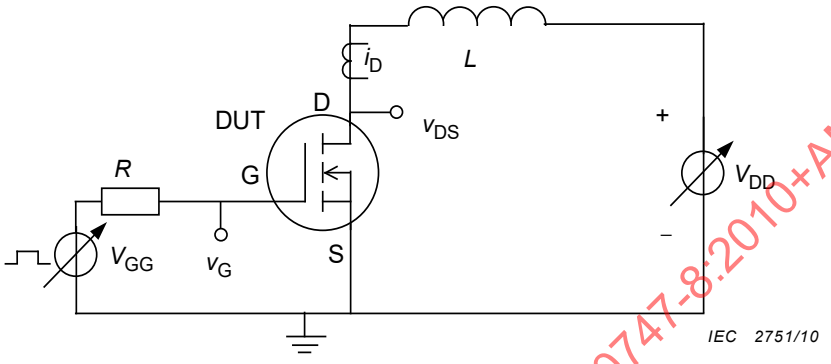


Figure 16 – Circuit for the inductive avalanche switching

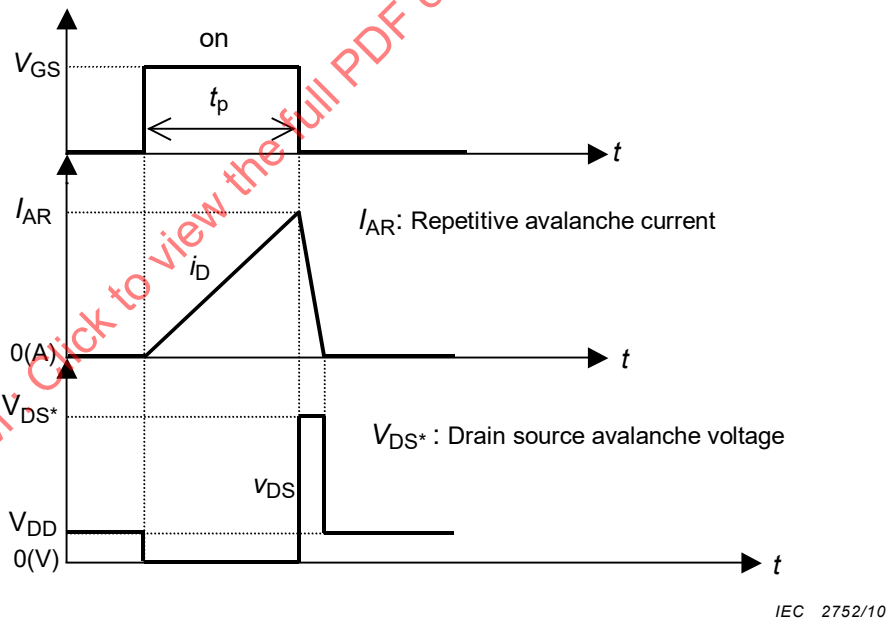


Figure 17 – Waveforms of I_D, V_{DS} and V_{GS} during unclamped inductive switching

– **Circuit descriptions and requirements**

L = inductive load

V_{DD} = adjustable voltage sources

V_{GG} = gate pulse generator

R = gate resistor as specified

– **Test procedure**

Temperature is set to the specified value. The supply voltage (V_{DD}) is set to the specified value. The turn-on time of the MOSFET is adjusted in such a way that the specified avalanche current is reached. Under these operating conditions, the DUT is operated with the specified number of pulses and repetition rate. The energy delivered to the DUT can be calculated as follows:

$$E_{AR} = ½\ L\ I_{AR}^2\ V_{DS*} / (V_{DS*} - V_{DD})$$

After the above test, confirm the acceptance defining characteristics of DUT are normal by the criteria of Table 2. DUT shall be within all specified parameter limits at the completion of the test. The measured value of V_{DS*} shall be greater than or equal to the minimum breakdown voltage $V_{(BR)DS*}$ with the permitted avalanche currents I_{AR}.

NOTE When V_{DD} is set to a smaller value compared with V_{DS*}, E_{AR} is calculated by using the approximate equation of $E_{AR} = ½\ L\ I_{AR}^2$.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DD}
- Gate-source voltage V_{GS}
- Drain current I_D
- Inductance L
- Frequency f

6.2.3.2 Non-repetitive avalanche switching energy (E_{AS})

– **Purpose**

To verify the non-repetitive avalanche switching energy.

– **Circuit diagram and waveforms**

See Figure 18 below.

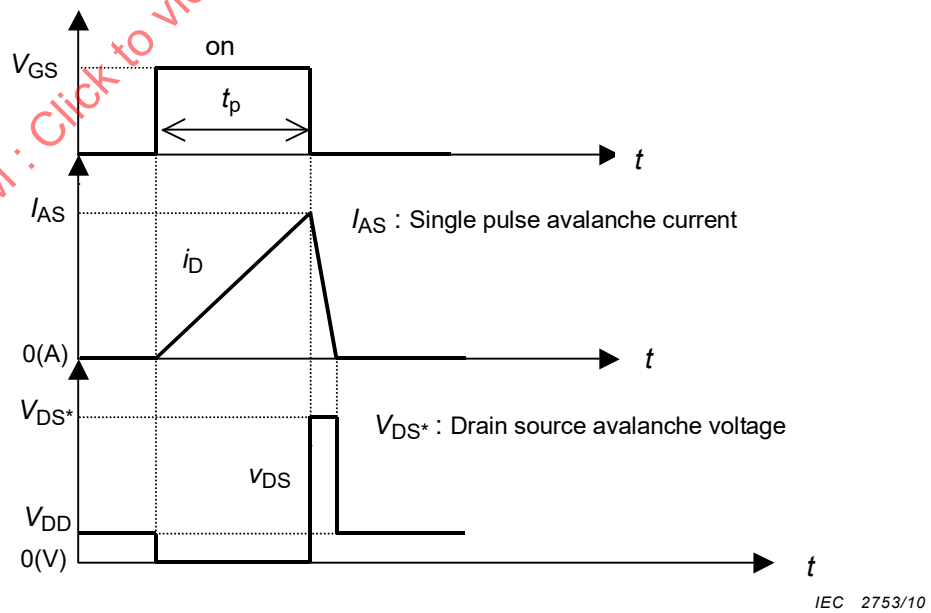


Figure 18 – Waveforms of I_D, V_{DS} and V_{GS} for the non-repetitive avalanche switching

– **Circuit descriptions and requirements**

L = inductive load

V_{DD} = adjustable voltage sources

V_{GG} = gate pulse generator

R_G = gate resistor as specified

– **Testing procedure**

Temperature is set to the specified value. The supply voltage (V_{DD}) is set to the specified value. The turn-on time of the MOSFET is adjusted in such a way that the specified avalanche current is reached. Under these operating conditions, the DUT is operated with the single pulse. The energy delivered to the DUT can be calculated as follows:

$$E_{AS} = ½\ L\ I_{AS}^2\ V_{DS*} / (V_{DS*} - V_{DD})$$

After the above test, confirm the acceptance defining characteristics of DUT are normal by the criteria of Table 2. DUT shall be within all specified parameter limits at the completion of the test. The measured value of V_{DS*} shall be greater than or equal to the minimum breakdown voltage $V_{(BR)DS*}$ with the permitted avalanche currents I_{AS}.

NOTE When V_{DD} is set to a smaller value compared with V_{DS*}, E_{AS} is calculated by using the approximate equation of $E_{AS} = ½\ L\ I_{AS}^2$.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DD}
- Gate-source voltage V_{GS}
- Drain current I_D
- Inductance L
- Single pulse

6.3 Methods of measurement

6.3.1 Breakdown voltage, drain to source ($V_{(BR)DS*}$)

– **Purpose**

To measure the drain to source breakdown voltage under specified conditions.

– **Circuit diagram**

See Figure 19 below.

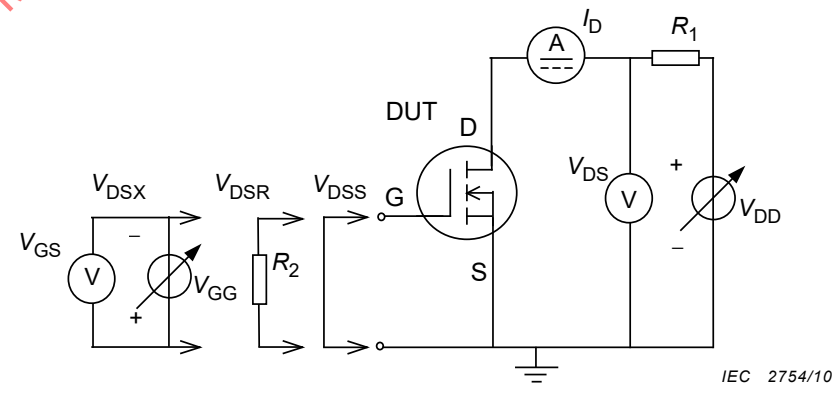


Figure 19 – Circuit diagrams for the measurement drain-source breakdown voltage

– **Circuit description and requirements**

V_{DD} and V_{GG} are the d.c. voltage supply. R_1 is a circuit protection resistor.