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Semiconductor devices –
Discrete devices –

Part 7-5:
Bipolar transistors for power switching applications

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES – DISCRETE DEVICES –

Part 7-5: Bipolar transistors for power switching applications

FOREWORD

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International Standard IEC 60747-7-5 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47E/279/FDIS	47E/283/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

A bilingual version of this standard may be issued at a later date.

SEMICONDUCTOR DEVICES – DISCRETE DEVICES –

Part 7-5: Bipolar transistors for power switching applications

1 Scope

This part of IEC 60747 gives requirements for bipolar switching transistors used for power switching application above 1 A.

NOTE Requirements concerning bipolar transistors in general can be found in IEC 60747-7.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60747-7, *Semiconductor devices – Part 7: Bipolar transistors*

IEC 60747-1:1983, *Semiconductor devices – Discrete devices and integrated circuits – Part 1: General*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
switching times
$t_{d(on)}$, t_r, t_s and t_f
as described in IEC 60747-1, but here the input waveform is the base current and the output waveform is the collector current

3.2
collector-emitter sustaining voltage
$V_{CE\_(SUS)}$
the collector-emitter breakdown voltage at higher values of collector current where the breakdown voltage is relatively constant over decreasing collector current for a specified termination between base and emitter terminals

3.3
turn-on energy (per pulse)
E_{on}
energy dissipated in transistor during turn-on

3.4
turn-off energy (per pulse)
E_{off}
energy dissipated in transistor during turn-off

4 Letter symbols – Energies

See IEC 60747-7.

Name and designation	Letter symbol	Remarks
Turn-on energy	E_{on}	Energy is always per pulse
Turn-off energy	E_{off}	

5 Essential ratings and characteristics

5.1 Ratings (limiting values)

Ratings shall be valid for the whole range of operating conditions as stated for the particular device, with reference to a curve where appropriate.

5.1.1 Temperatures

5.1.1.1 Minimum and maximum of operating temperatures, ambient or case or virtual junction (T_a or $T_{c\ or}$ Tvj)

5.1.1.2 Minimum and maximum of storage temperatures (T_{stg})

5.1.2 Currents

The ratings must cover the operation of the device over the range of operating temperatures. Where such ratings are temperature dependent, this dependence should be indicated.

5.1.2.1 Maximum continuous collector current (I_C)

5.1.2.2 Where appropriate, maximum peak repetitive collector current, under specified conditions (I_{CRM}).

5.1.2.3 Maximum continuous base current (I_B)

5.1.2.4 Where appropriate, maximum peak repetitive base current, under specified conditions (I_{BRM}).

5.1.2.5 Where appropriate, maximum emitter current, continuous and/or peak repetitive, under specified conditions (I_E, I_{ERM}).

5.1.3 Voltages

5.1.3.1 Maximum collector-base voltage with zero emitter current (V_{CBO})

5.1.3.2 Maximum collector-emitter voltage, either with zero base current or with a specified emitter-base reverse voltage (V_{CEO} or V_{CEX}).

5.1.3.3 Maximum emitter-base voltage with zero collector current (V_{EBO}).

5.1.3.4 Collector-emitter sustaining voltage (V_{CEXsus}).

Maximum rated value at specified collector current and specified base-emitter (reverse) voltage

5.1.4 Power dissipation

5.1.4.1 Maximum total power dissipation (without additional cooling for ambient-rated devices) up to ambient or case temperature of 25 °C (P_{tot}).

5.1.4.2 Derating factor above 25 °C or, for case-rated devices, derating curve

5.1.5 Safe operating areas

5.1.5.1 Forward biased safe operating area (FBSOA)

Diagram showing the area of collector currents (I_C) and collector-emitter voltages (V_{CE}) which the transistor will sustain simultaneously without being damaged by thermal overload or by the first or second breakdown, for d.c. and pulse operation.

Conditions to be specified:

– case temperature (T_c);

– pulse time (t_P);

– duty cycle (δ).

5.1.5.2 Reverse biased safe operating area (RBSOA)

Diagram showing the area of collector currents (I_C) and collector-emitter voltages (V_{CE}) which the transistor will sustain simultaneously for a short period of time during turn-off without being damaged

Conditions to be specified:

– case temperature (T_c);

– reverse base current (I_{B2});

– conditions in the drive circuit.

5.1.5.3 Short-circuit safe operating area (SCSOA)

The SCSOA is given by a pair of values of short-circuit duration ($t_{p(sc)}$) and collector-emitter voltage (V_{CE}) that may not be exceeded under the load short circuit conditions. The device may be turned on and turned off again for shorting a voltage source without failure.

5.2 Characteristics

5.2.1 Cut-off currents

NOTE One or more of these currents should be stated.

5.2.1.1 Collector-base current (I_{CBO})

– Maximum value at 25 °C, preferably at the maximum rated value of the collector-base voltage and with the emitter open-circuited.

– Maximum value at a high operating temperature, at a voltage preferably between 65 % and 85 % of the maximum rated collector-base voltage, and with the emitter open-circuited.

5.2.1.2 Collector-emitter current (I_{CEX})

– Maximum value at 25 °C, preferably at the maximum rated value of collector-emitter voltage and under specified base-emitter bias conditions.

– Maximum value at a high operating temperature, at a voltage preferably between 65 % and 85 % of the maximum rated collector-emitter voltage and under specified base-emitter bias conditions.

5.2.1.3 Collector-emitter current (I_{CES})

– Maximum value at 25 °C, preferably at the maximum rated value of the collector-emitter voltage and with the base short-circuited to the emitter.

– Maximum value at a high operating temperature, at a voltage preferably between 65 % and 85 % of the maximum rated collector-emitter voltage and with the base short-circuited to the emitter.

5.2.1.4 Collector-emitter current (I_{CER})

– Maximum value at 25 °C, preferably at the maximum rated collector-emitter voltage and with a specified base-emitter resistance.

– Maximum value at a high operating temperature, at a voltage preferably between 65 % and 85 % of the maximum rated collector-emitter voltage and with a specified base-emitter resistance.

5.2.1.5 Emitter-base current (I_{EBO})

– Maximum value at 25 °C at a specified high value of the emitter-base voltage and with the collector open-circuited.

– Maximum value at a high operating temperature and at a specified emitter-base voltage, and with the collector open-circuited.

5.2.2 Static value of common-emitter forward current transfer ratio *(h_{FE})*

Minimum value at 25 °C, at specified collector current and collector-emitter voltage.

5.2.3 Collector-emitter saturation voltage (V_{CEsat})

Maximum value at 25 °C, for at least one specified collector current and specified base current

5.2.4 Base-emitter saturation voltage (V_{BEsat})

Maximum value at 25 °C, at specified collector and base currents.

5.2.5 Turn-on energy (E_{on})

Maximum value per pulse with inductive load under specified conditions of T_a or T_c or T_{vj}, high V_{CE} , high I_C and I_B .

5.2.6 Turn-off energy (E_{off})

Maximum value per pulse with inductive load under specified conditions of T_a or T_c or T_{vj},high V_{CE} , high I_C and I_B.

5.2.7 Switching times

5.2.7.1 Turn-on delay time ($t_{d(on)}$)

Maximum value for resistive load under specified conditions.

5.2.7.2 Rise time (t_r)

Maximum value, at nominal values of collector current (I_C) and base forward current (I_{B1}).

5.2.7.3 Turn-on time (t_{on})

Maximum value, at nominal values of collector current (I_C), base forward current (I_{B1}) and base-emitter voltage (V_{BE}) prior to turn-on pulse.

5.2.7.4 Storage time (t_s)

Maximum value, at nominal values of collector current (I_C) and base forward and reverse currents (I_{B1} and I_{B2}).

5.2.7.5 Fall time (t_f)

Maximum value for resistive load under specified conditions.

5.2.7.6 Turn-off time (t_{off})

Maximum value, at nominal values of collector current (I_C) and base forward and reverse currents (I_{B1} and I_{B2}).

5.2.8 Thermal resistance junction to case ($R_{th(j-c)}$)

Maximum value for case-rated transistors.

5.2.9 Thermal resistance junction to ambient ($R_{th(j-a)}$)

Maximum value for ambient-rated transistors.

5.2.10 Transient thermal impedance junction to case ($Z_{th(j-c)}$)

For case-rated transistors, diagram showing the maximum value against the time which has elapsed after a step change in power dissipation.

5.2.11 Transient thermal impedance junction to ambient ($Z_{th(j-a)}$)

For ambient-rated transistors, diagram showing the maximum value against the time which has elapsed after a step change in power dissipation.

6 Measuring methods

6.1 Verification of ratings (limiting values)

Table 1 – Failure defining characteristics and failure criteria

Failure-defining Characteristics	Failure criteria	Measurement conditions
I_{CES}	I_{CES}> USL	Specified V_{CE}
V_{CEsat}	V_{CEsat}>USL	I_C specified for V_{CEsat}
USL: upper specified limit.		

6.1.1 Voltages and currents

6.1.1.1 Collector current (I_C)

6.1.1.1.1 Purpose

To verify that the collector current capability of a transistor is not less than the maximum rated value I_C under specified conditions.

6.1.1.1.2 Circuit diagram

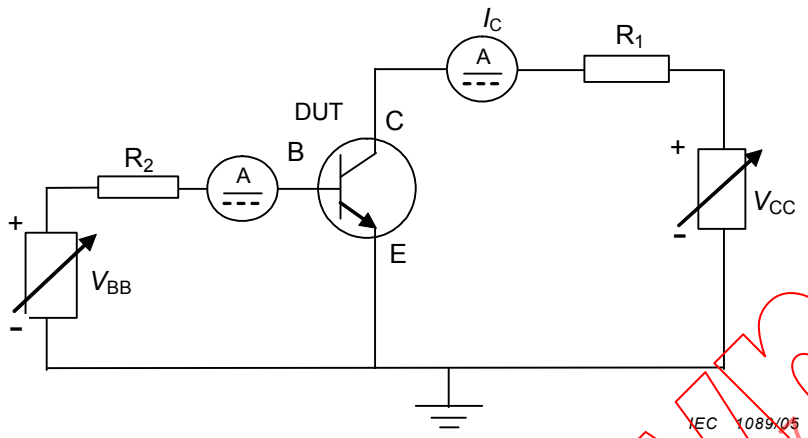


Figure 1 –Test circuit for collector current

6.1.1.1.3 Circuit description and requirement

R_1 and R_2 are resistors for circuit protection. V_{BB} and V_{CC} are the d.c. voltage supply.

6.1.1.1.4 Test procedure

The temperature (T_a or T_c or T_{vj}) and base current are set and kept to the specified value. The supply voltage (V_{CC}) is increased until I_C reaches the specified value. The test may be stopped when thermal equilibrium has been reached. After the above test, confirm transistor characteristics are normal. See Table 1.

6.1.1.1.5 Specified conditions

– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

– Collector current I_C.

– Base current I_B.

6.1.1.2 Peak collector current (I_{CM})

6.1.1.2.1 Purpose

To verify that the peak collector current capability of a transistor is not less than the maximum rated value I_{CM} under specified conditions.

6.1.1.2.2 Circuit diagram

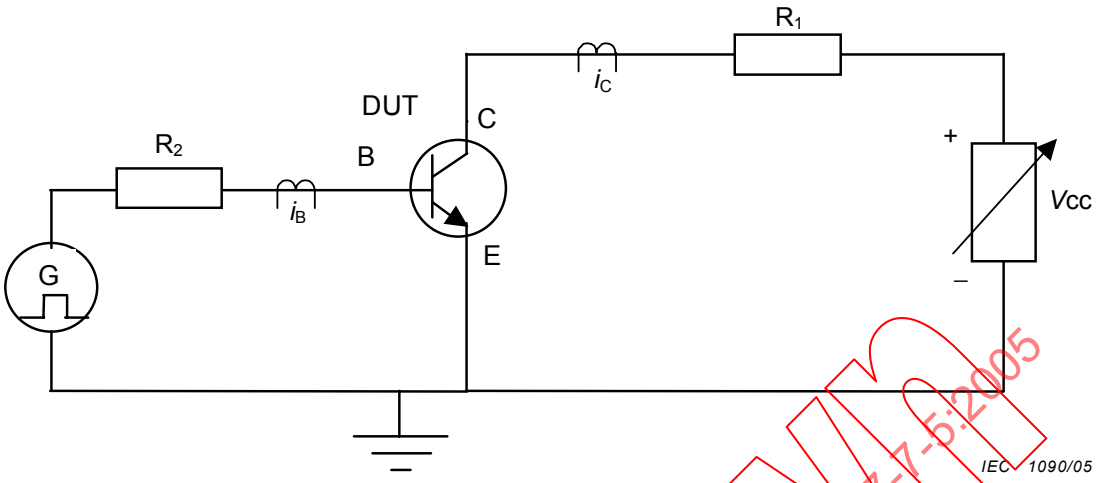


Figure 2 – Test circuit for peak collector current

6.1.1.2.3 Circuit description and requirement

R_1 and R_2 are resistors for circuit protection. V_{CC} is a voltage supply for collector current. G is a pulse generator for the base current.

6.1.1.2.4 Test procedure

The temperature (T_a or T_c or T_{vj}) and base current are set and kept to the specified value. The supply voltage (V_{CC}) is increased until I_C reaches the specified value. The test may be stopped when thermal equilibrium has been reached. After the above test, confirm that transistor characteristics are normal. See Table 1.

6.1.1.2.5 Specified conditions

– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

– Collector current I_C.

– Pulse base current (duration time, duty cycle).

6.1.1.3 Base current (I_B)

6.1.1.3.1 Purpose

To verify that the base current capability of a transistor is not less than the maximum rated value I_B under specified conditions.

6.1.1.3.2 Circuit diagram

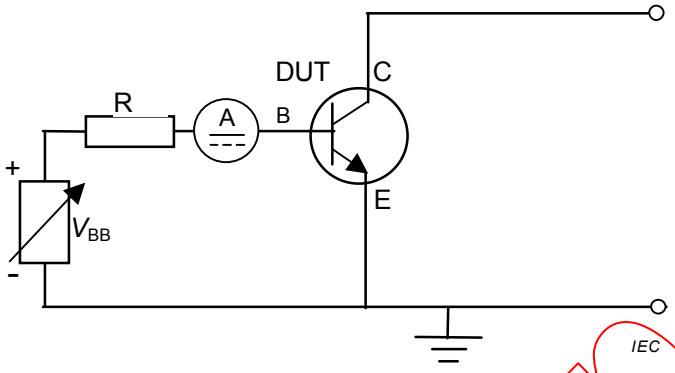


Figure 3 – Test circuit for base current

6.1.1.3.3 Circuit description and requirements

R is a resistor for circuit protection. V_{BB} is a d.c. voltage supply.

6.1.1.3.4 Test procedure

The temperature (T_a or T_c or T_{vj}) is set. The supply voltage (V_{BB}) is increased until I_B reaches the specified value. The test may be stopped when thermal equilibrium has been reached. After the above test, confirm that transistor characteristics are normal. See Table 1.

6.1.1.3.5 Specified conditions

– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

– Base current I_B.

6.1.1.4 Peak base current (I_{BM})

6.1.1.4.1 Purpose

To verify that the peak base current capability of a transistor is not less than the maximum rated value I_{BM} under specified conditions.

6.1.1.4.2 Circuit diagram

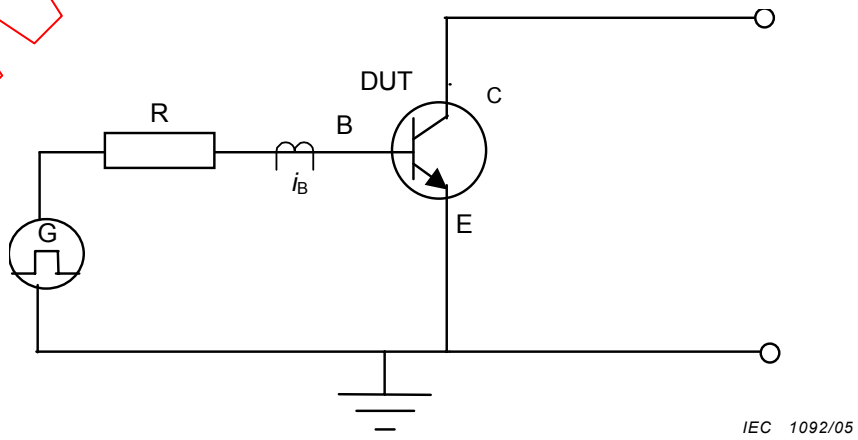


Figure 4 – Test circuit for peak base current

6.1.1.4.3 Circuit description and requirements

R is a resistor for circuit protection. G is a pulse generator.

6.1.1.4.4 Test procedure

The temperature (T_a or T_c or T_{vj}) is set. The supply voltage (G) is increased until I_B reaches the specified value. The test may be stopped when thermal equilibrium has been reached. After the above test, confirm that the transistor characteristics are normal. See Table 1.

6.1.1.4.5 Specified conditions

– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

– Pulse base current (duration time, duty cycle).

6.1.1.5 Collector-base voltage (V_{CBS}, V_{CBR} or V_{CBX})

6.1.1.5.1 Purpose

To verify that a transistor withstands the rated collector-base voltages V_{CBS}, V_{CBR} or V_{CBX} under specified conditions.

6.1.1.5.2 Circuit diagram

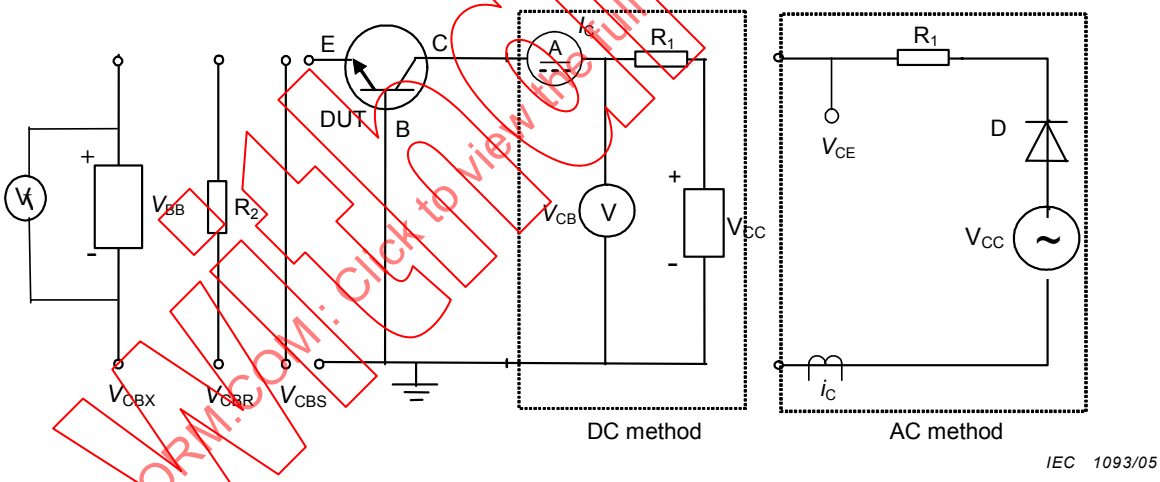


Figure 5 – Circuit for testing the collector-base voltage V_{CBS}, V_{CBR}, V_{CBX}

6.1.1.5.3 Circuit description and requirements

R_1 is a resistor for circuit protection. V_{CC} is the d.c. or a.c. voltage power supply. V_{BB} is a d.c. power supply.

6.1.1.5.4 Test procedure

There are two methods, i.e. the d.c. method and the a.c. method with circuits according to Figure 5. The base-emitter voltage is set to specified conditions. The collector-base voltage is set to the specified value. The collector-base leakage current I_C shall not exceed the specified value.

6.1.1.5.5 Specified conditions

– Ambient or case or virtual junction temperature T_c or T_a or T_{vj}.
– Base-emitter bias voltage $-V_{BE}$.

V_{CBX}: Base-emitter voltage – V_{BB}.

V_{CBR}: Resistor connected between base and emitter.

V_{CBS}: Short-circuit between base and emitter .

– Frequency of the generator V_{cc}, if different from 50 Hz to 60 Hz.

6.1.1.6 Collector-emitter voltage (V_{CES}, V_{CER} or V_{CEX})

6.1.1.6.1 Purpose

To verify that a transistor withstands the rated collector-emitter voltages V_{CES}, V_{CER} or V_{CEX} under specified conditions.

6.1.1.6.2 Circuit diagram

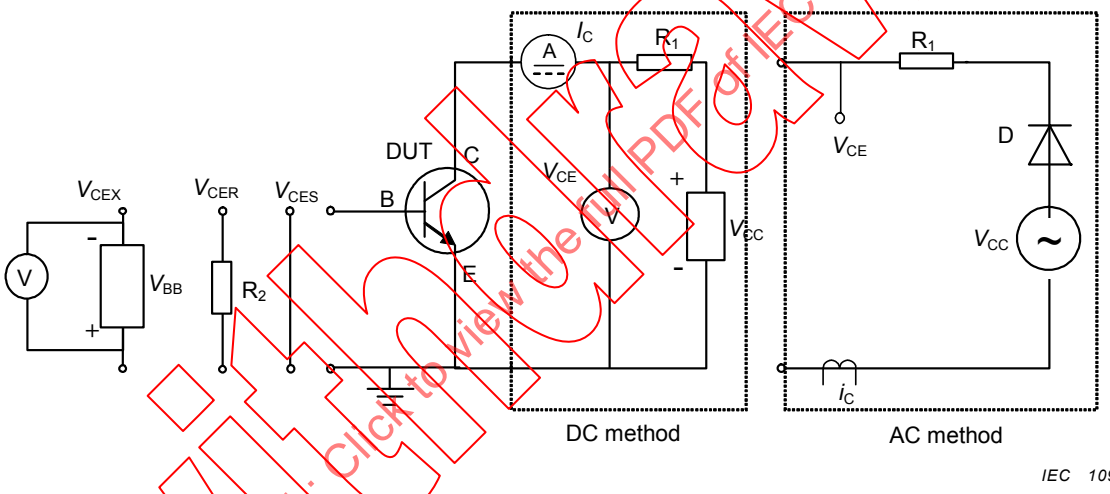


Figure 6 – Circuit for testing the collector-emitter voltage V_{CES}, V_{CER}, V_{CEX}

6.1.1.6.3 Circuit description and requirements

R_1 is a resistor for circuit protection. V_{CC} is the d.c. or a.c. voltage power supply. V_{BB} is the d.c. voltage supply.

6.1.1.6.4 Test procedure

There are two methods, i.e. the d.c. method and the a.c. method with circuits according to Figure 6. The base-emitter voltage is set to specified conditions. The collector-emitter voltage is set to the specified value. The collector emitter leakage current I_C shall not exceed the specified value.

6.1.1.6.5 Specified conditions

– Collector-emitter voltage V_{CE}.
– Ambient or case or virtual junction temperature T_c or T_a or T_{vj}.
– Base-emitter bias voltage $-V_{BE}$.

V_{CEX}: Base-emitter voltage – V_{BB}.

V_{CER}: Resistor connected between base and emitter.

V_{CES}: Short-circuit between base and emitter.

– Frequency of the generator *V*cc, if different from 50Hz to 60Hz.

6.1.1.7 Emitter-base voltage (V_{EB})

6.1.1.7.1 Purpose

To verify that a transistor withstands the rated emitter-base voltage V_{EB} under specified conditions.

6.1.1.7.2 Circuit diagram

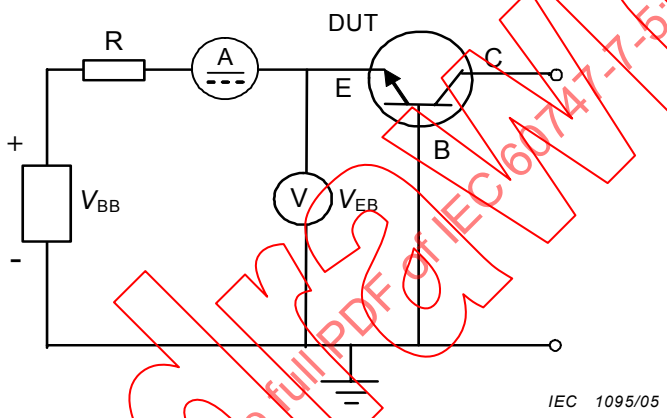


Figure 7 – Circuit for testing the emitter-base voltages V_{EB}

6.1.1.7.3 Circuit description and requirements

R is a resistor for circuit protection. V_{BB} is the d.c. voltage supply.

6.1.1.7.4 Test procedure

The emitter-base voltage V_{EB} is set to the specified value. The negative base leakage current shall not exceed the specified value I_{EBS}. A protective resistor R is provided.

6.1.1.7.5 Specified conditions

– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

– Negative base leakage current I_{EBS}.

6.1.2 Safe operating area (SOA)

6.1.2.1 Reverse biased safe operating area (RBSOA)

6.1.2.1.1 Purpose

To verify that a transistor operates reliably without failure in RBSOA

6.1.2.1.2 Circuit diagram and waveforms

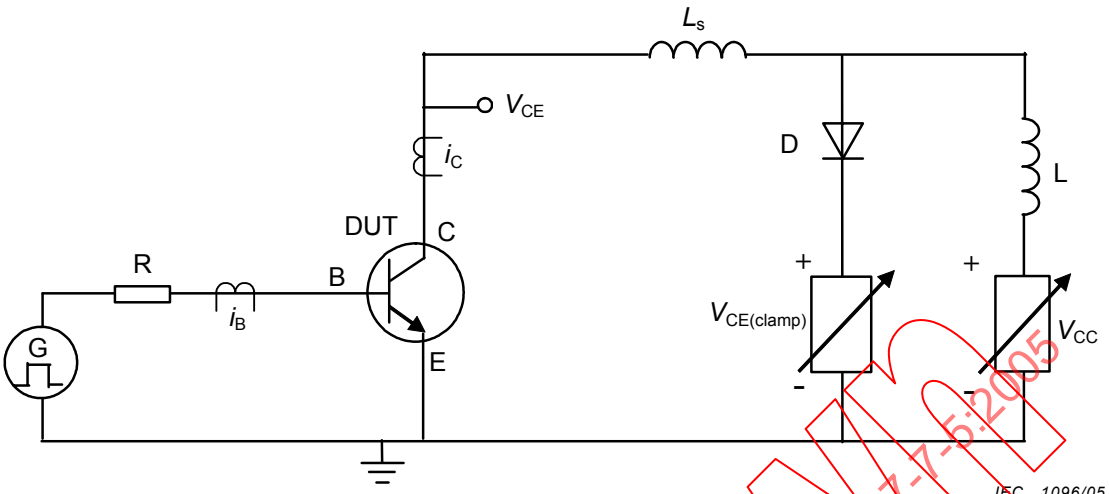


Figure 8 – Test circuit of reverse bias safe operating area (RBSOA)

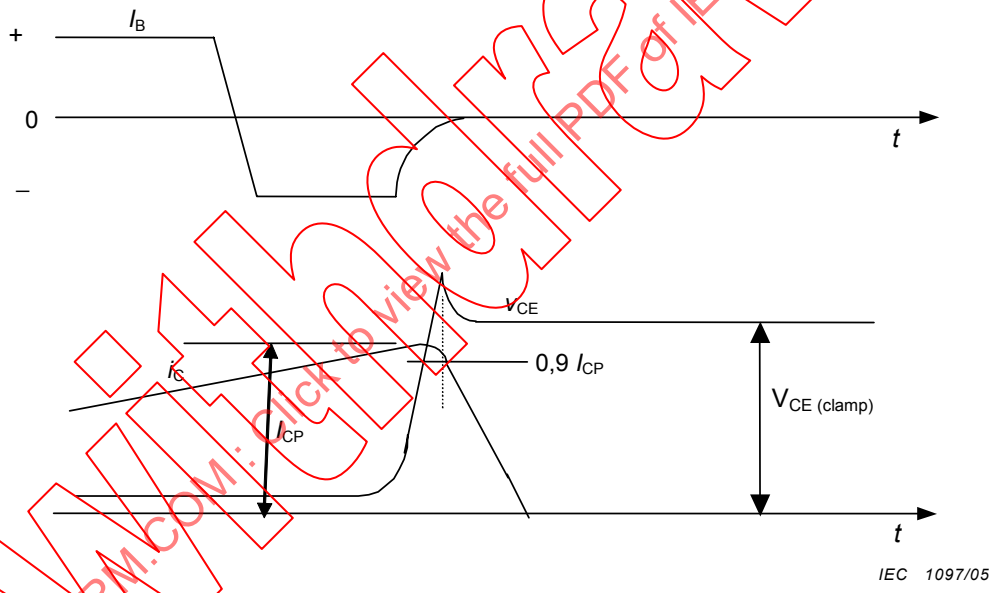
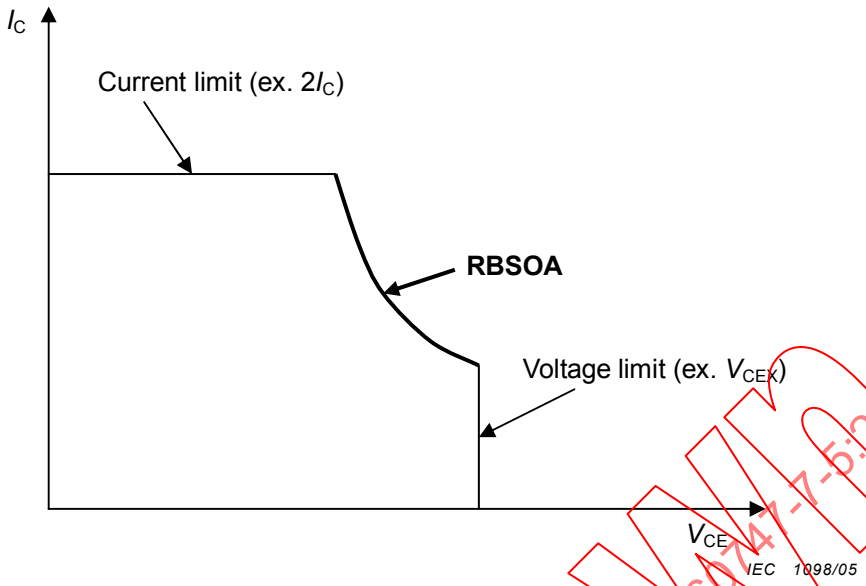


Figure 9a – Waveforms of base current I_B and collector current I_C during turn-off



NOTE This test should be applied for RBSOA as the above.

Figure 9b – RBSOA curves during turn-off

Figure 9 –Waveforms and curves for RBSOA

6.1.2.1.3 Circuit description and requirements

R is a resistor for circuit protection. V_{CC} is an adjustable voltage supply.

L is an inductive load. $V_{CE\ (clamp)}$ is an adjustable voltage source for the clamping voltage.

L_S is a stray circuit inductance. G is a pulse generator for the base current.

D is the clamping diode.

The value of load inductance *L* shall be high enough to apply $V_{CE\ (clamp)}$ to the DUT at least before the beginning of the fall time t_f.

6.1.2.1.4 Test procedure

The DUT is turned off at specified I_C. V_{CE} and I_E (I_C) are monitored. The DUT has to turn off I_C and withstand $V_{CE} = V_{CE\ (clamp)}$. After the above test, confirm that the DUT characteristics are normal. See Table 1.

6.1.2.1.5 Specified conditions

– Collector current I_C.
– Base reverse current I_{B2} .
– Collector-emitter voltage $V_{CE\ (clamp)}$.
– Single pulse or testing frequency f_{sw}.
– Inductance *L*.
– Value of unclamped stray inductance L_s.
– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

6.1.2.2 Short-circuit safe operating area (SCSOA)

6.1.2.2.1 Purpose

To verify that a transistor operates reliably without failure during a load short-circuit condition.

6.1.2.2.2 Circuit diagram and waveforms

Figures 10 and 11 show the circuit for testing SCSOA and switching waveforms. The circuit impedance of the collector supply circuit in Figure 10 shall be small enough that $V_{CC} = V_{CE}$.

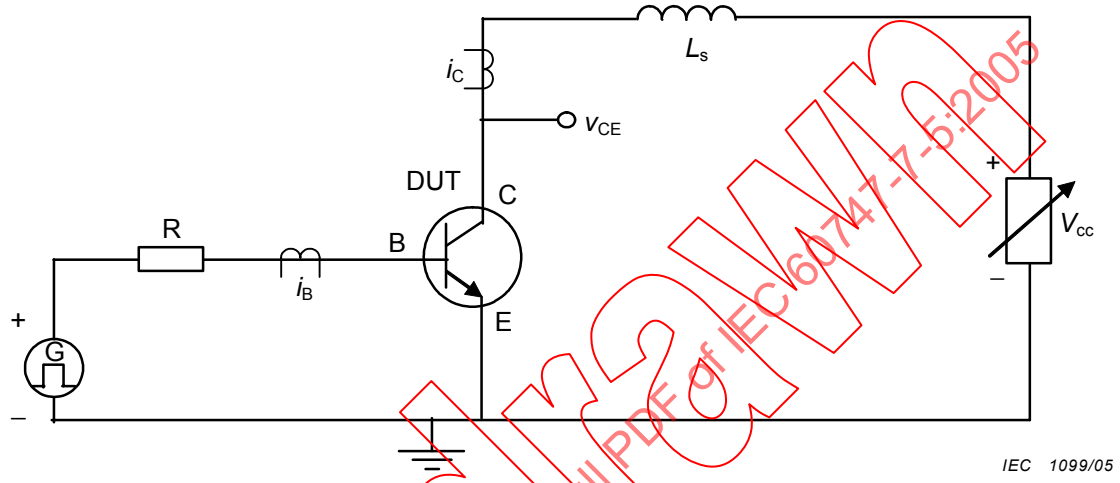


Figure 10 – Circuit for testing safe operating pulse duration at load short-circuit (SCSOA)

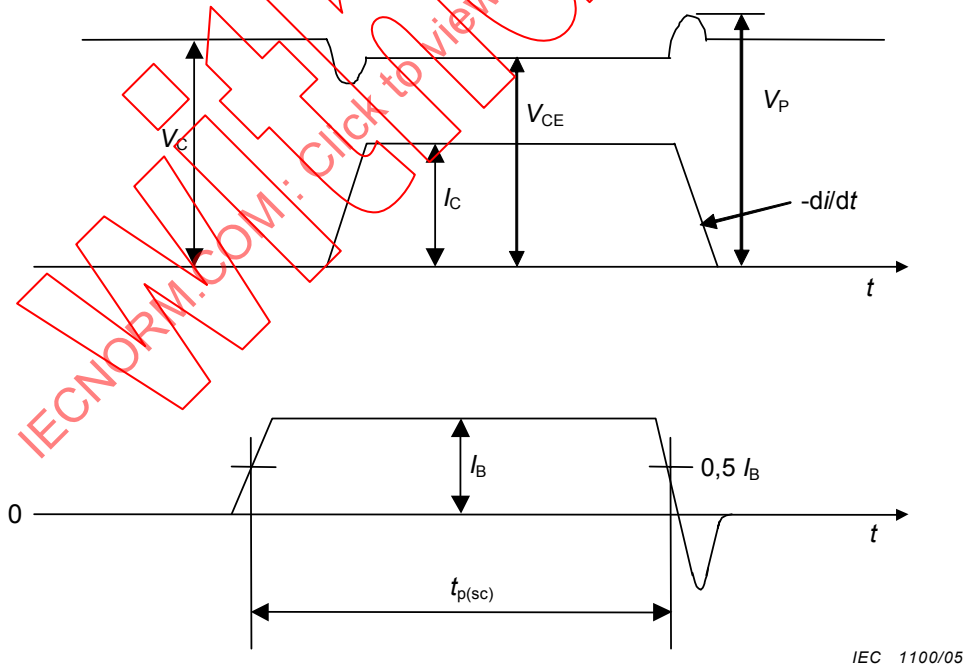


Figure 11 – Waveforms of base current I_B, collector current I_C and voltage V_{CE} during load short-circuit condition SCSOA

6.1.2.2.3 Circuit description and requirements

The circuit impedance of the collector supply circuit in Figure 10 shall be small enough that V_P is less than ($V_{CE} + L_S(-di/dt)$).

V_P is the transient peak voltage during load short-circuit condition.

R is a resistor for circuit protection. V_{CC} is an adjustable voltage source.

L_S is a stray circuit inductance. G is a pulse generator for the base current.

6.1.2.2.4 Test procedure

The temperature is set to the specified value. The base current and pulse duration are set to the specified values. The collector-emitter voltage V_{CE} is set to the specified value. The collector current I_C, V_{CE}, and I_B are monitored in order to see whether the transistor turns on and turns off correctly. After the above test, confirm that the DUT characteristics are normal. See Table 1.

6.1.2.2.5 Specified conditions

– Collector-emitter voltage $V_{CE} = V_{CC}$.
– Base current I_B.
– Pulse duration $t_{p(sc)}$.
– Value of stray inductance L_s.
– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

6.2 Methods of measurement

6.2.1 Turn-on time intervals and turn-on energy (per pulse)(E_{on})

6.2.1.1 Purpose

To measure the turn-on time intervals t_d, t_r, t_{on} and turn-on energy E_{on} of a transistor under specified conditions with inductive load.

6.2.1.2 Circuit diagram and waveforms

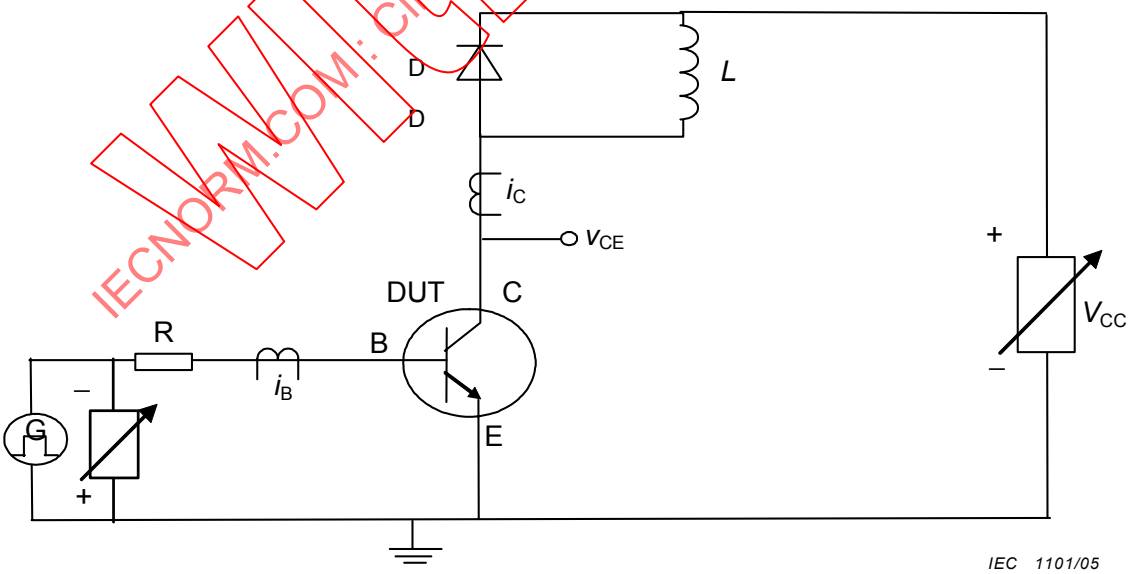


Figure 12 – Circuit diagram for measuring turn-on intervals and energy

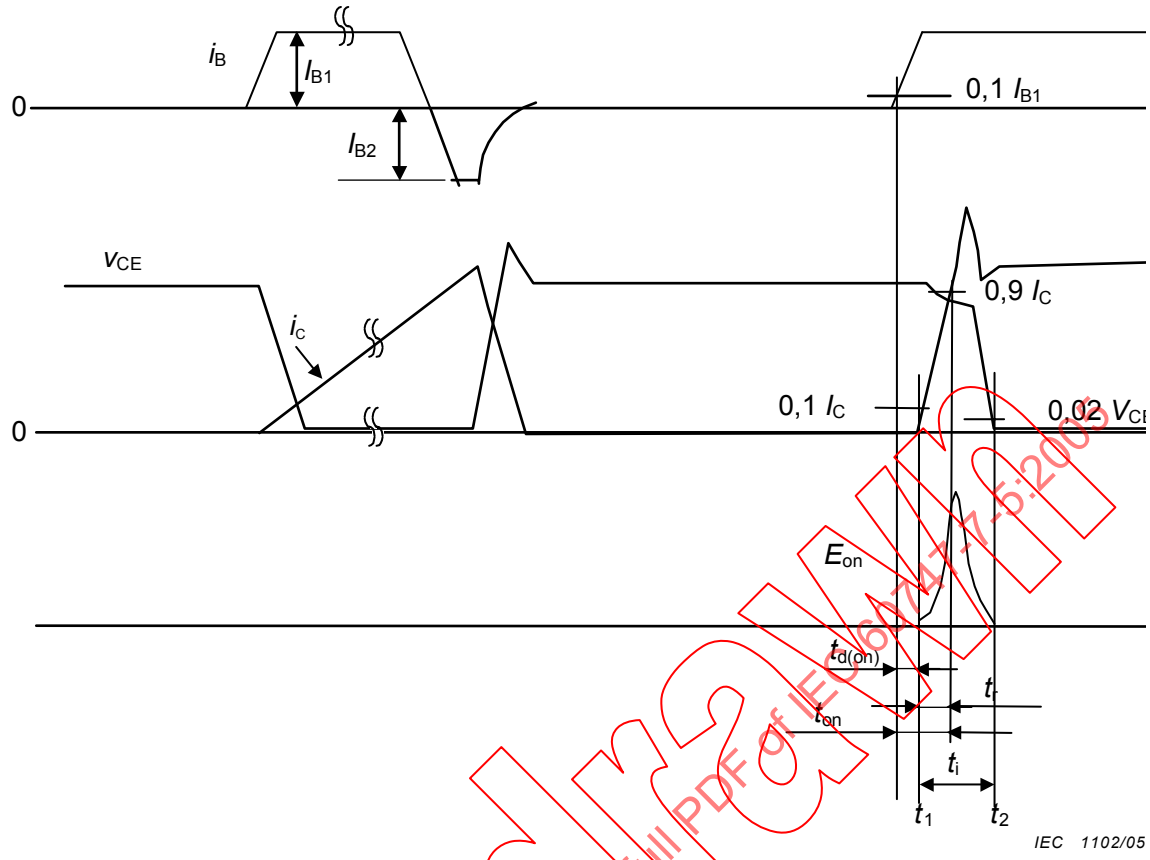


Figure 13 – Waveforms during turn-on intervals

6.2.1.3 Circuit description and requirements

R is a resistor for circuit protection.

V_{CC} is an adjustable voltage source.

L is an inductive load. G is a pulse generator for the base current.

D is a free wheeling diode.

6.2.1.4 Measurement procedure

The input pulse amplitude G_1 and the supply voltage V_{CC} are set to the specified values. The transistor is turned on and turned off twice and then the second turn on is observed. Waveforms of base current I_B, collector current I_C and collector-emitter voltage V_{CE} are monitored. E_{on} is calculated by the equation:

$$E_{on} = \int_{t_1}^{t_2} i_C \times v_{CE} \times \mathrm{d}t$$

6.2.1.5 Specified conditions

– Case or ambient or virtual junction temperature of the transistor and the diode.
– Voltage of intermediate circuit, V_{CC}.
– Inductor current I_L before turn-on.
– Base current I_B.
– Inductance L.
– Characteristics (Q_{rr}, I_{rrm} and t_{rr}) of freewheeling diode.

6.2.2 Turn-off time intervals and turn-off energy (per pulse) (E_{off})

6.2.2.1 Purpose

To measure the turn-off time intervals t_s, t_f t_{off} and turn-off energy E_{off} of a transistor under specified conditions with inductive load.

6.2.2.2 Circuit diagram and waveforms

The circuit diagram is the same as for Figure 12.

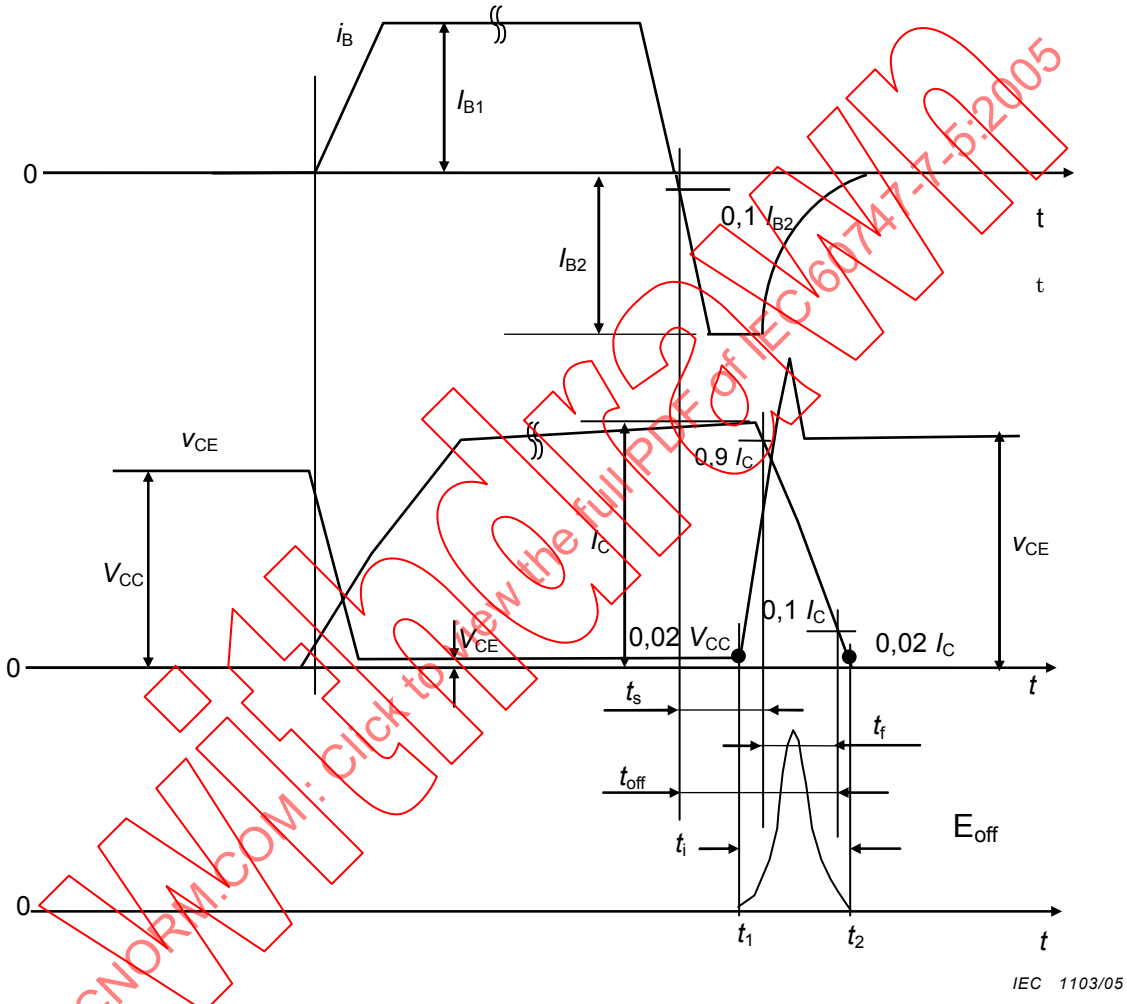


Figure 14 – Waveforms during turn-off intervals

6.2.2.3 Measurement procedure

The input pulse amplitude G_1 and the supply voltage V_{CC} are set to the specified values. The transistor is turned on and turned off. Waveforms of base current I_B, collector current I_C and collector-emitter voltage V_{CE} are monitored. E_{off} is calculated by the equation of integral:

$$E_{off} = \int_{t_1}^{t_2} i_C \times v_{CE} \times \mathrm{d}\,t$$

6.2.2.4 Specified conditions

– Case or ambient or virtual junction temperature of the transistor and the diode.
– Voltage of intermediate circuit, V_{CC}.
– Inductor current I_L before turn-off.
– Base current I_B.

7 Acceptance and reliability

7.1 Endurance and reliability tests, and test methods

The tests in this clause may be used where appropriate to augment, but not to replace, adequate manufacturing process control and are destructive.

7.1.1 General requirements

Chapter VIII, Section three, Clause 2 of IEC 60747-1 applies.

7.1.2 List of endurance tests

A choice of endurance tests is given in Figured 15 and 16.

7.1.3 Conditions for endurance tests

Test conditions and test circuits are described in Figures 15 and 16. The relevant specification will state which tests will apply.

7.1.4 Failure-defining characteristics and failure criteria for endurance and reliability tests

Failure-defining characteristics, their failure criteria and measurement conditions are listed in Table 2.

NOTE Characteristics should be measured in the sequence in which they are listed in this table, because the changes of characteristics caused by some failure mechanisms may be wholly or partially masked by the influence of other measurements.

Table 2 – Failure-defining characteristics for endurance and reliability tests

Failure-defining characteristics	Failure criteria (see note)	Measurement conditions
I_{CES}	I_{CES}> USL	Specified V_{CE}
V_{CEsat}	V_{CEsat}>USL	I_C specified for V_{CEsat}
R_{th}	R_{th} >1,0 USL	Specified I_C
USL: upper specification limit.		

7.1.5 Procedure in case of a testing error

The results of tests carried out using inaccurate or faulty test equipment shall not be included for the purpose of device assessment.