INTERNATIONAL STANDARD

IEC 60191-6-12

First edition
2002-06

Mechanical standardization of semiconductor devices –

Part 6-12:
General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch land grid array (FLGA) – Rectangular type

Normalisation mécanique des dispositifs à semiconducteurs –

Partie 6-12:
Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs pour montage en surface –
Guide de conception pour les boîtiers FLGA de type rectangulaire

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Guide de conception pour les boîtiers FLGA de type rectangulaire

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-12: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch land grid array (FLGA) – Rectangular type

FOREWORD

1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of the IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested National Committees.
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6) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. The IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 60191-6-12 has been prepared by subcommittee 47D: Mechanical standardization of semiconductor devices, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/493/FDIS	47D/507/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

A bilingual version of this publication may be issued at a later date.

The committee has decided that the contents of this publication will remain unchanged until 2004. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

INTRODUCTION

The demand for area array style packages exists because of the multi-functions and high performance of electrical equipment. The objective of this design guide is to standardize outlines and to get interchangeability of FLGA rectangular type packages. The terminal pitch and package outlines of these fine-pitch array packages are smaller than those of LGA packages.

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-12: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch land grid array (FLGA) – Rectangular type

1 Scope

This part of IEC 60191 provides common outline drawings and dimensions for all types of structures and composed materials of fine-pitch land grid array (hereinafter called FLGA) whose terminal pitch is less than, or equal to, 0,80 mm and whose package body outline is rectangular.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60191 (all parts), *Mechanical standardization of semiconductor devices*

3 Definitions

For the purposes of this part of IEC 60191, the following definitions, as well as those given in the other parts of this series, apply.

3.1
flanged type
type whose package body size (body length and width) consists of its own flange composed around the encapsulation or lid

3.2
type of real chip size
type whose package body size (body length and width) consists of an encapsulation around the real chip only

3.3
FLGA
packages with metal lands or metal bumps of which the terminal height is less than, or equal to, 100 µm, and whose terminal pitch is less than, or equal to, 0,80 mm, positioned in an array on the base plane of the package as external terminals

This package structure makes it possible to surface-mount the packages to the printed circuit board.

3.4
material designation
FLGA packages are classified according to the following two material designations:

3.4.1
plastic type (P-FLGA)
plastic-type classification is assigned to packages which consist of resin substrate as interposer material (for example, glass-epoxy, poly-imid)

3.4.2
ceramic type (C-FLGA)
ceramic-type classification is assigned to packages which consist of ceramic substrate as interposer material

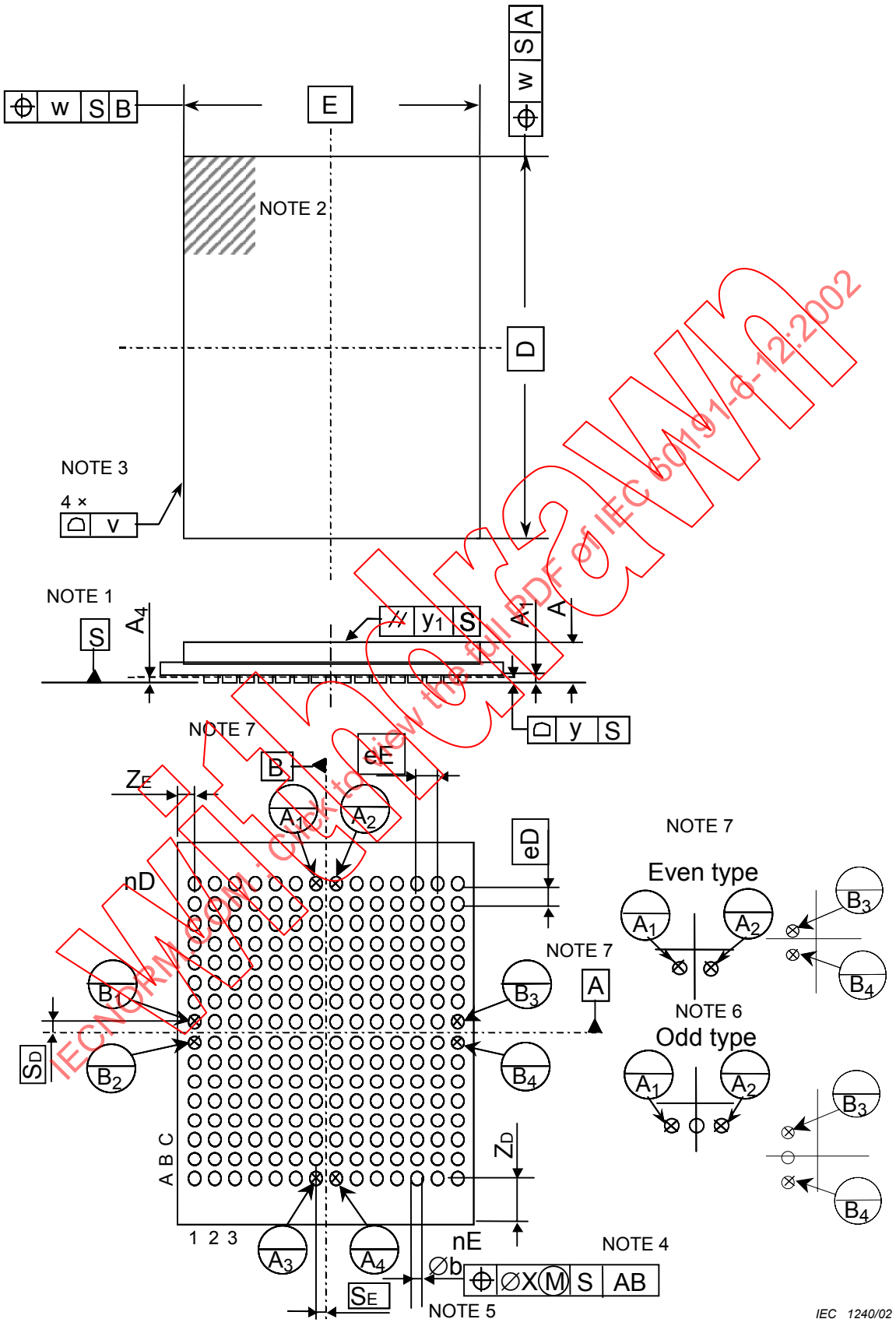


Figure 1 – Rectangular FLGA packages

NOTE 1 Indicates seating plane. Seating plane is defined by the plane that the carrier contacts to the mount surface.

NOTE 2 Indicates positional tolerance of the index mark.

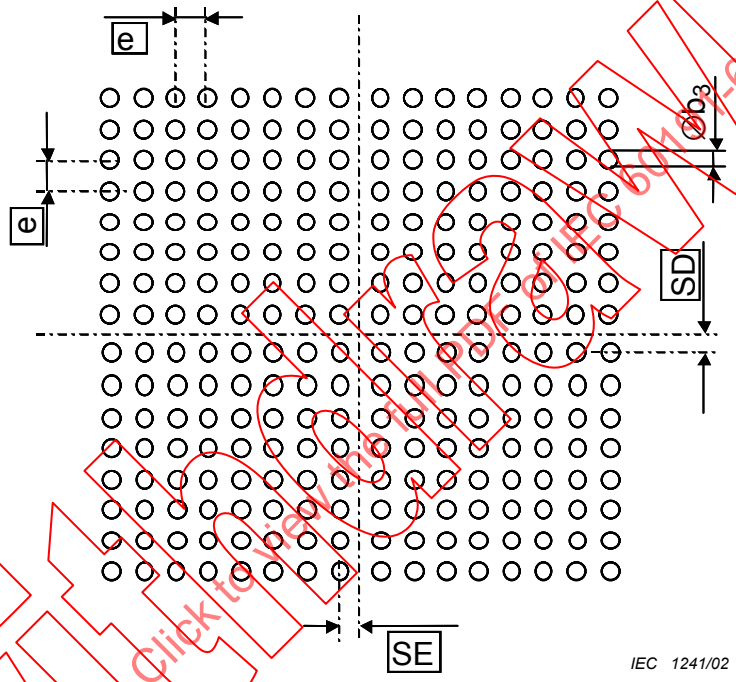
NOTE 3 Bilateral tolerance zone is applied to four sides of the package body.

NOTE 4 The positional tolerances are applied to all terminals.

NOTE 5 Terminal diameter is the maximum terminal profile when the package is projected vertically from the seating plane.

NOTE 6 SD and SE are stipulated the position of closest terminal with respect to datum lines A and B.

NOTE 7 Datum A and B are the axes defined by the centres of the opposite package sides of the ball. The definition of the centre applies to “Odd type” and “Even type”.



NOTE As foot circuit pattern design reference, the zone in which the terminals can be positioned is shown in this figure.

Figure 2 – Terminal zones

Table 1 – Group 1: Dimensions appropriate to mounting and interchangeability

Dimensions in millimetres

Name	Reference symbol	Stipulations	Recommended value	Supplement
Nominal dimension	E × D	Flanged type The combination of one digit below decimal point of package width E and package length D is considered as the nominal dimension Type of real chip size The combination of two digits below decimal point of package width E and package length D is considered as the nominal dimension	–	E < D is not defined
Package length	D	1) Flanged type Package length: Dnom D = 1,5, 2,0, 2,5, 3,0, 3,5, 4,0, 4,5, 5,0, 5,5, 6,0, 6,5, 7,0, 7,5, 8,0, 8,5, 9,0, 9,5, 10,0, 10,5, 11,0, 11,5, 12,0, 12,5, 13,0, 13,5, 14,0, 14,5, 15,0, 15,5, 16,0, 16,5, 17,0, 17,5, 18,0, 18,5, 19,0, 19,5, 20,0, 20,5, 21,0 2) Type of real chip size Package length: Dnom D = From 1,5 to 21,0	–	Dimension range shows nominal value
Package width	E	1) Flanged type Package width: Enom E = 1,5, 2,0, 2,5, 3,0, 3,5, 4,0, 4,5, 5,0, 5,5, 6,0, 6,5, 7,0, 7,5, 8,0, 8,5, 9,0, 9,5, 10,0, 10,5, 11,0, 11,5, 12,0, 12,5, 13,0, 13,5, 14,0, 14,5, 15,0, 15,5, 16,0, 16,5, 17,0, 17,5, 18,0, 18,5, 19,0, 19,5, 20,0, 20,5, 21,0 2) Type of real chip size Package width: Enom E = From 1,5 to 21,0	–	Dimension range shows nominal value

Table 1 – *(continued)*

<table>
<tr><th>Name</th><th>Reference symbol</th><th>Stipulations</th><th>Recommended value</th><th>Supplement</th></tr>
<tr><td>Tolerance of package lateral profile</td><td>v</td><td>v = 0,15</td><td>–</td><td>Include burrs</td></tr>
<tr><td>Package centre offset</td><td>w</td><td><table><tr><th>e</th><th>W</th></tr><tr><td>0,80</td><td>0,20</td></tr><tr><td>0,65</td><td>0,20</td></tr><tr><td>0,50</td><td>0,20</td></tr><tr><td>0,40</td><td>0,15</td></tr></table></td><td>–</td><td>–</td></tr>
<tr><td>Mounting height</td><td>A</td><td><table><tr><th></th><th>A max.</th></tr><tr><td>VFLGA</td><td>1,00</td></tr><tr><td>TFLGA</td><td>1,20</td></tr><tr><td>LFLGA</td><td>1,70</td></tr><tr><td>FLGA</td><td>2,00</td></tr></table></td><td>–</td><td>Include heat slug
Include package warpage and tilt</td></tr>
<tr><td>Stand-off height</td><td>A_1</td><td>Apply to FLGA
A_1 max. = 0,10</td><td>–</td><td>–</td></tr>
<tr><td rowspan="3">Terminal pitch</td><td>eD</td><td>eD = 0,80, 0,65, 0,50, 0,40</td><td>–</td><td>–</td></tr>
<tr><td>eE</td><td>eE = 0,80, 0,65, 0,50, 0,40</td><td></td><td></td></tr>
<tr><td>e</td><td>e = eD = eE</td><td></td><td></td></tr>
</table>

Table 1 – *(continued)*

<table>
<tr><th>Name</th><th>Reference symbol</th><th>Stipulations</th><th>Recommended value</th><th>Supplement</th></tr>
<tr><td>Terminal diameter</td><td>b</td><td>Apply to C-FLGA
<table>
<tr><th>e</th><th>min.</th><th>nom.</th><th>max.</th></tr>
<tr><td>0,80</td><td>0,45</td><td>0,50</td><td>0,55</td></tr>
<tr><td>0,65</td><td>0,35</td><td>0,40</td><td>0,45</td></tr>
<tr><td>0,50</td><td>0,25</td><td>0,30</td><td>0,35</td></tr>
<tr><td>0,40</td><td>0,20</td><td>0,25</td><td>0,30</td></tr>
</table>
Apply to P-FLGA
<table>
<tr><th>e</th><th>min.</th><th>nom.</th><th>max.</th></tr>
<tr><td>0,80</td><td>0,35</td><td>0,40</td><td>0,45</td></tr>
<tr><td>0,65</td><td>0,28</td><td>0,33</td><td>0,38</td></tr>
<tr><td>0,50</td><td>0,20</td><td>0,25</td><td>0,30</td></tr>
<tr><td>0,40</td><td>0,15</td><td>0,20</td><td>0,25</td></tr>
</table></td><td><table>
<tr><th>e</th><th>b nom</th></tr>
<tr><td>0,80</td><td>0,50</td></tr>
<tr><td>0,65</td><td>0,40</td></tr>
<tr><td>0,50</td><td>0,30</td></tr>
<tr><td>0,40</td><td>0,25</td></tr>
</table></td><td>–</td></tr>
<tr><td>Positional tolerance of terminal</td><td>x</td><td><table>
<tr><th>e</th><th>x</th></tr>
<tr><td>0,80</td><td>0,08</td></tr>
<tr><td>0,65</td><td>0,08</td></tr>
<tr><td>0,50</td><td>0,05</td></tr>
<tr><td>0,40</td><td>0,05</td></tr>
</table></td><td>–</td><td>–</td></tr>
<tr><td>Terminal coplanarity</td><td>y</td><td><table>
<tr><th>e</th><th>y</th></tr>
<tr><td>0,80</td><td>0,12</td></tr>
<tr><td>0,65</td><td>0,10</td></tr>
<tr><td>0,50</td><td>0,08</td></tr>
<tr><td>0,40</td><td>0,08</td></tr>
</table></td><td>–</td><td>–</td></tr>
<tr><td>Parallelism of package top surface</td><td>y_1</td><td>y_1 = 0,2</td><td>–</td><td>–</td></tr>
<tr><td>Centre terminal position in D-direction</td><td>S_D</td><td>When n_D is an odd number S_D = 0
When n_D is an even number S_D = e /2</td><td>–</td><td>–</td></tr>
</table>

Table 1 – *(continued)*

Name	Reference symbol	Stipulations	Recommended value	Supplement
Centre terminal position in E-direction	S_E	When n_E is an odd number $S_E = 0$ When n_E is an even number $S_E = e/2$	–	–
Terminal array		Terminal positions are designated by terminal pitch e, matrix size M_D, M_E, and centre terminal positions, S_D S_E.		
Number of terminals	n	Apply to only FLGA n max. = n_E max +1× n_D max. n_E max. × n_D max. +1 n_E max. +1 × n_D max. +1		"n" is "$M_E \times M_D$" in the table.
Matrix size in D-direction	n_D			
Matrix size in E-direction	n_E			

Table 2 – Group 2: Dimensions appropriate to mounting and gauging

Dimensions in millimetres

Name	Reference symbol	Stipulations	Recommended value	Supplement
Overhang in D-direction	Z_D	$Z_D = (D\ nom. - (M_D - 1) \times e)/2$	–	–
Overhang in E-direction	Z_E	$Z_E = (E\ nom. - (M_E - 1) \times e)/2$	–	–
Terminal diameter on terminal land area	b_3	b_3 = b max. + x	–	–

Individual outline drawing standard registration

To propose a new outline for an individual standard, the necessary information is entered in table 3 and the preparation of the standard proceeded with, at which time the asterisk in table 3 will be replaced by dimensions or letters.

Table 3 – Package dimensions

Reference number				
Outline type		****FLGA*****		
Reference symbol		Min.	Nom.	Max.
Group I	D		*	
	E		*	
	v			*
	w			*
	A			*
	A_1	*		*
	e		*	
	b	*		*
	x			*
	y			*
	y_1			*
	n		*	
	M_D		*	
	M_E		*	
	Terminal array		See note below	
Group II	S_D		*	
	S_E		*	
	Z_D		[*]	
	Z_E		[*]	
	b_3			*

NOTE In the terminal array selection, the array types are selected from full matrix, staggered matrix, and peripheral X-row matrix. X is the natural number. For the other array placements, they will be defined or illustrated when each type is registered for individual outline drawing standard.

Table 4 – D/E, nD/nE, n max. variation – e = 0,80 mm pitch FLGA flanged type

Dimensions in millimetres

D or E	nD max. –2 or nE max. –2	nD max. –1 or nE max. –1	nD max. or nE max.
1,50	–	–	2
2,00	–	2	3
2,50			
3,00	2	3	4
3,50			
4,00	3	4	5
4,50	4	5	6
5,00			
5,50	5	6	7
6,00	6	7	8
6,50			
7,00	7	8	9
7,50			
8,00	8	9	10
8,50	9	10	11
9,00			
9,50	10	11	12
10,00	11	12	13
10,50			
11,00	12	13	14
11,50			
12,00	13	14	15
12,50	14	15	16
13,00			
13,50	15	16	17
14,00	16	17	18
14,50			
15,00	17	18	19
15,50			
16,00	18	19	20
16,50	19	20	21
17,00			
17,50	20	21	22
18,00	21	22	23
18,50			
19,00	22	23	24
19,50			
20,00	23	24	25
20,50	24	25	26
21,00			

Table 5 – D/E, n_D/n_E, n max. variation – e = 0,65 mm pitch FLGA flanged type

Dimensions in millimetres

D or E	n_D max. –1 or n_E max. –1	n_D max. –2 or n_E max. –2	n_D max. or n_E max.
1,50	–	–	2
2,00	2	–	3
2,50	3	2	4
3,00			
3,50	4	3	5
4,00	5	4	6
4,50	6	5	7
5,00	7	6	8
5,50			
6,00	8	7	9
6,50	9	8	10
7,00	10	9	11
7,50			
8,00	11	10	12
8,50	12	11	13
9,00	13	12	14
9,50			
10,00	14	13	15
10,50	15	14	16
11,00	16	15	17
11,50	17	16	18
12,00			
12,50	18	17	19
13,00	19	18	20
13,50	20	19	21
14,00			
14,50	21	20	22
15,00	22	21	23
15,50	23	22	24
16,00			
16,50	24	23	25
17,00	25	24	26
17,50	26	25	27
18,00	27	26	28
18,50			
19,00	28	27	29
19,50	29	28	30
20,00	30	29	31
20,50			
21,00	31	30	32

Table 6 – D/E, nD/nE, n max. variation – e = 0,50 mm pitch FLGA flanged type

Dimensions in millimetres

D or E	nD max. –1 or nE max. –1	nD max. –2 or nE max. –2	nD max. or nE max.
1,50	2	–	3
2,00	3	2	4
2,50	4	3	5
3,00	5	4	6
3,50	6	5	7
4,00	7	6	8
4,50	8	7	9
5,00	9	8	10
5,50	10	9	11
6,00	11	10	12
6,50	12	11	13
7,00	13	12	14
7,50	14	13	15
8,00	15	14	16
8,50	16	15	17
9,00	17	16	18
9,50	18	17	19
10,00	19	18	20
10,50	20	19	21
11,00	21	20	22
11,50	22	21	23
12,00	23	22	24
12,50	24	23	25
13,00	25	24	26
13,50	26	25	27
14,00	27	26	28
14,50	28	27	29
15,00	29	28	30
15,50	30	29	31
16,00	31	30	32
16,50	32	31	33
17,00	33	32	34
17,50	34	33	35
18,00	35	34	36
18,50	36	35	37
19,00	37	36	38
19,50	38	37	39
20,00	39	38	40
20,50	40	39	41
21,00	41	40	42

Table 7 – D/E, nD/nE, n max. variation – e = 0,40 mm pitch FLGA flanged type

Dimensions in millimetres

D or E	nD max. –1 or nE max. –1	nD max. –2 or nE max. –2	nD max. or nE max.
1,50	2	–	3
2,00	3	2	4
2,50	5	4	6
3,00	6	5	7
3,50	7	6	8
4,00	8	7	9
4,50	10	9	11
5,00	11	10	12
5,50	12	11	13
6,00	13	12	14
6,50	15	14	16
7,00	16	15	17
7,50	17	16	18
8,00	18	17	19
8,50	20	19	21
9,00	21	20	22
9,50	22	21	23
10,00	23	22	24
10,50	25	24	26
11,00	26	25	27
11,50	27	26	28
12,00	28	27	29
12,50	30	29	31
13,00	31	30	32
13,50	32	31	33
14,00	33	32	34
14,50	35	34	36
15,00	36	35	37
15,50	37	36	38
16,00	38	37	39
16,50	40	39	41
17,00	41	40	42
17,50	42	41	43
18,00	43	42	44
18,50	45	44	46
19,00	46	45	47
19,50	47	46	48
20,00	48	47	49
20,50	50	49	51
21,00	51	50	52

Table 8 – D/E, n_D/n_E, n max. variation – e = 0,80 mm pitch FLGA real chip size type

Dimensions in millimetres

D or E	n_D max. –1 or n_E max. –1	n_D max. –2 or n_E max. –2	n_D max. or n_E max.
1,50~1,98	–	–	2
1,99~2,78	2	–	3
2,79~3,58	3	2	4
3,59~4,38	4	3	5
4,39~5,18	5	4	6
5,19~5,98	6	5	7
5,99~6,78	7	6	8
6,79~7,58	8	7	9
7,59~8,38	9	8	10
8,39~9,18	10	9	11
9,19~9,98	11	10	12
9,99~10,78	12	11	13
10,79~11,58	13	12	14
11,59~12,38	14	13	15
12,39~13,18	15	14	16
13,19~13,98	16	15	17
13,99~14,78	17	16	18
14,79~15,58	18	17	19
15,59~16,38	19	18	20
16,39~17,18	20	19	21
17,19~17,98	21	20	22
17,99~18,78	22	21	23
18,79~19,58	23	22	24
19,59~20,38	24	23	25
20,39~21,00	25	24	26